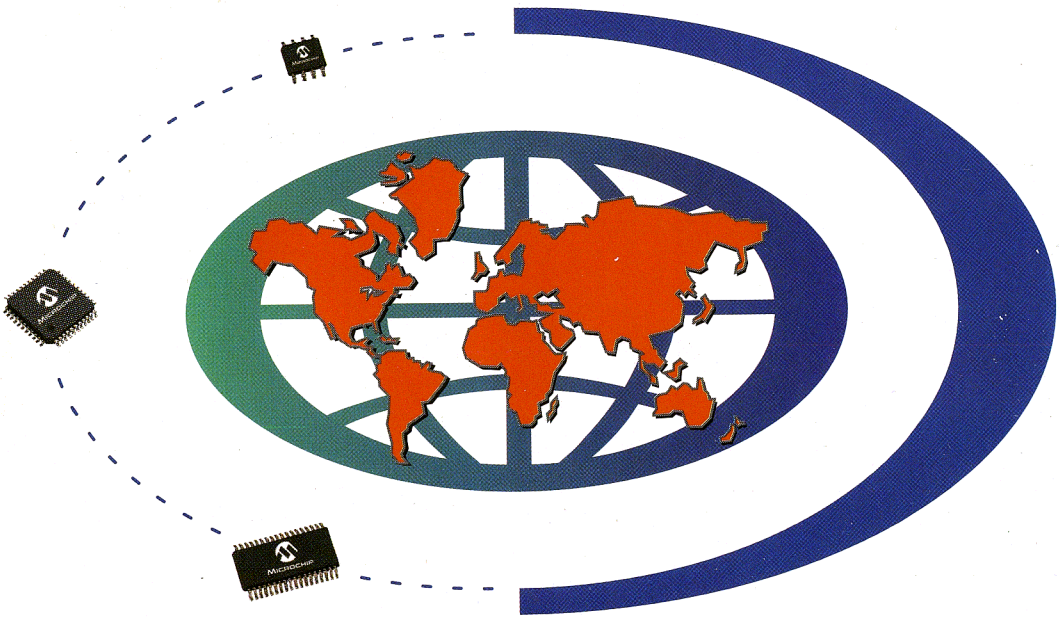
PIC16/17 MICROCONTROLLER DATA BOOK



1996/1997

MICROCHIP

The Embedded Control Solutions Company®

Microcontrollers • Non-Volatile Memories • ASSPs

MICROCHIP

Microchip PIC16/17 Microcontroller Data Book

SERVING A COMPLEX AND COMPETITIVE
WORLD WITH FIELD-PROGRAMMABLE
EMBEDDED CONTROL
SYSTEM SOLUTIONS

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October 1996/DS00158B

DATA BOOK CHANGES

In an effort to streamline our data book and reduce the repetition of duplicated information, we have made the following changes to the PIC16/17 Microcontroller data book.

- **Instruction Set Information** has been pulled from each individual data sheet and now appears in a separate Instruction Set Section, (Section 15).
- **Packaging Information** has been pulled from each individual data sheet and now appears as a comprehensive Packaging Section, (Section 22).
- **Development Tools Information and Microchip BBS and Internet Connection Information** has been pulled from each individual data sheet and now appears as a more complete and expanded Development Systems and Software Support Section (Section 16).

We constantly strive to implement continuous improvement in all of our products and documentation. Your feedba and input are important to us. If you have comments or suggestions, please use the reader response form in the ba of this data book.

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Microchip Technology Inc.

Company Profile

The Embedded Control Solutions Company®

Since its inception, Microchip Technology has focused its resources on delivering truly innovative semiconductor products to the global embedded control marketplace. To do this, we have focused our technology, engineering, manufacturing and marketing resources on two synergistic product lines: field-programmable 8-bit PIC16/17 microcontrollers (MCUs) and high-endurance Serial EEPROMs. Today, Microchip's expanding product portfolio is aimed at delivering a more comprehensive array of high-value solutions to a growing base of customers.

Highlights

Inside Microchip Technology you will find:

- An experienced executive team focused on innovation and committed to listening to our customers
- A focus on providing high-performance, cost-effective, field-programmable embedded control solutions
- 8-bit RISC field-programmable and ROM MCUs
- The world's first 8-pin MCU
- Patented KEELOQ® code hopping technology products
- QuickASIC™ gate array conversion technology
- Serial and Parallel EEPROMs and EPROMs
- A variety of end-user Application-Specific Standard Products (ASSP)
- Fully integrated manufacturing capabilities
- A global network of manufacturing and customer support facilities
- A unique corporate culture dedicated to continuous improvement
- Distributor network support worldwide including certified distribution FAEs

Business Scope

Microchip Technology Inc. manufacturers and markets a variety of VLSI CMOS semiconductor components to support the market for cost-effective embedded control solutions. In particular, the company specializes in highly integrated, field-programmable RISC MCUs, application-specific standard products and related non-volatile memory products to meet growing market requirements for high performance, yet economical embedded control capability in products. Microchip's products feature the industry's most economical One-Time-Programmable (OTP) EPROM, reprogrammable Flash and EEPROM, and ROM capability, along with the compact size, integrated functionality, ease of development and technical support so essential to timely and cost-effective product development by our customers.

Chandler, Arizona:

Company headquarters near Phoenix, Arizona; executive offices, R&D and wafer fabrication occupy this 242,000-square-foot multi-building facility.

Tempe, Arizona:

Microchip's 170,000-square-foot wafer fabrication facility provides increased manufacturing capacity today and for the future.

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Market Focus

Microchip targets selected markets where our advanced designs, progressive process technology and industry-leading product performance enable us to deliver decidedly superior performance. The company has positioned itself to maintain a dominant role as a supplier of high-performance, field-programmable MCUs and associated memory and logic products for embedded control applications which are found throughout the consumer, automotive, telecommunication, office automation and industrial control markets.

Fully Integrated Manufacturing

Microchip delivers fast turnaround and consistent quality through total control over all phases of production. Research and development, design, mask making, wafer fabrication, and the major part of assembly and quality assurance testing are conducted at facilities wholly-owned and operated by Microchip. Our integrated approach to manufacturing along with rigorous use of advanced Statistical Process Control (SPC) and a continuous improvement culture has resulted in high and consistent yields which have positioned Microchip as a quality leader in its global markets. Microchip's unique approach to SPC provides customers with excellent costs, quality, reliability and on-time delivery.

A Global Network of Plants and Facilities

Microchip is a global competitor providing local service to the world's technology centers. The Company's design and technology advancement facilities are located in Chandler and Tempe, Arizona. Product and technology development are located here, along with front-end wafer fabrication and wafer probe and sort.

In 1994, Microchip purchased a second wafer fabrication facility in Tempe, Arizona – thirteen miles from its Chandler, Arizona, headquarters. The additional 170,000 square foot facility meets the increased production requirements of a growing customer base, and provides production capacity which more than doubles that of Chandler. Assembly and test facilities, predominantly located in Kaohsiung, Taiwan, and Bangkok, Thailand, house the technology and assembly and test equipment necessary for modern plastic and ceramic packaging.

During fiscal 1996, Microchip invested more than $115 million for capital additions to the Tempe Fab II facility and for construction of an additional testing facility in Asia. These investments have led to significant improvements in the Company's output and overall cost structure.

Sales and application offices are located in key cities throughout the Americas, Asia/Pacific, Japan and Europe. Offices are staffed to meet the high quality expectations of our customers, and can be accessed for technical and business support.

Embedded Control Overview

Unlike "processor" applications such as personal computers and workstations, the computing or controlling elements of embedded control applications are buried inside the application. The user of the product is only concerned with the very top-level user interface (such as keypads, displays and high-level commands). Very rarely does an end-user know (or care to know) the embedded controller inside (unlike the conscientious PC users, who are intimately familiar not only with the processor type, but also its clock speed, DMA capabilities and so on).

It is, however, most vital for designers of embedded control products to select the most suitable controller and companion devices. Embedded control products are found in all market segments: consumer, commercial, PC peripherals, telecommunications (including fast-emerging personal telecommunication products), automotive and industrial. Most often embedded control products must meet special requirements: cost-effectiveness, low power, small footprint, and a high level of system integration.

Typically, most embedded control systems are designed around a MCU which integrates on-chip program memory, data memory (RAM) and various peripheral functions, such as timers and serial communication. In addition, these systems also usually require complementary Serial EEPROM memories, display drivers, keypads or small displays.

Microchip Technology has established itself as a leading supplier of field-programmable embedded control solutions. The combination of high-performance MCUs from the PIC12CXXX, PIC16C5X, PIC16CXXX and PIC17CXXX families, along with non-volatile memory products, provide the basis for this leadership.

Microchip is committed to continuous innovation and improvement in design, manufacturing and technical support to provide the best possible embedded control solutions to you.

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PIC16/17 MCU Overview and Roadmap

PIC16/17 MCUs from Microchip combine high performance, low cost, and small package size, offering the best price/performance ratio in the industry. More than 100 million of these devices ship each year to cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

Microchip offers four families of 8-bit MCUs to best fit your needs: PIC12CXXX 8-pin, PIC16C5X 12-bit program word, PIC16CXXX 14-bit program word and PIC17CXXX 16-bit program word MCU families.

All families offer OTP, low-voltage and low-power options, as well as various packaging options. Selected members are available in ROM and reprogrammable EEPROM versions.

The widely-accepted PIC16C5X, PIC16CXXX and PIC17CXXX families are the industry's only 8-bit MCUs using a high-speed RISC architecture. Today, these families are joined by the industry's first 8-pin MCU family of devices – the PIC12CXXX. The PIC12CXXX combines the 8-bit high-speed RISC architecture of the PIC16/17 families with the smallest footprint MCU. Microchip pioneered the use of RISC architecture to obtain high speed and instruction efficiency.

PIC12CXXX: 8-Pin, 8-Bit Family

PIC12CXXX family packs Microchip's powerful RISC-based PIC16/17 architecture into 8-pin DIP and SOIC packages. These PIC12CXXX products have a 12-bit wide instruction set, low operating voltage of 2.5V and small package footprints. Future versions of the PIC12CXXX will include devices with the 14-bit wide instruction set, interrupt handling and a deeper hardware stack. All of these features provide an intelligence level to applications not previously available because of cost or size.

PIC16C5X: 12-Bit Architecture Family

PIC16C5X is the well established base-line family offering the most cost-effective solution. These PIC16C5X products have a 12-bit wide instruction set and are currently offered in 18-, 20- or 28-pin packages. In the SOIC and SSOP packaging options, these are among the smallest footprint MCUs. Low-voltage operation down to 2.0V for OTPs make this family ideal for battery operated applications.

PIC16CXXX: 14-Bit Architecture Family

The PIC16CXXX family offers a wide-range of options, from 18-pin to 68-pin packages as well as low to high levels of peripheral integration. This family has a 14-bit wide instruction set, interrupt handling capability and a deep 8-level hardware stack. The PIC16CXXX family provides the performance and versatility to meet the requirements of more demanding, yet cost-sensitive, mid-range 8-bit applications.

The PIC14C000 Programmable Mixed-Signal Controller allows engineers to design intelligent controllers for smart batteries, battery chargers, battery status monitoring, uninterruptible power supplies, HVAC, and other data acquisition and processing required for managing energy. The PIC14C000 can support any battery technology including Li Ion, NiMH, NiCd, Pb acid, Zinc Air. In addition, the product's I^2C™ port enables any system OEM, battery pack VAR, and battery manufacturer to design, build, and market SBD-compliant products supporting the System Management Bus standard.

PIC17CXXX: 16-Bit Architecture Family

The PIC17CXXX family offers the world's fastest execution performance of any 8-bit MCU family in the industry. The PIC17CXXX family extends the PIC16/17 MCU's high- performance RISC architecture with a 16-bit instruction word, enhanced instruction set and powerful vectored interrupt handling capabilities. A powerful array of precise on-chip peripheral features provide the performance for the most demanding 8-bit applications.

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PIC16/17 MCU Naming Convention

The PIC16/17 architecture offers users a wide range of cost/ performance options of any 8-bit MCU family. In order to identify the families, the following naming conventions have been applied to the PIC16/17 MCUs.

TABLE 1: PIC16/17 MCU NAMING CONVENTION

Family		Architectural Features	Name	Technology	Products
PIC17CXXX	8-bit High-Performance MCU Family	• 16-bit wide instruction set • Internal/external vectored interrupts • DC - 25 MHz clock speed • 160 ns instruction cycle (@ 25 MHz) • Hardware multiply	PIC17C4X	OTP program memory, digital only	PIC17C42A, PIC17C43, PIC17C44
			PIC17CR4X	ROM program memory, digital only	PIC17CR42, PIC17CR43
			PIC17C75X	OTP program memory with mixed-signal functions	PIC17C756 (Planned)
PIC16CXXX	8-bit Mid-Range MCU Family	• 14-bit wide instruction set • Internal/external interrupts • DC - 20 MHz clock speed (Note 1) • 200 ns instruction cycle (@ 20 MHz)	PIC14CXXX	OTP program memory with A/D and D/A functions	PIC14C000
			PIC16C55X	OTP program memory, digital only	PIC16C554, PIC16C556, PIC16C558
			PIC16C6X	OTP program memory, digital only	PIC16C62, PIC16C62A, PIC16C63, PIC16C64, PIC16C64A, PIC16C65, PIC16C65A
			PIC16CR6X	ROM program memory, digital only	PIC16CR62, PIC16CR63, PIC16CR64, PIC16CR65
			PIC16C62X	OTP program memory with comparators	PIC16C620, PIC16C621, PIC16C622
			PIC16C7X	OTP program memory with analog functions (i.e. A/D)	PIC16C710, PIC16C71, PIC16C711, PIC16C715, PIC16C72, PIC16C73, PIC16C73A, PIC16C74, PIC16C74A
			PIC16F8X	Flash program and EEPROM data memory	PIC16C84
					PIC16F83, PIC16F84
			PIC16CR8X	ROM program and EEPROM data memory	PIC16CR83, PIC16CR84
			PIC16C9XX	OTP program memory, LCD driver	PIC16C923, PIC16C924
PIC16C5X	8-bit Base-Line MCU Family	• 12-bit wide instruction set • DC - 20 MHz clock speed • 200 ns instruction cycle (@ 20 MHz)	PIC16C5X PIC16C5XA	OTP program memory, digital only	PIC16C52, PIC16C54, PIC16C54A, PIC16C55, PIC16C56, PIC16C57, PIC16C58A
			PIC16CR5X PIC16CR5XA	ROM program memory, digital only	PIC16CR54A, PIC16CR57B, PIC16CR58A
PIC12CXXX	8-bit, 8-pin MCU Family	• 12-bit wide instruction set • DC - 4 MHz clock speed • 1000 ns instruction cycle (@ 4 MHz)	PIC12C5XX	OTP program memory, digital only	PIC12C508, PIC12C509

Note 1: The maximum clock speed for some devices is less than 20 MHz.

Please check with your local Microchip distributor, sales representative or sales office for the latest product information.

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The Advantage of Field Programmability

The PIC16/17 MCU family provides a unique combination of a high-performance RISC processor with cost-effective OTP technology. Cost-effective OTP provides many benefits to the user at prices which can be comparable to competing ROM solutions. The benefits include:

1. Quick time-to-market.
2. Ease of code changes.
3. Ability to provide adaptable solutions to end-customer requirements.
4. Ability to meet upside potential via inventory positions at Microchip or worldwide distribution.
5. Reduced scrappage in manufacturing.
6. Reduced inventory in manufacturing.
7. Reduced work-in-process liability.

For most manufacturers, getting the product to market quickly has become the number one goal as global markets have become more competitive. Time-to-market puts pressure on all functions within the manufacturing process: development, purchasing, production, marketing and sales. Field-programmable OTP technology streamlines the process for all stages in the product life cycle. In the early product development stages, a programmable MCU allows much of the functionality to be implemented in software which can be modified more easily than hardware-only solutions.

In the manufacturing stage, the compression of the product life cycle curve puts pressure on the management of inventory and manufacturing cycle times. Minimizing inventory reduces the ability to meet upside demand. Using a traditional ROM-based MCU limits the ability to respond to the market with product enhancements or semi-customized products for specific customers. Using the standard OTP-based PIC16/17 MCU solves all these issues. Inventory can be managed effectively by using the same device in several systems. Costs can be reduced due to volume purchasing. Upsides can be met from either safety stock, directly from Microchip, or local distributors who regularly inventory all PIC16/17 MCU devices. A sudden decline in demand means no work-in-process ROM-based inventory and any excess safety stock can be consumed by the other products using the same standard device.

OTP is the 'Flexible Manufacturing' technology of the MCU world. As competition intensifies, the demand for customer-specific products increases. Having the ability to change (for example, the appearance of LCD displays or add extra features in a timely manner) can be a key competitive advantage. Programming the OTP device on the manufacturing floor allows easy customizing and internal tracking of the devices for each specific customer. Customization can significantly increase the overall product life cycle to provide better return on investment and help minimize the threat of competition.

Current PIC16/17 MCU product families include advanced features such as sophisticated timers, embedded analog-to- digital converters, extended instruction/data memory, inter-processor communication (I^2C bus, SPI™ and USARTs) and ROM, RAM, EPROM, EEPROM and Flash memories.

All PIC16/17 families are supported by user-friendly development systems including; assembler, software simulator, C Compiler, fuzzy logic development software, programmers and in-circuit emulators.

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Development Systems

Microchip is committed to providing useful and innovative solutions to your embedded system designs. Our installed base of application development systems has grown to an impressive 75,000 systems worldwide. Significantly, more than half of the total system shipments over the past six years took place within the past 18 months.

Among support products offered are the PICMASTER® Real-Time Universal In-circuit Emulator running under the Windows® environment. Microchip's MPLAB™, a complete Integrated Development Environment (IDE), is provided with PICMASTER. MPLAB allows the user to edit, compile and emulate from a single user interface, making the developer productive very quickly. The MPLAB interface is easy-to-learn and easy-to-use, and can help to reduce overall system development time. PICMASTER is designed to provide product development engineers with an optimized design tool for developing target applications. This universal in-circuit emulator provides a complete MCU design tool set for all MCUs in the PIC12CXXX, PIC16C5X, PIC16CXXX and PIC17CXXX families. A CE compliant version of PICMASTER is available for European Union (EU) countries.

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP MCUs. PRO MATE® II, the full-featured, modular device programmer, enables you to quickly and easily program user software into PIC16/17 MCUs. The PRO MATE II operates as a stand-alone unit or in conjunction with a PC compatible host system. The PICSTART® Plus and Lite development kits, are low-cost development systems for the PIC12CXXX, PIC16C5X/PIC16CXXX and PIC17CXXX MCUs. PICSEEKIT and PICSEESTART provide product development engineers with a cost-effective and timely design tool solution for the MTA8XXXX family. PICDEM low-cost demonstration boards are simple boards which demonstrate the capabilities of the full range of Microchip's MCUs. Users can program the sample MCUs provided with PICDEM boards, on a PRO MATE II or PICSTART programmer, and easily test firmware. KEELOQ Evaluation and Programming Tools support Microchip's HCS Secure Data Products.

The Serial EEPROM Designer's Kit includes everything necessary to read, write, erase or program special features of any Microchip Serial EEPROM product including *Smart Serials*™ and secure serials. The *Total Endurance*™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system. The *TrueGauge*® development tool supports system development with the MTA11200B TrueGauge Intelligent Battery Management IC.

TABLE 2: PIC16/17 SYNERGISTIC DEVELOPMENT TOOLS

Development Tool	Name	PIC12CXXX	PIC16C5X	PIC16CXXX	PIC17CXXX
Integrated Development Environment (IDE)	MPLAB™	✔	✔	✔	✔
Universal Macro-Assembler	MPASM	✔	✔	✔	✔
C Compiler	MPLAB-C	✔	✔	✔	✔
Full-Featured, Modular In-Circuit Emulator	PICMASTER®	✔	✔	✔	✔
Low-Cost Modular In-Circuit Emulator	ICEPIC	—	✔	✔	—
Full-Featured, Modular Device Programmer	PRO MATE® II	✔	✔	✔	✔
Entry-Level Development Kit with Programmer	PICSTART® Plus	✔	✔	✔	✔
Low-Cost Entry Level Development Kit	PICSTART® Lite	✔	✔	✔	Planned
Fuzzy Logic Development Software	*fuzzy*TECH®-MP	✔	✔	✔	✔
Application Code Generator	MP-DriveWay™	—	✔	✔	✔

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Software Support

Microchip's PIC16/17 MCU families are supported by an assembler, compiler, software simulator, fuzzy logic development software and application code generator. MPASM is a universal macro assembler supporting Microchip's entire product line of MCUs. A full-featured Integrated Development Environment (MPLAB), C-Compiler and Fuzzy Logic tools are also available for three MCU families. MP-DriveWay is an easy-to-use Windows-based Application Code Generator for visually configuring all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language.

Microchip endeavors at all times to provide the best service and responsiveness possible to its customers. The Microchip Systems Bulletin Board Service (BBS) is one service to facilitate this service. It's a multi-faceted tool that can provide you with information on a number of different topics.

Special Interest Groups (SIGs) available through the BBS can provide you with the opportunity to discuss issues and topics of interest with others that share your interest or questions. The BBS is regularly used to distribute technical information, application notes, source code, errata sheets, bug reports, interim patches for Microchip systems products, and user contributed files for distribution.

The Microchip Internet Home Page can provide you with the latest technical information, production-released software for development tools, application notes and promotional news on Microchip products and technology. The Microchip Web address is http://www.microchip.com.

Please see the Development Systems and Software Support Section for more information on the Microchip BBS and WWW site.

Application-Specific Standard Products (ASSPs)

Microchip ASSPs provide value-added embedded control solutions by combining PIC16/17 MCU architecture, non-volatile memory, and innovative software technology for vertical applications. These products incorporate technology that offers a complete solution that is both unique to the customer and standard in manufacture to Microchip. In addition, Microchip ASSPs reduce or remove the barriers for customers to use Microchip solutions, in their products, through the use of software, embedded in secure OTP- or ROM-based MCUs. These MCUs are packaged to provide the highest integration, to the customer, at the best overall system cost.

The TrueGauge MTA11200B is the most accurate and most integrated battery management and charging solution available today. The TrueGauge family incorporates Microchip/SPAN patented technology which digitally integrates battery charge and discharge current to provide an accurate (>97% typical) state of charge indication. The family operates with NiCd and NiMH and lead acid battery packs from 3 VDC to 25 VDC. These products are ideal for portable PC, cellular phone, and portable consumer product applications.

The MTE1122 Energy Management Controller combines Microchip's proprietary PIC16/17 8-bit RISC MCU technology with a unique, patent pending power management firmware algorithm in a single package. This device, by monitoring and controlling the supply requirements into an AC induction motor, effectively reduces the power consumed by the motor. The MTE1122 is available in both plastic DIP and space-saving SOIC packages, and operates over commercial and industrial ranges.

Ease-of-use, low voltage, and low cost make the MTA41XXX mouse and trackball MCU firmware solutions ideal for implementing new designs for both PCs and Apple® computers. The products in the MTA41XXX family are 18-lead, low-power, CMOS MCU ICs combined with application-specific software. By adding a few external components, the user can easily realize a complete mouse or trackball system.

The MTA8XXXX PICSEE® family of cost-effective system solutions integrates PIC16/17 MCUs with EEPROM technology. These PICSEE devices are ideally suited for automotive security, keyless entry, remote control, telecommunication applications and data acquisition. The combined product assembly techniques provide the user the highest performance solution in a compact and cost-effective package.

Future ASSP products will include advanced features such as mixed analog and digital capability as well as an ever broadening family of turnkey software solutions for the embedded control market.

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Application-Specific Integrated Circuits (ASICs)

In June 1996, Microchip acquired quick-turn ASIC specialist ASIC Technical Solutions, Inc. With the acquisition, Microchip now offers the QuickASIC™ family which replaces standard field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs) with a masked ASIC at a substantially reduced price per unit compared to programmable logic devices. Microchip's QuickASIC family offers turnkey digital design conversion of any FPGA/CPLD device by transforming its net list into a masked ASIC – with very fast lead times of two-to-four weeks from design signoff to first production. QuickASIC devices can be used for any application prototyping with FPGAs/CPLDs including multimedia, data communications, telecommunications and computer peripherals.

In addition, Microchip plans call for customers being given the opportunity to combine Microchip's powerful RISC-based PIC16/17 MCU core with configurable gate arrays, providing a much wider range of flexibility, power ranges and custom functionality.

Serial EEPROM Overview

Microchip offers one of the broadest selections of CMOS Serial EEPROMs on the market for embedded control systems. Serial EEPROMs are available in a variety of densities, operating voltages, bus interface protocols, operating temperature ranges and space saving packages.

Densities:

Currently range from 1K to 64K with higher density devices in development.

Bus Interface Protocols:

All major protocols are covered: I²C™, Microwire® and SPI.

Operating Voltages:

In addition to standard 5V devices there are two low voltage families. The "LC" devices operate down to 2.5V, while the breakthrough "AA" family operates, in both read and write mode, down to 1.8V, making these devices highly suitable for alkaline and NiCd battery powered applications.

Temperature Ranges:

Like all Microchip devices, Serial EEPROMs are offered in Commercial (0°C to +70°C), Industrial (-40°C to +85°C) and Automotive (-40°C to +125°C) operating temperature ranges.

Packages:

The focus is on small packages. Small footprint packages include: 8-lead DIP, 8-lead SOIC in JEDEC and EIAJ body widths, and 14-lead SOIC. The SOIC comes in two body widths; 150 mil and 207 mil.

Technology Leadership:

Microchip's Serial EEPROMs are backed by a 10 million Erase/Write cycle guarantee – an endurance breakthrough unmatched by its competitors. Microchip's erase/write cycle endurance is among the best in the world, and only Microchip offers such unique and powerful development tools as the Total Endurance disk. This mathematical software model is an innovative tool used by system designers to optimize Serial EEPROM performance and reliability within the application.

The Company has also developed the world's first 64K Smart Serial EEPROM. Device densities range from 256 bits up to 64K bits. Another first is the 24LC21, a single chip DDC1/DDC2™-compatible solution for plug-and-play video monitors. In addition, Microchip released a high-speed 1 MHz 2-wire Serial EEPROM device ideal for high-performance embedded systems.

Microchip is a high-volume supplier of Serial EEPROMs to all the major markets worldwide including consumer, automotive, industrial, computer and communications. To date, more than 300 million units have been produced. Microchip continues to develop new Serial EEPROM solutions for embedded control applications.

Parallel EEPROM Overview

CMOS Parallel EEPROM devices from Microchip are available in 4K, 16K and 64K densities. The manufacturing process used for these EEPROMs ensures 10,000 to 100,000 write and erase cycles typical. Data retention is more than 10 years. Fast write times are less than 200 µs. These EEPROMs work reliably under demanding conditions and operate efficiently at temperatures from -40°C to +85°C. Microchip's expertise in advanced SOIC, TSOP and VSOP surface mount packaging supports our customers' needs in space-sensitive applications.

Typical applications include computer peripherals, engine control, telecommunications and pattern recognition.

OTP EPROM Overview

Microchip's CMOS EPROM devices are produced in densities from 64K to 512K. Typical applications include computer peripherals, instrumentation, and automotive devices. Microchip's expertise in surface mount Packaging on SOIC, TSOP and VSOP packages led to the development of the Surface Mount OTP EPROM market where Microchip is a leading supplier today. Microchip is also a leading supplier of low-voltage EPROMs for battery powered applications.

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Secure Data Products Overview

Microchip's patented KEELOQ code hopping technology is the perfect solution for remote keyless entry and logical/physical access control systems. The initial device in the family, HCS300 encoder, will replace current fixed code encoders in transmitter applications and provide a low cost, integrated solution. The KEELOQ family is rapidly expanding with the HCS301 (high voltage encoder) and HCS200 (low-end, low-cost encoder). High-end encoders (HCS360 and HCS361) that meet OEM specifications and requirements.

Microchip provides flexible decoder solutions by providing optimized routines for Microchip's PIC16/17 MCUs. This allows the designer to combine the decoder and system functionality in a MCU. The decoder routines are available under a license agreement. The HCS509 and HCS512 are the first decoder devices in the KeeLoq family. These devices are single chip decoder solutions and simplify designs by handling learning and decoding of transmitters.

The KEELOQ product family is expanding to include enhanced encoders and decoders. Typical applications include automotive RKE, alarm and immobilizer systems, garage door openers and home security systems.

Ease of Production Utilizing Quick Turn Programming (QTP) and Serialized Quick Turn Programming (SQTP SM)

Recognizing the needs of high-volume manufacturing operations, Microchip has developed two programming methodologies which make the OTP products as easy to use in manufacturing as they are efficient in the system development stage.

Quick Turn Programming allows factory programming of OTP products prior to delivery to the system manufacturing operation. PIC16/17, EPROM and Serial EEPROM products can be automatically programmed, with the users program, during the final stages of the test operation at Microchip's assembly and test operations in the Philippine Islands, Taiwan and Thailand. This low-cost programming step allows the elimination of programming during system manufacturing and essentially allows the user to treat the PIC16/17 and memory products as custom ROM products. With one- to four-week lead times on QTP products, the user no longer needs to plan for the extended ROM masking lead times and masking charges associated with custom ROM products. This capability, combined with the off-the-shelf availability of standard OTP product, ensures the user of product availability and the ability to reduce his time-to-market once product development has been completed.

Unique in the 8-bit MCU market is Microchip's ability to enhance the QTP capability with Serialized Quick Turn Programming (SQTP). SQTP allows for the programming of devices with unique, random or serialized identification codes. As each PIC16/17 device is programmed with the customers program code, a portion of the program memory space can be programmed with a unique ID, accessible from normal program memory, which will allow the user to provide each device with a unique identification. This capability is ideal for embedded systems applications where the transmission of key codes or identification of the device as a node within a network is essential. Taking advantage of this capability allows the system designer to eliminate the requirement for expensive off-chip code implementation using DIP switches or non-volatile memory components. The SQTP offering, pioneered by Microchip, provides the embedded systems designer with a low cost means of putting a unique and custom device into every system or node.

Future Products and Technology

Microchip is constantly developing advanced process technology modules and products that will be integrated into present product lines to continue to achieve a range of compatible processes. Current production technology utilizes lithography dimensions down to 0.7 microns.

Microchip's research and development activities include exploring new process technologies and products that have industry leadership potential. Particular emphasis is placed on products that can be put to work in high-performance broad-based markets.

Equipment is continually updated to bring the most sophisticated process, CAD and testing tools online. Cycle times for new technology development are continuously reduced by using in-house mask generation, a high-speed pilot line within the manufacturing facility and continuously improving methodologies.

More advanced technologies are under development, as well as advanced CMOS RISC-based MCU, ASSP and CMOS EEPROM and EPROM, and QuickASIC products. Objective specifications for new products are developed by listening to our customers and by close co-operation with our many customer-partners worldwide.

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PIC16/17 8-BIT MICROCONTROLLER FAMILY

Product	Program Memory OTP Bytes	Program Memory OTP Words	Data RAM Bytes	Max. Speed MHz	I/O Ports	ADC 8-Bits	Serial I/O	PWM	DAC 8-Bits	Brown-Out Detection	Comparators	Timers	In-System Programming	Other Features	ROM Equivalent	Packages
PIC12CXXX — 1000ns Instruction Execution, 33/35 Instructions																
PIC12C508*	768	512x12	25	4	6							1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12C509*	1536	1024x12	41	4	6							1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12C670*	896	512x14	80	4	6	2						1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12C671*	1792	1024x14	80	4	6	2						1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12F680*	896	512x14 (Flash)	80 (16 E²)	4	6							1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12F681*	1792	1024x14 (Flash)	80 (16 E²)	4	6							1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC16C5X — 200ns Instruction Execution, 33 Instructions																
PIC16C52	576	384x12	25	4	12							1		10mA source/sink per I/O, 2.5V	—	18P, 18SO
PIC16C54	768	512x12	25	20	12							1+WDT		20mA source and 25mA sink per I/O, 2.5V	PIC16CR54A	18P, 18JW, 18SO, 20SS
PIC16C54A	768	512x12	25	20	12							1+WDT		20mA source and 25mA sink per I/O, 2.0V	PIC16FR54A	18P, 18JW, 18SO, 20SS
PIC16C55	768	512x12	24	20	20							1+WDT		20mA source and 25mA sink per I/O, 2.5V	PIC16FR55	28P, 28JW, 28SP, 28SO, 28SS
PIC16C56	1536	1024x12	25	20	12							1+WDT		20mA source and 25mA sink per I/O, 2.5V	PIC16FR56	18P, 18JW, 18SO, 20SS
PIC16C57	3072	2048x12	72	20	20							1+WDT		20mA source and 25mA sink per I/O, 2.5V	PIC16FR57	28P, 28JW, 28SP, 28SO, 28SS
—	3072 (ROM)	2048x12	72	20	20							1+WDT		20mA source and 25mA sink per I/O, 2.5V	PIC16CR57B	28P, 28JW, 28SP, 28SO, 28SS
PIC16C58A	3072	2048x12	73	20	12							1+WDT		20mA source and 25mA sink per I/O, 2.0V	PIC16CR58A	18P, 18SO, 20SS
PIC16CXX — 4-12 Interrupts, 200ns Instruction Execution, 35 Instructions, Upwardly Compatible with PIC16C5X																
PIC14C000	7168	4096x14	192	20	20	8 SLAC	I²C™/ SMB	2	2			2+WDT	Yes	25mA source/sink, temperature sensor, GSM averaging, internal oscillator	—	28SP, 28SO, 28SS, 28JW
PIC16C554	896	512x14	80	20	13							1+WDT	Yes	25mA source/sink per I/O, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C556	1792	1024x14	80	20	13							1+WDT	Yes	25mA source/sink per I/O, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C558	3584	2048x14	128	20	13							1+WDT	Yes	25mA source/sink per I/O, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C61	1792	1024x14	36	20	13							1+WDT	Yes	20mA source and 25mA sink per I/O	—	18P, 18SO, 18JW
PIC16C62	3584	2048x14	128	20	22		I²C/ SPI™	1				3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	PIC16FR62	28SP, 28SO, 28SS, 28JW
PIC16C62A	3584	2048x14	128	20	22		I²C/SPI	1		Yes		3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	PIC16CR62	28SP, 28SO, 28SS, 28JW
PIC16C63	7168	4096x14	192	20	22		USART/ I²C/SPI	2		Yes		3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	PIC16CR63*	28SP, 28SO, 28JW
PIC16C64	3584	2048x14	128	20	33		I²C/SPI	1				3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, Capture/Compare/PWM	PIC16FR64	40P, 40JW, 44L, 44PQ
PIC16C64A	3584	2048x14	128	20	33		I²C/SPI	1		Yes		3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, Capture/Compare/PWM	PIC16CR64	40P, 40JW, 44L, 44PQ, 44PT
PIC16C65	7168	4096x14	192	20	33		USART/ I²C/SPI	2				3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	PIC16FR65	40P, 40JW, 44L, 44PQ
PIC16C65A	7168	4096x14	192	20	33		USART/ I²C/SPI	2		Yes		3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	PIC16CR65*	40P, 40JW, 44L, 44PQ, 44PT

* Contact Microchip Technology for availability date.

Abbreviations:

ADC = Analog-to-Digital Converter
CAP = Capture
CCP = Capture/Compare/PWM
DAC = Digital-to-Analog Converter
E² = EEPROM (Reprogrammable)
I²C = Inter-integrated Circuit Bus
PWM = Pulse Width Modulator
SPI = Serial Peripheral Interface
USART = Universal Synchronous/Asynchronous Receiver/Transmitter
WDT = Watchdog Timer
SLAC = Slope A/D Converter, up to 16 bits

Packages:

CL = Windowed CERQUAD
JW = Windowed CERDIP
L = Plastic Leaded Chip Carrier (PLCC)
P = Plastic DIP
PQ = Plastic Quad Flat Pack (PQFP)
SO = Plastic Small Outline (SOIC)
SP = Plastic Skinny DIP
SS = Plastic Shrink Small Outline (SSOP)
PT = Plastic Thin Quad Flat Pack (TQFP)

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PIC16/17 8-BIT MICROCONTROLLER FAMILY

Product	Program Memory OTP Bytes	Program Memory OTP Words	Data RAM Bytes	Max. Speed MHz	I/O Ports	ADC 8-Bits	Serial I/O	PWM	DAC 8-Bits	Brown-Out Detection	Comparators	Timers	In-System Programming	Other Features	ROM Equivalent	Packages
PIC16CXXX — 4–12 Interrupts, 200ns Instruction Execution, 35 Instructions, Upwardly Compatible with PIC16C5X (Continued)																
PIC16C620	896	512x14	80	20	13					Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, 2.5V	PIC16FR620	18P, 18SO, 20SS, 18JW
PIC16C621	1792	1024x14	80	20	13					Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, 2.5V	PIC16FR621	18P, 18SO, 20SS, 18JW
PIC16C622	3584	2048x14	128	20	13					Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, 2.5V	PIC16FR622	18P, 18SO, 20SS, 18JW
PIC16C642*	7168	4096x14	176	20	22					Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	28SP, 28SO, 28JW
PIC16C662*	7168	4096x14	176	20	22					Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	40P, 40JW, 44L, 44PQ, 44PT
PIC16C710	896	512x14	36	20	13	4				Yes		1+WDT	Yes	25mA source/sink per I/O	PIC16FR710	18P, 18SO, 20SS, 18JW
PIC16C71	1792	1024x14	36	20	13	4						1+WDT	Yes	20mA source/sink per I/O	PIC16FR71	18P, 18SO, 18JW
PIC16C711	1792	1024x14	68	20	13	4				Yes		1+WDT	Yes	25mA source/sink per I/O	PIC16FR711	18P, 18SO, 20SS, 18JW
PIC16C72	3584	2048x14	128	20	22	5	I²C/SPI	1		Yes		3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	PIC16FR72	28SP, 28SO, 28JW, 28SS
PIC16C73	7168	4096x14	192	20	22	5	USART/ I²C/SPI	2				3+WDT	Yes	25mA source/sink per I/O, 2 Capture/Compare/PWM	PIC16FR73	28SP, 28SO, 28JW
PIC16C73A	7168	4096x14	192	20	22	5	USART/ I²C/SPI	2		Yes		3+WDT	Yes	25mA source/sink per I/O, 2 Capture/Compare/PWM	PIC16FR73A	28SP, 28SO, 28JW
PIC16C74	7168	4096x14	192	20	33	8	USART/ I²C/SPI	2				3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	PIC16FR74	40P, 40JW, 44L, 44PQ
PIC16C74A	7168	4096x14	192	20	33	8	USART/ I²C/SPI	2		Yes		3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	PIC16FR74A	40P, 40JW, 44L, 44PQ, 44PT
PIC16F83	896 (Flash)	512x14 (Flash)	36 (64 E²)	10	13							1+WDT	Yes	20mA source and 25mA sink per I/O, 64 bytes data EEPROM, 2.0V Operation	PIC16CR83	18P, 18SO
PIC16C84	1792 (E²PROM)	1024x14 (E²PROM)	36 (64 E²)	10	13							1+WDT	Yes	20mA source and 25mA sink per I/O, 64 bytes data EEPROM, 2.0V Operation	—	18P, 18SO
PIC16F84	1792 (Flash)	1024x14 (Flash)	68 (64 E²)	10	13							1+WDT	Yes	20mA source and 25mA sink per I/O, 64 bytes data EEPROM, 2.0V Operation	PIC16CR84	18P, 18SO
PIC16C923	7168	4096x14	176	8	52		I²C/SPI	1				3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, LCD module, static, 1/2, 1/3, 1/4 multiplex	—	64SP, 68CL, 68L, 64PQ
PIC16C924	7168	4096x14	176	8	52	5	I²C/SPI	1				3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, LCD module, static, 1/2, 1/3, 1/4 multiplex	—	64SP, 68CL, 68L, 64PQ
PIC17CXXX — 120ns Instruction Execution Including Multiply, 58 Instructions, Upwardly Compatible with PIC16CXXX/PIC16C5X																
PIC17C42A	4096	2048x16	232	33	33		USART	2				4+WDT		20mA source and 35mA sink per I/O, 2 I/O w/60mA sink, 2 Capture, externally expandable, 1 cycle 8x8 multiply	PIC17CR42	40P, 40JW, 44L, 44PQ, 44PT
PIC17C43	8192	4096x16	454	33	33		USART	2				4+WDT		20mA source and 35mA sink per I/O, 2 I/O w/60mA sink, 2 Capture, externally expandable, 1 cycle 8x8 multiply	PIC17CR43	40P, 40JW, 44L, 44PQ, 44PT
PIC17C44	16384	8192x16	454	33	33		USART	2				4+WDT		20mA source and 35mA sink per I/O, 2 I/O w/60mA sink, 3 Capture, externally expandable, 1 cycle 8x8 multiply	PIC17FR44	40P, 40JW, 44L, 44PQ, 44PT
PIC17C756*	32768	16384 x16	902	33	50	12 (10-Bits)	USART (2), I²C/SPI	3		Yes		4+WDT		20mA source and 35mA sink per I/O, 2 I/O w/60mA sink, 4 Capture, externally expandable, 1 cycle 8x8 multiply	—	64SP, 68CL, 68L, 64PQ

* Contact Microchip Technology for availability date.

Abbreviations:

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CAP = Capture
CCP = Capture/Compare/PWM
DAC = Digital-to-Analog Converter
E² = EEPROM (Reprogrammable)
I²C = Inter-integrated Circuit Bus
PWM = Pulse Width Modulator
SPI = Serial Peripheral Interface
USART = Universal Synchronous/Asynchronous Receiver/Transmitter
WDT = Watchdog Timer
SLAC = Slope A/D Converter, up to 16 bits

Packages:

CL = Windowed CERQUAD
JW = Windowed CERDIP
L = Plastic Leaded Chip Carrier (PLCC)
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PQ = Plastic Quad Flat Pack (PQFP)
SO = Plastic Small Outline (SOIC)
SP = Plastic Skinny DIP
SS = Plastic Shrink Small Outline (SSOP)
PT = Plastic Thin Quad Flat Pack (TQFP)

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SECURE DATA PRODUCTS

Product	Transmission Code Length Bits	Code Hopping Bits	Programmable Encryption Key Bits	Seed Length	Operating Voltage	Function	Other Features	Packages
KEELOQ® Encoder Devices								
HCS200	66	32	64	32	3.5V to 13.0V	7	Entry Level, Fixed Code Support, Battery Low Indicator	8P, 8SO
HCS300	66	32	64	32	2.0V to 6.3V	15	LED Drive, Overflow bits, Time-out, Battery Low Indicator	8P, 8SO
HCS301	66	32	64	32	3.5V to 13.0V	15	Same as HCS300	8P, 8SO
HCS360*	67	32	64	48	2.0V to 6.6V	15	IR Mode, PWM and Manchester Coding, 2 independent counters, 2-Bit CRC	8P, 8SO
HCS361*	67	32	64	48	2.0V to 6.6V	15	IR Mode, PWM and VPWM Coding, 2 independent counters, 2-Bit CRC	8P, 8SO

* Contact Microchip Technology Inc. for availability date.

Product	Reception Length Bits	Encoders Supported	Transmitters Supported	Operating Voltage	Functions	Other Features	Packages
KEELOQ Decoder Devices							
HCS509	56	NTQ104, NTQ105, NTQ106, HCS200, HCS300, HCS301, HCS360, HCS361	Up to 4	3.0V to 6.0V	3 (F1, F2, F3); Repeat, Master, Delay	Single-chip replacement for NTQ109 with NTQ106	18P, 18SO
HCS512	67	NTQ104, NTQ105, NTQ106, HCS200, HCS300, HCS301, HCS360, HCS361	Up to 4	3.0V to 6.0V	S0, S1, S2, S3, VLow, Serial	Single-chip decoder with secure learning	18P, 18SO

SERIAL ELECTRICALLY ERASABLE PROMs (EEPROM)

Product	E/W Cycles	Density (Organization)	Write Speed	Max. Clock Freq.	Operating Voltage	Unique Features	Packages
3-WIRE SERIAL EEPROM FAMILY							
93C06	1M	256 bits (x16)	1 ms/byte	1 MHz	4.5V to 5.5V	These devices are primarily for applications which require fast byte write and/or extended temperature (–40°C to +125°C).	P, SN, SM
93C46	1M	1K bits (x16)	1 ms/byte	1 MHz	4.5V to 5.5V		P, SN, SM
93C76	10M	8K bits (x8 or x16)	10 ms	2 MHz	4.0V to 5.5V		P, SN
93C86	10M	16K bits (x8 or x16)	10 ms	2 MHz	4.0V to 5.5V		P, SN
93LC46	1M	1K bits (x8 or x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN, SM
93LC56	10M	2K bits (x8 or x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN, SM, SL
93LC66	10M	4K bits (x8 or x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN, SM, SL
93LC76	10M	8K bits (x8 or x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN
93LC86	10M	16K bits (x8 or x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN
93LC46B	1M	1K bits (x16)	10 ms	2 MHz	2.5V to 6.0V	The B version on the 3-wire devices designates a x16 only device; the organization is not selectable.	P, SN, SM
93LC56B	10M	2K bits (x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN, SM, SL
93LC66B	10M	4K bits (x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN, SM, SL
93AA46	1M	1K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN, SM
93AA56	10M	2K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN, SM
93AA66	10M	4K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN, SM
93AA76	10M	8K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN
93AA86	10M	16K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN
93LCS56	1M	2K (x16)	10 ms	2 MHz	2.5V to 6.0V	The "S" indicates software write protection of user defined memory space.	P, SN, SM, SL
93LCS66	1M	4K (x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN, SM, SL
Special Features Included in all 3-wire Serial EEPROM Family Types:				Automatic ERAL before WRAL Self-timed erase and write cycles Sequential read function		Power on/off data protection circuitry Industry standard 3-wire serial I/O	
2-WIRE SERIAL EEPROM FAMILY*							
24C01A	1M	1K bits (x8)	1 ms/byte	100 kHz	4.5V to 5.5V	The 24C01A, 24C02A and 24C04A are for applications which require fast byte write and/or extended temperature.	P, SN, SM
24C02A	1M	2K bits (x8)	1 ms/byte	100 kHz	4.5V to 5.5V		P, SN, SM
24C04A	1M	4K bits (x8)	1 ms/byte	100 kHz	4.5V to 5.5V		P, SN, SM, SL
24C08B	1M	8K bits (x8)	10 ms	100 kHz	4.5V to 5.5V	The 24C08B and 24C16B versions are for 5.0V only applications which require extended temperature (–40°C to +125°C).	P, SN, SM, SL
24C16B	1M	16K bits (x8)	10 ms	100 kHz	4.5V to 5.5V		P, SN, SL
Special Features Included in all 2-wire Serial EEPROM Family Types:				2-wire serial interface bus, I²C compatible Self-timed write cycle		Factory programming available Page write mode	

* The B version on the 2-wire devices designates: no functional address (A0, A1, A2) pins, 400 kHz operation, Schmitt trigger inputs for greater noise protection, longer byte write cycle time, larger input buffer.

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SERIAL ELECTRICALLY ERASABLE PROMs (EEPROM)

Product	E/W Cycles	Density (Organization)	Write Speed	Max. Clock Freq.	Operating Voltage	Unique Features	Packages
2-WIRE SERIAL EEPROM FAMILY* (Continued)							
24LC01B	10M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Hardware write protect. Schmitt trigger inputs.	P, SN, SM
24LC02B	1M	2K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM
24LC04B	1M	4K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM, SL
24LC08B	1M	8K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM, SL
24LC16B	10M	16K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM, SL
24AA01	10M	1K bits (x8)	10 ms	400 kHz	1.8V to 5.5V	Hardware write protect. Schmitt trigger inputs.	P, SN, SM
24AA02	1M	2K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM
24AA04	1M	4K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM, SL
24AA08	1M	8K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM, SL
24AA16	10M	16K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM, SL
24C32	10M/100K	32K bits (x8)	5 ms/page	400 kHz	4.5V to 5.5V	Incorporates a 4K high endurance block (not relocatable) to ensure 10,000,000	P, SM
24LC32	10M/100K	32K bits (x8)	5 ms/page	400 kHz	2.5V to 6.0V	Erase/Write cycles, a 1 page by 8 line input cache (64 bytes) for fast write loads and is	P, SM
24AA32	10M/100K	32K bits (x8)	5 ms/page	100 kHz	1.8V to 6.0V	cascadable up to 8 parts.	P, SM
24C32A	1M	32K bits (x8)	5 ms/page	400 kHz	4.5V to 5.5V	JEDEC SOIC "SN" (150 mil wide) package.	SN, P, SM
24LC32A	1M	32K bits (x8)	5 ms/page	400 kHz	2.5V to 6.0V		SN, P, SM
24AA32A	1M	32K bits (x8)	5 ms/page	100 kHz	1.8V to 6.0V		SN, P, SM
24FC16	10M	16K bits (x8)	10 ms	1 MHz	4.5V to 5.5V	1 MHz Maximum Clock Rate.	P, SN
24FC32	10M/100K	32K bits (x8)	5 ms/page	1 MHz	4.5V to 5.5V		P, SM
24FC65	10M/100K	64K bits (x8)	5 ms/page	1 MHz	4.5V to 5.5V		P, SM
24LC21	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Completely implements DDC1™/DDC2™ interface for monitor identification.	P, SN
24LCS21	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Improved noise filter. Software enabled Hardware Write Protection pin.	P, SN
24LC21A	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Same as 24LC21 with return to DDC1 feature.	P, SN
24LCS21A	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Same as 24LCS21 with return to DDC1 feature.	P, SN
24LC41A	1M	1K or 4K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Dual Mode, Dual-Port device. Completely implements DDC1/DDC2 interface for monitor identification (DDC port). Also includes 4K bit MCU port.	P
24LCS52	10M	2K bits (x8)	10 ms/page	400 kHz	2.5V to 5.5V	Serial Presence Detect (SPD) device for PC memory modules.	P, SN, ST
24LC164	10M	16K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Cascadable 16K-bit Serial EEPROM.	P, SN
24AA164	10M	16K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN
24LC174	10M	16K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Cascadable 16K-bit Serial EEPROM.	P, SN
24AA174	10M	16K bits (x8)	10 ms	400 kHz	1.8V to 5.5V	Specially addressed one-time-programmable (OTP) 16 byte security block.	P, SN
24C01SC	10M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Smart card specific memory device. Meets ISO Standard 7816 requirements.	S, W
24C02SC	1M	2K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Smart card specific memory device. Meets ISO Standard 7816 requirements.	S, W
85C72	1M	1K bits (x8)	1 ms/byte	100 kHz	4.5V to 5.5V	CMOS version of PCD8572	P, SM
85C82	1M	2K bits (x8)	1 ms/byte	100 kHz	4.5V to 5.5V	CMOS version of PCD8582	P, SM
85C92	1M	4K bits (x8)	1 ms/byte	100 kHz	4.5V to 5.5V	Memory upgrade of PCD8582	P, SM, SL
Special Features Included in all 2-wire Serial EEPROM Family Types:				2-wire serial interface bus, I²C compatible		Factory programming available Page write mode Self-timed write cycle	
* The B version on the 2-wire devices designates: no functional address (A0, A1, A2) pins, 400 kHz operation, Schmitt trigger inputs for greater noise protection, longer byte write cycle time, larger input buffer.							
SMART SERIAL™ EEPROM FAMILY							
24C65	10M/100K	64K bits (x8)	5 ms/page	400 kHz	4.5 to 5.5V	Relocatable 4K bit block of ultra high endurance memory to ensure 10,000,000 E/W cycles,	P, SM
24LC65	10M/100K	64K bits (x8)	5 ms/page	400 kHz	2.5 to 6.0V	1 page by 8 line input cache (64 bytes) for fast write loads, cascadable up to for	P, SM
24AA65	10M/100K	64K bits (x8)	5 ms/page	100 kHz	1.8 to 6.0V	Erase/Write protection in 4K blocks.	P, SM
Special Features Included in all Smart Serial EEPROM Family Types:				2-wire serial interface bus Self-timed Erase/Write cycle Power on/off data protection circuitry		Factory programming available Page write operation Programmable software write protect Schmitt trigger inputs for noise suppression Split Endurance/relocatable high endurance block Output slope control to eliminate ground bounce	
SPI™ SERIAL EEPROM FAMILY							
25C040*	10M	4K bits (x8)	5 ms	3 MHz	4.5V to 5.5V	Supports SPI Modes 0, 3	P, SN, ST
25C080*	10M	8K bits (x8)	5 ms	3 MHz	4.5V to 5.5V		P, SN
25C160*	10M	16K bits (x8)	5 ms	3 MHz	4.5V to 5.5V		P, SN
25C320*	1M	32K bits (x8)	5 ms	3 MHz	4.5V to 5.5V		P, SN, ST
25LC040*	10M	4K bits (x8)	5 ms	2 MHz	2.5V to 6.0V	Supports SPI Modes 0, 3	P, SN, ST
25LC080*	10M	8K bits (x8)	5 ms	2 MHz	2.5V to 6.0V		P, SN
25LC160*	10M	16K bits (x8)	5 ms	2 MHz	2.5V to 6.0V		P, SN
25LC320*	1M	32K bits (x8)	5 ms	2 MHz	2.5V to 6.0V		P, SN, ST
25AA040*	10M	4K bits (x8)	5 ms	1 MHz	1.8V to 6.0V	Supports SPI Modes 0, 3	P, SN, ST
25AA080*	10M	8K bits (x8)	5 ms	1 MHz	1.8V to 6.0V		P, SN
25AA160*	10M	16K bits (x8)	5 ms	1 MHz	1.8V to 6.0V		P, SN
25AA320*	1M	32K bits (x8)	5 ms	1 MHz	1.8V to 6.0V		P, SN, ST
Special Features Included on all SPI Serial EEPROM types:			Page write mode	HOLD pin	Software enabled block write protection	Hardware write protect pin	

PARALLEL ELECTRICALLY ERASABLE PROMs (EEPROM)

Product	Density (Organization)	Byte Write Time	Number of Pins	Packages	Unique Features
STANDARD SERIES					
28C04A	4K bits (x8)	1 ms	24 32	P L	
28C16A	16K bits (x8)	1 ms	24 28 32	P TS, VS L	
28C17A	16K bits (x8)	1 ms	24 28 32	P, SO TS, VS L	Ready/Busy Pin.
28C64A	64K bits (x8)	1 ms	28 32	P, SO, TS, VS L	
28LV64A	64K bits (x8)	1 ms	28 32	P, SO, TS, VS L	Low voltage capability down to 3.0V
FAST BYTE WRITE SERIES					
28C04AF	4K bits (x8)	200 µs	24 32	P L	
28C16AF	16K bits (x8)	200 µs	24 28 32	P TS, VS L	
28C17AF	16K bits (x8)	200 µs	24 28 32	P, SO TS, VS L	Ready/Busy Pin.
28C64AF	64K bits (x8)	200 µs	28 32	P, SO, TS, VS L	

Special Features included in all Parallel EEPROMs: Access times of 150, 200, 250 ns (Except 28LV64A; Access Time = 300ns); Commercial and Industrial Temperature Ranges; 4.5V to 5.5V Operating Range (Except 28LV64A; Operating Voltage = 2.7V to 3.6V)

ELECTRICALLY PROGRAMMABLE READY ONLY MEMORYS (EPROM)

Product	Size	Organization	Access Time (ns)	Operating Voltage	Packages	Temperature Range C = Commercial (0°C to +70°C) I = Industrial (–40°C to +85°C) E = Extended (–40°C to +125°C)
STANDARD EPROM FAMILY						
27C64-25	64K bits	8Kx8	250	4.5V to 5.5V	P, SO, L	C, I
27C64-20	64K bits	8Kx8	200	4.5V to 5.5V	P, SO, L	C, I
27C64-17	64K bits	8Kx8	170	4.5V to 5.5V	P, SO, L	C, I
27C64-15	64K bits	8Kx8	150	4.5V to 5.5V	P, SO, L	C, I
27C64-12	64K bits	8Kx8	120	4.5V to 5.5V	P, SO, L	C, I
27C128-25	128K bits	16Kx8	250	4.5V to 5.5V	P, SO, L	C, I
27C128-20	128K bits	16Kx8	200	4.5V to 5.5V	P, SO, L	C, I
27C128-17	128K bits	16Kx8	170	4.5V to 5.5V	P, SO, L	C, I
27C128-15	128K bits	16Kx8	150	4.5V to 5.5V	P, SO, L	C, I
27C128-12	128K bits	16Kx8	120	4.5V to 5.5V	P, SO, L	C, I
27C256-20	256K bits	32Kx8	200	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C256-15	256K bits	32Kx8	150	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C256-12	256K bits	32Kx8	120	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C256-10	256K bits	32Kx8	100	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C256-90	256K bits	32Kx8	90	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C512A-20	512K bits	64Kx8	200	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C512A-15	512K bits	64Kx8	150	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C512A-12	512K bits	64Kx8	120	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C512A-10	512K bits	64Kx8	100	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C512A-90	512K bits	64Kx8	90	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27LV64-30	64K bits	8Kx8	300	3.0V to 5.5V	P, SO, L, TS	C
27LV64-25	64K bits	8Kx8	250	3.0V to 5.5V	P, SO, L, TS	C
27LV64-20	64K bits	8Kx8	200	3.0V to 5.5V	P, SO, L, TS	C
27LV256-30	256K bits	32Kx8	300	3.0V to 5.5V	P, SO, L, TS, VS	C, I
27LV256-25	256K bits	32Kx8	250	3.0V to 5.5V	P, SO, L, TS, VS	C, I
27LV256-20	256K bits	32Kx8	200	3.0V to 5.5V	P, SO, L, TS, VS	C, I
SERIAL EPROM FAMILY						
37LV36	35K bits	1134x32	10 MHz clock	3.0V to 6.0V	P, SO, L	C, I
37LV65	64K bits	2048x32	10 MHz clock	3.0V to 6.0V	P, SO, L	C, I
37LV128	128K bits	4096x32	10 MHz clock	3.0V to 6.0V	P, SO, L	C, I

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QuickASIC™ MASK PROGRAMMED GATE ARRAYS

Product	Typical ASIC Usable Gates	Typical FPGA Equivalent Gates	I/Os	Packages						Unique Features
				8-pin SO	16-, 20-, 24-, 28-pin SOIC	20-, 28-, 44-, 67-, 84-pin PLCC	64-, 80-, 100-, 128-pin PQFP	144-, 160-, 208-, 240-pin PQFP	64-, 80-, 100-, 128-, 144-pin TQFP	
QIC7K	7K	10K	85	X	X	X	X	*	X	QuickASICs are pin-for-pin FPGA (field programmable gate array) replacements. Microchip will convert all popular FPGAs and CPLDs (complex programmable logic devices) available on the market today.
QIC14K	14K	20K	118	*	X	X	X	X	X	
QIC21K	21K	30K	151	*	*	X	X	X	X	
QIC28K	28K	40K	174	*	*	X	X	X	X	
QIC42K	42K	60K	208	*	*	X	X	X	X	
QIC56K	56K	80K	240	*	*	X	X	X	X	
QIC84K	84K	120K	304	*	*	*	X	X	X	

X = Array package combination available. * = Contact Microchip.

DEVELOPMENT SYSTEMS

Product	**MPLAB™ Integrated Development Environment	MPLAB-C Compiler	MP-DriveWay™ Applications Code Generator	fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Development Tool	***PICMASTER®/ PICMASTER-CE In-Circuit Emulator System	ICEPIC Low-Cost In-Circuit Emulator	****PRO MATE™ II Universal Programmer	PICSTART® Lite Ultra Low-Cost Development Kit	PICSTART Plus Low-Cost Universal Development Kit
PIC16/17 Microcontroller Development Systems									
PIC12C508, 509*	SW007002	SW006005	—	—	EM167015/EM167101	—	DV007003	—	DV003001
PIC14000	SW007002	SW006005	—	—	EM147001/EM147101	—	DV007003	—	DV003001
PIC16C52, 54, 54A, 55, 56, 57, 58A	SW007002	SW006005	SW006006	DV005001/DV005002	EM167015/EM167101	EM167201	DV007003	DV162003	DV003001
PIC16C554, 556, 558	SW007002	SW006005	—	DV005001/DV005002	EM167033/EM167113	—	DV007003	—	DV003001
PIC16C61	SW007002	SW006005	SW006006	DV005001/DV005002	EM167021/N/A	EM167205	DV007003	DV162003	DV003001
PIC16C62, 62A, 64, 64A	SW007002	SW006005	SW006006	DV005001/DV005002	EM167025/EM167103	EM167203	DV007003	DV162002	DV003001
PIC16C620, 621, 622	SW007002	SW006005	SW006006	DV005001/DV005002	EM167023/EM167109	EM167202	DV007003	DV162003	DV003001
PIC16C63, 65, 65A, 73, 73A, 74, 74A	SW007002	SW006005	SW006006	DV005001/DV005002	EM167025/EM167103	EM167204	DV007003	DV162002	DV003001
PIC16C642, 662*	SW007002	SW006005	—	—	EM167035/EM16715	—	DV007003	DV162002	DV003001
PIC16C71	SW007002	SW006005	SW006006	DV005001/DV005002	EM167027/EM167105	EM167205	DV007003	DV162003	DV003001
PIC16C710, 711	SW007002	SW006005	SW006006	DV005001/DV005002	EM167027/EM167105	—	DV007003	DV162003	DV003001
PIC16C72	SW007002	SW006005	SW006006	—	EM167025/EM167103	—	DV007003	DV162002	DV003001
PIC16F83, F84	SW007002	SW006005	SW006006	DV005001/DV005002	EM167029/EM167107	—	DV007003	DV162003	DV003001
PIC16C84	SW007002	SW006005	SW006006	DV005001/DV005002	EM167029/EM167107	EM167206	DV007003	DV162003	DV003001
PIC16C923, 924*	SW007002	SW006005	SW006006	DV005001/DV005002	EM167031/EM167111	—	DV007003	—	DV003001
PIC17C42, 42A, 43, 44	SW007002	SW006005	SW006006	DV005001/DV005002	EM177007/EM177107	—	DV007003	—	DV003001

* Contact Microchip Technology for availability date.
** MPLAB Integrated Development Environment includes MPLAB-SIM Simulator and MPASM Assembler.
*** All PICMASTER and PICMASTER-CE ordering part numbers above include PRO MATE II programmer.
**** PRO MATE socket modules are ordered separately.
See *Development Systems Ordering Guide* for specific ordering part numbers.

Product	SEEVAL® Designer's Kit	Hopping Code Security Programmer Kit	Hopping Code Security Evaluation/ Demonstration Kit
Memory and Secure Data Products Development Systems			
All 2- and 3-wire Serial EEPROMs	DV243001	N/A	N/A
HCS200, 300, 301*	N/A	PG306001	DM303001

*Contact Microchip Technology for availability date. See *Development Systems Ordering Guide* for specific ordering part numbers.

NOTES:

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MICROCHIP

2

SECTION 2
PIC12C5XX MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC12C5XX 8-Pin, 8-Bit Microcontroller **2-1**

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MICROCHIP

PIC12C5XX

8-Pin, 8-Bit CMOS Microcontroller

Devices included in this Data Sheet:

PIC12C508 and PIC12C509 are 8-bit microcontrollers packaged in 8-lead packages. They are based on the Enhanced PIC16C5X family.

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (1 µs) except for program branches which are two-cycle
- Operating speed: DC - 4 MHz clock input
  DC - 1 µs instruction cycle

Device	EPROM	RAM
PIC12C508	512 x 12	25
PIC12C509	1024 x 12	41

- 12-bit wide instructions
- 8-bit wide data path
- Seven special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions
- Internal 4 MHz RC oscillator with programmable calibration
- In-circuit serial programming

Peripheral Features:

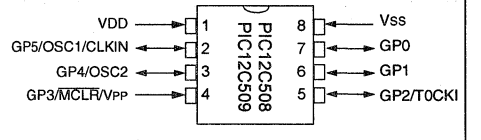
- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Wake-up from SLEEP on pin change
- Internal pull-ups on I/O pins
- Selectable oscillator options:
  - INTRC: Internal 4 MHz RC oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - LP: Power saving, low frequency crystal
- Internal pull-up on $\overline{MCLR}$ pin

CMOS Technology:

- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.5V to 5.5V
  - Industrial: 2.5V to 5.5V
- Low power consumption
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz
  - < 1 µA typical standby current

Pin Diagram

PDIP, SOIC



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To Our Valued Customers

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1.0 GENERAL DESCRIPTION

The PIC12C5XX from Microchip Technoiogy is a family of low-cost, high performance, 8-bit, fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/ single cycle instructions. All instructions are single cycle (1 µs) except for program branches which take two cycles. The PIC12C5XX delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC12C5XX products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including INTRC internal oscillator mode and the power-saving LP (Low Power) oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC12C5XX are available in the cost-effective One-Time-Programmable (OTP) versions which are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC12C5XX products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC12C5XX series fits perfectly in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The EPROM technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC12C5XX series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic and PLD's in larger systems, coprocessor applications).

TABLE 1-1: PIC12C5XX FAMILY OF DEVICES

	Clock	Memory			Peripherals		Features				
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (words)	Data Memory (bytes)	Timer Module(s)	Wake-up from SLEEP on pin change	I/O Pins	Input Pins	Internal Pull-ups	Voltage Range (Volts)	In-Circuit Serial Programming	Number of Instructions	Packages
PIC12C508	4	512	25	TMR0	Yes	5	1	Yes	2.5-5.5	Yes	33	8-pin PDIP, 8-pin SOIC
PIC12C509	4	1024	41	TMR0	Yes	5	1	Yes	2.5-5.5	Yes	33	8-pin PDIP, 8-pin SOIC

All PIC12C5XX devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC12C5XX devices use serial programming with data pin GP0 and clock pin GP1.

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2.0 PIC12C5XX DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12C5XX Product Identification System at the back of this data sheet to specify the correct part number.

2.1 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12C5XX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC12C5XX uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (1µs @ 4MHz) except for program branches.

The PIC12C508 address 512 x 12 of program memory, the PIC12C509 addresses 1K x 12 of program memory. All program memory is internal.

The PIC12C5XX can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC12C5XX has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC12C5XX simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC12C5XX device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

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FIGURE 3-1: PIC12C5XX BLOCK DIAGRAM

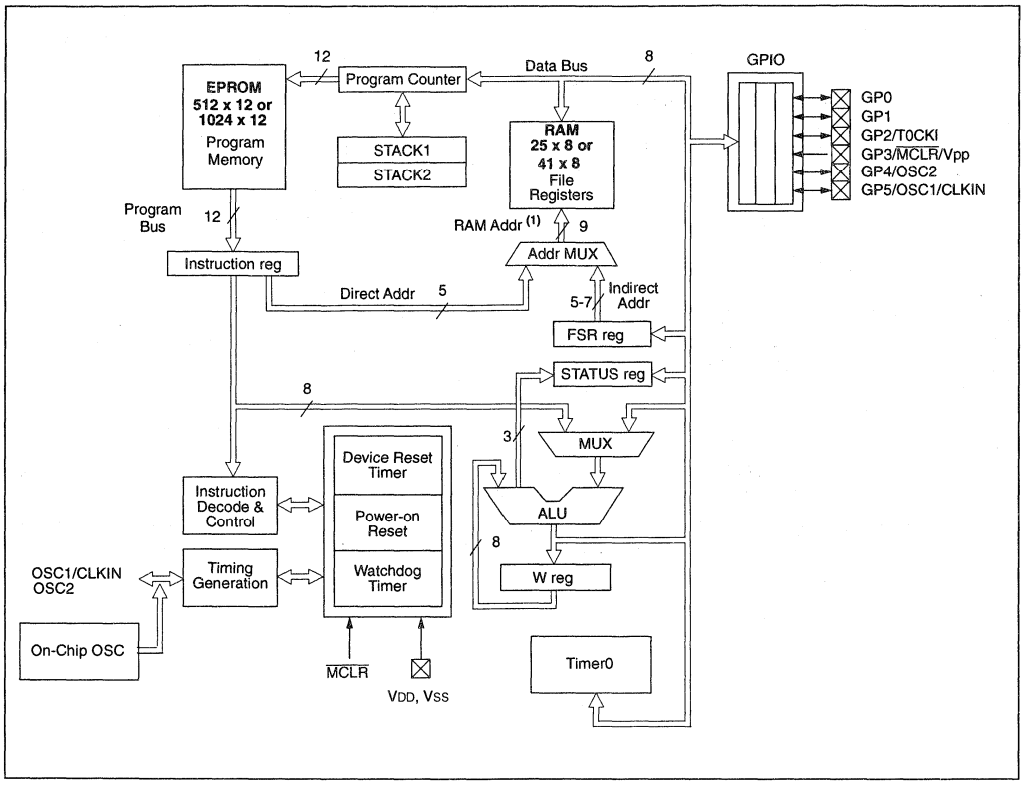

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TABLE 3-1: PIC12C5XX PINOUT DESCRIPTION

Name	DIP Pin #	SOIC Pin #	I/O/P Type	Buffer Type	Description
GP0	7	7	I/O	TTL/ST	Bi-directional I/O port/ serial programming clock. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP1	6	6	I/O	TTL/ST	Bi-directional I/O port/ serial programming data. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP2/T0CKI	5	5	I/O	ST	Bi-directional I/O port. Can be configured as T0CKI.
GP3/$\overline{\text{MCLR}}$/VPP	4	4	I	TTL	Input port/master clear (reset) input/programming voltage input. When configured as $\overline{\text{MCLR}}$, this pin is an active low reset to the device. Voltage on $\overline{\text{MCLR}}$/VPP must not exceed VDD during normal device operation. Can be software programmed for internal weak pull-up and wake-up from SLEEP on pin change. Weak pull-up always on if configured as $\overline{\text{MCLR}}$
GP4/OSC2	3	3	I/O	TTL	Bi-directional I/O port/oscillator crystal output. Connections to crystal or resonator in crystal oscillator mode (XT and LP modes only, GPIO in other modes).
GP5/OSC1/CLKIN	2	2	I/O	TTL/ST	Bidirectional IO port oscillator crystal input/external clock source input (GPIO in Internal RC mode only, OSC1 in all other oscillator modes).
VDD	1	1	P	—	Positive supply for logic and I/O pins
VSS	8	8	P	—	Ground reference for logic and I/O pins

Legend: I = input, O = output, I/O = input/output, P = power, — = not used, TTL = TTL input, ST = Schmitt Trigger input

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

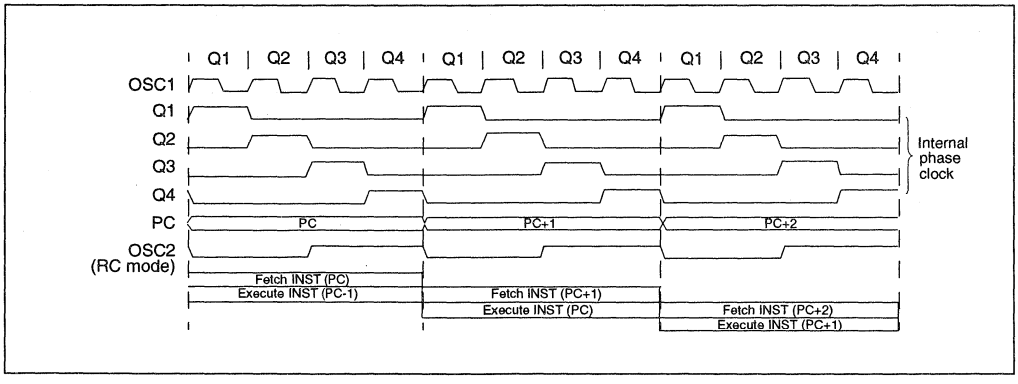
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

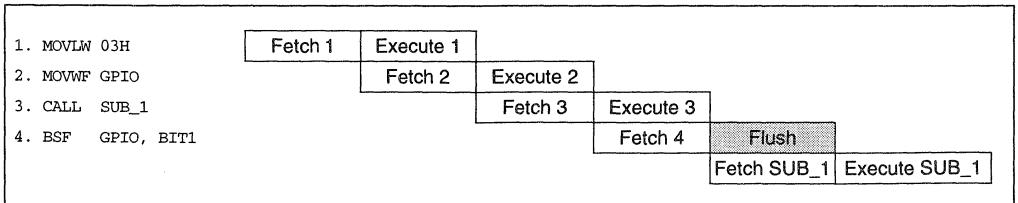
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 MEMORY ORGANIZATION

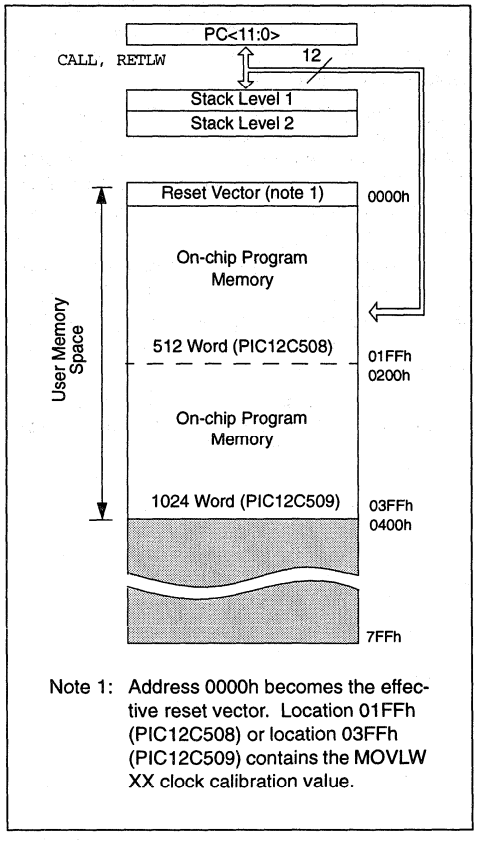
PIC12C5XX memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one STATUS register bit. For the PIC12C509 with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Select Register (FSR).

4.1 Program Memory Organization

The PIC12C508 and PIC12C509 each have a 12-bit Program Counter (PC) capable of addressing a 2K x 12 program memory space.

Only the first 512 x 12 (0000h-01FFh) for the PIC12C508 and 1K x 12 (0000h-03FFh) for the PIC12C509 are physically implemented. Refer to Figure 4-1. Accessing a location above these boundaries will cause a wrap-around within the first 512 x 12 space (PIC12C508) or 1K x 12 space (PIC12C509). The reset vector is at 0000h. Location 01FFh (PIC12C508) or location 03FFh (PIC12C509) contains the internal clock oscillator calibration value. This value should never be overwritten.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12C5XX



Note 1: Address 0000h becomes the effective reset vector. Location 01FFh (PIC12C508) or location 03FFh (PIC12C509) contains the MOVLW XX clock calibration value.

2

4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC12C508, the register file is composed of 7 special function registers and 25 general purpose registers (Figure 4-2).

For the PIC12C509, the register file is composed of 7 special function registers, 25 general purpose registers, and 16 general purpose registers that may be addressed using a banking scheme (Figure 4-3).

4.2.1 GENERAL PURPOSE REGISTER FILE

The general purpose register file is accessed either directly or indirectly through the file select register FSR (Section 4.7).

FIGURE 4-2: PIC12C508 REGISTER FILE MAP

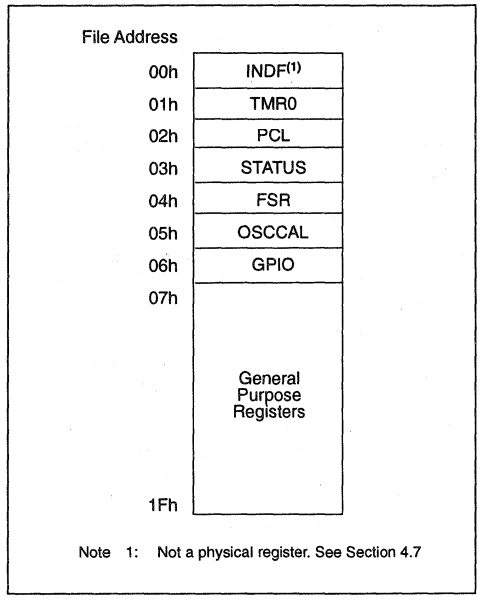
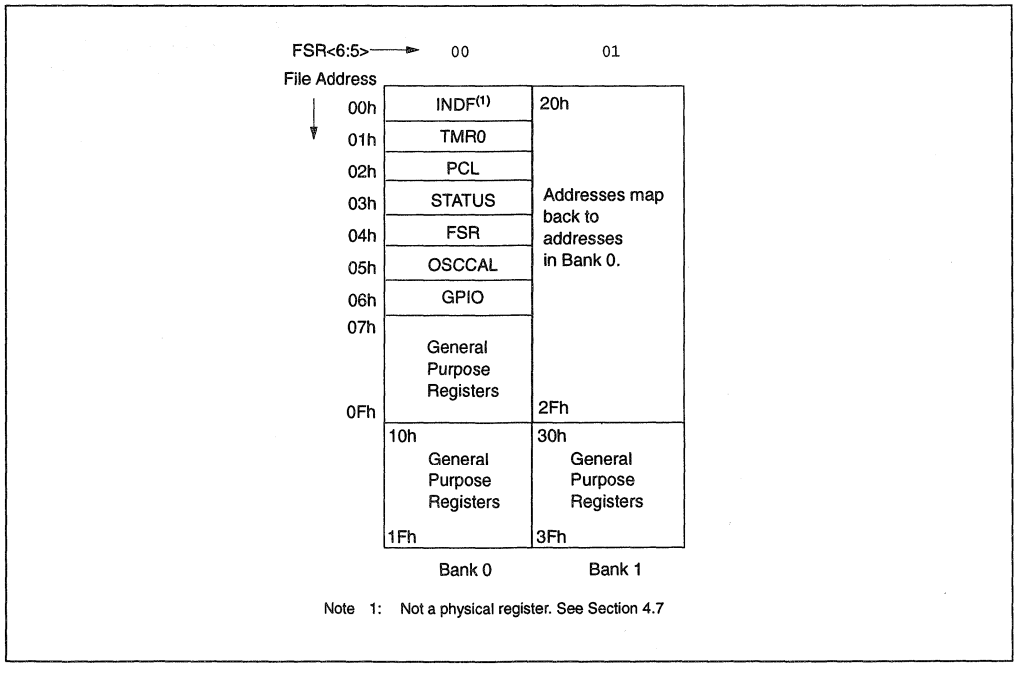


FIGURE 4-3: PIC12C509 REGISTER FILE MAP



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4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset	Value on Wake-up on Pin Change
N/A	TRIS	I/O control registers								--11 1111	--11 1111	--11 1111
N/A	OPTION	Contains control bits to configure Timer0, Timer0/WDT prescaler, interrupt on change, and weak pull-ups								1111 1111	1111 1111	1111 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu	uuuu uuuu
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111	1111 1111
03h	STATUS	GPWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu	100q quuu
04h	FSR (12C508)	Indirect data memory address pointer								111x xxxx	111u uuuu	111u uuuu
04h	FSR (12C509)	Indirect data memory address pointer								110x xxxx	11uu uuuu	11uu uuuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu	1uuu uuuu
05h	OSCCAL	CAL7	CAL6	CAL5	CAL4	—	—	—	—	0111 ----	uuuu ----	uuuu ----
06h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu	--uu uuuu

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 7.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 for an explanation of how to access these bits.

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bit for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Instruction Set Summary.

FIGURE 4-4: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
GPWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **GPWUF**: GPIO reset bit
1 = Reset from wake-up from SLEEP on pin change
0 = After power up or other reset

bit 6: **Unimplemented**

bit 5: **PA0**: Program page preselect bits
1 = Page 1 (200h - 3FFh) - PIC12C509
0 = Page 0 (000h - 1FFh) - PIC12C508 and PIC12C509
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: $\overline{TO}$: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: $\overline{PD}$: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF	SUBWF	RRF or RLF
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSB or MSB, respectively
0 = A carry did not occur	0 = A borrow occurred	

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4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<7:0> bits.

Note that TRIS overrides OPTION control if $\overline{GPPU}$ is enabled and $\overline{GPWU}$ is disabled.

Note: If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin.

Note: If the TOCS bit is set to '1', GP2 is forced to be an input even if TRIS GP2 = '0'

FIGURE 4-5: OPTION REGISTER

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset
Reference Table 4-1 for other resets.

bit 7: **$\overline{GPWU}$**: Enable wake-up on pin change (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6: **$\overline{GPPU}$**: Enable weak pull-ups (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Transition on internal instruction cycle clock, Fosc/4

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high to low transition on the T0CKI pin
0 = Increment on low to high transition on the T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

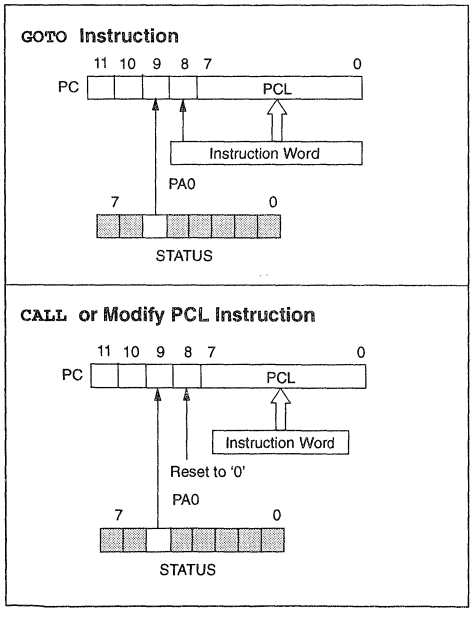
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-6).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-6).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC,5.

Note: Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-6: LOADING OF PC BRANCH INSTRUCTIONS - PIC12C508/C509



4.5.1 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the oscillator calibration instruction. After executing MOVLW XX, the PC will roll over to location 00h, and begin executing user code.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.6 Stack

PIC12C5XX devices have a 12-bit wide hardware push/pop stack.

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

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4.7 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x10    ;initialize pointer
        movwf   FSR     ; to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR,F   ;inc pointer
        btfsc   FSR,4   ;all done?
        goto    NEXT    ;NO, clear next
CONTINUE
        :               ;YES, continue
```

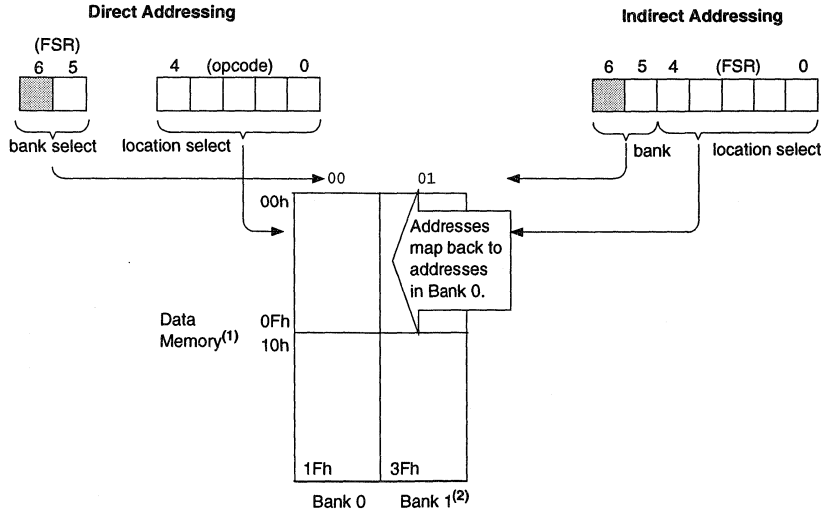
The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC12C508: Does not use banking. FSR<6:5> are unimplemented and read as '1's.

PIC12C509: Uses FSR<5>. Selects between bank 0 and bank 1. FSR<6> is unimplemented, read as '1'.

FIGURE 4-7: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Section 4.2.

Note 2: PIC12C509 only

NOTES:

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5.0 I/O PORT

As with any other register, the I/O register can be written and read under program control. However, read instructions (e.g., `MOVF GPIO,W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers are all set. GP0 and GP1 can be programmed in software with weak pull-ups.

5.1 GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP5:GP0). Bits 7 and 6 are unimplemented and read as '0's. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions the pins will read as '0' during port read. Pins GP0, GP1, and GP3 can be configured with weak pull-ups and also with wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If pin 4 is configured as $\overline{MCLR}$, weak pull-up is always on and wake-up on change for this pin is not set.

5.2 TRIS Register

The output driver control register is loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are GP3 which is input only and GP2 which may be controlled by the option register, see Section 4.4.

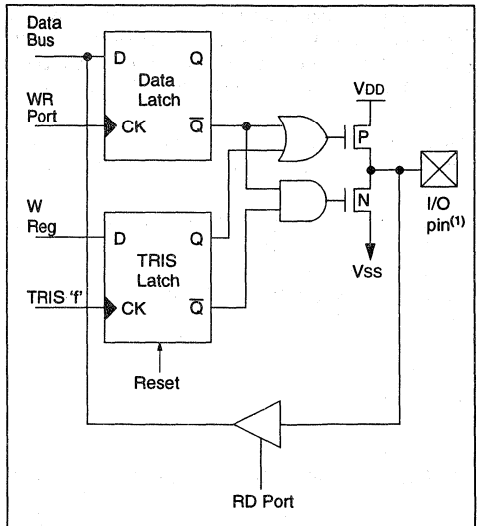
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.3 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins, except GP3 which is input only, may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF GPIO,W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset	Value on Wake-up on Pin Change
N/A	TRIS	I/O control registers								--11 1111	--11 1111	--11 1111
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111	1111 1111
03H	STATUS	GPWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu	100q quuu
06h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu	--uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = see tables in Section 7.7 for possible values.

5.4 I/O Programming Considerations

5.4.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit5 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

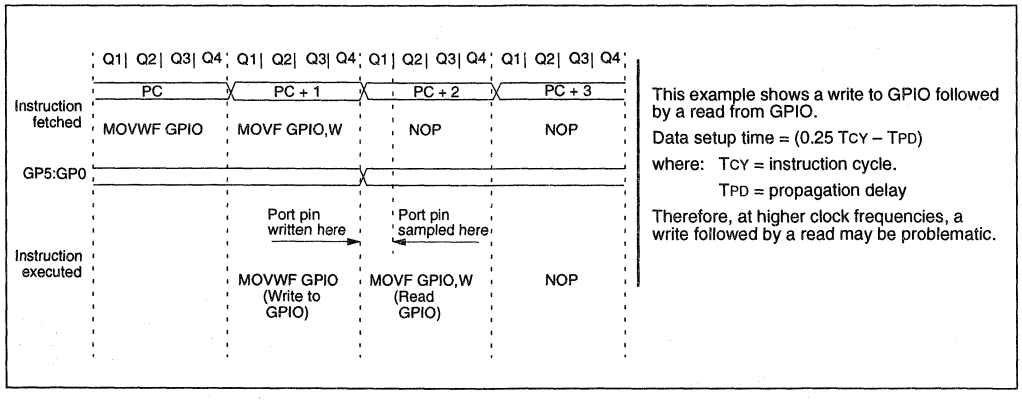
EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial GPIO Settings
; GPIO<5:3> Inputs
; GPIO<2:0> Outputs
;GPIO<6> have external pull-ups and are
;not connected to other circuitry
;
;                    GPIO latch  GPIO pins
;                    ----------  ----------
  BCF   GPIO, 5    ;--01 -ppp   --11 pppp
  BCF   GPIO, 4    ;--10 -ppp   --11 pppp
  MOVLW 007h        ;
  TRIS  GPIO       ;--10 -ppp   --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;GP4 to be latched as the pin value (High).
```

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-2: SUCCESSIVE I/O OPERATION



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6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

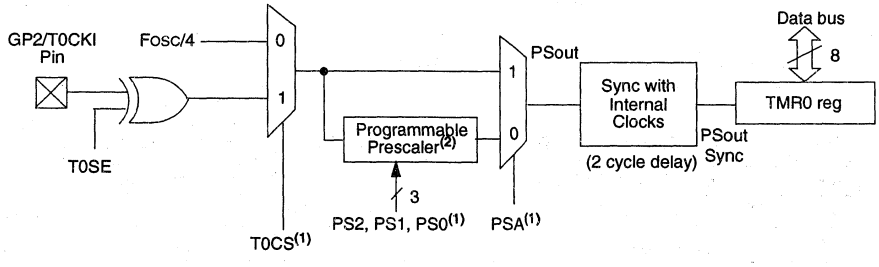
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

2

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-5).

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

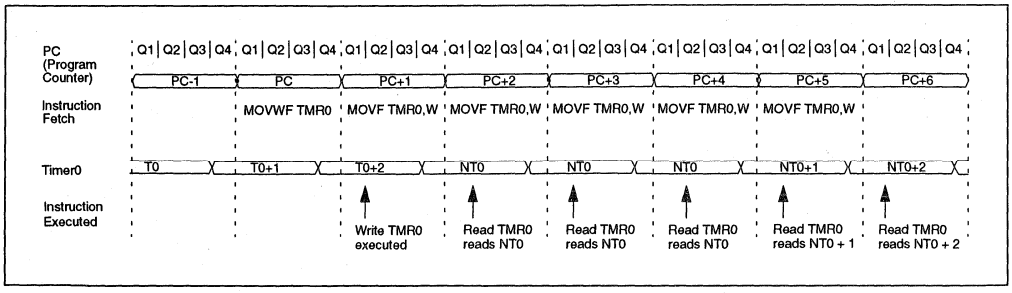


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

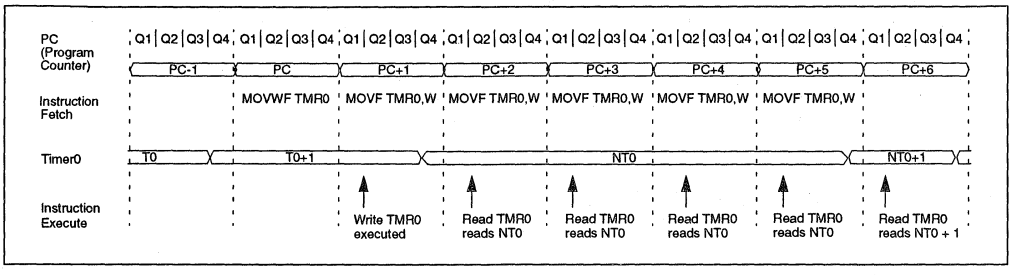


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset	Value on Wake-up on Pin Change
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu	uuuu uuuu
N/A	OPTION	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111	1111 1111
N/A	TRIS	I/O control registers								--11 1111	--11 1111	--11 1111

Legend: Shaded cells not used by Timer0, - = unimplemented, x = unknown, u = unchanged,

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6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

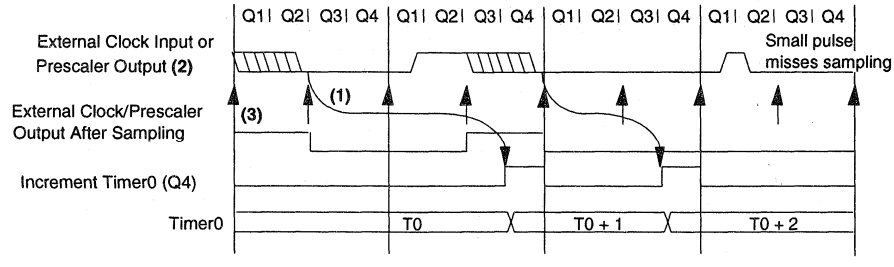
6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

6.1.3 OPTION REGISTER EFFECT ON GP2 TRIS

If the option register is set to read TIMER0 from the pin, the port is forced to an input regardless of the TRIS register setting.

FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 7.6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the

following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

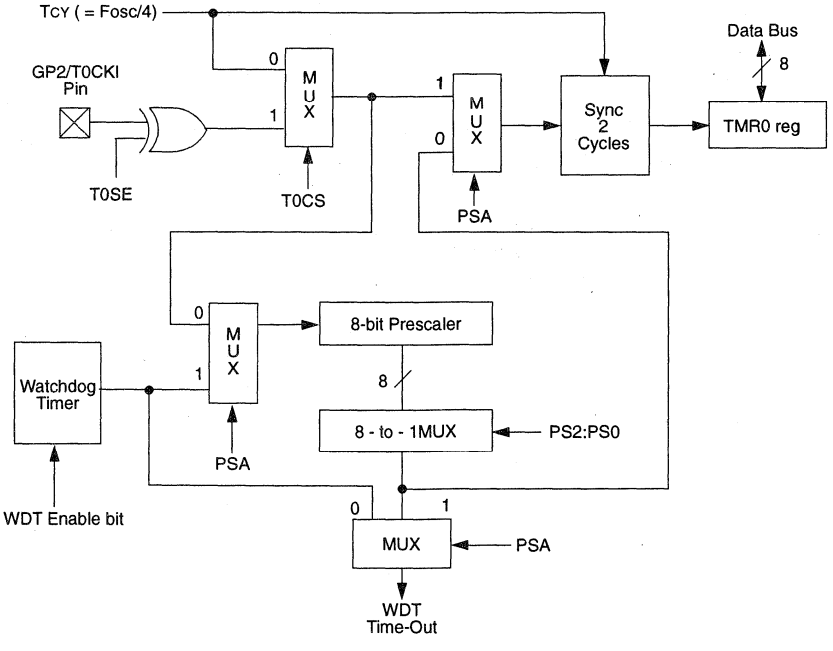
```
CLRF    TMR0            ;Clear TMR0
CLRWDT                  ;Clears WDT and
                        ;prescaler
MOVLW   'xxxx1xxx'      ;Select new prescale
OPTION                  ;value
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ;prescaler
MOVLW   'xxxx0xxx'      ;Select TMR0, new
                        ;prescale value and
                        ;clock source
OPTION
```

FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

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7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC12C5XX family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- Reset
  - Power-On Reset (POR)
  - Device Reset Timer (DRT)
  - Wake-up from SLEEP on pin change
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit Serial Programming

The PIC12C5XX has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. If using XT or LP selectable oscillator options, there is always an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. If using INTRC or EXTRC there is an 18 ms delay only on VDD power-up. With this timer on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through a change on input pins or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4 MHz oscillator. The EXTRL RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

The PIC12C5XX configuration word consists of 5 bits. Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type, one bit is the Watchdog Timer enable bit, and one bit is the $\overline{MCLR}$ enable bit. One bit is the code protection bit (Figure 7-1).

OTP devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" on the inside back cover).

FIGURE 7-1: CONFIGURATION WORD FOR PIC12C508 OR PIC12C509

—	—	—	—	—	—	—	MCLRE	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address(1): FFFh

bit 11-5: **Unimplemented**

bit 4: **MCLRE:** $\overline{MCLR}$ enable bit.
1 = $\overline{MCLR}$ enabled
0 = $\overline{MCLR}$ disabled

bit 3: **CP:** Code protection bit.
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits
11 = EXTRC - external RC oscillator
10 = INTRC - internal RC oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC12C5XX Programming Specifications to determine how to access the configuration word. This register is not user addressable during device operation.

7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

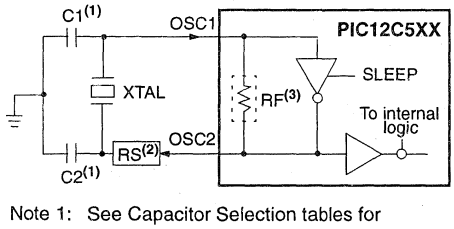
The PIC12C5XX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz Oscillator
- EXTRC: External Resistor/Capacitor

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 7-2). The PIC12C5XX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 7-3).

FIGURE 7-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen (approx. value = 10 MΩ).

FIGURE 7-3: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)

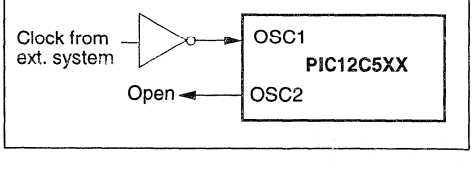


TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12C5XX

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12C5XX

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF

Note 1: For $V_{DD} > 4.5V$, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

PRELIMINARY

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7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 7-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 7-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

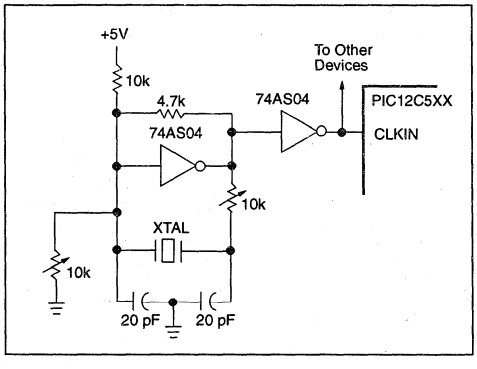
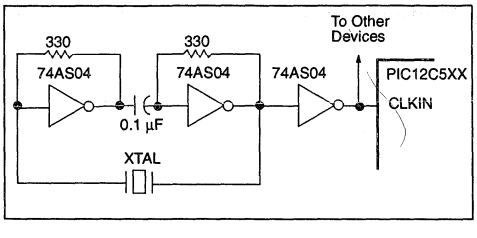


Figure 7-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



7.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

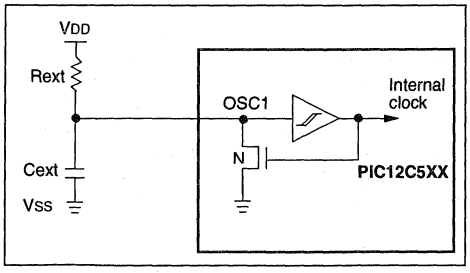
Figure 7-6 shows how the R/C combination is connected to the PIC12C5XX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

FIGURE 7-6: RC OSCILLATOR MODE



7.2.5 INTERNAL 4 MHZ RC OSCILLATOR

The internal RC oscillator provides a fixed 4 MHz (nominal) system clock.

In addition, a calibration instruction is programmed into the top of memory which indicates the calibration value for the internal RC oscillator. This value, OSCCAL, is programmed as a `MOVLW XX` instruction where XX is the calibration value, and is placed at the reset vector. This will load the W register with the calibration value upon reset and the PC will then roll over to 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

7.3 RESET

The device differentiates between various kinds of reset:

a) Power on reset (POR)

b) $\overline{\text{MCLR}}$ reset during normal operation

c) $\overline{\text{MCLR}}$ reset during SLEEP

d) WDT time-out reset during normal operation

e) WDT time-out reset during SLEEP

f) Wake-up from SLEEP on pin change

Some registers are not reset in any way; they are unknown on POR and unchanged in any other reset. Most other registers are reset to "reset state" on power-on reset (POR), on $\overline{\text{MCLR}}$ or WDT reset during normal operation. They are not affected by a WDT reset during SLEEP or $\overline{\text{MCLR}}$ reset during SLEEP, since these resets are viewed as resumption of normal operation. The exceptions to this are $\overline{\text{TO}}$, $\overline{\text{PD}}$, and GPWUF bits. They are set or cleared differently in different reset situations. These bits are used in software to determine the nature of reset. See Table 7-3 for a full description of reset states of all registers.

TABLE 7-3: RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT time-out Wake-up on Pin Change
W	—	qqqq xxxx (1)	qqqq uuuu (1)
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	?00? ?uuu (2)
FSR (12C508)	04h	111x xxxx	111u uuuu
FSR (12C509)	04h	110x xxxx	11uu uuuu
OSCCAL	05h	0111 ----	uuuu ----
GPIO	06h	--xx xxxx	--uu uuuu
OPTION	—	1111 1111	1111 1111
TRIS	—	--11 1111	--11 1111

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', ? = value depends on condition.

Note 1: Bits <7:4> of W register contain oscillator calibration (OSCCAL) values due to `MOVLW XX` instruction at top of memory.

Note 2: See Table 7-6 for reset value for specific conditions

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TABLE 7-4: RESET CONDITION FOR SPECIAL REGISTERS

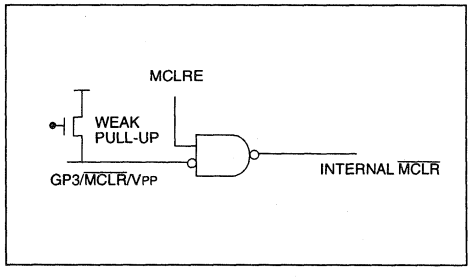
	STATUS Addr: 03h	PCL Addr: 02h
Power on reset	0001 1xxx	1111 1111
$\overline{MCLR}$ reset during normal operation	000u uuuu	1111 1111
$\overline{MCLR}$ reset during SLEEP	0001 0uuuu	1111 1111
WDT reset during SLEEP	0000 0uuu	1111 1111
WDT reset normal operation	0000 1uuu	1111 1111
Wake-up from SLEEP on pin change	1001 0uuu	1111 1111

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'.

7.3.1 $\overline{MCLR}$ ENABLE

This configuration bit when unprogrammed (left in the '1' state) enables the external $\overline{MCLR}$ function. When programmed, the $\overline{MCLR}$ function is tied to the internal VDD, and the pin is assigned to be a GPIO. See Figure 7-7.

FIGURE 7-7: $\overline{MCLR}$ SELECT



7.4 Power-On Reset (POR)

The PIC12C5XX family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations.

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, tie the $\overline{MCLR}$ pin directly to VDD. An internal weak pull-up resistor is implemented using a transistor. Refer to Table 8-5 for the pull-up resistor ranges. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 7-8.

The Power-On Reset circuit and the Device Reset Timer (Section 7.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

A power-up example where $\overline{MCLR}$ is tied to VSS is shown in Figure 7-9. VDD is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset TDRT msec after $\overline{MCLR}$ goes high.

In Figure 7-10, the on-chip Power-On Reset feature is being used ($\overline{MCLR}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 7-11 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the GP3/$\overline{MCLR}$/VPP pin, and when the GP3/$\overline{MCLR}$/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 7-10).

Note:	When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information refer to Application Notes *"Power-Up Considerations"* - AN522 and *"Power-up Trouble Shooting"* - AN607.

FIGURE 7-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

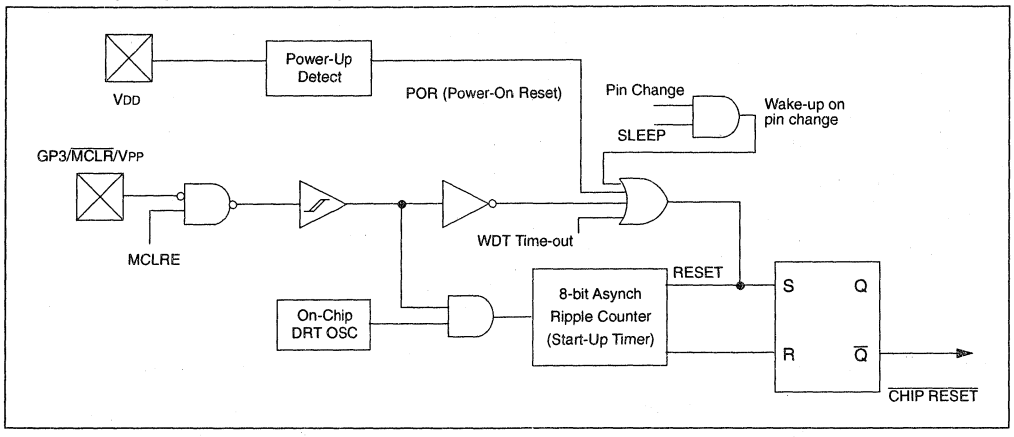


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FIGURE 7-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ PULLED LOW)

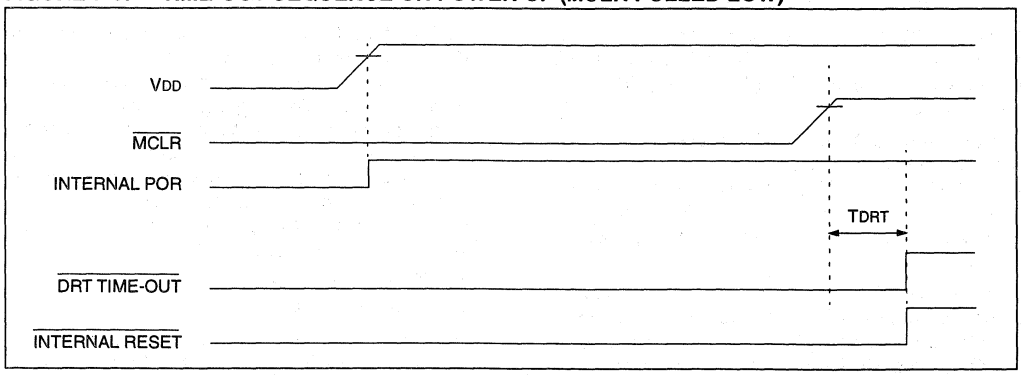


FIGURE 7-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD): FAST VDD RISE TIME

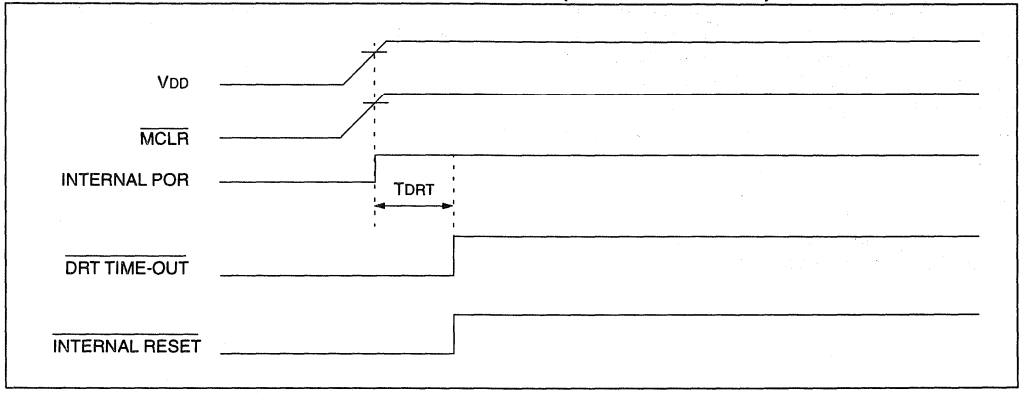
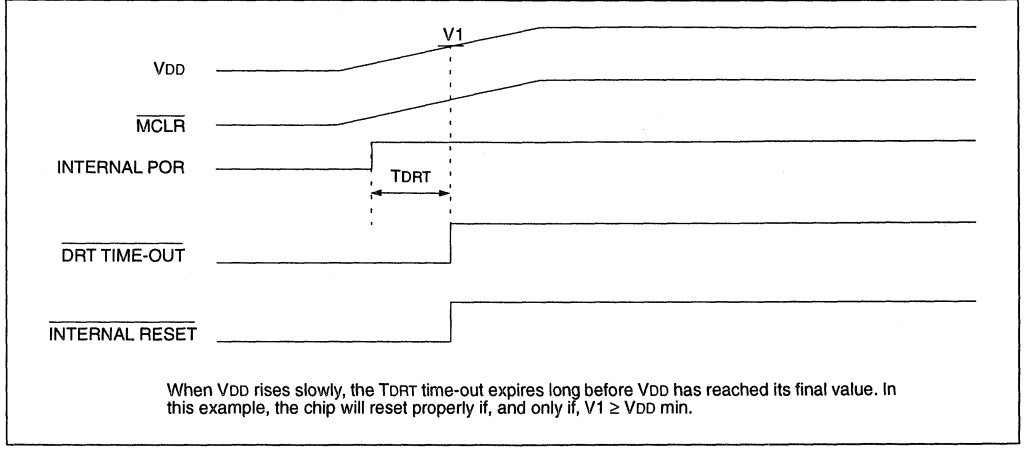


FIGURE 7-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD): SLOW VDD RISE TIME



When VDD rises slowly, the TDRT time-out expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ VDD min.

7.5 Device Reset Timer (DRT)

In the PIC12C5XX, the DRT runs any time the device is powered up. DRT runs from RESET only in XT and LP modes. It is disabled from RESET in INTRC and EXTRC modes.

The Device Reset Timer (DRT) provides a fixed 18 ms nominal time-out on reset. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the GP3/$\overline{\text{MCLR}}$/VPP pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the $\overline{\text{MCLR}}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out (only in XT and LP modes). This is particularly important for applications using the WDT to wake from SLEEP mode automatically.

7.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the external RC oscillator of the GP5/OSC1/CLKIN pin and the internal 4 MHz oscillator. That means that the WDT will run even if the clock on the GP5/OSC1/CLKIN and GP4/OSC2 pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC12C5XX Programming Specifications to determine how to access the configuration word.

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7.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

FIGURE 7-12: WATCHDOG TIMER BLOCK DIAGRAM

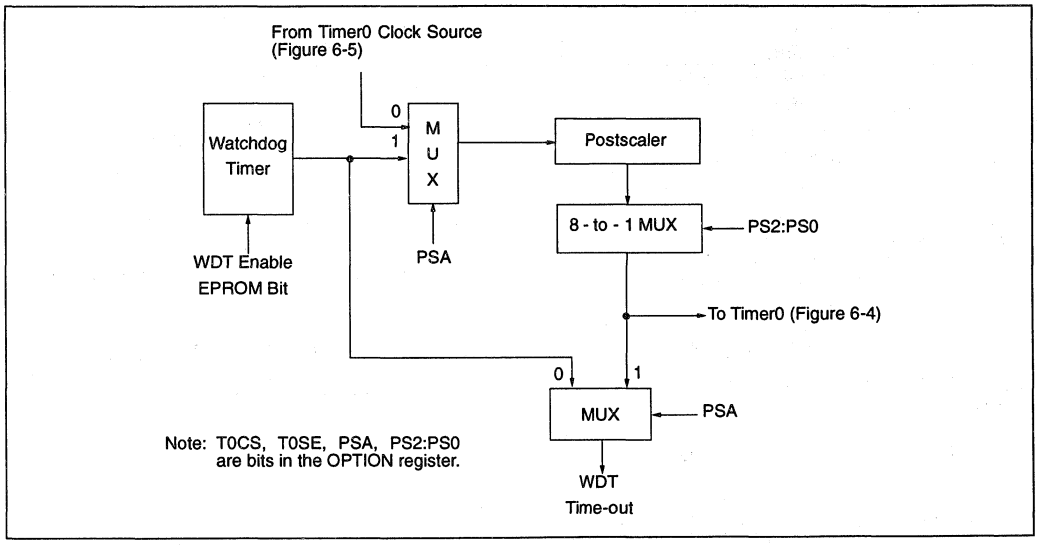


TABLE 7-5: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset	Value on Wake-up on Pin Change
N/A	OPTION	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer, – = unimplemented, read as '0', u = unchanged

7.7 Time-Out Sequence, Power Down, and Wake-up from SLEEP Status Bits (TO/PD/GPWUF)

The $\overline{TO}$, $\overline{PD}$, and GPWUF bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) reset, or a $\overline{MCLR}$ or WDT reset.

TABLE 7-6: $\overline{TO}$/$\overline{PD}$/GPWUF STATUS AFTER RESET

GPWUF	$\overline{TO}$	$\overline{PD}$	RESET caused by
0	0	0	WDT wake-up from SLEEP
0	0	1	WDT time-out (not from SLEEP)
0	1	0	$\overline{MCLR}$ wake-up from SLEEP
0	1	1	Power-up
0	u	u	$\overline{MCLR}$ not during SLEEP
1	1	0	Wake-up from SLEEP on pin change

Legend: Legend: u = unchanged
Note 1: The $\overline{TO}$, $\overline{PD}$, and GPWUF bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$, and GPWUF status bits.

These STATUS bits are only affected by events listed in Table 7-7.

TABLE 7-7: EVENTS AFFECTING $\overline{TO}$/$\overline{PD}$ STATUS BITS

Event	GPWUF	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	0	1	1	
WDT Time-out	0	0	u	No effect on $\overline{PD}$
SLEEP instruction	u	1	0	
CLRWDT instruction	u	1	1	
Wake-up from SLEEP on pin change	1	1	0	

Legend: u = unchanged
A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 7-6 reflects the status of $\overline{TO}$ and $\overline{PD}$ after the corresponding event.

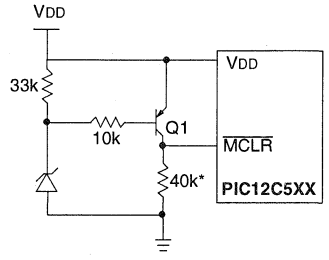
Table 7-4 lists the reset conditions for the special function registers, while Table 7-3 lists the reset conditions for all the registers.

7.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12C5XX devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-13 and Figure 7-14.

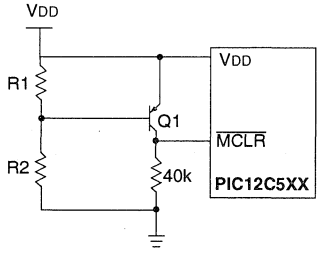
FIGURE 7-13: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

*Refer to Figure 7-7 and Table 8-5 for internal weak pull-up on $\overline{MCLR}$.

FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

*Refer to Figure 7-7 and Table 8-5 for internal weak pull-up on $\overline{MCLR}$.

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7.9 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

7.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the GP3/$\overline{MCLR}$/VPP pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or VSS and the GP3/$\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC) if $\overline{MCLR}$ is enabled.

7.9.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. An external reset input on GP3/$\overline{MCLR}$/VPP pin.
2. A Watchdog Timer time-out reset (if WDT was enabled).
3. A change on input pin GP0, GP1, or GP3

These events cause a device reset. The $\overline{TO}$, $\overline{PD}$, and GPWUF bits can be used to determine the cause of device reset.. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF bit indicates a change in state while in SLEEP at pins GP0, GP1, or GP3 (since the last time there was a file or bit operation on GP port).

Caution: Right before entering SLEEP, read the input pins. When in SLEEP, wake up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before reentering SLEEP, a wake up will occur immediately even if no pins change while in SLEEP mode.

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

7.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

2

7.12 In-Circuit Serial Programming

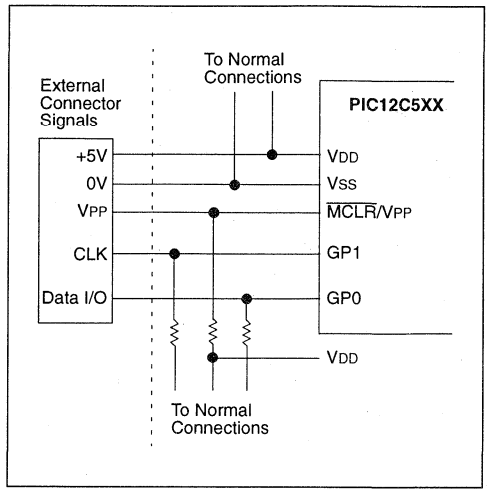
The PIC12C5XX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the GP1 and GP0 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). GP1 becomes the programming clock and GP0 becomes the programming data. Both GP1 and GP0 are Schmitt Trigger inputs in this mode.

After reset, a 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC12C5XX Programming Specifications.

A typical in-circuit serial programming connection is shown in Figure 7-15.

FIGURE 7-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



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8.0 ELECTRICAL CHARACTERISTICS - PIC12C5XX

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –40°C to +85°C
Storage Temperature ..... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14 V
Voltage on all other pins with respect to V_{SS} ..... –0.6 V to (V_{DD} + 0.6 V)
Total Power Dissipation (1) ..... 700 mW
Max. Current out of V_{SS} pin ..... 200 mA
Max. Current into V_{DD} pin ..... 150 mA
Max. Current into V_{DD} pin (Vclamp active) ..... 100 mA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. Output Current sunk by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin ..... 25 mA
Max. Output Current sourced by I/O port (PORTA) ..... 100 mA
Max. Output Current sourced by I/O port with V_{DD} clamp active(PORTA) ..... 50 mA
Max. Output Current sunk by I/O port (PORTA) ..... 100 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD}-V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100W should be used when applying a low level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFORMATION

8.1 DC CHARACTERISTICS: PIC12508/509 (Commercial) PIC12508/509 (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5		5.5	V	FOSC = DC to 4 MHz
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See section on Power-on Reset for details
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See section on Power-on Reset for details
Supply Current(3)	IDD	—	1.8	2.4	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 5.5 V
		—	1.8	2.4	mA	INTRC Option FOSC = 4 MHz, VDD = 5.5 V
		—	15	27	µA	LP OPTION, Commercial Temperature FOSC = 32 kHz, VDD = 3.0 V, WDT disabled
		—	19	35	µA	LP OPTION, Industrial Temperature FOSC = 32 kHz, VDD = 3.0 V, WDT disabled
Power-Down Current (5)	IPD					
WDT Enabled		—	4	12	µA	VDD = 3.0 V, Commercial
		—	5	14	µA	VDD = 3.0 V, Industrial
WDT Disabled		—	0.25	4	µA	VDD = 3.0 V, Commercial
		—	0.3	5	µA	VDD = 3.0 V, Industrial

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

ADVANCE INFORMATION

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8.2 DC CHARACTERISTICS: PIC12508/509 (Commercial) PIC12508/509 (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 8.1.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$		VSS		0.15 VDD	V	
OSC1		VSS		0.15 VDD	V	EXTRC option only(4)
OSC1		VSS		0.3 VDD	V	XT and LP options
Input High Voltage						
I/O ports	VIH	2.0		VDD	V	4.0 V< VDD ≤ 5.5 V(5)
		0.2VDD+1V		VDD	V	Full VDD range(5)
$\overline{MCLR}$ (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	EXTRC option only(4)
		0.7 VDD		VDD	V	XT and LP options
Input Leakage Current(2,3)	IIL					For VDD ≤ 5.5 V
I/O ports		–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$		20	130	250	µA	VPIN = VSS + 0.25 V(2)
			0.5	+5	µA	VPIN = VDD
OSC1		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, XT and LP options
Output Low Voltage						
I/O ports	Vol			0.6	V	IOL = 8.7 mA, VDD = 4.5 V
Output High Voltage(3,4)						
I/O ports	VOH	VDD –0.7			V	IOH = –5.4 mA, VDD = 4.5 V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC12C5XX devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

ADVANCE INFORMATION

8.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

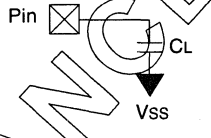
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 8-1: LOAD CONDITIONS - PIC12C5XX



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

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8.4 Timing Diagrams and Specifications

FIGURE 8-2: EXTERNAL CLOCK TIMING - PIC12C5XX

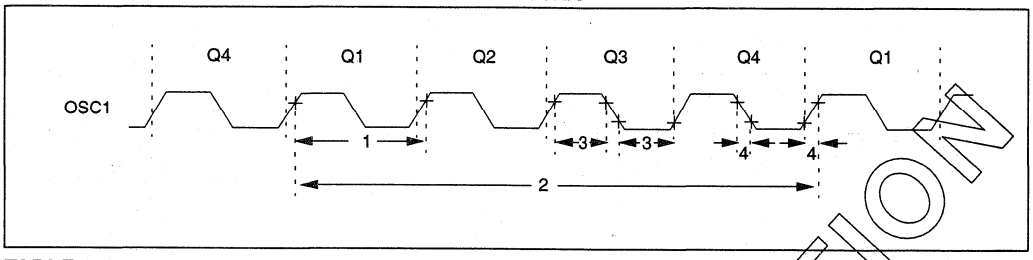

TABLE 8-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC12C5XX

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), Operating Voltage VDD range is described in Section 8.1

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4	MHz	EXTRC osc mode
			DC	—	4	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4	MHz	EXTRC osc mode
			0.1	—	4	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(2)	250	—	—	ns	EXTRC osc mode
			250	—	—	ns	XT osc mode
			5	—	—	ms	LP osc mode
		Oscillator Period(2)	250	—	—	ns	EXTRC osc mode
			250	—	10,000	ns	XT osc mode
			5	—	—	ms	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			2*	—	—	ms	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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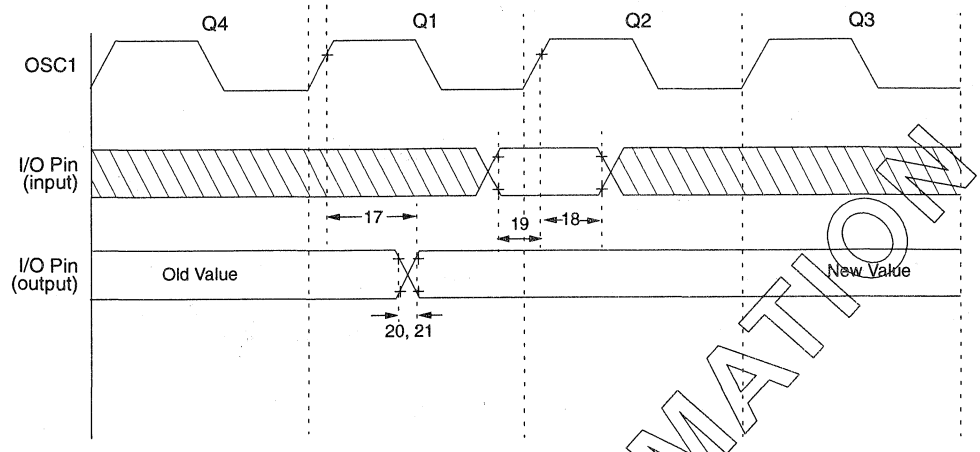
FIGURE 8-3: I/O TIMING - PIC12C5XX



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 8-2: TIMING REQUIREMENTS - PIC12C5XX

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 8.1					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 8-1 for loading conditions.

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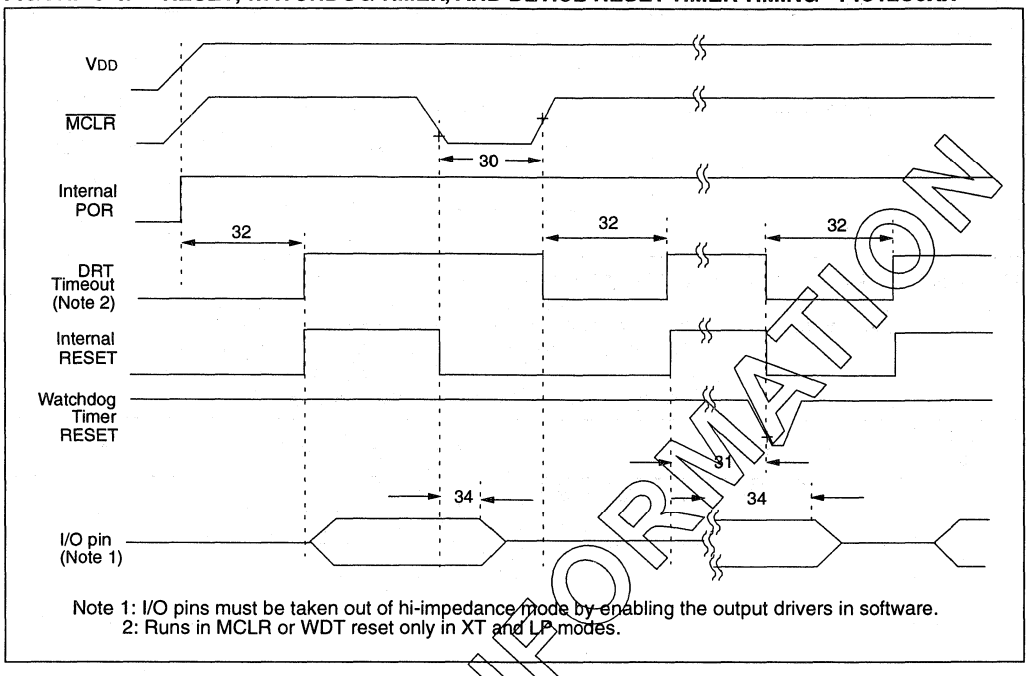
FIGURE 8-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC12C5XX



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.
2: Runs in MCLR or WDT reset only in XT and LP modes.

TABLE 8-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC12C5XX

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 8.1					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	MCLR Pulse Width (low)	2000*	—	—	ns	VDD = 5 V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	VDD = 5 V (Commercial)
32	TDRT	Device Reset Timer Period(2)	9*	18*	30*	ms	VDD = 5 V (Commercial)
34	TioZ	I/O Hi-impedance from MCLR Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested

2: DRT runs only on power-up and in normal execution in EXTRC and INTRC modes, and never runs in test modes. (i.e. does not run on wake-up from sleep)

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FIGURE 8-5: TIMER0 CLOCK TIMINGS - PIC12C5XX

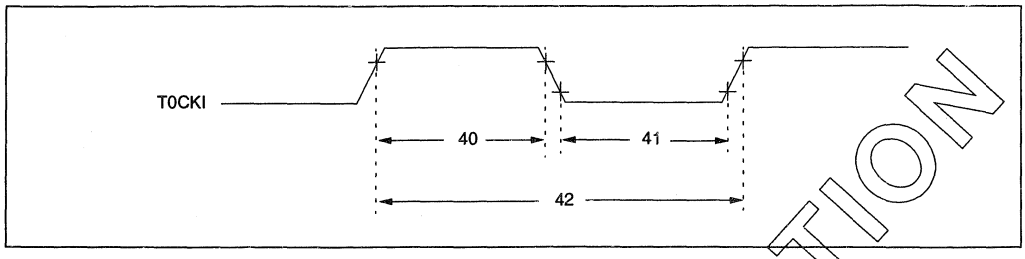

TABLE 8-4: TIMER0 CLOCK REQUIREMENTS - PIC12C5XX

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 8.1.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or TCY + 40* / N	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 8-5: $\overline{MCLR}$ PULL-UP RESISTOR RANGES

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
2.5	-40	43*	66	100*	kΩ
2.5	25	47*	74	111*	kΩ
2.5	85	50*	79	119*	kΩ
5.5	-40	25	36	48	kΩ
5.5	25	30*	42	56*	kΩ
5.5	85	32	46	63	kΩ

* These parameters are characterized but not tested.

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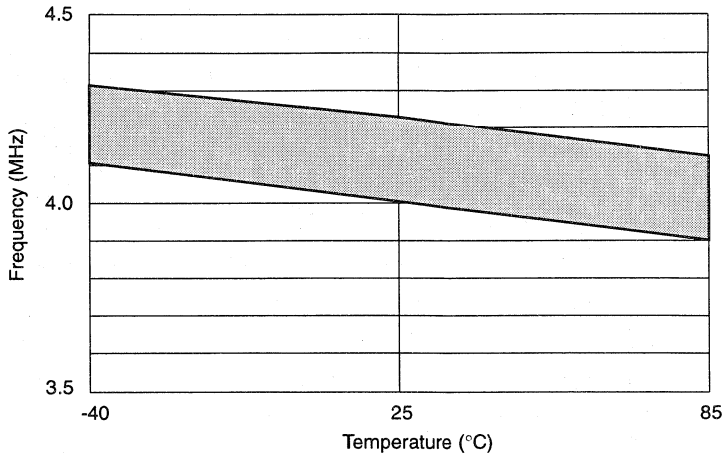
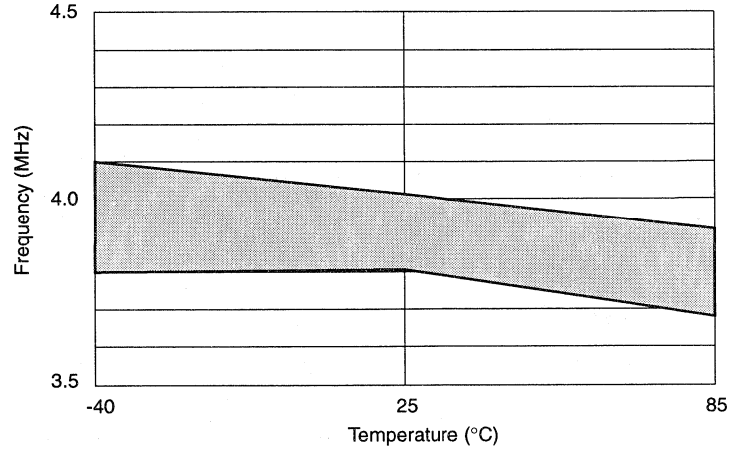
FIGURE 8-6: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (V_{DD} = 5.5V)



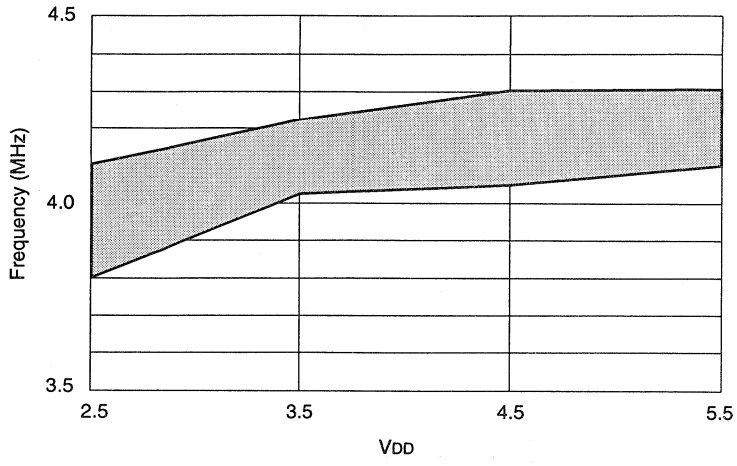
Note: Altering calibration value by 1 is approximately a 4ns change.

FIGURE 8-7: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (V_{DD} = 2.5V)



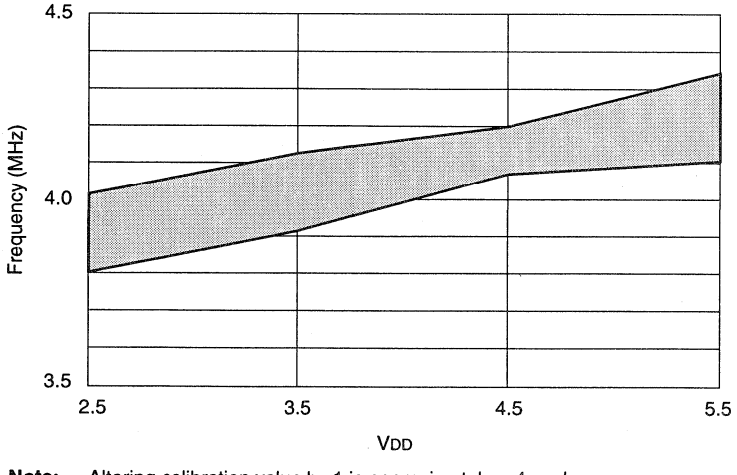
Note: Altering calibration value by 1 is approximately a 4ns change.

FIGURE 8-8: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. VDD AT TEMPERATURE = -40°C



Note: Altering calibration value by 1 is approximately a 4ns change.

FIGURE 8-9: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. VDD AT TEMPERATURE = 25°C



Note: Altering calibration value by 1 is approximately a 4ns change.

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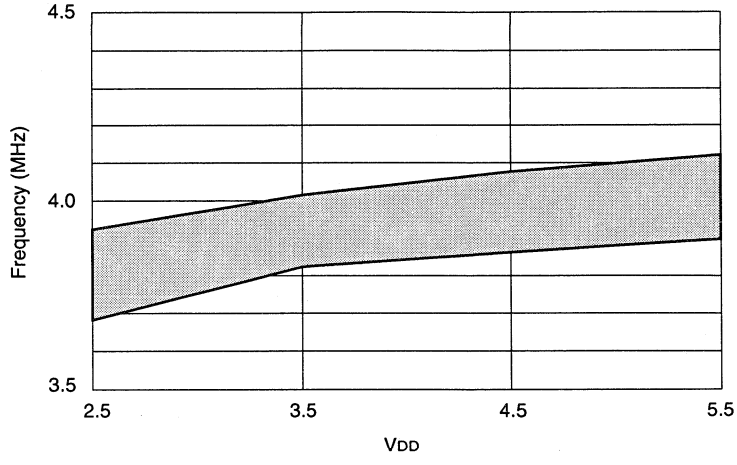
FIGURE 8-10: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. VDD AT TEMPERATURE = 85°C



Note: Altering calibration value by 1 is approximately a 4ns change.

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PIC12C5XX PRODUCT IDENTIFICATION SYSTEM

PART NO. -XX X /XX XXX

Pattern:	Special Requirements	
Package:	SM	= 200 mil SOIC
	P	= 300 mil PDIP
Temperature Range:	-	= 0°C to +70°C
	I	= -40°C to +85°C
Frequency Range:	04	= 4 MHz
Device	PIC12C508 PIC12C509 PIC12C508T (Tape & reel for SOIC only) PIC12C509T (Tape & reel for SOIC only)	

Examples

a) PIC12C508-04/P Commercial Temp., PDIP Package, 4 MHz, normal VDD limits

b) PIC12C508-04I/SM Industrial Temp., SOIC package, 4 MHz, normal VDD limits

c) PIC12C509-04I/P Industrial Temp., PDIP package, 4 MHz, normal VDD limits

Please contact your local sales office for exact ordering procedures.

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
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MICROCHIP

SECTION 3
PIC14000 MICROCONTROLLER PRODUCT SPECIFICATIONS

3

PIC14000 28-Pin Programmable Mixed Signal Controller 3-1

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PIC14000

28-Pin Programmable Mixed Signal Controller

High-Performance RISC CPU:

- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
- 4096 x 14 on-chip EPROM program memory
- 192 x 8 general purpose registers (SRAM)
- 6 internal and 5 external interrupt sources
- 38 special function hardware registers
- Eight-level hardware stack

Analog Peripherals Features:

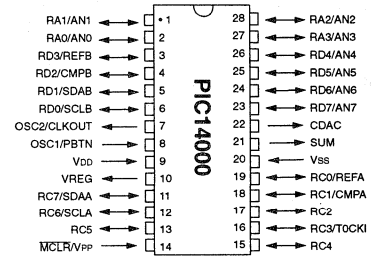
- Slope Analog-to-Digital (A/D) converter
  - Eight external input channels including two channels with selectable level shift inputs
  - Six internal input channels
  - 16-bit programmable timer with capture register
  - 16 ms maximum conversion time at maximum (16-bit) resolution and 4 MHz clock
  - 4-bit programmable current source
- Internal bandgap voltage reference
- Factory calibrated with calibration constants stored in EPROM
- On-chip temperature sensor
- Voltage regulator control output
- Two comparators with programmable references
- On-chip low voltage detector

Special Microcontroller Features:

- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Multi-segment programmable code-protection
- Selectable oscillator options
  - Internal 4 MHz oscillator
  - External crystal oscillator
- Serial in-system programming (via two pins)

Pin Diagram

PDIP, SOIC, SSOP, Windowed CERDIP



Digital Peripherals Features:

- 22 I/O pins with individual direction control
- High current sink/source for direct LED drive
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler
- 16-bit A/D timer: can be used as a general purpose timer
- I^2C^{TM} serial port compatible with System Management Bus

CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range (2.7V to 6.0V)
- Commercial and Industrial Temperature Range
- Low power dissipation (typical)
  - < 3 mA @5V, 4 MHz operating mode
  - < 300 µA @3V (Sleep mode: clocks stopped with analog circuits active)
  - < 5 µA @3V (Hibernate mode: clocks stopped, analog inactive, and WDT disabled)

Applications:

- Battery Chargers
- Battery Capacity Monitoring
- Uninterruptable Power Supply Controllers
- Power Management Controllers
- HVAC Controllers
- Sensing and Data Acquisition

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1.0 GENERAL DESCRIPTION

The PIC14000 features include medium to high resolution A/D conversion (10 to 16 bits), temperature sensing, closed loop charge control, serial communication, and low power operation.

The PIC14000 uses a RISC Harvard architecture CPU with separate 14-bit instruction and 8-bit data buses. A two-stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches, which require two cycles. A total of 35 instructions are available. Additionally, a large register set is included.

PIC16/17 microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers.

Features:

The PIC14000 is a 28-pin device with these features:

- 4K of EPROM
- 192 bytes of RAM
- 22 I/O pins

The analog peripherals include:

- 8 external analog input channels, two with level shift inputs
- 6 internal analog input channels
- 2 comparators with programmable references
- A bandgap reference
- An internal temperature sensor
- A programmable current source

In addition, the I^2C serial port through a multiplexer supports two separate I^2C channels.

A special oscillator option allows either an internal 4 MHz oscillator or an external crystal oscillator. Using the internal 4 MHz oscillator requires no external components.

The PIC14000 contains three timers, the Watchdog Timer (WDT), Timer0 (TMR0), and A/D Timer (ADTMR). The Watchdog Timer includes its own on-chip RC oscillator providing protection against software lock-up. TMR0 is a general purpose 8-bit timer/counter with an 8-bit prescaler. It may be clocked externally using the RC3/T0CKI pin. The ADTMR is intended for use with the slope A/D converter, but can also be used as a general purpose timer. It has an associated capture register which can be used to measure the time between events.

An internal low-voltage detect circuit allows for tracking of voltage levels. Upon detecting the low voltage condition, the PIC14000 can be instructed to save its operating state then enter an idle state.

The internal band-gap reference is used for calibrating the measurements of the analog peripherals. The calibration factors are stored in EPROM and can be used to achieve high measurement accuracy.

Power savings modes are available for portable applications. The SLEEP and HIBERNATE modes offer different levels of power savings. The PIC14000 can wake up from these modes through interrupts or reset.

A UV erasable CERDIP packaged version is ideal for code development, while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

The PIC14000 fits perfectly in applications for battery charging, capacity monitoring, and data logging. The EPROM technology makes customization of application programs (battery characteristics, feature sets, etc.) extremely fast and convenient. The small footprint packages make this microcontroller based mixed signal device perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC14000 very versatile in other applications such as temperature monitors/controllers.

1.1 Family and Upward Compatibility

Code written for PIC16C6X/7X can be easily ported to the PIC14000 (see Appendix A).

1.2 Development Support

The PIC14000 is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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2.0 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. The PIC14000 Product Selection System section at the end of this data sheet provides the devices options to be selected for your specific application and production requirements. When placing orders, please use the "PIC14000 Product Identification System" at the back of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes.

Note:	Please note that erasing the device will also erase the pre-programmed calibration factors. Please refer to AN621 for more information.

Microchip's PICSTART®, PICSTART-PLUS and PRO MATE™ programmers all support programming of the PIC14000. Third party programmers also are available; refer to the *Microchip Third Party Guide* for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates or small volume applications.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

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3.0 ARCHITECTURAL OVERVIEW

The PIC14000 addresses 4K x 14 program memory. All program memory is internal. The PIC14000 can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC14000 has an orthogonal instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC14000 simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC14000 contains an 8-bit ALU and working register. The ALU performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ bit and a $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram for the PIC14000 is shown in Figure 3-1, its corresponding pin description is shown in Table 3-1.

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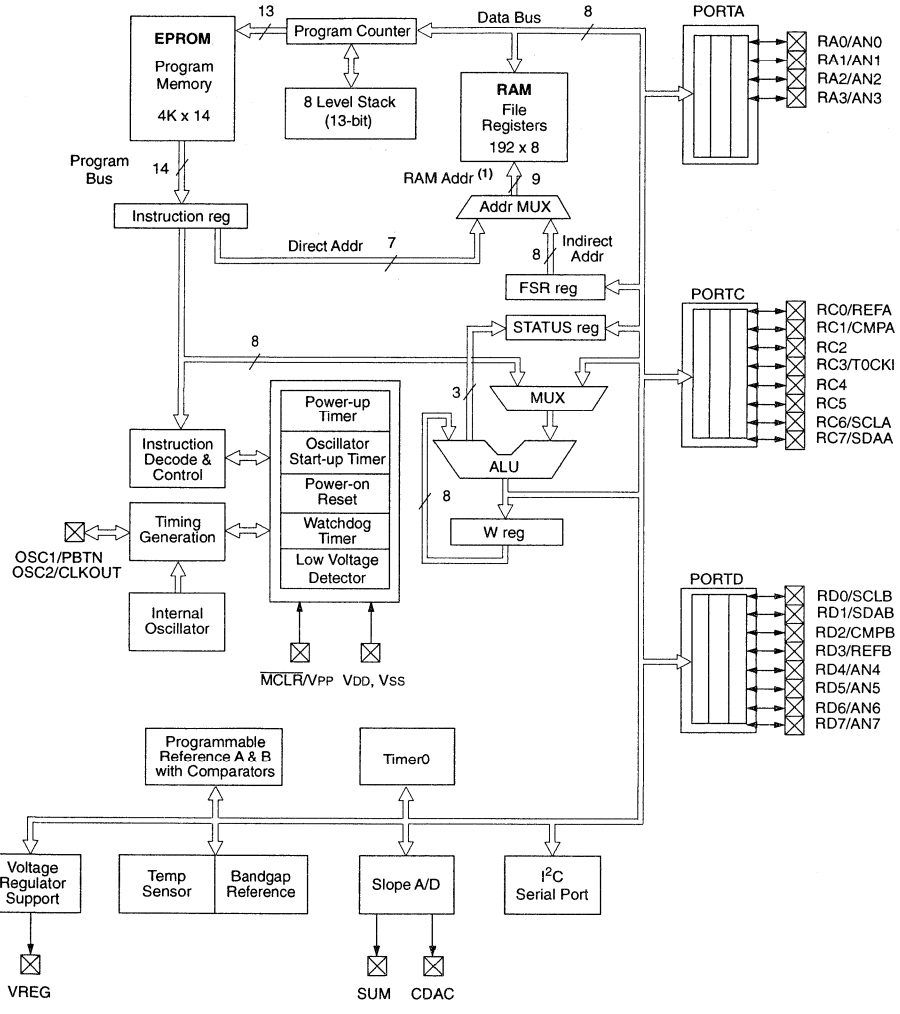
FIGURE 3-1: PIC14000 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.

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TABLE 3-1: PIN DESCRIPTIONS

Pin Name	Pin No.	I/O	Pin Type Input	Pin Type Output	Description
CDAC	22	O	—	AN	A/D ramp current source output. Normally connected to external capacitor to generate a linear voltage ramp.
RA0/AN0	2	I/O	AN/ST	CMOS	Analog input channel 0. This pin can also serve as a general-purpose I/O.
RA1/AN1	1	I/O	AN/ST	CMOS	Analog input channel 1. This pin can connect to a level shift network. If enabled, a +0.5V offset is added to the input voltage. This pin can also serve as a general-purpose I/O.
RA2/AN2	28	I/O	AN/ST	CMOS	Analog input channel 2. This pin can also serve as a general purpose digital I/O.
RA3/AN3	27	I/O	AN/ST	CMOS	Analog input channel 3. This pin can also serve as a general purpose digital I/O.
SUM	21	O	—	AN	AN1 summing junction output. This pin can be connected to an external capacitor for averaging small duration pulses.
RC0/REFA	19	I/O-PU	ST	CMOS	LED direct-drive output or programmable reference A output. This pin can also serve as a GPIO. If enabled, this pin has a weak internal pull-up to VDD.
RC1/CMPA	18	I/O-PU	ST	CMOS	LED direct-drive output or comparator A output. This pin can also serve as a GPIO. If enabled, this pin has a weak internal pull-up to VDD.
RC2	17	I/O-PU	ST	CMOS	LED direct-drive output. This pin can also serve as a GPIO. If enabled, this pin has a weak internal pull-up to VDD
RC3/T0CKI	16	I/O-PU	ST	CMOS	LED direct-drive output. This pin can also serve as a GPIO, or an external clock input for Timer0. If enabled, this pin has a weak internal pull-up to VDD.
RC4	15	I/O-PU	ST	CMOS	LED direct-drive output. This pin can also serve as a GPIO. If enabled, a change on this pin can cause a CPU interrupt. If enabled, this pin has a weak internal pull-up to VDD.
RC5	13	I/O-PU	ST	CMOS	LED direct-drive output. This pin can also serve as a GPIO. If enabled, a change on this pin can cause a CPU interrupt. If enabled, this pin has a weak internal pull-up to VDD.
RC6/SCLA	12	I/O	ST/SM	NPU/OD (No P-diode)	General purpose I/O. If enabled, is multiplexed as synchronous serial clock for I^2C interface. Also is the serial programming clock. If enabled, a change on this pin can cause a CPU interrupt. This pin has an N-channel pull-up device which is disabled in I^2C mode.
RC7/SDAA	11	I/O	ST/SM	NPU/OD (No P-diode)	General purpose I/O. If enabled, is multiplexed as synchronous serial data I/O for I^2C interface. Also is the serial programming data line. If enabled, a change on this pin can cause a CPU interrupt. This pin has an N-channel pull-up device which is disabled in I^2C mode.
RD0/SCLB	6	I/O	ST/SM	NPU/OD (No P-diode)	General purpose I/O. If enabled, is multiplexed as synchronous serial clock for I^2C interface. This pin has an N-channel pull-up device which is disabled in I^2C mode.
RD1/SDAB	5	I/O	ST/SM	NPU/OD (No P-diode)	General purpose I/O. If enabled, is multiplexed as synchronous serial data I/O for I^2C interface. This pin has an N-channel pull-up device which is disabled in I^2C mode.
RD2/CMPB	4	I/O-PU	AN/ST	CMOS	General purpose I/O or comparator B output.

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TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin No.	I/O	Pin Type Input	Pin Type Output	Description
RD3/REFB	3	I/O-PU	AN/ST	CMOS	General purpose I/O or programmable reference B output.
RD4/AN4	26	I/O	AN/ST	CMOS	Analog input channel 4. This pin can also serve as a GPIO.
RD5/AN5	25	I/O	AN/ST	CMOS	Analog input channel 5. This pin can connect to a level shift network. If enabled, a +0.5V offset is added to the input voltage. This pin can also serve as a GPIO.
RD6/AN6	24	I/O	AN/ST	CMOS	Analog input channel 6. This pin can also serve as a GPIO.
RD7/AN7	23	I/O	AN/ST	CMOS	Analog input channel 7. This pin can also serve as a GPIO.
VREG	10	O	—	AN	This pin is an output to control the gate of an external N-FET for voltage regulation.
OSC1/PBTN	8	I-PU	ST	—	IN Mode: Input with weak pull-up resistor, can be used to generate an interrupt. HS Mode: External oscillator input.
OSC2/ CLKOUT	7	O	—	CMOS	IN Mode: General purpose output. HS Mode: External oscillator/clock output.
$\overline{\text{MCLR}}$/VPP	14	I/PWR	ST		Master clear (reset) input / programming voltage input. This pin is an active low reset to the device.
VDD	9	PWR			Positive supply connection
VSS	20	GND			Return supply connection

Legend:

Type:	Definition:
TTL	TTL-compatible input
CMOS	CMOS-compatible input or output
ST	Schmitt Trigger input, with CMOS levels
SM	SMBus compatible input
OD	Open-drain output. An external pull-up resistor is required if this pin is used as an output.
NPU	N-channel pull-up. This pin will pull-up to approximately VDD - 1.0V when outputting a logical '1'.
PU	Weak internal pull-up (10K-50K ohms)
No-P diode	No P-diode to VDD. This pin may be pulled above the supply rail (to 6.0V maximum).
AN	Analog input or output

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1 or the internal oscillator) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. The program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2.

3.2 Instruction Flow/Pipelining

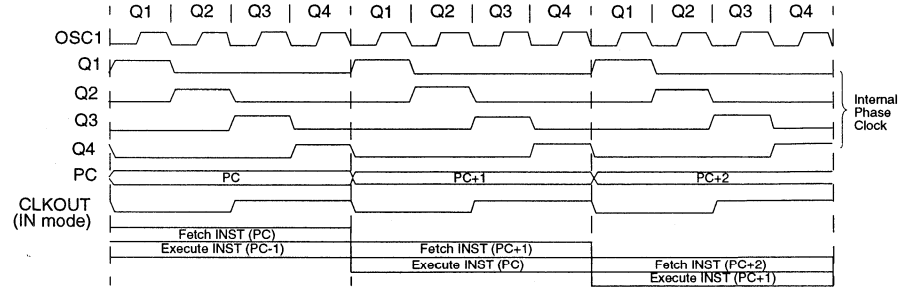
An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

3

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

```
1. MOVLW   55h
2. MOVWF   PORTB
3. CALL    SUB_1
4. BSF     PORTA, BIT3
```

Fetch 1	Execute 1				
	Fetch 2	Execute 2			
		Fetch 3	Execute 3		
			Fetch 4	Flush	
				Fetch SUB_1	

All instructions are single cycle, except for program branches. These take two cycles since the fetched instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

NOTES:

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4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

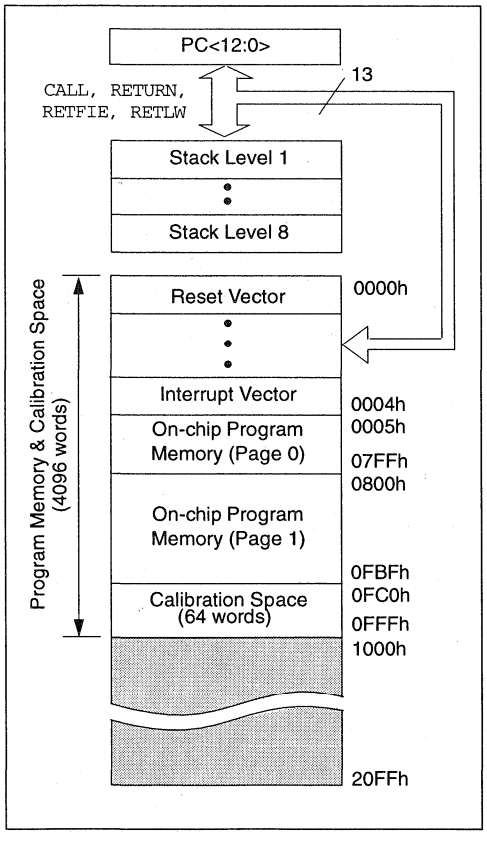
The PIC14000 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 4K x 14 (0000-0FFFh) are physically implemented. Accessing a location above the physically implemented address will cause a wraparound. The reset vector is at 0000h and the interrupt vector is at 0004h (Figure 4-1).

The 4096 words of Program Memory space are divided into:

- Address Vectors (addr 0000h-0004h)
- Program Memory Page 0 (addr 0005h-07FFH)
- Program Memory Page 1 (addr 0800h-0FBFh)
- Calibration Space (64 words, addr 0FC0h-0FFFh)

Program code may reside in Page 0 and Page 1.

FIGURE 4-1: PIC14000 PROGRAM MEMORY MAP AND STACK



4.1.1 CALIBRATION SPACE

The calibration space is not used for instructions. This section stores constants and factors for the arithmetic calculations to calibrate the analog measurements.

TABLE 4-1: CALIBRATION DATA OVERVIEW*

Address	Parameter	Symbol	Units	Format
0FC0h-0FC3h	Slope reference ratio	K_{REF}	N/A	32-bit floating point**
0FC4h-0FC7h	Bandgap reference voltage	K_{BG}	Volts	32-bit floating point
0FC8h-0FCBh	Temperature sensor voltage	V_{THERM}	Volts	32-bit floating point
0FCCh-0FCFh	Temperature sensor coefficient	K_{TC}	Volts/ degree Celsius	32-bit floating point
0FD0h	Internal oscillator frequency multiplier	F_{OSC}	N/A	byte
0FD2h	WDT time-out	T_{WDT}	ms	byte

* Refer to AN621 for details.

** Microchip modified IEEE754 32-bit floating point format. Refer to application note AN575 for details.

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TABLE 4-2: CALIBRATION CONSTANT ADDRESSES

Address	Data
0FC0h	K_{REF}, exponent
0FC1h	K_{REF}, mantissa high byte
0FC2h	K_{REF}, mantissa middle byte
0FC3h	K_{REF}, mantissa low byte
0FC4h	K_{BG}, exponent
0FC5h	K_{BG}, mantissa high byte
0FC6h	K_{BG}, mantissa middle byte
0FC7h	K_{BG}, mantissa low byte
0FC8h	V_{THERM}, exponent
0FC9h	V_{THERM}, mantissa high byte
0FCAh	V_{THERM}, mantissa middle byte
0FCBh	V_{THERM}, mantissa low byte
0FCCh	K_{TC}, exponent
0FCDh	K_{TC}, mantissa high byte
0FCEh	K_{TC}, mantissa middle byte
0FCFh	K_{TC}, mantissa low byte
0FD0h	F_{OSC}, unsigned byte
0FD1h	reserved
0FD2h	T_{WDT}, unsigned byte
0FD3h - 0FF8h	reserved
0FF9h-Fh	calibration space checksums

4.2 Data Memory Organization

The data memory (Figure 4-2) is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected when the RP0 bit in the STATUS register is cleared. Bank 1 is selected when the RP0 bit in the STATUS register is set. Each bank extends up to 7Fh (128 bytes). The first 32 locations of each bank are reserved for the Special Function Registers. Several Special Function Registers are mapped in both Bank 0 and Bank 1. The general purpose registers, implemented as static RAM, are located from address 20h through 7Fh, and A0 through FF.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly, or indirectly through the file select register FSR (Section 4.4).

FIGURE 4-2: REGISTER FILE MAP

File Address			
00h	Indirect add.(*)	Indirect addr.(*)	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	RESERVED	RESERVED	86h
07h	PORTC	TRISC	87h
08h	PORTD	TRISD	88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	ADTMRL	PCON	8Eh
0Fh	ADTMRH	SLPCON	8Fh
10h			90h
11h			91h
12h			92h
13h	I^2CBUF	I^2CADD	93h
14h	I^2CCON	I^2CSTAT	94h
15h	ADCAPL		95h
16h	ADCAPH		96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh		PREFA	9Bh
1Ch		PREFB	9Ch
1Dh		CMCON	9Dh
1Eh		MISC	9Eh
1Fh	ADCON0	ADCON1	9Fh
20h	General Purpose Register (96 Bytes)	General Purpose Register (96 Bytes)	A0h
7F			FF

* Not a physical register.
Shaded areas are unimplemented memory locations, read as '0's.

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4.2.2 SPECIAL FUNCTION REGISTERS

The special function registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (Table 4-3). These registers are static RAM.

The special registers are classified into two sets. Special registers associated with the "core" functions are described in this section. Those registers related to the operation of the peripheral features are described in the section specific to that peripheral.

TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC14000

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank0									
00h*	INDF (Indirect Address)	Addressing this location uses contents of the FSR to address data memory (not a physical register).							
01h	TMR0	Timer0 data							
02h*	PCL	Program Counter's (PC's) least significant byte							
03h*	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04h*	FSR	Indirect data memory address pointer							
05h	PORTA	PORTA data latch.							
06h	Reserved	Reserved for emulation.							
07h	PORTC	PORTC data latch							
08h	PORTD	PORTD data latch							
09h	Reserved								
0Ah*	PCLATH	Buffered register for the upper 5 bits of the Program Counter (PC)							
0Bh*	INTCON	GIE	PEIE	T0IE	r	r	T0IF	r	r
0Ch	PIR1	CMIF	—	—	PBIF	I^2CIF	RCIF	ADCIF	OVFIF
0Dh	Reserved								
0Eh	ADTMRL	A/D capture timer data least significant byte							
0Fh	ADTMRH	A/D capture timer data most significant byte							
10h	Reserved								
11h	Reserved								
12h	Reserved								
13h	I^2CBUF	I^2C Serial Port Receive Buffer/Transmit Register							
14h	I^2CCON	WCOL	I^2COV	I^2CEN	CKP	I^2CM3	I^2CM2	I^2CM1	I^2CM0
15h	ADCAPL	A/D capture latch least significant byte							
16h	ADCAPH	A/D capture latch most significant byte							
17h	Reserved								
18h	Reserved								
19h	Reserved								
1Ah	Reserved								
1Bh	Reserved								
1Ch	Reserved								
1Dh	Reserved								
1Eh	Reserved								
1Fh	ADCON0	ADCS3	ADCS2	ADCS1	ADCS0	—	AMUXOE	ADRST	ADZERO

Legend
— = unimplemented bits, read as '0' but cannot be overwritten
r = reserved bits, default is POR value and **should not be overwritten with any value**
Reserved indicates reserved register and **should not be overwritten with any value**
* indicates registers that can be addressed from either bank

TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC14000 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank1									
80h*	INDF (Indirect Address)	Addressing this location uses contents of FSR to address data memory (not a physical register).							
81h	OPTION	$\overline{RCPU}$	r	TOCS	TOSE	PSA	PS2	PS1	PS0
82h*	PCL	Program Counter's (PC's) least significant byte							
83h*	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
84h*	FSR	Indirect data memory address pointer							
85h	TRISA	PORTA Data Direction Register							
86h	Reserved	Reserved for emulation							
87h	TRISC	PORTC Data Direction Register							
88h	TRISD	PORTD Data Direction Register							
89h	Reserved								
8Ah*	PCLATH	Buffered register for the upper 5 bits of the Program Counter (PC)							
8Bh*	INTCON	GIE	PEIE	T0IE	r	r	T0IF	r	r
8Ch	PIE1	CMIE	—	—	PBIE	I^2CIE	RCIE	ADCIE	OVFIE
8Dh	Reserved								
8Eh	PCON	r	—	—	—	—	—	$\overline{POR}$	$\overline{LVD}$
8Fh	SLPCON	HIBEN	—	REFOFF	LSOFF	OSCOFF	CMOFF	TEMPOFF	ADOFF
90h	Reserved								
91h	Reserved								
92h	Reserved								
93h	I^2CADD	I^2C Synchronous Serial Port Address Register							
94h	I^2CSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
95h	Reserved								
96h	Reserved								
97h	Reserved								
98h	Reserved								
99h	Reserved								
9Ah	Reserved								
9Bh	PREFA	PRA7	PRA6	PRA5	PRA4	PRA3	PRA2	PRA1	PRA0
9Ch	PREFB	PRB7	PRB6	PRB5	PRB4	PRB3	PRB2	PRB1	PRB0
9Dh	CMCON	—	CMBOUT	CMBOE	CPOLB	—	CMAOUT	CMAOE	CPOLA
9Eh	MISC	SMHOG	SPGNDB	SPGNDA	I^2CSEL	SMBUS	INCLKEN	OSC2	OSC1
9Fh	ADCON1	ADDAC3	ADDAC2	ADDAC1	ADDAC0	PCFG3	PCFG2	PCFG1	PCFG0

Legend
— = unimplemented bits, read as '0' but cannot be overwritten
r = reserved bits, default is POR value and **should not be overwritten with any value**
Reserved indicates reserved register and **should not be overwritten with any value**
* indicates registers that can be addressed from either bank

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4.2.2.1 STATUS REGISTER

The STATUS register, shown in Figure 4-3, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC14000 and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{borrow}$ and $\overline{digit\ borrow}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

3

FIGURE 4-3: STATUS REGISTER

83h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
Read/Write	R/W	R/W	R/W	R	R	R/W	R/W	R/W
POR value FFh	0	0	0	1	1	X	X	X

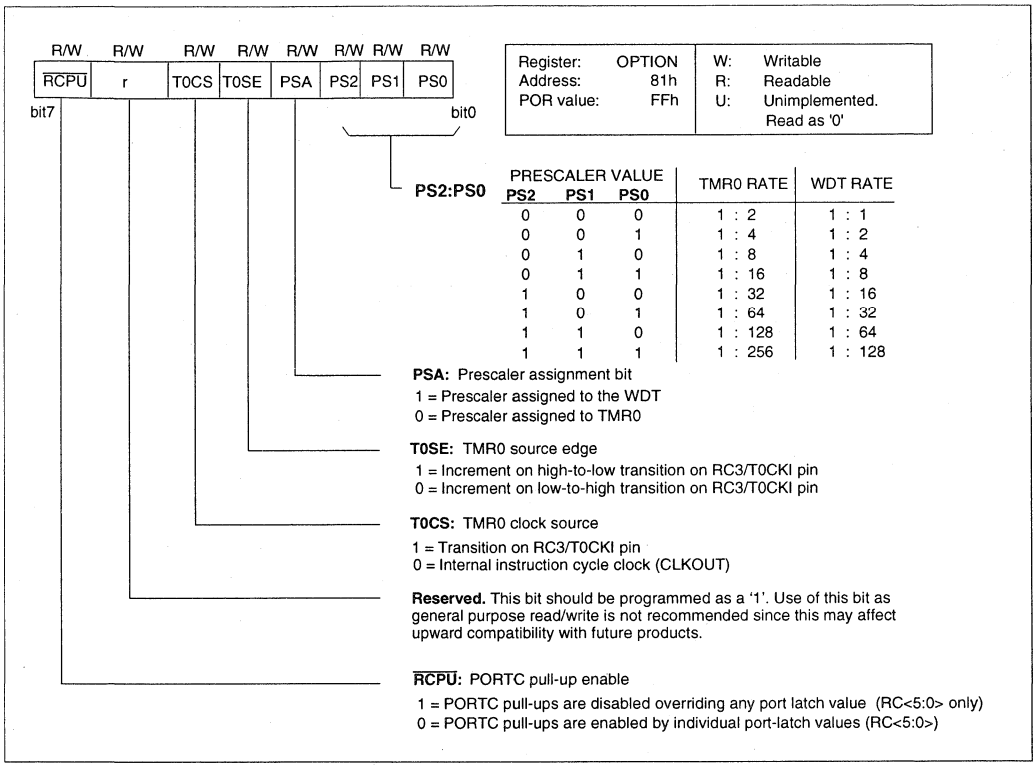
Bit	Name	Function
B7	IRP	Not used. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.
B6	RP1	Not used. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.
B5	RP0	Register page select for direct addressing. 1 = Bank1 (80h - FFh) 0 = Bank0 (00h - 7Fh) Each page is 128 bytes. Only the RP0 bit is used.
B4	$\overline{TO}$	Time-out bit. 1 = After power-up and by the CLRWDT and SLEEP instruction. 0 = A watchdog timer time-out has occurred.
B3	$\overline{PD}$	Power down bit. 1 = After power-up or by a CLRWDT instruction. 0 = By execution of the SLEEP instruction.
B2	Z	Zero bit. 1 = The result of an arithmetic or logic operation is zero. 0 = The result of an arithmetic or logical operation is not zero.
B1	DC	Digit carry / $\overline{borrow}$ bit. For ADDWF and ADDLW instructions. 1 = A carry-out from the 4th low order bit of the result. 0 = No carry-out from the 4th low order bit of the result. Note: For Borrow, the polarity is reversed.
B0	C	Carry / $\overline{borrow}$ bit. For ADDWF and ADDLW instructions. 1 = A carry-out from the most significant bit of the result occurred. Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register. 0 = No carry-out from the most significant bit of the result. Note: For Borrow the polarity is reversed.

4.2.2.2 OPTION REGISTER

The OPTION register (Address 81h) is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, TMR0, and the weak pull-ups on PORTC<5:0>. Bit 6 is reserved.

Note: To achieve a 1:1 prescaler assignment, assign the prescaler to the WDT (PSA=1)

FIGURE 4-4: OPTION REGISTER



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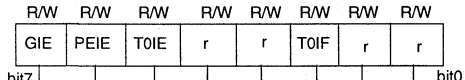
4.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register which contains the various enable and flag bits for the Timer0 overflow and peripheral interrupts. Figure 4-5 shows the bits for the INTCON register.

Note: The T0IF will be set by the specified condition even if the corresponding Interrupt Enable Bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling interrupt, clear the interrupt flag, to ensure that the program does not immediately branch to the peripheral interrupt service routine

FIGURE 4-5: INTCON REGISTER



Register:	INTCON	W:	Writable
Address:	0Bh or 8Bh	R:	Readable
POR value:	0000 000xb	U:	Unimplemented, read as '0'

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

T0IF: TMR0 overflow interrupt flag

1 = The TMR0 has overflowed
Must be cleared by software
0 = TMR0 did not overflow

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

T0IE: TMR0 interrupt enable bit

1 = Enables T0IF interrupt
0 = Disables T0IF interrupt

PEIE: Peripheral interrupt enable bit

1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

GIE: Global interrupt enable

1 = Enables all un-masked interrupts
0 = Disables all interrupts

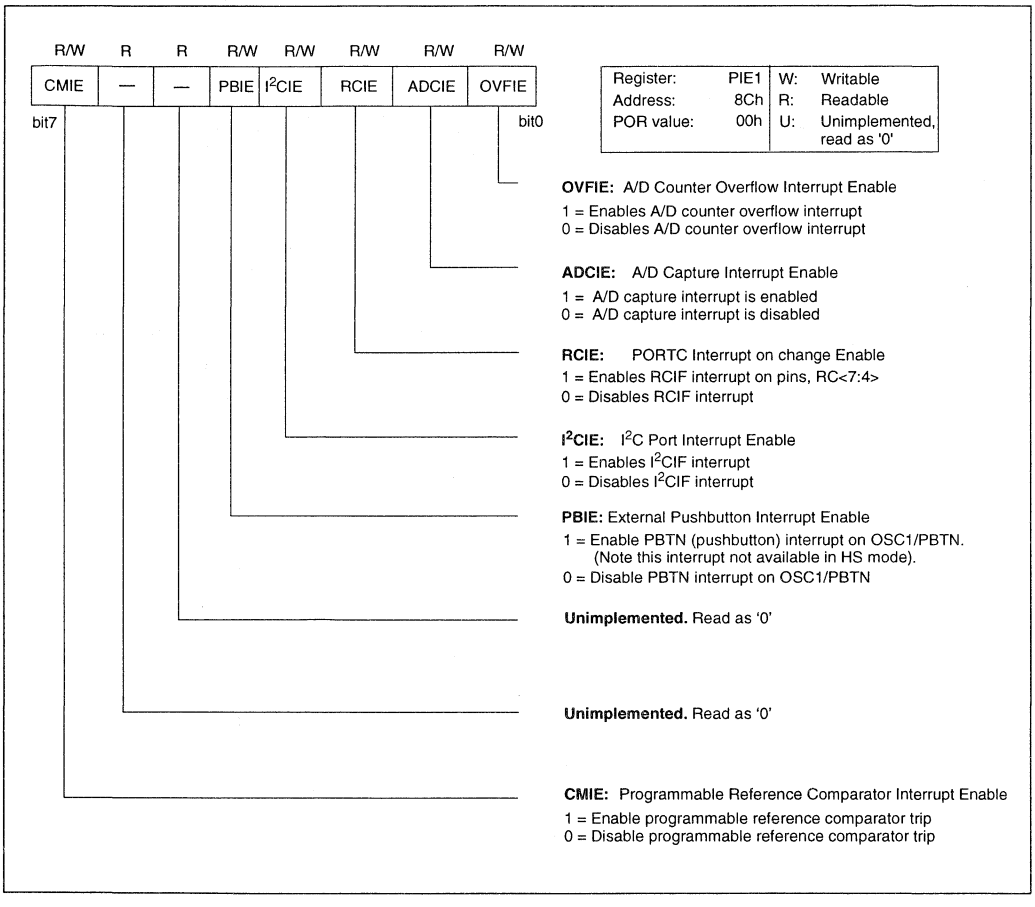
3

4.2.2.4 PIE1 REGISTER

This register contains the individual enable bits for the Peripheral interrupts including A/D capture event, I^2C serial port, PORTC change and A/D capture timer overflow, and external push button.

Note: INTCON<6> must be enabled to enable any interrupt in PIE1.

FIGURE 4-6: PIE1 REGISTER



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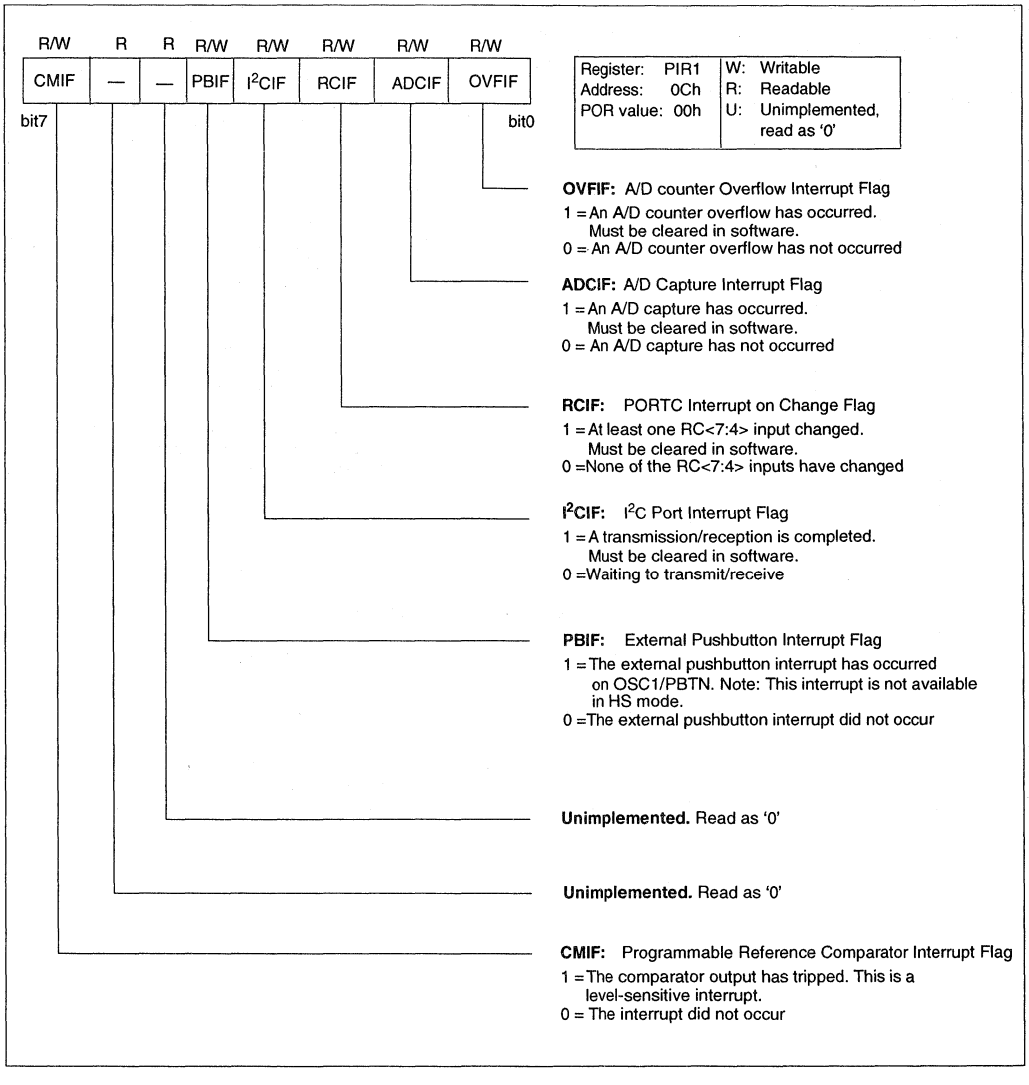
4.2.2.5 PIR1 REGISTER

This register contains the individual flag bits for the Peripheral interrupts (Figure 4-7).

Note: These bits will be set by the specified condition, even if the corresponding Interrupt Enable bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling an interrupt, the user may wish to clear the corresponding interrupt flag, to ensure that the program does not immediately branch to the Peripheral Interrupt service routine.

FIGURE 4-7: PIR1 REGISTER



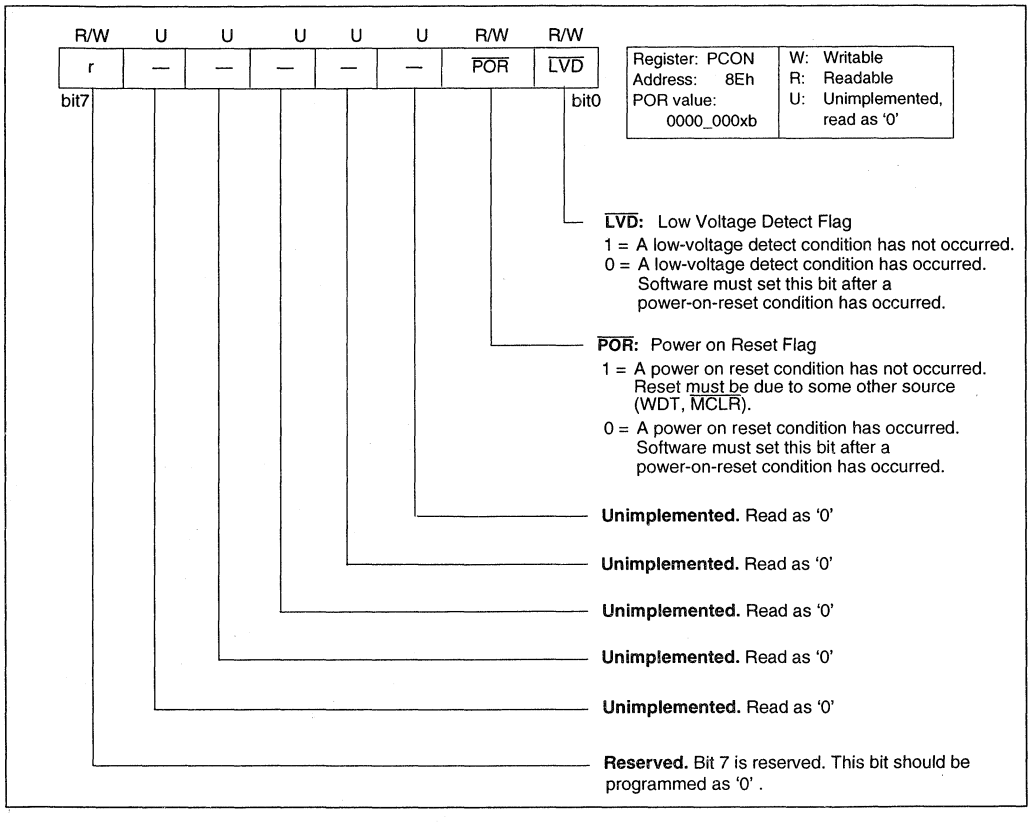
4.2.2.6 PCON REGISTER

The Power Control (PCON) register status contains 2 flag bits to allow differentiation between a Power-on Reset, an external $\overline{MCLR}$ reset, WDT reset, or low-voltage condition (Figure 4-8).

These bits are cleared on POR. The user must set these bits following POR. On a subsequent reset if POR is cleared, this is an indication that the reset was due to a power-on reset condition.

Note: $\overline{LVD}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{LVD}$ is cleared, indicating a low voltage condition has occurred.

FIGURE 4-8: PCON REGISTER



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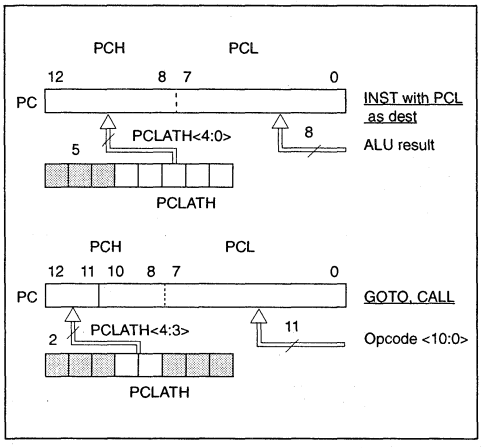
4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte, PCL, is a readable and writable register. The high byte of the PC (PCH) is not directly readable or writable. PCLATH is a holding register for PC<12:8> where contents are transferred to the upper byte of the program counter. When PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH as shown in Figure 4-9.

FIGURE 4-9: LOADING OF PC IN DIFFERENT SITUATIONS



Note: On POR, the contents of the PCLATH register are unknown. The PCLATH should be initialized before a CALL, GOTO, or any instruction that modifies the PCL register is executed.

4.3.1 COMPUTED GOTO

When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note "Table Read Using the PIC16CXX"(AN556).

4.3.2 STACK

The PIC14000 has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed in the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a "PUSH" or a "POP" operation.

The stack operates as a circular buffer. This means that after the stack has been "PUSHed" eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instruction mnemonics called PUSH nor POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, or RETFIE instructions, or the vectoring to an interrupt address

4.3.3 PROGRAM MEMORY PAGING

The PIC14000 has 4K of program memory, but the CALL and GOTO instructions only have a 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 4K program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (Figure 4-9). When doing a CALL or GOTO instruction, the user must ensure that this page bit (PCLATH<3>) is programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<3> is not required for the return instructions (which pops the PC from the stack).

Note: The PIC14000 ignores the PCLATH<4> bit, which is used for program memory pages 2 and 3 (1000h-1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0X500
BSF     PCLATH, 3 ; Select page 1 (800h-FFFh)
CALL    SUB1_P1   ; Call subroutine in
        :         ; page 1 (800h-FFFh)
        :
        :
ORG 0X900
SUB1 P1 :         ; called subroutine
        :         ; page 1 (800h-FFFh)
        :
RETURN            ; return to page 0
                  ; (000h-7FFh)
```

4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

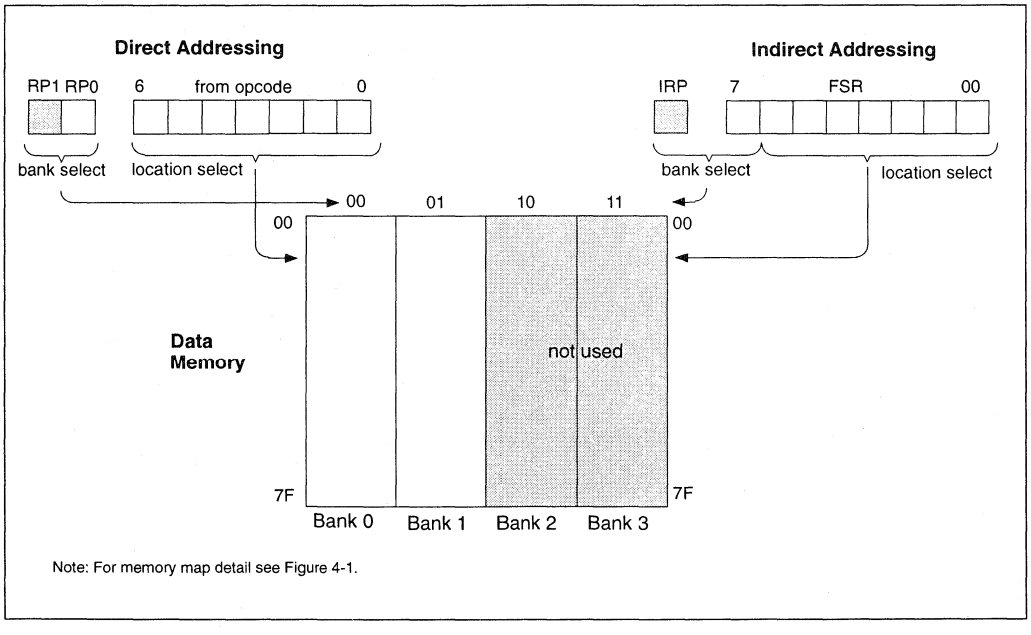
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-10. However, IRP is not used in the PIC14000.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movf    FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;no clear next
                        ;yes continue
CONTINUE:
```

FIGURE 4-10: INDIRECT/INDIRECT ADDRESSING



Note: For memory map detail see Figure 4-1.

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5.0 I/O PORTS

The PIC14000 has three ports, PORTA, PORTC and PORTD, described in the following paragraphs. Generally, PORTA is used as the analog input port. PORTC is used for general purpose I/O and for host communication. PORTD provides additional I/O lines. Four lines of PORTD may function as analog inputs.

5.1 PORTA and TRISA

PORTA is a 4-bit wide port with data register located at location 05h and corresponding data direction register (TRISA) at 85h. PORTA can operate as either analog inputs for the internal A/D converter or as general purpose digital I/O ports. These inputs are Schmitt Triggers when used as digital inputs, and have CMOS drivers as outputs.

PORTA pins are multiplexed with analog inputs. ADCON1<1:0> bits control whether these pins are analog or digital as shown in Section 8.7. When configured to the digital mode, reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. When selected as an analog input, these pins will read as '0's.

Note: On Reset, PORTA is configured as analog inputs

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs. A '1' in each location configures the corresponding port pin as an input. This register resets to all '1's, meaning all PORTA pins are initially inputs. The data register should be initialized prior to configuring the port as outputs. See Figure 5-2 and Figure 5-3.

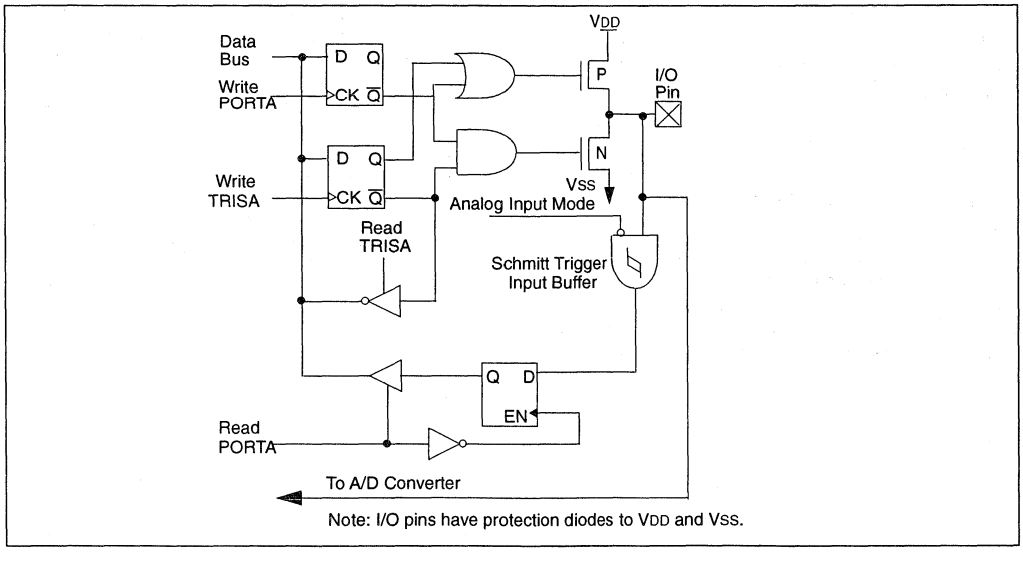
PORTA inputs go through a Schmitt Trigger AND gate that is disabled when the input is in analog mode. Refer to Figure 5-1.

Note that bits RA<7:4> are unimplemented and always read as '0'. Unused inputs should not be left floating to avoid leakage currents. All pins have input protection diodes to VDD and VSS.

EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF   PORTA        ;Initialize PORTA by setting
                    ;output data latches
BSF    STATUS, RP0  ;Select Bank1
MOVLW  0x0F         ;Value used to initialize
                    ;data direction
MOVWF  TRISA        ;Set RA<3:0> as inputs
```

FIGURE 5-1: PORTA BLOCK DIAGRAM



Note: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-2: PORTA DATA REGISTER

05h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTA	—	—	—	—	RA3/AN3	RA2/AN2	RA1/AN1	RA0/AN0
Read/Write	U	U	U	U	R/W	R/W	R/W	R/W
POR value 0xh	0	0	0	0	X	X	X	X

Bit	Name	Function
B7-B4	—	Unimplemented. Reads as'0'.
B3	RA3/AN3	GPIO or analog input. Returns value on pin RA3/AN3 when used as a digital input. When configured as an analog input, reads as '0'.
B2	RA2/AN2	GPIO or analog input. Returns value on pin RA2/AN2 when used as a digital input. When configured as an analog input, reads as '0'.
B1	RA1/AN1	GPIO or analog input. Returns value on RA1/AN1 when used as a digital input. This pin can connect to a level shift network. If enabled, a +0.5V offset is added to the input voltage. When configured as an analog input, reads as '0'.
B0	RA0/AN0	GPIO or analog input. Returns value on pin RA0/AN0 when used as a digital input. When configured as an analog input, reads as '0'.

5.2 PORTC and TRISC

PORTC is a 8-bit wide bidirectional port, with Schmitt Trigger inputs, that serves the following functions depending on programming:

- Direct LED drive (PORTC<7:0>).
- I^2C communication lines (PORTC<7:6>), refer to Section 7.0 I^2C Serial Port.
- Interrupt on change function (PORTC<7:4>), discussed below and in Section 10.3 Interrupts.
- Programmable reference and comparator outputs.
- Timer0 clock source on RC3

The PORTC data register is located at location 07h and its data direction register (TRISC) is at 87h.

PORTC<5:0> have weak internal pull-ups (~100 uA typical). A single control bit can turn on all the pull-ups. This is done by clearing bit $\overline{RCPU}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on power-on reset and in hibernate mode.

When using PORTC<0> as an analog output (CMCON<1> bit is set), the TRISC<0> bit should be cleared to disable the weak pull-up on this pin. Refer to Table 5-1.

Four of the PORTC pins, RC<7:4> have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur. In other words, any pin RC<7:4> configured as an output is excluded from the interrupt on change comparison. The input pins of RC<7:4> are compared with the old value latched on the last read of PORTC. The "mismatch" outputs of RC<7:4> are OR'ed together to assert the RCIF flag (PIR1 register<2>) and cause a CPU interrupt, if enabled.

Note: If the I^2C function is enabled, (I^2CCON<5>, address 14h), RC<7:6> are automatically excluded from the interrupt-on-change comparison.

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This interrupt can wake the device up from SLEEP. The user, in the interrupt service routine, can clear the interrupt in one of two ways:

- Disable the interrupt by clearing the RCIE (PIE1<2>) bit
- Read PORTC. This will end mismatch condition. Then, clear the RCIF (PIR1<2>) bit.

A mismatch condition will continue to set the RCIF bit. Reading PORTC will end the mismatch condition, and allow the RCIF bit to be cleared.

If bit CMAOE (CMCON<1>) is set, the RC0/REFA pin becomes the programmable reference A and analog output. Pin RC1/CMPA becomes the comparator A output.

Note:	Setting CMAOE changes the definition of RC0/REFA and RC1/CMPA, bypassing the PORTC data and TRISC register settings.

PORTC<7:6> also serves multiple functions. These pins act as the I^2C data and clock lines when the I^2C module is enabled. They also serve as the serial programming interface data and clock line for in-circuit programming of the EPROM.

The TRISC register controls the direction of the PORTC pin. A '1' in each location configures the corresponding port pin as an input. Upon reset, this register sets to FFh, meaning all PORTC pins are initially inputs. The data register should be initialized prior to configuring the port as outputs.

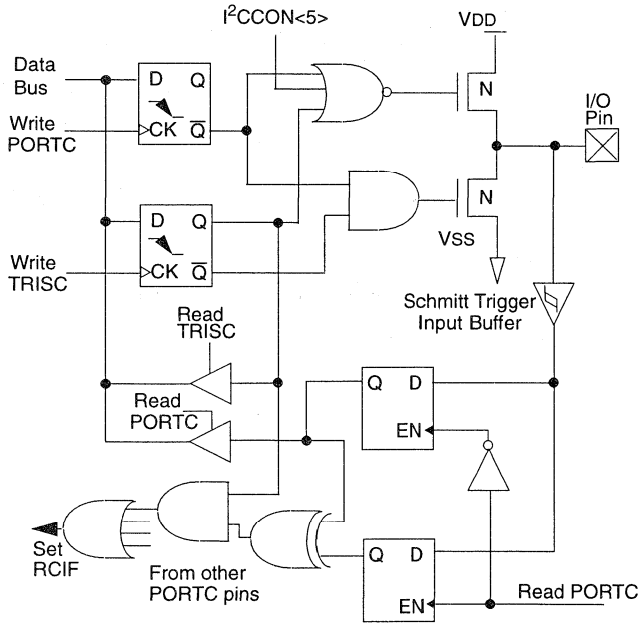
Unused inputs should not be left floating to avoid leakage currents. All pins have input protection diodes to VDD and VSS.

EXAMPLE 5-2: INITIALIZING PORTC

```
CLRF    PORTC       ; Initialize PORTC data
                    ;    latches before setting
                    ;    the data direction
                    ;    register
BSF     STATUS, RP0 ; Select Bank1
MOVLW   0xCF        ; Value used to initialize
                    ; data direction
MOVWF   TRISC       ; Set RC<3:0> as inputs
                    ;    RC<5:4> as outputs
                    ;    RC<7:6> as inputs
```

3

FIGURE 5-3: BLOCK DIAGRAM OF PORTC<7:6> PINS

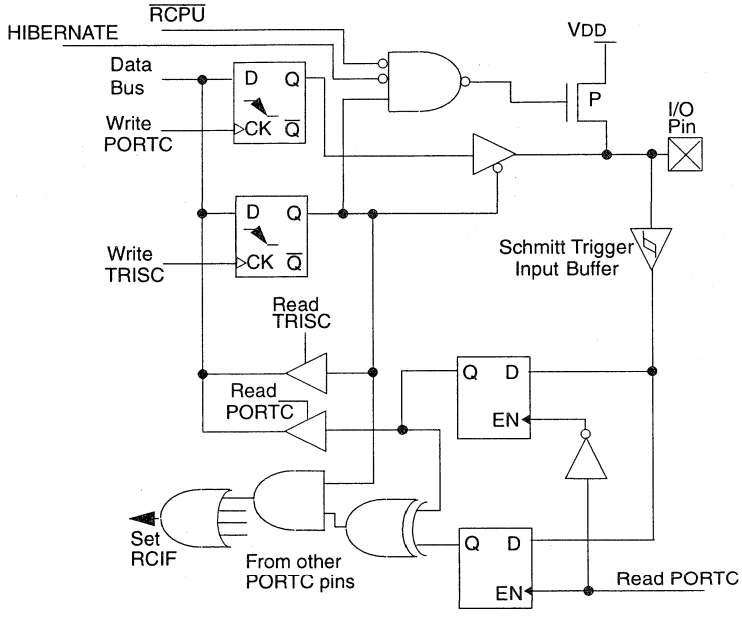


Note: I/O pins have protection diodes to VDD and VSS. These pins do not have a P-channel pull-up.

TABLE 5-1: PORT RC0 PIN CONFIGURATION SUMMARY

RC0 Pin Configuration	TRISC<0>	$\overline{\text{RCPU}}$ OPTION<7>	CMAOE CMCON<1>	Comment
Digital Input (weak pull-up)	1	0	0	
Digital Input (no pull-up)	1	1	0	
Digital Output	0	X	0	
Analog Output	0	X	1	Must clear TRISC<0> to disable pull-up when used as an analog output.

FIGURE 5-4: BLOCK DIAGRAM OF PORTC<5:4> PINS



1. I/O pins have protection diodes to VDD and VSS.
2. Port Latch = '1' and TRISC = '1' enables weak pull-up if $\overline{\text{RCPU}}$ = '0' in OPTION register.

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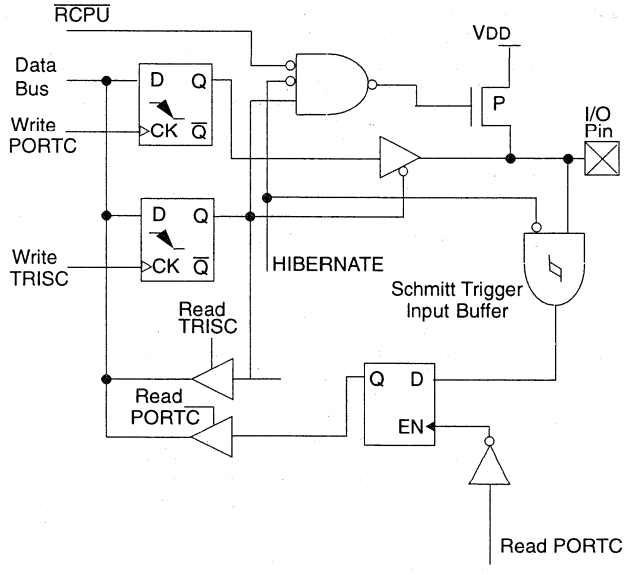
FIGURE 5-5: BLOCK DIAGRAM OF PORTC<3:0> PINS



1. I/O pins have protection diodes to VDD and VSS.
2. Port Latch ='1' and TRISC ='1' enables weak pull-up if $\overline{RCPU}$ ='0' in OPTION register.
3. If the CMAOE bit (CMCON<1>) is set to'1', RC0 becomes REFA, RC1 becomes CMPA, ignoring the PORTC<1:0> data and TRISC<1:0> register settings.

FIGURE 5-6: PORTC DATA REGISTER

07h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTC	RC7/SDAA	RC6/SCLA	RC5	RC4	RC3/T0CKI	RC2	RC1/CMPA	RC0/REFA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value xxh	x	x	x	x	x	x	x	x

Bit	Name	Function
B7	RC7/SDAA	Synchronous serial data I/O for I^2C interface. Also is the serial programming data line. This pin can also serve as a general purpose I/O. If enabled, a change on this pin can cause a CPU interrupt. This pin has an N-channel pull-up to VDD which is disabled in I^2C mode.
B6	RC6/SCLA	Synchronous serial clock for I^2C interface. Also is the serial programming clock. This pin can also serve as a general purpose I/O. If enabled, a change on this pin can cause a CPU interrupt. This pin has an N-channel pull-up to VDD which is disabled in I^2C mode.
B5	RC5	LED direct-drive output. This pin can also serve as a GPIO. If enabled, a change on this pin can cause a CPU interrupt. If enabled, this pin has a weak internal pull-up to VDD.
B4	RC4	LED direct-drive output. This pin can also serve as a GPIO. If enabled, a change on this pin can cause a CPU interrupt. If enabled, this pin has a weak internal pull-up to VDD.
B3	RC3/T0CKI	LED direct-drive output. This pin can also serve as a GPIO. If enabled, this pin has a weak internal pull-up to VDD. T0CKI is enabled as TMR0 clock via the OPTION register.
B2	RC2	LED direct-drive output. This pin can also serve as a GPIO. If enabled, this pin has a weak internal pull-up to VDD.
B1	RC1/CMPA	LED direct-drive output. This pin can also serve as a GPIO, or comparator A output. If enabled, this pin has a weak internal pull-up to VDD.
B0	RC0/REFA	LED direct-drive output. This pin can also serve as a GPIO, or programmable reference A output. If enabled, this pin has a weak internal pull-up to VDD.

U= unimplemented, X = unknown.

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5.2.1 TRISC PORTC DATA DIRECTION REGISTER

This register defines each pin of PORTC as either an input or output under software control. A '1' in each location configures the corresponding port pin as an input. This register resets to all '1's, meaning all PORTC pins are initially inputs. The data register should be initialized prior to configuring the port as outputs.

FIGURE 5-7: TRISC REGISTER

87h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value FFh	1	1	1	1	1	1	1	1

Bit	Name	Function
B7	TRISC7	Control direction on pin RC7/SDAA (has no effect if I^2C is enabled): 0 = pin is an output 1 = pin is an input
B6	TRISC6	Control direction on pin RC6/SCLA (has no effect if I^2C is enabled): 0 = pin is an output 1 = pin is an input
B5	TRISC5	Control direction on pin RC5: 0 = pin is an output 1 = pin is an input
B4	TRISC4	Control direction on pin RC4: 0 = pin is an output 1 = pin is an input
B3	TRISC3	Control direction on pin RC3: 0 = pin is an output 1 = pin is an input
B2	TRISC2	Control direction on pin RC2: 0 = pin is an output 1 = pin is an input
B1	TRISC1	Control direction on pin RC1/CMPA (has no effect if the CMAOE bit is set): 0 = pin is an output 1 = pin is an input
B0	TRISC0	Control direction on pin RC0/REFA (has no effect if the CMAOE bit is set): 0 = pin is an output 1 = pin is an input

U= unimplemented, X = unknown.

5.3 PORTD and TRISD

PORTD is an 8-bit port that may be used for general purpose I/O. Four pins can be configured as analog inputs.

FIGURE 5-8: BLOCK DIAGRAM OF PORTD<7:4> PINS

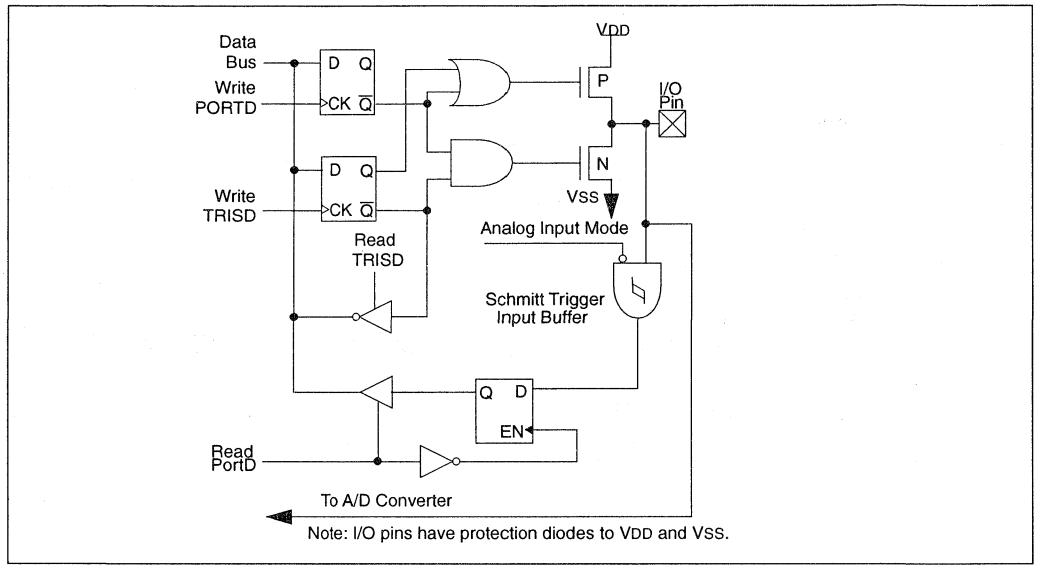
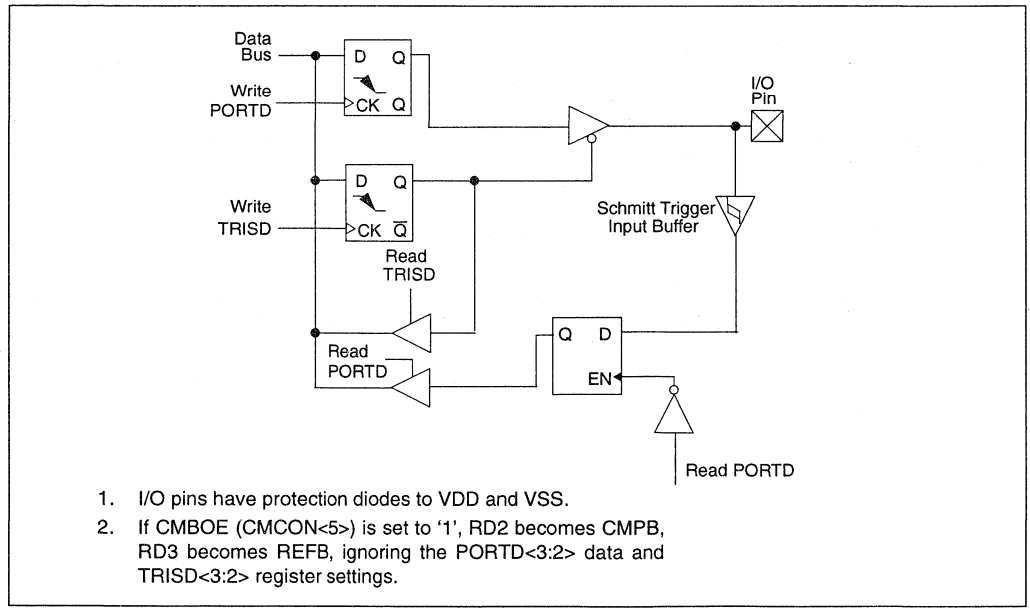


FIGURE 5-9: BLOCK DIAGRAM OF PORTD<3:2> PINS



1. I/O pins have protection diodes to VDD and VSS.
2. If CMBOE (CMCON<5>) is set to '1', RD2 becomes CMPB, RD3 becomes REFB, ignoring the PORTD<3:2> data and TRISD<3:2> register settings.

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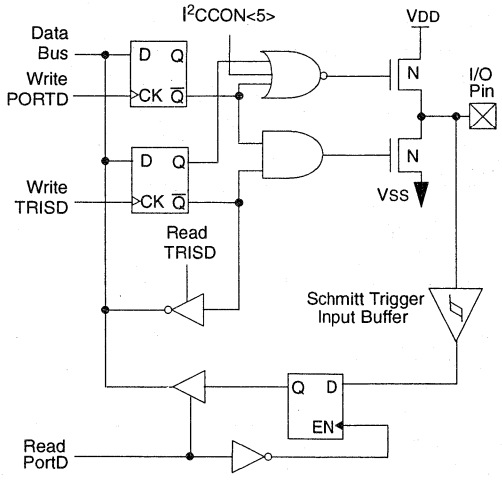
FIGURE 5-10: BLOCK DIAGRAM OF PORTD<1:0> PINS



Note: I/O pins have protection diodes to VDD and VSS. These pins do not have a P-channel pull-up.

FIGURE 5-11: PORTD DATA REGISTER

08h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTD	RD7/AN7	RD6/AN6	RD5/AN5	RD4/AN4	RD3/REFB	RD2/CMPB	RD1/SDAB	RD0/SCLB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value xxh	X	X	X	X	X	X	X	X

Bit	Name	Function
B7	RD7/AN7	GPIO or analog input. Returns value on pin RD7/AN7 when used as a digital input. When configured as an analog input, reads as '0'.
B6	RD6/AN6	GPIO or analog input. Returns value on pin RD6/AN6 when used as a digital input. When configured as an analog input, reads as '0'.
B5	RD5/AN5	GPIO or analog input. This pin can connect to a level shift network. If enabled, a +0.5V offset is added to the input voltage. When configured as an analog input, reads as '0'.
B4	RD4/AN4	GPIO or analog input. Returns value on pin RD4/AN4 when used as a digital input. When configured as an analog input, reads as '0'.
B3	RD3/REFB	This pin can serve as a GPIO, or programmable reference B output.
B2	RD2/CMPB	This pin can serve as a GPIO, or comparator B output.
B1	RD1/SDAB	Alternate synchronous serial data I/O for I^2C interface enabled by setting the I^2CSEL bit in the MISC register. This pin can also serve as a general purpose I/O. This pin has an N-channel pull-up to VDD which is disabled in I^2C mode.
B0	RD0/SCLB	Alternate synchronous serial clock for I^2C interface, enabled by setting the I^2CSEL bit in the MISC register. This pin can also serve as a general purpose I/O. This pin has an N-Channel pull-up to VDD which is disabled in I^2C mode.

Legend: U = unimplemented, read as '0', x = unknown.

FIGURE 5-12: TRISD REGISTER

88h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value FFh	1	1	1	1	1	1	1	1

Bit	Name	Function
B7	TRISD7	Control direction on pin RD7/AN7: 0 = pin is an output 1 = pin is an input
B6	TRISD6	Control direction on pin RD6/AN6: 0 = pin is an output 1 = pin is an input
B5	TRISD5	Control direction on pin RD5/AN5: 0 = pin is an output 1 = pin is an input
B4	TRISD4	Control direction on pin RD4/AN4: 0 = pin is an output 1 = pin is an input
B3	TRISD3	Control direction on pin RD3/REFB (has no effect if the CMBOE bit is set): 0 = pin is an output 1 = pin is an input
B2	TRISD2	Control direction on pin RD2/CMPB (has no effect if the CMBOE bit is set): 0 = pin is an output 1 = pin is an input
B1	TRISD1	Control direction on pin RD1/SDAB: 0 = pin is an output 1 = pin is an input
B0	TRISD0	Control direction on pin RD0/SCLB: 0 = pin is an output 1 = pin is an input

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If the CMBOE bit (CMCON<5>) is set, the RD3/REFB pin becomes the programmable reference B output and pin RD2/CMPB becomes the comparator B output.

Note:	Setting CMBOE changes the definition of RD3/REFB and RD2/CMPB, bypassing the PORTD data and TRISD register settings.

PORTD<1:0> also serve multiple functions. These pins act as the I^2C data and clock lines when the I^2C module is enabled.

The TRISD register controls the direction of the Port D pins. A '1' in each location configures the corresponding port pin as an input. Upon reset, this register sets to FFh, meaning all PORTD pins are initially inputs. The data register should be initialized prior to configuring the port as outputs.

Unused inputs should not be left floating to avoid leakage currents. All pins have input protection diodes to VDD and VSS.

EXAMPLE 5-3: INITIALIZING PORTD

```
CLRF    PORTD          ; Initialize PORTD data
                       ;    latches before setting
                       ;    the data direction
                       ;    register
BSF     STATUS, RP0    ; Select Bank1
MOVLW   0xFF           ; Value used to initialize
                       ; data direction
MOVWF   TRISD          ; Set RD<7:0> as inputs
```

5.4 I/O Programming Considerations

5.4.1 BI-DIRECTIONAL I/O PORTS

Reading the port register reads the values of the port pins. Writing to the port register writes the value to the port latch. Some instructions operate internally as read-modify-write. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation, and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTC will cause all eight bits of PORTC to be read into the CPU. Then the BSF operation takes place on bit5 and PORTC is written to the output latches. If another bit of PORTC is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a LOW or HIGH should not be driven from external devices at the same time in order to change the level on this pin ("wire-or", "wire-and"). The resulting high output currents may damage the chip.

Example 5-4 shows the effect of two sequential read modify write instructions (ex. BCF, BSF, etc.) on an I/O Port.

EXAMPLE 5-4: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings:   PORTC<7:4> Inputs
;
;                         PORTC<3:0> Outputs
; PORTC<7:6> have external pull-up and are not
; connected to other circuitry
;
;                         PORT  latch  PORT pins
;                         ----------   ----------

   BCF  PORTC, 7          ; 01pp pppp   11pp pppp
   BCF  PORTC, 6          ; 10pp pppp   11pp pppp
   BSF  STATUS,RP0        ;
   BCF  TRISC, 7          ; 10pp pppp   11pp pppp
   BCF  TRISC, 6          ; 10pp pppp   10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused
; RC7 to be latched as the pin value (High).
```

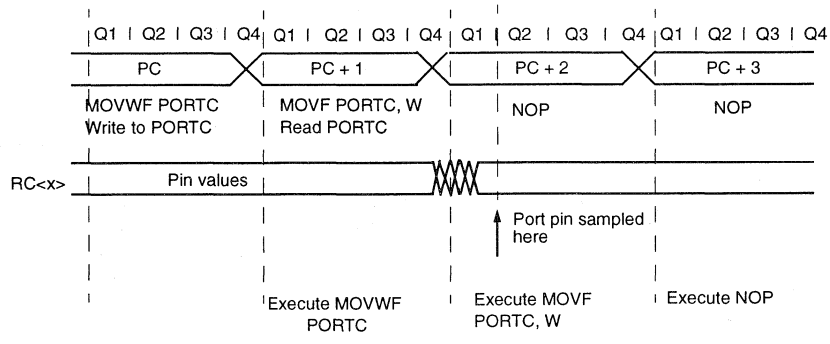
5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle. Therefore, care must be exercised if a write operation is followed by a read operation on the same I/O port.

The sequence of instructions should be such to allow the pin voltage to stabilize before the next instruction which causes that port to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-13: SUCCESSIVE I/O OPERATION

Example showing write to PORTC followed by immediate read. Some delays in settling may cause "old" Port data to be read, especially at higher clock frequencies. Data setup time = (0.25 Tcyc- Tpd), where Tcyc = instruction cycle time.



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6.0 TIMER MODULES

The PIC14000 contains two general purpose timer modules, Timer0 (TMR0) and the Watchdog Timer (WDT). The ADTMR is described in the A/D section.

The Timer0 module is identical to the Timer0 module of the PIC16C7X enhanced core products. It is an 8-bit overflow counter.

The Timer0 module has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer (WDT). PSA (OPTION<3>) assigns the prescaler, and PS2:PS0 (OPTION<2:0>) determines the prescaler value. Timer0 can increment at the following rates: 1:1 (when prescaler assigned to Watchdog Timer), 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, 1:256.

The Timer0 module has the following features:

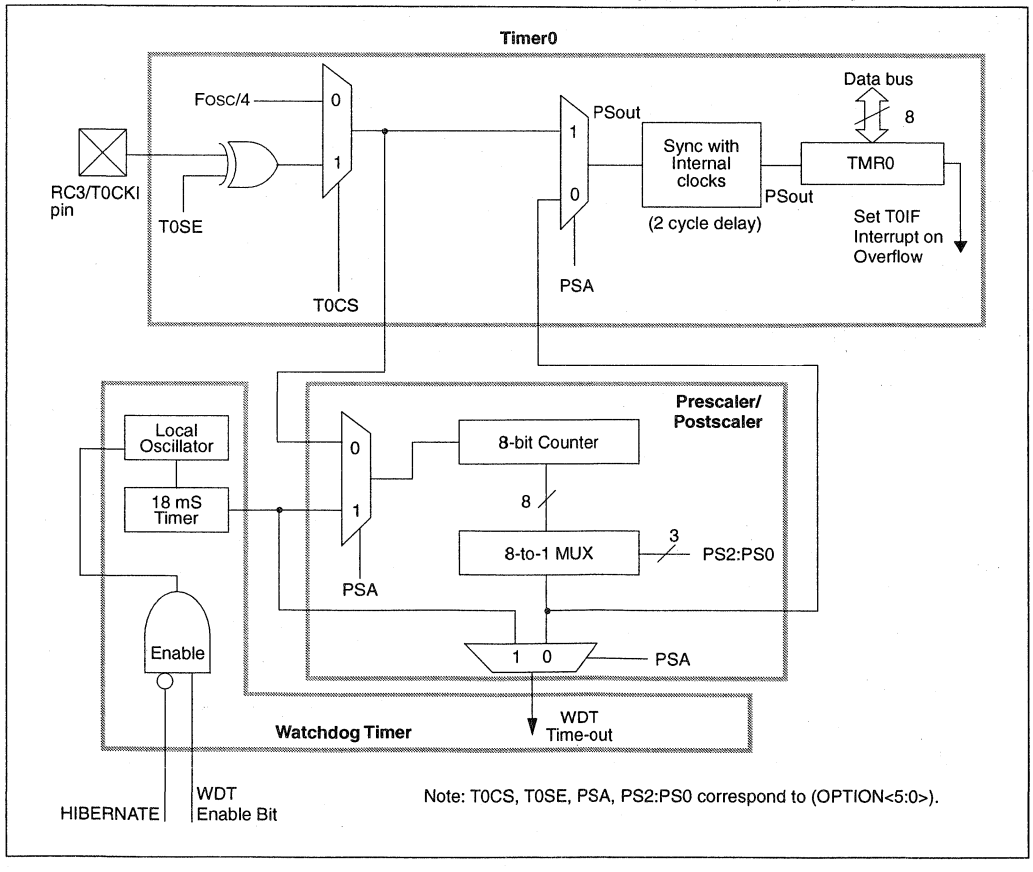
- 8-bit timer
- Readable and writable (file address 01h)
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 6-1 is a simplified block diagram of the Timer0 module.

The Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can compensate by writing an adjusted value to TMR0.

3

FIGURE 6-1: TIMER0 AND WATCHDOG TIMER BLOCK DIAGRAM



6.1 Timer0 Interrupt

The TMR0 interrupt is generated when the Timer0 overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing bit T0IE (INTCON<5>). Flag bit T0IF (INTCON<2>) must be cleared in software by the TMR0 module interrupt service routine before re-enabling this interrupt. The Timer0 module interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. The timing of the Timer0 interrupt is shown in Figure 6-4.

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

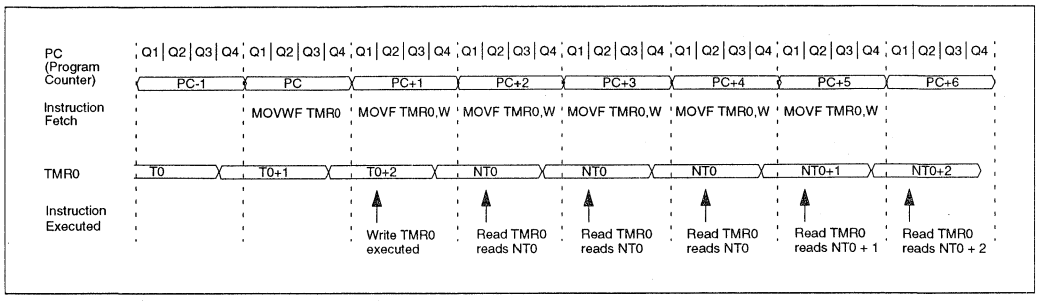


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

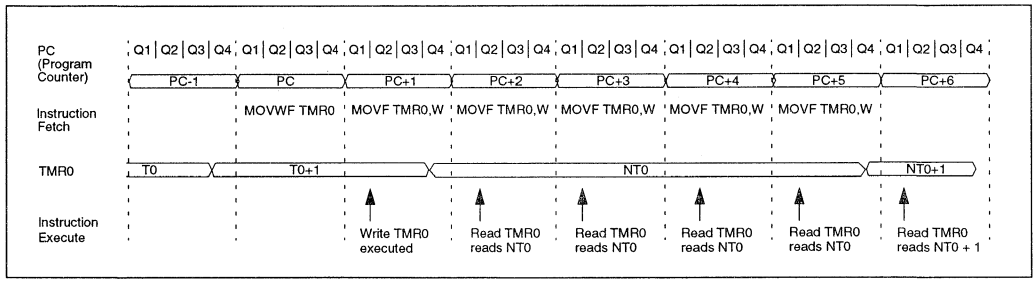
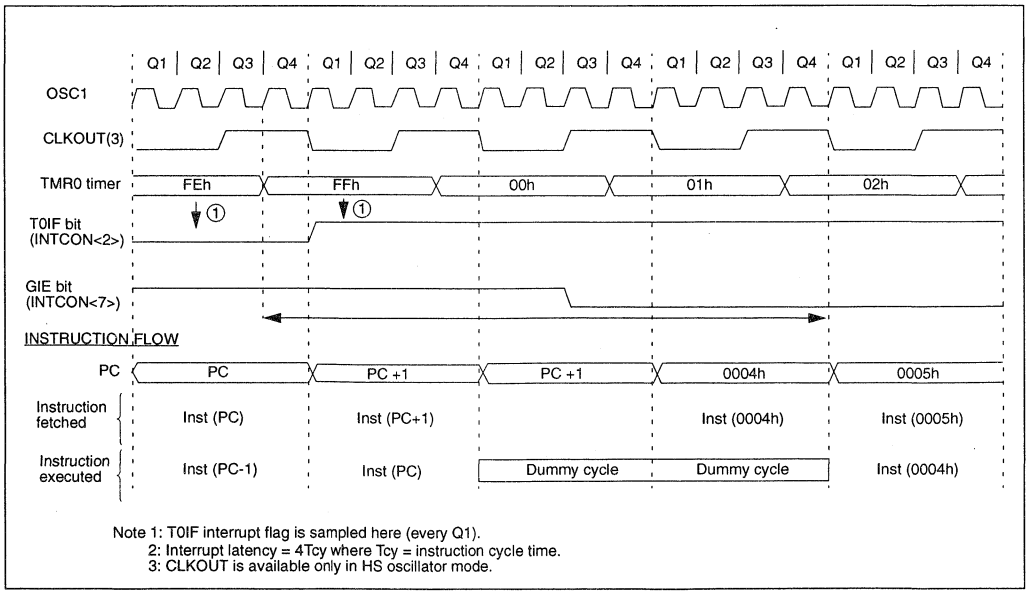


FIGURE 6-4: TIMER0 INTERRUPT TIMING



Note 1: T0IF interrupt flag is sampled here (every Q1).
2: Interrupt latency = 4Tcy where Tcy = instruction cycle time.
3: CLKOUT is available only in HS oscillator mode.

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6.2 Using Timer0 with External Clock

When the external clock input (pin RC3/T0CKI) is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of TMR0 after synchronization.

6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns).

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns.

6.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

6.3 Prescaler

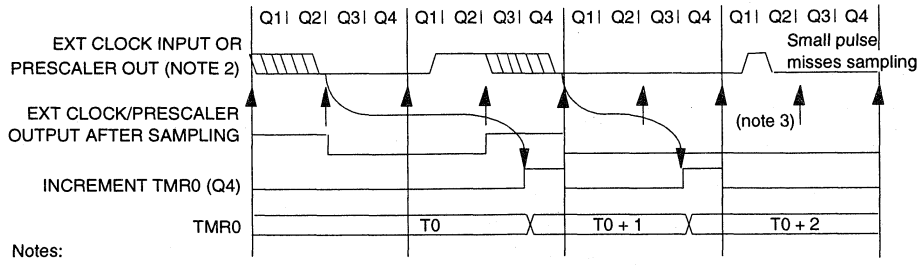
An 8-bit counter is available as a prescaler for the Timer0 module, or as a post-scaler for the Watchdog Timer (Figure 6-1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

Bit PSA and PS2:PS0 (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the Timer0 module (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

3

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Notes:

1. Delay from clock input change to TMR0 increment is 3 Tosc to 7 Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on TMR0 input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
 1.BCF    STATUS,RP0  ;Skip if already in
                      ; Bank 0
 2.CLRWDT             ;Clear WDT
 3.CLRF   TMR0        ;Clear TMR0 & Prescaler
 4.BSF    STATUS, RP0 ;Bank 1
 5.MOVLW '00101111'b; These 3 lines (5, 6, 7)
 6.MOVWF OPTION       ; are required only
                      ; if desired PS<2:0>
 7.CLRWDT             ; are 000 or 001
 8.MOVLW '00101xxx'b ;Set Postscaler to
 9.MOVWF OPTION       ; desired WDT rate
10.BCF    STATUS, RP0 ;Return to Bank 0
```

To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 6-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ;prescaler
BSF     STATUS, RP0
MOVLW   B'xxxx0xxx'     ;Select TMR0, new
                        ;prescale value and
                        ;clock source
MOVWF   OPTION
BCF     STATUS, RP0
```

TABLE 6-1: SUMMARY OF TIMER0 REGISTERS

Register Name	Function	Address	Power-on Reset Value
TMR0	Timer/counter register	01h	xxxx xxxx
OPTION	Configuration and prescaler assignment bits for TMR0.	81h	1111 1111
INTCON	TMR0 overflow interrupt flag and mask bits.	0Bh	0000 000x

Legend: x = unknown,
Note 1: For reset values of registers in other reset situations refer to Table 10-4.

TABLE 6-2: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	TMR0	TIMER0 TIMER/COUNTER							
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	r	r	T0IF	r	r
81h	OPTION	RCPU	r	T0CS	T0SE	PSA	PS2	PS1	PS0
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0

Legend: r = Reserved locations
Shaded boxes are not used by Timer0 module

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7.0 INTER-INTEGRATED CIRCUIT SERIAL PORT (I^2C™)

The I^2C module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The I^2C module is compatible with the following interface specifications:

- Inter-Integrated Circuit (I^2C)
- System Management Bus (SMBus)

Note: The I^2C module on PIC14000 only supports I^2C mode. This is different from the standard module used on the PIC16C7X family, which supports both I^2C and SPI modes. Caution should be exercised to avoid enabling SPI mode on the PIC14000.

This section provides an overview of the Inter-IC(I^2C) bus. The I^2C bus is a two-wire serial interface developed by the Philips Corporation. The original specification, or standard mode, was for data transfers of up to 100 Kbps. An enhanced specification, or fast mode, supports data transmission up to 400 Kbps. Both standard mode and fast mode devices will inter-operate if attached to the same bus.

The I^2C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master" (generates the clock) while the other device(s) acts as the "slave". All portions of the slave protocol are implemented in the I^2C module's hardware, except general call support, while portions of the master protocol will need to be addressed in the PIC14000 software. Table 7-1 defines some of the I^2C bus terminology. For additional information on the I^2C interface specification, please refer to the Philips Corporation document *"The I^2C-bus and How to Use It"*.

In the I^2C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to talk to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read from or write to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. They may operate in either of these two states:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level when no device is pulling the line down. The number of devices that may be attached to the I^2C bus is limited only by the maximum bus loading specification of 400 pF.

7.1 Initiating and Terminating Data Transfer

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP determine the start and stop of data transmission. The START is defined as a high to low transition of SDA when SCL is high. The STOP is defined as a low to high transition of SDA when SCL is high. Figure 7-1 shows the START and STOP. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP, when data is being transmitted the SDA line can only change state when the SCL line is low.

FIGURE 7-1: I^2C START AND STOP CONDITIONS

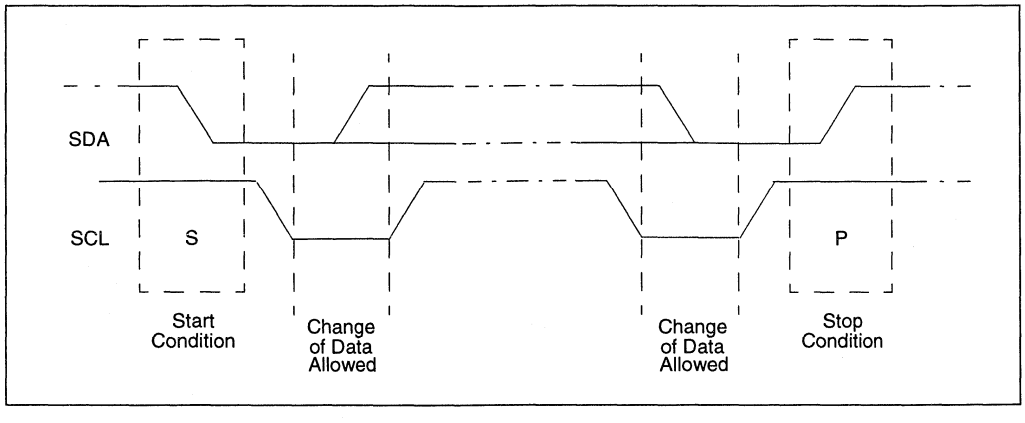
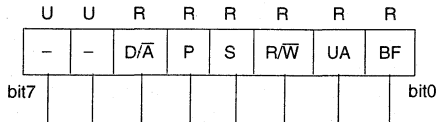


FIGURE 7-2: I²CSTAT: I²C PORT STATUS REGISTER



Register:	I²CSTAT	W: Writable bit
Address:	94h	R: Readable bit
POR value:	00h	U: Unimplemented, read as '0'

BF: Buffer full

Receive
1 = Receive complete, I²CBUF is full
0 = Receive not complete, I²CBUF is empty

Transmit
1 = Transmit in progress, I²CBUF is full
0 = Transmit complete, I²CBUF is empty

UA: Update Address (10-bit I²C slave mode only)
1 = Indicate that the user needs to update the address in the I²CADD register.
0 = Address does not need to be updated

R/$\overline{W}$: Read/write bit information
This bit holds the R/$\overline{W}$ bit information received following the last address match. This bit is only valid during the transmission.
The user may use this bit in software to determine whether transmission or reception is in progress.
1 = Read
0 = Write

S: Start bit
This bit is cleared when the I²C module is disabled (I²CEN is cleared)
1 = Indicates that a start bit has been detected last. This bit is 0 on reset.
0 = Start bit was not detected last

P: Stop bit
This bit is cleared when the I²C module is disabled (I²CEN is cleared)
1 = Indicates that a stop bit has been detected last.
0 = Stop bit was not detected last

D/$\overline{A}$: Data/$\overline{Address}$ bit
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was address

Unimplemented: read as '0'

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FIGURE 7-3: I^2CCON: I^2C PORT CONTROL REGISTER

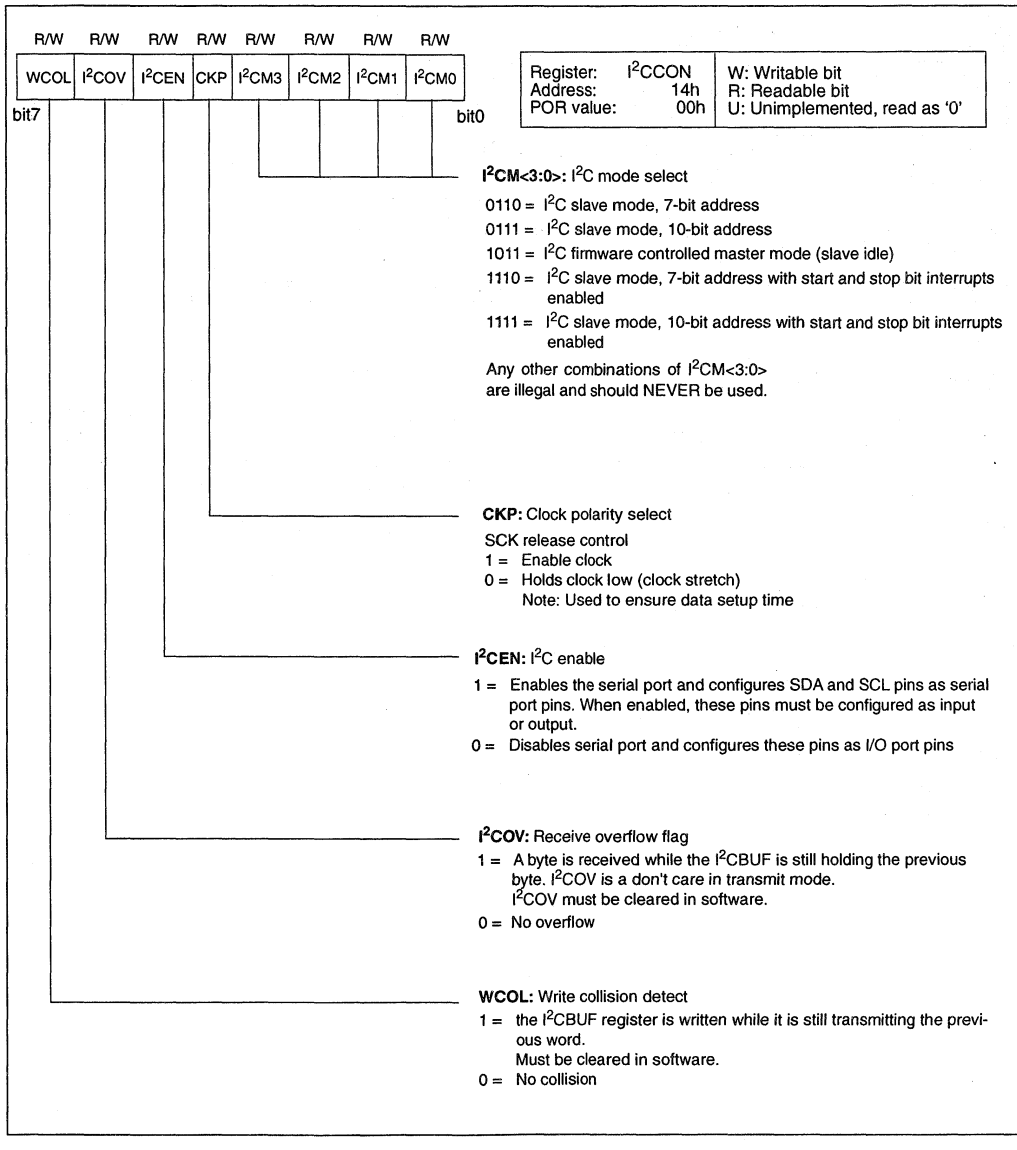


TABLE 7-1: I^2C BUS TERMINOLOGY

Term	Description
Transmitter	The device that sends the data to the bus.
Receiver	The device that receives the data from the bus.
Master	The device which initiates the transfer, generates the clock, and terminates the transfer.
Slave	The device addressed by a master.
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensures that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

FIGURE 7-4: I^2C 7-BIT ADDRESS FORMAT

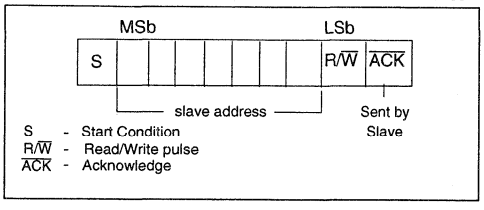
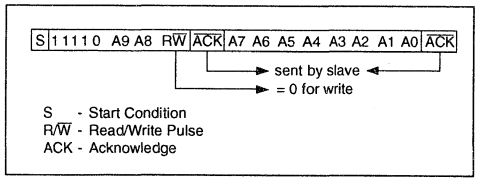


FIGURE 7-5: I^2C 10-BIT ADDRESS FORMAT



7.2 Addressing I^2C Devices

There are two address formats. The simplest is the 7-bit address format with a R/$\overline{W}$ bit (Figure 7-4). The address is the most significant seven bits of the byte. For example when loading the I^2CADD register, the least significant bit is a "don't care". The more complex is the 10-bit address with a R/$\overline{W}$ bit (Figure 7-5). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

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7.3 Transfer Acknowledge

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit ($\overline{ACK}$). This is shown in Figure 7-6. When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP (Figure 7-1).

If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge. The slave then releases the SDA line so the master can generate the STOP. The master can also generate the STOP during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state can be accomplished by setting SMHOG (MISC<7>) high. Clearing MISC<7> will resume the data transfer. Figure 7-7 shows a data transfer waveform.

Figure 7-8 and Figure 7-9 show master-transmitter and master-receiver data transfer sequences.

FIGURE 7-6: I^2C SLAVE-RECEIVER ACKNOWLEDGE

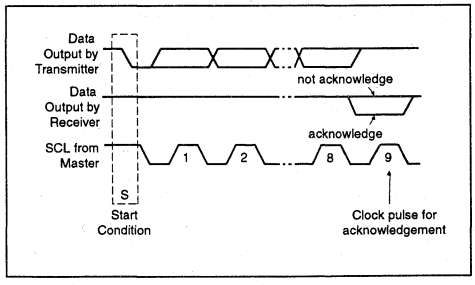
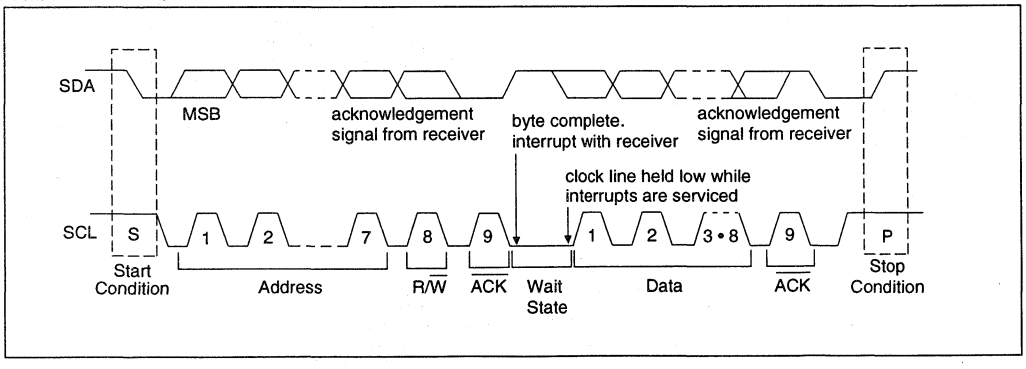


FIGURE 7-7: SAMPLE I^2C DATA TRANSFER



When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START (Sr) must be generated. This condition is identical to the START (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 7-10.

FIGURE 7-8: MASTER - TRANSMITTER SEQUENCE

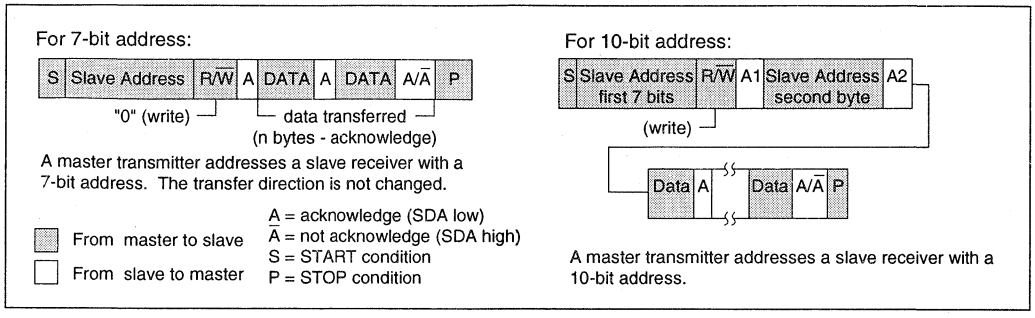


FIGURE 7-9: MASTER - RECEIVER SEQUENCE

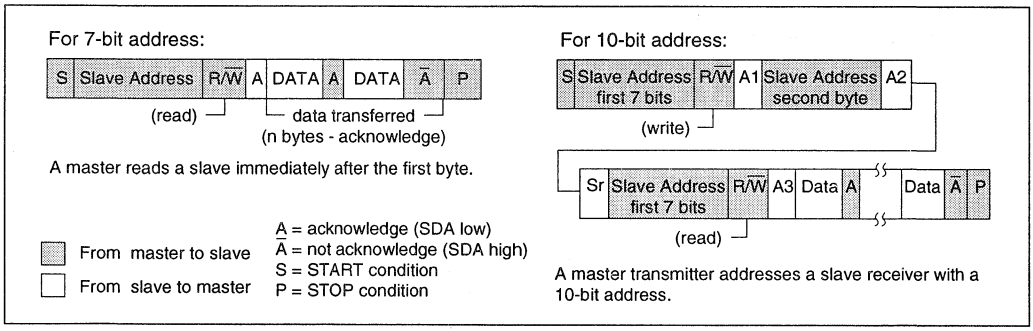
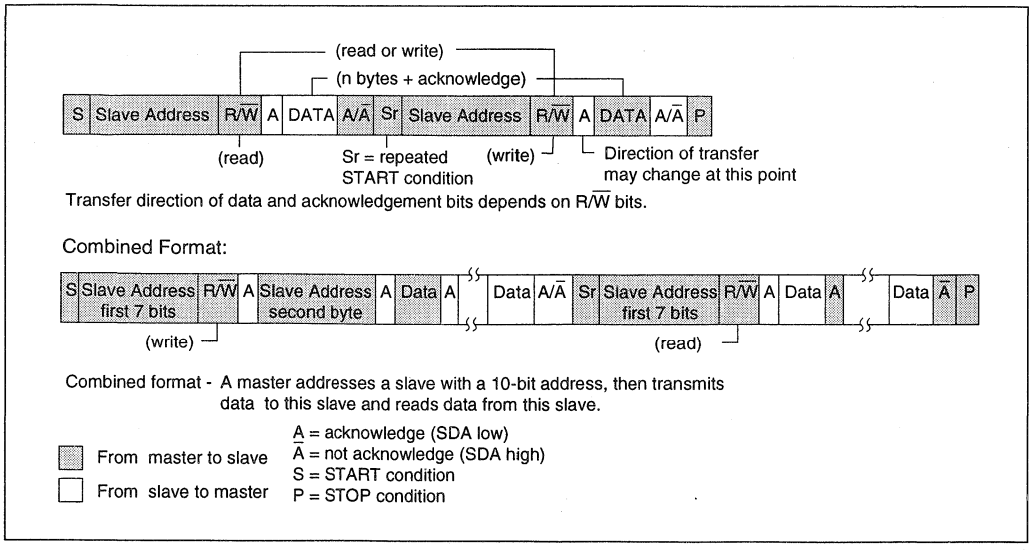


FIGURE 7-10: COMBINED FORMAT



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7.4 Multi-Master Operation

The I^2C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

7.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure 7-11) and turns off its data output stage. A master which lost arbitrating can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

- A repeated START
- A STOP and a data bit
- A repeated START and a STOP

Care needs to be taken to ensure that these conditions do not occur.

7.4.2 CLOCK SYNCHRONIZATION

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCA line high time is determined by the device with the shortest high period. This is shown in the Figure 7-12.

FIGURE 7-11: MULTI-MASTER ARBITRATION (2 MASTERS)

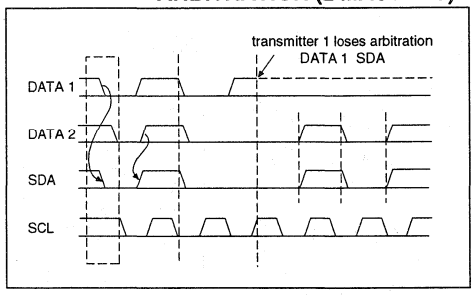
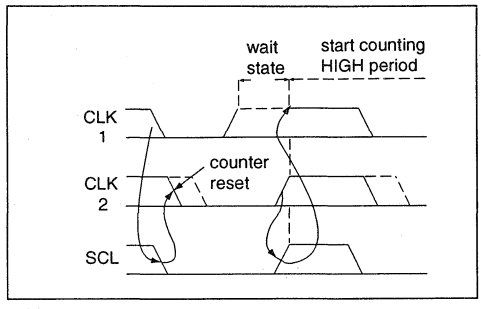
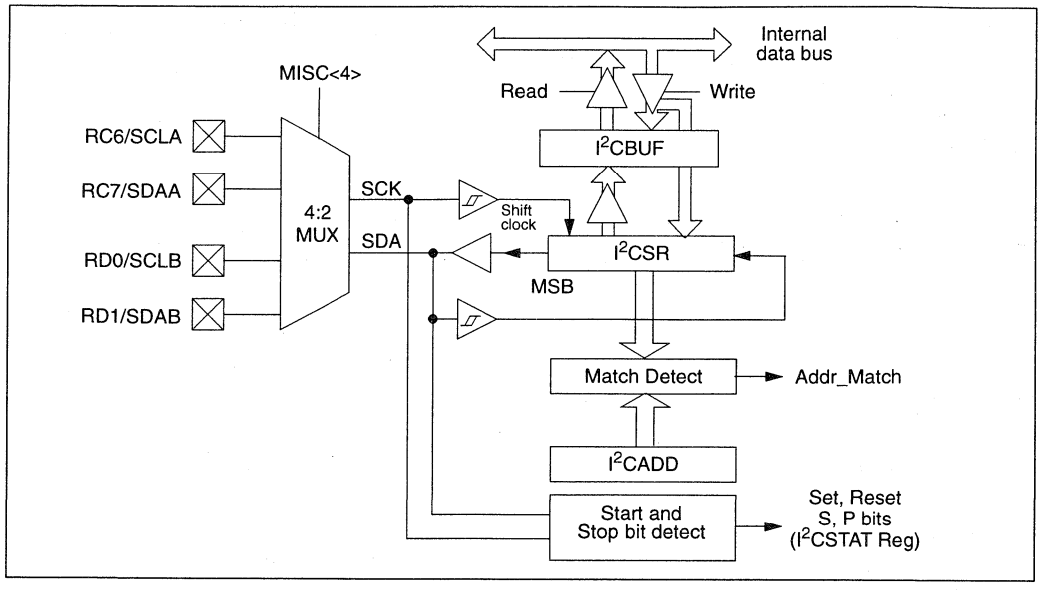


FIGURE 7-12: I^2C CLOCK SYNCHRONIZATION



3

FIGURE 7-13: I²C BLOCK DIAGRAM



7.5 I²C Operation

The I²C module in I²C mode fully implements all slave functions, and provides support in hardware to facilitate software implementations of the master functions. The I²C module implements the standard and fast mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC6/SCLA pin, which is the I²C clock, and the RC7/SDAA pin which acts as the I²C data. The I²C module can also be accessed via the RD0/SCLB and RD1/SDAB pins by setting I²CSEL (MISC<4>).The user must configure these pins as inputs or outputs through the TRISC<7:6> or TRISD<1:0> bits. A block diagram of the I²C module in I²C mode is shown in Figure 7-13. The I²C module functions are enabled by setting the I²CCON<5> bit.

The I²C module has five registers for I²C operation. These are the:

- I²C Control Register (I²CCON)
- I²C Status Register (I²CSTAT)
- Serial Receive/Transmit Buffer (I²CBUF)
- I²C Shift Register (I²CSR) - Not directly accessible
- Address Register (I²CADD)

The I²CCON register (14h) allows control of the I²C operation. Four mode selection bits (I²CCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
- I²C Firmware Controlled Master mode, slave is idle

Selection of any I²C mode with the I²CEN bit set, forces the SCL and SDA pins to be open collector, provided these pins are set to inputs through the TRISC bits.

The I²CSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The I²CSTAT register is read only.

The I²CBUF is the register to which transfer data is written to or read from. The I²CSR register shifts the data in or out of the device. In receive operations, the I²CBUF and I²CSR create a double buffered receiver. This allows reception of the next byte before reading the last byte of received data. When the complete byte is received, it is transferred to the I²CBUF and PIR1<3> is set. If another complete byte is received before the I²CBUF is read, a receiver overflow has occurred and the I²CCON<6> is set.

The I²CADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1 1 1 1 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7-A0).

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7.5.1 SLAVE MODE

In slave mode, the SCLx and SDAx pins must be configured as inputs (TRISC<7:6> or TRISD<1:0> are set). The I^2C module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer from an address match is received, the hardware automatically will generate the acknowledge ($\overline{ACK}$) pulse, and then load the I^2CBUF with the received value in the I^2CSR.

There are two conditions that will cause the I^2C module not to give this $\overline{ACK}$ pulse. These are if either (or both) occur:

- the Buffer Full (BF), $I^2CSTAT<0>$, bit was set before the transfer was received, or
- the Overflow (I^2COV), $I^2CCON<6>$ bit was set before the transfer was received.

In this case, the I^2CSR value is not loaded into the I^2CBUF, but the I^2CIF bit is set. Table 7-2 shows what happens when a data transfer byte is received, given the status of the BF and I^2COV bits. The shaded boxes show the conditions where user software did not properly clear the overflow condition. The BF flag is cleared by reading the I^2CBUF register while the I^2COV bit is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification as well as the requirement of the I^2C module is shown in the AC timing specifications.

3

TABLE 7-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received				
BF	I^2COV	I^2CSR-> I^2CBUF	Generate $\overline{ACK}$ Pulse	Set I^2CIF bit (I^2C interrupt if enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

7.5.1.1 ADDRESSING

Once the I^2C module has been enabled, the I^2C waits for a START to occur. Following the START, the 8-bits are shifted into the I^2CSR. All incoming bits are sampled with the rising edge of the clock (SCL) line. The $I^2CSR<7:1>$ is compared to the I^2CADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and I^2COV bits are clear, the following things happen:

- I^2CSR loaded into I^2CBUF
- Buffer Full (BF) bit is set
- $\overline{ACK}$ pulse is generated
- I^2C Interrupt Flag (I^2CIF) is set (interrupt is generated if enabled (I^2CIE set) on falling edge of ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave (Figure 7-5). The five most significant bits (MSbs) of the first address byte specify if this is a 10-bit address. The R/$\overline{W}$ bit (bit 0) must specify a write, so the slave device will received the second address byte. For a 10-bit address the first byte would equal '1 1 1 1 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for 10-bit address are as follows, with steps 7-9 for slave-transmitter:

1. Receive first (high) byte of address (I^2CIF, BF and UA are set).
2. Update I^2CADD with second (low) byte of address (clears UA and releases SCL line).
3. Read I^2CBUF (clears BF) and clear I^2CIF.
4. Receive second (low) byte of address (I^2CIF, BF and UA are set).
5. Update I^2CADD with first (high) byte of address (clears UA, if match releases SCL line).
6. Read I^2CBUF (clears BF) and clear I^2CIF
7. Receive Repeated START.
8. Receive first (high) byte of address (I^2CIF and BF are set).
9. Read I^2CBUF (clears BF) and clear I^2CIF.

7.5.1.2 RECEPTION

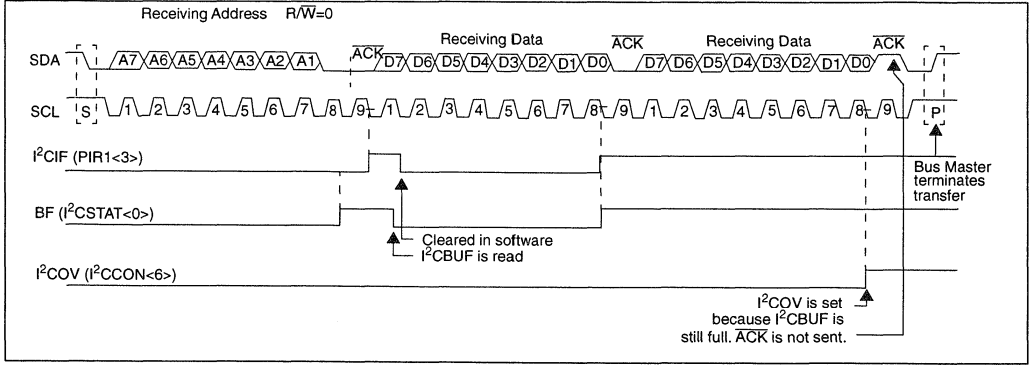
When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, the R/$\overline{W}$ bit of the I^2CSTAT register is cleared. The received address is loaded into the I^2CBUF.

When the address byte overflow condition exists then no acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either the BF bit ($I^2CSTAT<0>$) is set or the I^2COV bit ($I^2CCON<6>$) is set (Figure 7-14).

An I^2CIF interrupt is generated for each data transfer byte. The I^2CIF bit must be cleared in software, and the I^2CSTAT register is used to determine the status of the byte. In master mode with slave enabled, three interrupt sources are possible. Reading BF, P and S will indicate the source of the interrupt.

Caution: BF is set after receipt of eight bits and automatically cleared after the I^2CBUF is read. However, the flag is not actually cleared until receipt of the acknowledge pulse. Otherwise extra reads appear to be valid.

FIGURE 7-14: I^2C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



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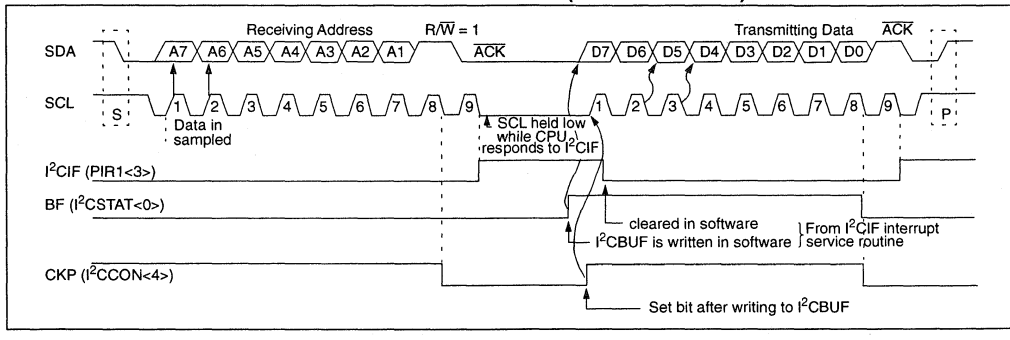
7.5.1.3 TRANSMISSION

When the R/$\overline{W}$ bit of the address byte is set and an address match occurs, the R/$\overline{W}$ bit of the I^2CSTAT register is set. The received address is loaded into the I^2CBUF The $\overline{ACK}$ pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the I^2CBUF register, which also loads the I^2CSR register. Then the SCL pin should be enabled by setting the CKP bit (I^2CCON<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 7-15).

A I^2CIF interrupt is generated for each data transfer byte. The I^2CIF bit must be cleared in software, and the I^2CSTAT register is used to determine the status of the byte. The I^2CIF bit is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. The slave then monitors for another occurrence of the START bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the I^2CBUF register, which also loads the I^2CSR register. Then the SCL pin should be enabled by setting the CKP bit (I^2CCON<4>).

FIGURE 7-15: I^2C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



7.5.2 MASTER MODE

Master mode operation is supported by interrupt generation on the detection of the START and STOP. The STOP(P) and START(S) bits are cleared from a reset or when the I^2C module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are cleared.

In master mode, the SCL and SDA lines are manipulated by changing the corresponding TRISC<7:6> or TRISD<1:0> bits to an output (cleared). The output level is always low, regardless of the value(s) in PORTC<7:6> or PORTD<1:0>. So when transmitting data, a "1" data bit must have the TRISC<7> or TRISD<1> bit set (input) and a "0" data bit must have the TRISC<7> or TRISD<1> bit cleared (output). The same scenario is true for the SCL line with the TRISC<6> or TRISD<0> bit.

The following events will cause the I^2C interrupt Flag (I^2CIF) to be set (I^2C interrupt if enabled):

- START
- STOP
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle ($I^2CM3...I^2CM0$ = 1011b) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

7.5.3 MULTI-MASTER MODE

In multi-master mode, the interrupt generation on the detection of the START and STOP allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the I^2C module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are cleared. When the bus is busy, enabling the I^2C interrupt will generate the interrupt when the STOP occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and low level is present, the device needs to release the SDA and SCL lines (set TRISC<7:6>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, the device may being addressed. If addressed an $\overline{ACK}$ pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

TABLE 7-3: REGISTERS ASSOCIATED WITH I^2C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8Bh	INTCON	GIE	PEIE	T0IE	r	r	T0IF	r	r
0Ch	PIR1	CMIF	—	—	PBIF	I^2CIF	RCIF	ADCIF	OVFIF
8Ch	PIE1	CMIE	—	—	PBIE	I^2CIE	RCIE	ADCIE	OVFIE
13h	I^2CBUF	I^2C Serial Port Receive Buffer/Transmit Register							
93h	I^2CADD	I^2C mode Synchronous Serial Port (I^2C mode) Address Register							
14h	I^2CCON	WCOL	I^2CON	I^2CEN	CKP	I^2CM3	I^2CM2	I^2CM1	I^2CM0
94h	I^2CSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
9Eh	MISC	SMHOG	SPGNDB	SPGNDA	I^2CSEL	SMBUS	INCLKEN	OSC2	OSC1
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
88h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0

Legend: — = Unimplemented location, read as '0'
r = reserved locations, default is POR value and **should not be overwritten with any value**

Note: Shaded boxes are not used by the I^2C module.

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FIGURE 7-16: MISC REGISTER

9Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MISC	SMHOG	SPGNDB	SPGNDA	I^2CSEL	SMBUS	INCLKEN	OSC2	OSC1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
POR value 00h	0	0	0	0	0	0	0	X

Bit	Name	Function
B7	SMHOG	SMHOG enable 1 = Stretch I^2C CLK signal (hold low) when receive data buffer is full (refer to Section 7.5.4). For pausing I^2C transfers while preventing interruptions of A/D conversions. 0 = Disable I^2C CLK stretch.
B6	SPGNDB	Serial Port Ground Select 1 = PORTD<1:0> ground reference is the RD5/AN5 pin. 0 = PORTD<1:0> ground reference is Vss.
B5	SPGNDA	Serial Port Ground Select 1 = PORTC<7:6> ground reference is the RA1/AN1 pin. 0 = PORTC<7:6> ground reference is Vss.
B4	I^2CSEL	I^2C Port select Bit. 1 = PORTD<1:0> are used as the I^2C clock and data lines. 0 = PORTC<7:6> are used as the I^2C clock and data lines.
B3	SMBus	SMBus-Compatibility Select 1 = SMBus compatibility mode is enabled. PORTC<7:6> and PORTD<1:0> have SMBus-compatible input thresholds. 0 = SMBus-compatibility is disabled. PORTC<7:6> and PORTD<1:0> have Schmitt Trigger input thresholds.
B2	INCLKEN	Oscillator Output Select (available in IN mode only). 1 = Output IN oscillator signal divided by four on OSC2 pin. 0 = Disconnect IN oscillator signal from OSC2 pin.
B1	OSC2	OSC2 output port bit (available in IN mode only). Writes to this location affect the OSC2 pin in IN mode. Reads return the value of the output latch.
B0	OSC1	OSC1 input port bit (available in IN mode only). Reads from this location return the status of the OSC1 pin in IN mode. Writes have no effect.

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FIGURE 7-17: OPERATION OF THE I^2C IN IDLE_MODE, RCV_MODE OR XMIT_MODE

```
IDLE_MODE (7-bit):
if (Addr_match)                 {   Set interrupt;
                                    if (R/W = 1)    {   Send ACK = 0;
                                                        set XMIT_MODE;
                                                    }
                                    else if (R/W = 0) set RCV_MODE;
                                }

RCV_MODE:
if ((I2CBUF=Full) OR (I2COV = 1))
        {   Set I2COV;
            Do not acknowledge;
        }
else    {   transfer I2CSR → I2CBUF;
            send ACK = 0;
        }
Receive 8-bits in I2CSR;
Set interrupt;

XMIT_MODE:
While ((I2CBUF = Empty) AND (CKP=0)) Hold SCL Low;
Send byte;
Set interrupt;
if (ACK Received = 1)           {   End of transmission;
                                    Go back to IDLE_MODE;
                                }
else if (ACK Received = 0)  Go back to XMIT_MODE;

IDLE_MODE (10-Bit):
If (High_byte_addr_match AND (R/W = 0))
        {   PRIOR_ADDR_MATCH = FALSE;
            Set interrupt;
            if ((I2CBUF = Full) OR ((I2COV = 1))
                    {   Set I2COV;
                        Do not acknowledge;
                    }
            else    {   Set UA = 1;
                        Send ACK = 0;
                        While (I2CADD not updated) Hold SCL low;
                        Clear UA = 0;
                        Receive Low_addr_byte;
                        Set interrupt;
                        Set UA = 1;
                        If (Low_byte_addr_match)
                                {   PRIOR_ADDR_MATCH = TRUE;
                                    Send ACK = 0;
                                    while (I2CADD not updated) Hold SCL low;
                                    Clear UA = 0;
                                    Set RCV_MODE;
                                }
                    }
        }
else if (High_byte_addr_match AND (R/W = 1)
        {   if (PRIOR_ADDR_MATCH)
                    {   send ACK = 0;
                        set XMIT_MODE;
                    }
            else PRIOR_ADDR_MATCH = FALSE;
        }
```

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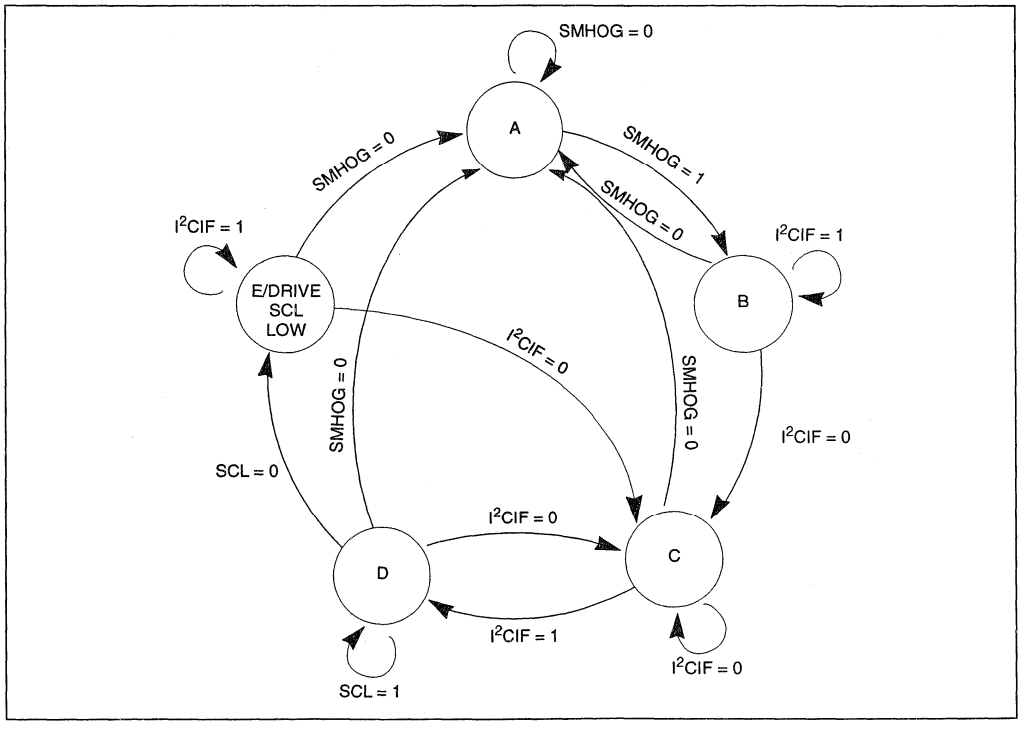
7.5.4 SMBus™ AND ACCESS.bus™ CONSIDERATIONS

PIC14000 is compliant with the SMBus specification published by Intel. Some key points to note regarding the bus specifications and how it pertains to the PIC14000 hardware are listed below:

- SMBus has fixed input voltage thresholds. PIC14000 I/O buffers have programmable levels that can be selected to be compatible with both SMBus threshold levels via the SMBus and SPGND bits in the MISC register.
- A mechanism to stretch the I^2C clock time has been implemented to support SMBus slave transactions. The SMHOG bit (MISC<7>) allows hardware to automatically force and hold the I^2C clock line low when a data byte has been received. This prevents the SMBus master from overflowing the receive buffer in instances where the microcontroller may be to busy servicing higher priority tasks to respond to a I^2C module interrupt. Or, if the microcontroller is in SLEEP mode and needs time to wake-up and respond to the I^2C interrupt.

FIGURE 7-18: SMHOG STATE MACHINE



NOTES:

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8.0 ANALOG MODULES FOR A/D CONVERSION

8.1 Overview

The PIC14000 includes analog components to create a slope A/D converter including:

- Comparator
- 4-bit programmable current source
- 16-channel analog mux
- 16-bit timer with capture register

Each channel is converted independently by means of a slope conversion method using a single precision comparator. The programmable current source feeds an external 0.1 µF (nominal) capacitor to generate the ramp voltage used in the conversion.

8.2 Conversion Process

These are the steps to perform data conversion:

- Clear REFOFF (SLPCON<5>) and ADOFF (SLPCON<0>) bits to enable the A/D module.
- Initialize ADCON1<7:4> to initialize the programmable current source.
- Set ADRST (ADCON0<1>), for a minimum of 200 µs to stop the timer and fully discharge the ramp capacitor to ground.
- The A/D timer (ADTMR) increments from 0000h to FFFFh and must be initialized before each conversion.
- To start a conversion, clear ADRST through software, it will allow the timer to begin counting and the ramp capacitor to begin charging.
- When the ramp voltage exceeds the analog input, the comparator output changes from high to low.
- This transition causes a capture event and copies the current A/D timer value into the 16-bit capture register.
- An interrupt is generated to the CPU if enabled.

Note: The A/D timer continues to run following a capture event.

The maximum A/D timer count is 65,536. It can be clocked by the on-chip or external oscillator. At a 4 MHz oscillation frequency, the maximum conversion time is 16.38 ms for a full count. A typical conversion should complete before full-count is reached. A timer overflow flag is set once the timer rolls over (FFFFh to 0000h), and an interrupt is sent to the CPU, if enabled.

End-user calibration is simplified or eliminated by making use of the on-chip EPROM. Internal component values are measured at factory final test and stored in the memory for use by the application firmware.

Periodic conversion cycles should be performed on the bandgap and slope references (described in Section 9.0) to compensate for A/D component drift. Measurements for the reference voltage count are equated to the voltage value stored into EPROM during calibration. All other channel measurements are compensated for by ratioing the actual count with the bandgap count and multiplying by the bandgap voltage value stored in EPROM. Since all measurements are relative to the reference, offset voltages inherent in the comparator are cancelled out. See AN624, "PIC14000 A/D Theory and Implementation" for further details of A/D operation.

The analog components used in the conversion and the A/D timer can be disabled during idle periods for maximum power savings. Power-saving can be achieved via software and/or hardware control (Section 10.8).

8.3 A/D Timer (ADTMR) Module

The A/D timer (ADTMR) is comprised of a 16-bit up timer, which is incremented every oscillator cycle. ADTMR is reset to 0000h by a power-up reset; otherwise the software must initialize it after each conversion. A separate 16-bit capture register (ADCAP) is used to capture the ADTMR count if an A/D capture event occurs (see below). Both the A/D timer and capture register are readable and writable. The low byte of the A/D timer (ADTMRL) is accessed at location 0Eh while the high byte (ADTMRH) is accessed at location 0Fh. Similarly, the low byte of the A/D capture register (ADCAP) is accessed at location 15h, and the high byte is located at 16h.

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Caution: Reading or writing the ADTMR register during an A/D conversion cycle can produce unpredictable results and is not recommended.

Note: The correct sequence for writing the ADTMR register is HI byte followed by LO byte. Reversing this order will prevent the A/D timer from running.

During conversion one or both of the following events will occur:

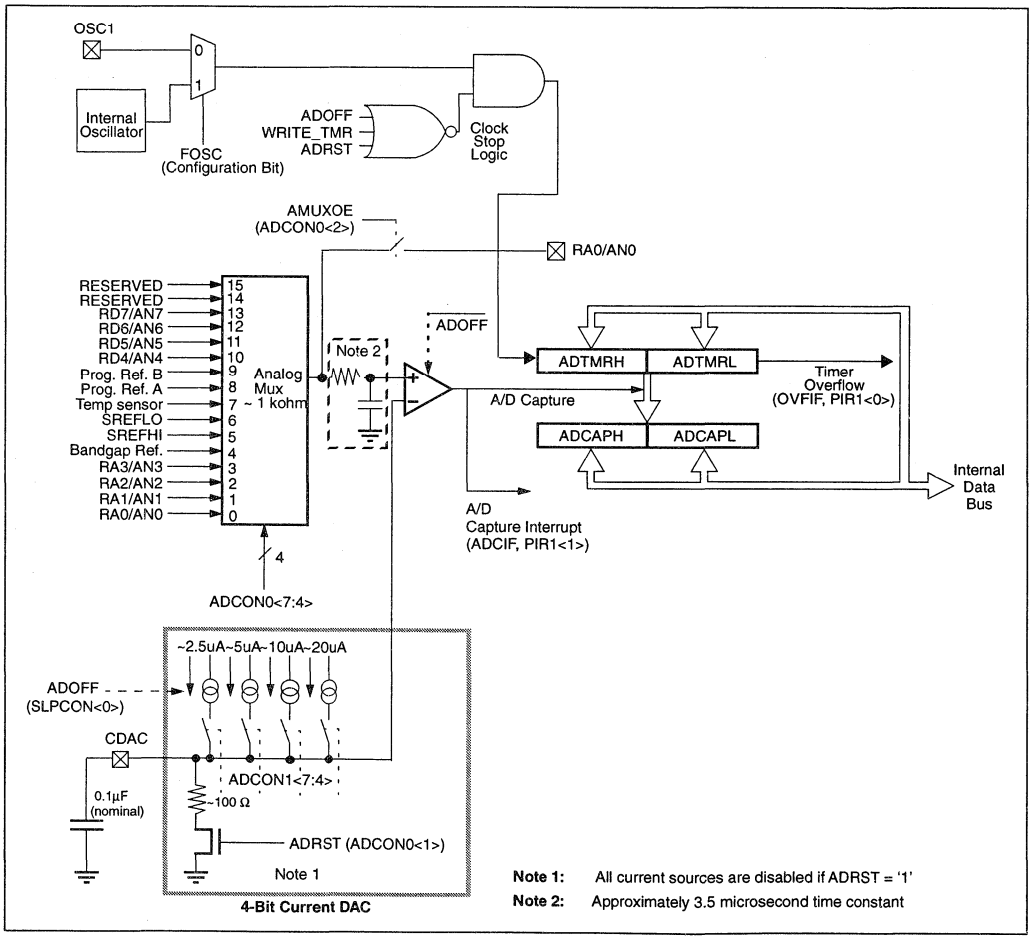
1. capture event
2. timer overflow

In a capture event, the comparator trips when the slope voltage on the CDAC output exceeds the input voltage, causing the comparator output to transition from high to low. This causes a transfer of the current timer count to the capture register and sets the ADCIF flag (PIR1<1>).

A CPU interrupt will be generated if bit ADCIE (PIE1<1>) is set to '1' (interrupt enabled). In addition, the Global Interrupt Enable and Peripheral Interrupt Enables (INTCON<7,6>) must also be set. Software is responsible for clearing the ADCIF flag prior to the next conversion cycle. Note that this interrupt can only occur once per conversion cycle.

In a timer overflow condition, the timer rolls over from FFFFh to 0000h, and a capture overflow flag (OVFIF) is asserted (PIR1<0>). The timer continues to increment following a timer overflow. A CPU interrupt can be generated if bit OVFIE (PIE1<0>) is set (interrupt enabled). In addition, the Global Interrupt Enable and Peripheral Interrupt Enables (INTCON<7,6>) must also be set. Software is responsible for clearing the OVFIF flag prior to the next conversion cycle.

FIGURE 8-1: A/D BLOCK DIAGRAM



Note 1: All current sources are disabled if ADRST = '1'

Note 2: Approximately 3.5 microsecond time constant

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FIGURE 8-2: EXAMPLE A/D CONVERSION CYCLE

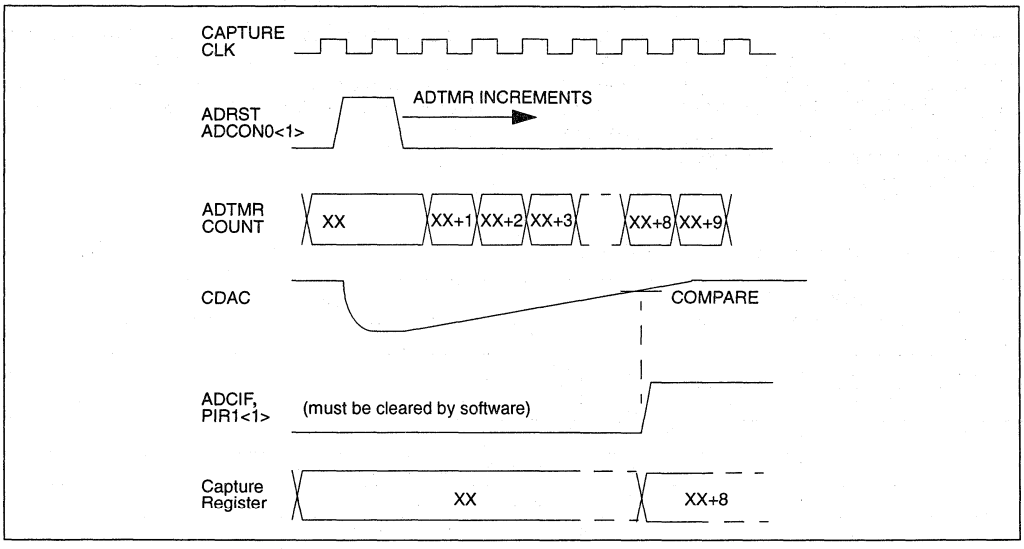

FIGURE 8-3: A/D CAPTURE TIMER (LOW BYTE)

0Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTMRL	b7	b6	b5	b4	b3	b2	b1	b0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

FIGURE 8-4: A/D CAPTURE TIMER (HIGH BYTE)

0Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTMRH	b15	b14	b13	b12	b11	b10	b9	b8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

FIGURE 8-5: A/D CAPTURE REGISTER (LOW BYTE)

15h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCAPL	b7	b6	b5	b4	b3	b2	b1	b0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

FIGURE 8-6: A/D CAPTURE REGISTER (HIGH BYTE)

16h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCAPH	b15	b14	b13	b12	b11	b10	b9	b8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Legend: U= unimplemented, X = unknown.

8.4 A/D Comparator

The PIC14000 includes a high gain comparator for A/D conversions. The positive input terminal of the A/D comparator is connected to the output of an analog mux through an RC low-pass filter. The nominal time-constant for the RC filter is 3.5 µs. The negative input terminal is connected to the external 0.1 µF (nominal) ramp capacitor.

8.5 Analog Mux

A total of 16 channels are internally multiplexed to the single A/D comparator positive input. Four configuration bits (ADCON0<7:4>) select the channel to be converted. Refer to Table 8-1 for channel assignments.

TABLE 8-1: A/D CHANNEL ASSIGNMENT

ADCON0(7:4)				A/D Channel
0	0	0	0	RA0/AN0 pin
0	0	0	1	RA1/AN1 pin
0	0	1	0	RA2/AN2 pin
0	0	1	1	RA3/AN3 pin
0	1	0	0	Bandgap reference voltage
0	1	0	1	Slope reference SREFHI
0	1	1	0	Slope reference SREFLO
0	1	1	1	Internal temperature sensor
1	0	0	0	Programmable reference A output
1	0	0	1	Programmable reference B output
1	0	1	0	RD4/AN4 pin
1	0	1	1	RD5/AN5 pin
1	1	0	0	RD6/AN6 pin
1	1	0	1	RD7/AN7 pin
1	1	1	0	Reserved
1	1	1	1	Reserved

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8.6 Programmable Current Source

Four configuration bits (ADCON1<7:4>) are used to control a programmable current source for generating the ramp voltage to the A/D comparator. It allows compensation for full-scale input voltage, clock frequency and CDAC capacitor tolerance variations. The current values range from 0 to 33.75 µA (nominal) in 2.25 µA increments. The intermediate values of the current source are as follows:

TABLE 8-2: PROGRAMMABLE CURRENT SOURCE SELECTION

ADCON1<7:4>				Current Source Output
0	0	0	0	OFF - all current sources disabled
0	0	0	1	2.25 µA
0	0	1	0	4.5 µA
0	0	1	1	6.75 µA
0	1	0	0	9 µA
0	1	0	1	11.25 µA
0	1	1	0	13.5 µA
0	1	1	1	15.75 µA
1	0	0	0	18 µA
1	0	0	1	20.25 µA
1	0	1	0	22.5 µA
1	0	1	1	24.75 µA
1	1	0	0	27 µA
1	1	0	1	29.25 µA
1	1	1	0	31.5 µA
1	1	1	1	33.75 µA

The programmable current source output is tied to the CDAC pin and is used to charge an external capacitor to generate the ramp voltage for the A/D comparator. (Refer to Figure 8-1.) This capacitor should have a low voltage-coefficient as found in teflon, polypropylene, or polystyrene capacitors, for optimum results. The capacitor must be discharged at the beginning of each conversion cycle by asserting ADRST (ADCON0<1>) for at least 200 µs to allow a complete discharge. Asserting ADRST disables the current sources internally. Current flow begins when ADRST is cleared.

8.7 A/D Control Registers

Two A/D control registers are provided on the PIC14000 to control the conversion process. These are ADCON0 (1Fh) and ADCON1 (9Fh). Both registers are readable and writable.

TABLE 8-3: A/D CONTROL AND STATUS REGISTER 0

1Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCON0	ADCS3	ADCS2	ADCS1	ADCS0	—	AMUXOE	ADRST	ADZERO
Read/Write	R/W	R/W	R/W	R/W	U	R/W	R/W	R/W
POR value 02h	0	0	0	0	0	0	1	0

Bit	Name	Function
B7-B4	ADCS3 ADCS2 ADCS1 ADCS0	A/D Channel Selects. Refer to Table 8-1.
B3	—	Unimplemented. Read as '0'.
B2	AMUXOE	Analog Mux Output Enable 1 = Connect AMUX Output to RA0/AN0 pin (overrides TRISA<0> setting) 0 = RA0/AN0 pin normal
B1	ADRST	A/D Reset Control Bit 1 = Stop the A/D Timer, discharge CDAC capacitor 0 = Normal operation (A/D running)
B0	ADZERO	A/D Zero Select Control. (Refer to Section 9.2) 1 = Enable zeroing operation on RA1/AN1 and RD5/AN5 0 = Normal operation (sample RA1/AN1 and RD5/AN5 pins)

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TABLE 8-4: A/D CONTROL AND STATUS REGISTER 1

9Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCON1	ADDAC3	ADDAC2	ADDAC1	ADDAC0	PCFG3	PCFG2	PCFG1	PCFG0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B4	ADDAC3 ADDAC2 ADDAC1 ADDAC0	A/D Current Source Selects. Refer to Table 8-2.
B3-B2	PCFG3 PCFG2	PORTD Configuration Selects (See Table 8-5)
B1-B0	PCFG1 PCFG0	PORTA Configuration Selects (See Table 8-5)

TABLE 8-5: PORTA AND PORTD CONFIGURATION

ADCON1<1:0>	RA0/AN0	RA1/AN1	RA2/AN2	RA3/AN3
ADCON1<3:2>	RD4/AN4	RD5/AN5	RD6/AN6	RD7/AN7
0 0	A	A	A	A
0 1	A	A	A	D
1 0	A	A	D	D
1 1	D	D	D	D

Legend: A = Analog input, D = Digital I/O

8.8 A/D Speed, Resolution and Capacitor Selection

The conversion time for the A/D converter on the PIC14000 can be calculated using the equation:

$$\text{Conversion Time} = (1/Fosc) \times 2^N$$

Where Fosc is the oscillator frequency and N is the number of bits of resolution desired.

Therefore at 4MHz, the conversion time for 16 bits is 16.384 msec. Conversely, it is 256 µsec for 10 bits.

Choosing the correct ramp capacitor for the CDAC pin is required to achieve the desired resolution, conversion time and full scale input voltage. The equation for selecting the ramp capacitor value is:

Capacitor = (conversion time in seconds) X (current source output in amps) / (full scale in volts)

Table 8-6 provides example capacitor values for the desired A/D resolution, conversion time, and full scale voltage measurement.

TABLE 8-6: CDAC CAPACITOR SELECTION (EXAMPLES FOR FULL SCALE OF 3.5V AND 1.5V)

A/D Resolution (Bits)	Conversion Time (Seconds)	Full Scale (Volts)	A/D Current Source Output (µamps)	Calculated CDAC Capacitor (Farads)	CDAC Capacitor Nearest Standard Value
16	0.016384	3.5	24.75	1.17E-07	.1uF
14	0.004096	3.5	24.75	2.93E-08	.022uF
12	0.001024	3.5	24.75	7.31E-09	6800pF
16	0.016384	1.5	24.75	2.73E-07	0.22µF
14	0.004096	1.5	24.75	6.83E-08	68nF
12	0.001024	1.5	24.75	1.71E-08	15nF

Note: Assumes Fosc of 4 MHz.

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9.0 OTHER ANALOG MODULES

The PIC14000 has additional analog modules for mixed signal applications. These include:

- bandgap voltage reference
- comparators with programmable references
- internal temperature sensor
- voltage regulator control

9.1 Bandgap Voltage Reference

The bandgap reference circuit is used to generate a 1.2V nominal stable voltage reference for the A/D and the low-voltage detector. The bandgap reference is channel 4 of the analog mux. The bandgap reference voltage is stored in the calibration space EPROM (See Table 4-2). To enable the bandgap reference REFOFF (SLPCON<5>) must be cleared.

9.2 Level-Shift Networks

The RA1/AN1 and RA5/AN5 pins have an internal level-shift network. A current source and resistor are used to bias the pin voltage by about +0.5V into a range usable by the A/D converter. The nominal value of bias current source is 5 µA and the resistor is 100 kohms.

The level-shift function can be turned on by clearing the LSOFF bit (SLPCON<4>) to '0'.

Note:	The minimum voltage permissible at the RA1/AN1 and RA5/AN5 pins is -0.3V. The input protection diodes will begin to turn on beyond -0.3V, introducing significant errors in the A/D readings. Under no conditions should the pin voltage fall below -0.5V.

9.2.1 ZEROING/FILTERING SWITCHES

The RA1/AN1 and RA5/AN5 inputs also have a matched pair of pass gates useful for current-measurement applications. One gate is connected between the pin and the level-shift network. The second pass gate is connected to ground as shown in Figure 9-1. By setting the ADZERO bit (ADCON0<0>), a zero-current condition is simulated. Subsequent A/D readings are calculated relative to this zero count from the A/D. This zeroing of the current provides very high accuracies at low current values where it is most needed.

For additional noise filtering or for capturing short duration periodic pulses, an optional filter capacitor may be connected from the SUM pin to ground (this feature is available for RA1/AN1 only). This forms an RC network with the internal 100 kohm (nominal) bias resistor to act as a low pass filter. The capacitor size can be adjusted for the desired time constant.

A switch is included between the output from the RA1/AN1 level-shift network and the SUM pin. This switch is closed during A/D sampling periods and is automatically opened during a zeroing operation (if ADZERO = '1'). If not required in the system, this pin should be left floating (not connected).

Setting the LSOFF bit (SLPCON<4>) disables the level-shift networks, so the RA1/AN1 and RA5/AN5 pins can continue to be used as general-purpose analog inputs.

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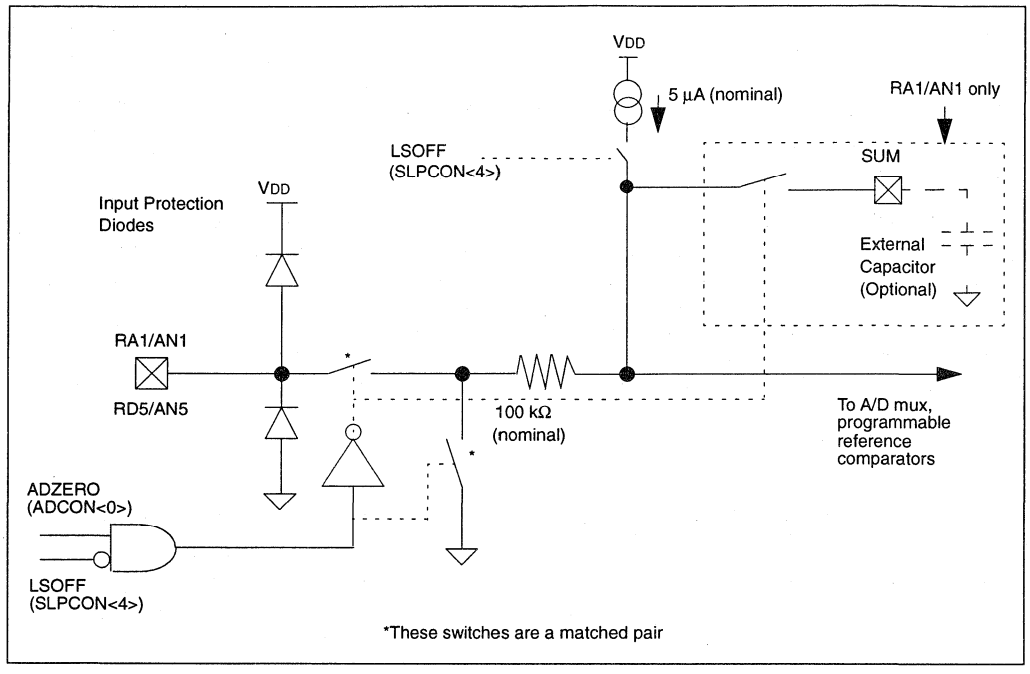
FIGURE 9-1: LEVEL-SHIFT NETWORKS



9.3 Slope Reference Voltage Divider

The slope reference voltage divider circuit, consisting of a buffer amplifier and resistor divider, is connected to the internal bandgap reference producing two other voltage references called SREFHI and SREFLO (see Figure 9-2). SREFHI is nominally the same as the bandgap voltage, 1.2V, and SREFLO is nominally 0.13V. These reference voltages are available on two of the analog multiplexer channels. The A/D module and firmware can measure the SREFHI and SREFLO voltages, and in conjunction with the KREF and KBG calibration data correct for the A/D's offset and slope errors. See AN624 for further details.

9.4 Internal Temperature Sensor

The internal temperature sensor is connected to the channel 7 input of the A/D converter. The sensor voltage is 1.05V nominal at 25°C and its temperature coefficient is approximately 3.7mV/°C. The sensor voltage at 25°C and the temperature coefficient values are stored in the calibration space EPROM (See Table 4-2). To enable the temperature sensor, the TEMPOFF bit (SLPCON<1>) must be cleared.

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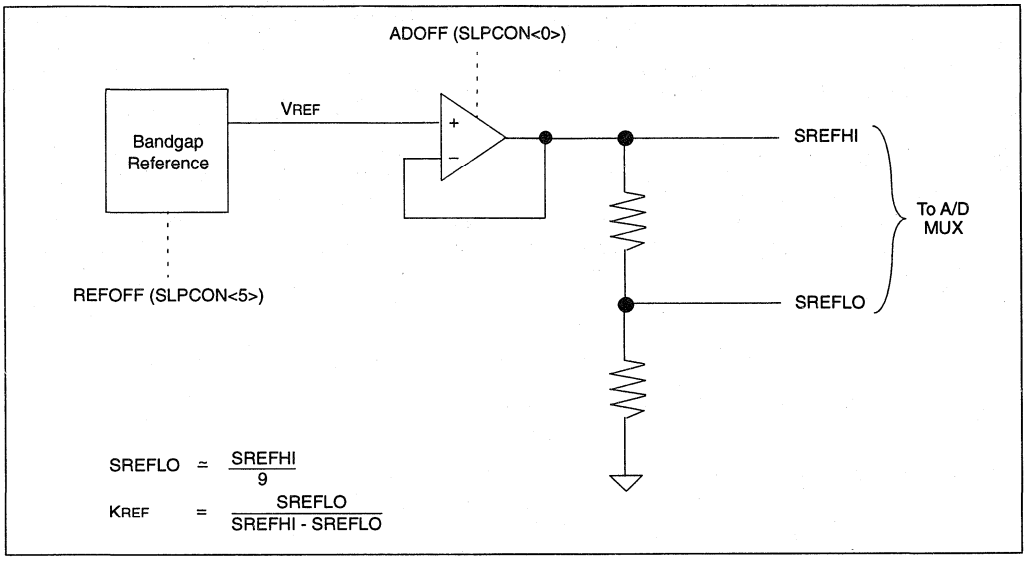
FIGURE 9-2: SLOPE REFERENCE DIVIDER



9.5 Comparator and Programmable Reference Modules

9.5.1 COMPARATORS

The PIC14000 includes two independent low-power comparators for comparing the programmable reference outputs to either the RA1/AN1 or RA5/AN5 pins. The negative input of each comparator is tied to one of the reference outputs as shown in Figure 9-3. The comparator positive inputs are connected to the output of the RA1/AN1 and RA5/AN5 level-shift networks.

At reset, the RA1/AN1 level-shift output is connected to the positive inputs of both comparators. This allows a window comparison of the RA1/AN1 voltage using the two programmable references and comparators. Setting CMBOE (CMCON<5>) changes the configuration so that RA1/AN1 and RA5/AN5 may be independently monitored.

The comparator outputs can be read by the CMAOUT (CMCON<2>) and CMBOUT (CMCON<6>) bits. These are read-only bits and writes to these locations have no effect.

Either a rising or falling comparator output can generate an interrupt to the CPU as controlled by the polarity bits CPOLA (CMCON<0>) and CPOLB (CMCON<4>). The CMIF bit (PIR1<7>) interrupt flag is set whenever the exclusive-OR of the comparator output CMxOUT and the CPOLx bits equal a logic one. As with other peripheral interrupts, the corresponding enable bit CMIE (PIE1<7>) must also be set to enable the comparator interrupt. In addition, the global interrupt enable and peripheral interrupt enable bits INTCON<7:6> must also be set. This comparator interrupt is level sensitive.

The comparator outputs are visible at either RC1/CMPA or RD2/CMPB pins by setting the CMAOE (CMCON<1>) or CMBOE (CMCON<5>) bits. Setting CMxOE does not affect the comparator operation. It only enables the pin function regardless of the port TRIS register setting.

Both the references and the comparators are enabled by clearing the CMOFF (SLPCON<2>) bit.

9.5.2 PROGRAMMABLE REFERENCES

The PIC14000 includes two independent, programmable voltage references. Each reference is built using two resistor ladders, bandgap-referenced current source, and analog multiplexers. The first ladder contains 32 taps, and is divided into three ranges (upper, middle, and lower) to provide a coarse voltage adjustment. The coarse ladder includes 1k and 10k resistors yielding a step size of either 5 or 50 mV (nominal) depending on the selected range. Figure 9-8 shows the comparator and reference architecture.

A second ladder contains eight taps, and is connected across the selected coarse ladder resistor to increase resolution. This subdivides the coarse ladder step by approximately 1/8. Thus, resolutions approaching 5/8 mV are obtainable.

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Two registers PREFA (9Bh) and PREFB (9Ch) are used to select the reference output voltages. The PREFx<7:3> bits select the output from the coarse ladder, while PREFx<2:0> bits are for the fine-tune adjustment. Table 9-1 and Table 9-2 show the reference decoding.

These voltages are visible at either RC0/REFA or RD3/REFB pins by setting the CMAOE (CMCON<1>) or CMBOE (CMCON<5>) bits. Setting CMxOE does not affect the reference voltages. It only enables the pin function regardless of the port TRIS register setting. These outputs are not buffered, so they cannot directly drive any DC loads.

The reference outputs are also connected to two independent comparators, COMPA and COMPB. Thus, the references can be used to set the comparator trippoints. The A/D converter can also monitor the reference outputs via A/D channels 8 and 9. Refer to Section 8 for the description of the A/D operation.

The programmable reference output is designed to track the output from the level shift network. However, there will always be some mismatch due to component drift. For best accuracy, the A/D should be used to periodically calibrate the references to the desired set-point.

FIGURE 9-3: COMPARATOR AND PROGRAMMABLE REFERENCE BLOCK DIAGRAM (ONE OF TWO SHOWN)

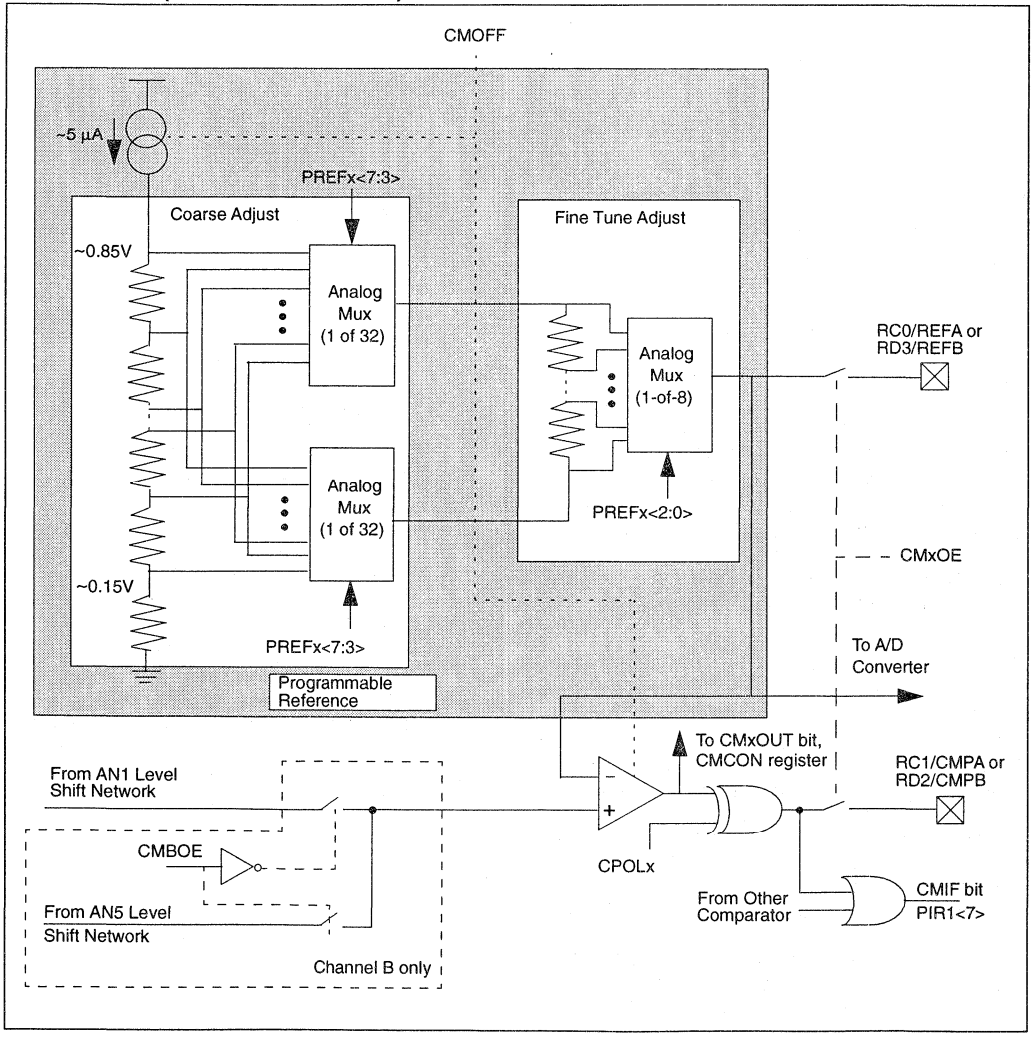

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TABLE 9-1: PROGRAMMABLE REFERENCE COARSE RANGE SELECTION

	PREFx<7:3>					Nominal Output Voltage Range (V)
Upper	0	1	1	1	1	0.8000 - 0.8500
	0	1	1	1	0	0.7500 - 0.8000
	0	1	1	0	1	0.7000 - 0.7500
	0	1	1	0	0	0.6500 - 0.7000
	0	1	0	1	1	0.6000 - 0.6500
	0	1	0	1	0	0.5500 - 0.6000
Middle	0	1	0	0	1	0.5450 - 0.5500
	0	1	0	0	0	0.5400 - 0.5450
	0	0	1	1	1	0.5350 - 0.5400
	0	0	1	1	0	0.5300 - 0.5350
	0	0	1	0	1	0.5250 - 0.5300
	0	0	1	0	0	0.5200 - 0.5250
	0	0	0	1	1	0.5150 - 0.5200
	0	0	0	1	0	0.5100 - 0.5150
	0	0	0	0	1	0.5050 - 0.5100
	0	0	0	0	0	0.5000 - 0.5050
	1	0	0	0	0	0.4950 - 0.5000
	1	0	0	0	1	0.4900 - 0.4950
	1	0	0	1	0	0.4850 - 0.4900
	1	0	0	1	1	0.4800 - 0.4850
	1	0	1	0	0	0.4750 - 0.4800
	1	0	1	0	1	0.4700 - 0.4750
	1	0	1	1	0	0.4650 - 0.4700
	1	0	1	1	1	0.4600 - 0.4650
	1	1	0	0	0	0.4550 - 0.4600
	1	1	0	0	1	0.4500 - 0.4550
Lower	1	1	0	1	0	0.4000 - 0.4500
	1	1	0	1	1	0.3500 - 0.4000
	1	1	1	0	0	0.3000 - 0.3500
	1	1	1	0	1	0.2500 - 0.3000
	1	1	1	1	0	0.2000 - 0.2500
	1	1	1	1	1	0.1500 - 0.2000

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TABLE 9-2: PROGRAMMABLE REFERENCE FINE RANGE SELECTION

PREFx<2:0>			Fractional Value Of The Coarse Range
0	0	0	1/8
0	0	1	1/4
0	1	0	3/8
0	1	1	1/2
1	0	0	5/8
1	0	1	3/4
1	1	0	7/8
1	1	1	1

FIGURE 9-4: PROGRAMMABLE REFERENCE TRANSFER FUNCTION

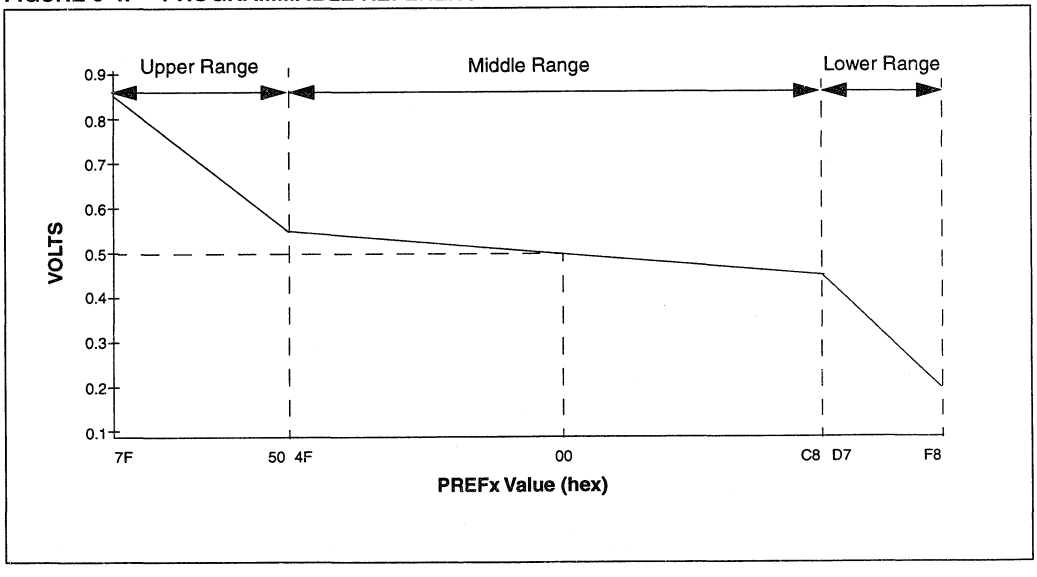

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FIGURE 9-5: COMPARATOR CONTROL REGISTER

9Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMCON	U	CMBOUT	CMBOE	CPOLB	U	CMAOUT	CMAOE	CPOLA
Read/Write	—	R	R/W	R/W	—	R	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7	—	Unimplemented. Read as '0'.
B6	CMBOUT	Comparator B Output Reading this bit returns the status of the comparator B output. Writes to this bit have no effect.
B5	CMBOE	Comparator B Output Enable 1 = Comparator B output is available on RD2/CMPB pin and Reference B output is available on RD3/REFB pin. 0 = RD2/CMPB and RD3/REFB assume normal PORTD function.
B4	CPOLB	Comparator B Polarity Bit 1 = Invert the output of comparator B. 0 = Do not invert the output of comparator B.
B3	—	Unimplemented. Read as '0'.
B2	CMAOUT	Comparator A Output Reading this bit returns the status of the comparator A output. Writes to this bit have no effect.
B1	CMAOE	Comparator A Output Enable 1 = Comparator A output is available on RC1/CMPA pin and Reference A output is available on RC0/REFA pin. 0 = RC0/REFA and RC1/CMPA assume normal PORTC function.
B0	CPOLA	Comparator A Polarity Bit 1 = Invert the output of comparator A. 0 = Do not invert the output of comparator A.

FIGURE 9-6: PREFA REGISTER

9Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREFA	PRA7	PRA6	PRA5	PRA4	PRA3	PRA2	PRA1	PRA0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B0	PRA7 PRA6 PRA5 PRA4 PRA3 PRA2 PRA1 PRA0	Programmable Reference A Voltage Select Bits. See Table 9-1 and Table 9-2 for decoding.

FIGURE 9-7: PREFB REGISTER

9Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREFB	PRB7	PRB6	PRB5	PRB4	PRB3	PRB2	PRB1	PRB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B0	PRB7 PRB6 PRB5 PRB4 PRB3 PRB2 PRB1 PRB0	Programmable Reference B Voltage Select Bits. See Table 9-1 and Table 9-2 for decoding.

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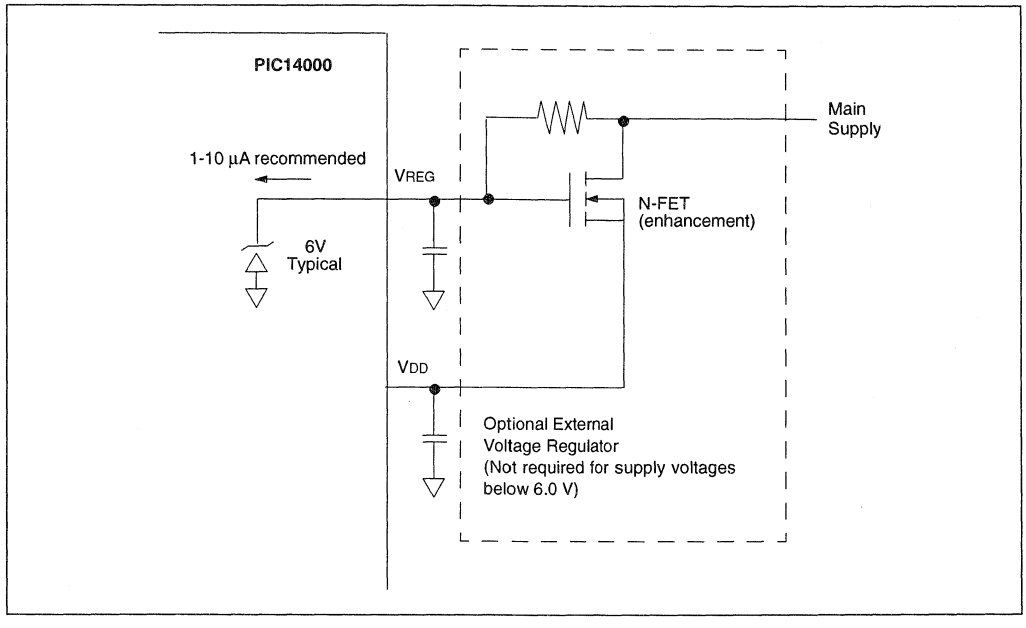
9.6 Voltage Regulator Output

For systems with a main supply voltage above 6V, an inexpensive, low quiescent current voltage regulator can be formed by connecting the VREG pin to an external resistor and FET as shown in Figure 9-8. This circuit will provide a VDD of about 5V, after the voltage drop across the FET.

FIGURE 9-8: VOLTAGE REGULATOR CIRCUIT



NOTES:

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10.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC14000 has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- OSC (oscillator) selection
  - Crystal/resonator
  - Internal oscillator
- Reset options
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP and HIBERNATE modes
- Code protection
- In-circuit serial programming

These features will be described in the following sections.

10.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 10-1: CONFIGURATION WORD

2007h	Bit 13-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BITS	r	CPC	r	CPP1	CPP0	$\overline{\text{PWRTE}}$	WDTE	r	FOSC
Read/Write	R/W	R/W	Reserved	R/W	R/W	R/W	R/W	Reserved	R/W
Erased value	1	1	1	1	1	1	1	1	1

Bit	Name	Function
B13-B8	r	Reserved
B7	CPC	Calibration Space Code Protection Bit 1 = Calibration space is readable and programmable 0 = Calibration space is write protected
B6	r	Reserved
B5	CPP1	Program Space Code Protection Bit 1 = Program space is readable and programmable 0 = Program space is read/write protected
B4	CPP0	Program Space Code Protection Bit 1 = Program space is readable and programmable 0 = Program space is read/write protected
B3	$\overline{\text{PWRTE}}$	Power-up Timer Enable Bit 1 = Power-up timer is disabled 0 = Power-up timer is enabled
B2	WDTE	Watchdog Timer Enable Bit 1 = WDT is enabled 0 = WDT is disabled
B1	r	Reserved
B0	FOSC	Oscillator Selection Bit 1 = IN oscillator (internal) 0 = HS oscillator (crystal/resonator)

10.2 Oscillator Configurations

The PIC14000 can be operated with two different oscillator options. The user can program a configuration word (CONFIG<0>) to select one of these:

- HS High Speed Crystal/Ceramic Resonator (CONFIG<0> ='0')
- IN Internal oscillator (CONFIG<0> ='1') (Default)

10.2.1 INTERNAL OSCILLATOR CIRCUIT

The PIC14000 includes an internal oscillator option that offers additional cost and board-space savings. No external components are required. The nominal operating frequency is 4 MHz. The frequency is measured and stored into the calibration space in EPROM.

By selecting IN mode OSC1/PBTN becomes a digital input (with weak internal pull-up resistor) and can be read via bit MISC<0>. Writes to this location have no effect. The OSC1/PBTN input is capable of generating an interrupt to the CPU if enabled (Section 10.6). Also, the OSC2 pin becomes a digital output for general purpose use and is accessed via MISC<1>. Writes to this bit directly affect the OSC2 pin. Reading this bit returns the contents of the output latch. The MISC register format is shown in Figure 10-2.

The OSC2 pin can also output the IN oscillator frequency, divided-by-four, by setting INCLKEN (MISC<2>).

Note: The OSC2 output buffer provides less drive than standard I/O.

FIGURE 10-2: MISC REGISTER

9Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MISC	SMHOG	SPGNDB	SPGNDA	I^2CSEL	SMBUS	INCLKEN	OSC2	OSC1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
POR value 00h	0	0	0	0	0	0	0	X

Bit	Name	Function
B7	SMHOG	SMHOG enable 1 = Stretch I^2C CLK signal (hold low) when receive data buffer is full (refer to Section 7.5.4). For pausing I^2C transfers while preventing interruptions of A/D conversions. 0 = Disable I^2C CLK stretch.
B6	SPGNDB	Serial Port Ground Select 1 = PORTD<1:0> ground reference is the RD5/AN5 pin. 0 = PORTD<1:0> ground reference is Vss.
B5	SPGNDA	Serial Port Ground Select 1 = PORTC<7:6> ground reference is the RA1/AN1 pin. 0 = PORTC<7:6> ground reference is Vss.
B4	I^2CSEL	I^2C Port select Bit. 1 = PORTD<1:0> are used as the I^2C clock and data lines. 0 = PORTC<7:6> are used as the I^2C clock and data lines.
B3	SMBus	SMBus-Compatibility Select 1 = SMBus compatibility mode is enabled. PORTC<7:6> and PORTD<1:0> have SMBus-compatible input thresholds. 0 = SMBus-compatibility is disabled. PORTC<7:6> and PORTD<1:0> have Schmitt Trigger input thresholds.
B2	INCLKEN	Oscillator Output Select (available in IN mode only). 1 = Output IN oscillator signal divided by four on OSC2 pin. 0 = Disconnect IN oscillator signal from OSC2 pin.
B1	OSC2	OSC2 output port bit (available in IN mode only). Writes to this location affect the OSC2 pin in IN mode. Reads return the value of the output latch.
B0	OSC1	OSC1 input port bit (available in IN mode only). Reads from this location return the status of the OSC1 pin in IN mode. Writes have no effect.

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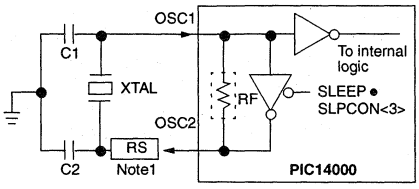
10.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATOR

In HS mode, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. A parallel cut crystal is required. Use of a series cut crystal may give a frequency outside of the crystal manufacturer's specifications. When in HS mode, the device can have an external clock source to drive the OSC1 pin.

FIGURE 10-3: CRYSTAL/CERAMIC RESONATOR OPERATION (HS OSC CONFIGURATION)



See Table 10-1 and Table 10-2 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.

FIGURE 10-4: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)

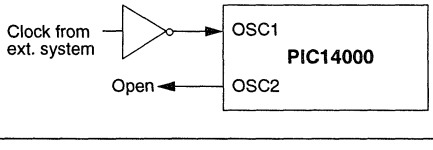


TABLE 10-1: CERAMIC RESONATORS

Mode	Freq	C1	C2
HS	4 MHz	15 - 68 pF	15 - 68 pF
	8 MHz	10 - 68 pF	10 - 68 pF
	16 MHz	10 - 22 pF	10 - 22 pF

Note: Recommended values of C1 and C2 are identical to the ranges tested table.
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

Resonators Used:		
4 MHz	Murata Erie CSA4.00MG	+/-.5%
8 MHz	Murata Erie CSA8.00MT	+/-.5%
16 MHz	Murata Erie CSA16.00MX	+/-.5%

All resonators used did not have built-in capacitors.

TABLE 10-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	C1	C2
HS	4 MHz	15 - 33 pF	15 - 33 pF
	8 MHz	15 - 47 pF	15 - 47 pF
	20 MHz	15 - 47 pF	15 - 47 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
For VDD > 4.5V, C1 = C2 ≈ 30pf is recommended.

10.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 10-5 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 10-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

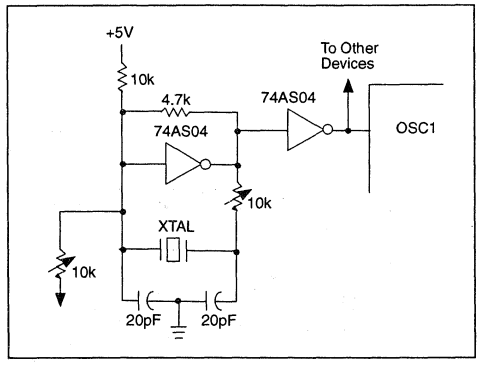
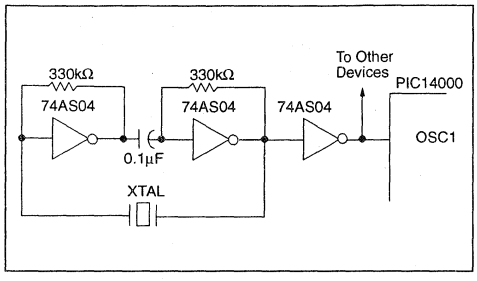


Figure 10-6 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 10-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



10.3 Reset

The PIC14000 differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{MCLR}$ Reset during normal operation
- $\overline{MCLR}$ Reset during SLEEP
- WDT Reset (normal operation)

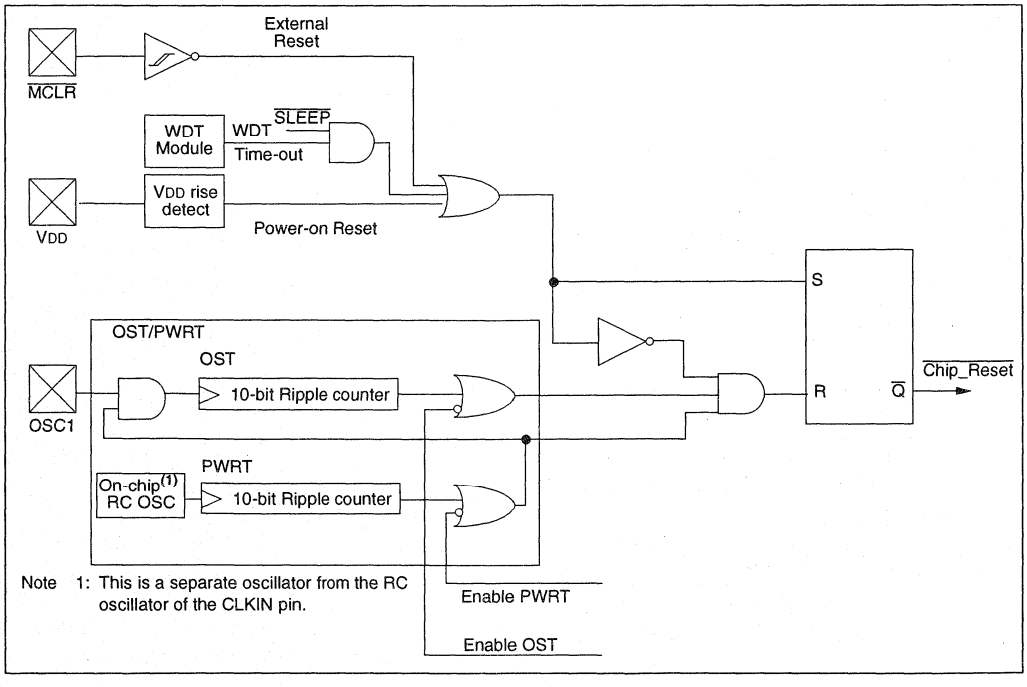
Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on the $\overline{MCLR}$ and WDT Reset, and on $\overline{MCLR}$ Reset during SLEEP. They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 10-3. These bits are used in software to determine the nature of the reset. See Table 10-5 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 10-7.

The devices all have a $\overline{MCLR}$ noise filter in the $\overline{MCLR}$ reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

FIGURE 10-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.

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TABLE 10-3: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{TO}$	$\overline{PD}$	Meaning
0	1	1	Power-On Reset
0	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	1	WDT reset during normal operation
1	0	0	WDT time-out wakeup from sleep
1	1	1	$\overline{MCLR}$ reset during normal operation
1	1	0	$\overline{MCLR}$ reset during SLEEP or HIBERNATE, or interrupt wake-up from SLEEP or HIBERNATE.

10.4 Low-Voltage Detector

The PIC14000 contains an integrated low-voltage detector. The supply voltage is divided and compared to the bandgap reference output. If the supply voltage (V_{DD}) falls below V_{TRIP-}, then the low-voltage detector will cause $\overline{LVD}$ (PCON<0>) to be reset. This bit can be read by software to determine if a low voltage condition occurred. This bit must be set by software.

The nominal values of the low-voltage detector trip points are as follows:

- V_{TRIP-} = 2.55V
- V_{TRIP+} = 2.60V
- Hysteresis (V_{TRIP+} – V_{TRIP-}) = 55 mV

10.5 Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)

10.5.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to V_{DD}. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for V_{DD} is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*."

10.5.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from $\overline{POR}$. The power-up timer operates from a local internal oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A configuration bit, $\overline{PWRTE}$, can disable (if set, or unprogrammed) or enable (if cleared, or programmed) the power-up timer.

The power-up timer delay will vary from chip to chip and due to V_{DD} and temperature.

10.5.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycles (from OSC1 input) delay after the PWRT delay is over. This guarantees that the crystal oscillator or resonator has started and stabilized.

10.5.4 IN OSCILLATOR START-UP

There is an 8-cycle delay in IN mode to ensure stability only after a Power-on Reset (POR) or wake-up from SLEEP.

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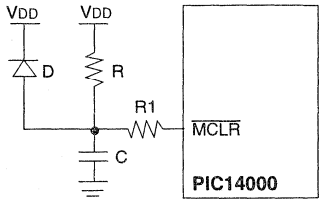
10.5.5 TIMEOUT SEQUENCE

On power-up the time-out sequence is as follows: First the PWRT time-out is invoked after $\overline{POR}$ has expired. The OST is activated only in HS (crystal oscillator) mode. The total time-out will vary based on the oscillator configuration and $\overline{PWRTE}$ status. For example, in IN mode, with $\overline{PWRTE}$ unprogrammed (PWRT disabled), there will be no time-out delay at all. Figure 11-4 depicts the power-on reset time-out sequences.

Table 10-4 shows the reset conditions for some special registers, while Table 10-5 shows the reset conditions for all registers.

FIGURE 10-8: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



1. External power-on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{MCLR}$ pin is 5 µA). A larger voltage drop will degrade VIH level on $\overline{MCLR}$ pin.
3. R1 = 100 Ω to 1 KΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to ESD or EOS.

TABLE 10-4: RESET CONDITION FOR SPECIAL REGISTERS

Condition	PCL Addr: 02h	STATUS Addr: 03h	PCON Addr: 8Eh
Power-on Reset	000h	0001 1xxx	0--- --0x
$\overline{MCLR}$ reset during normal operation	000h	0001 1uuu	u--- --ux
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	u--- --ux
WDT reset during normal operation	000h	0000 1uuu	u--- --ux
WDT during SLEEP	PC + 1	uuu0 0uuu	u--- --ux
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	u--- --ux

Legend: u = unchanged
x = unknown
- = unimplemented, read as '0'

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

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TABLE 10-5: RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on Reset	MCLR reset during - normal operation - SLEEP WDT time-out during normal operation	Wake-up from SLEEP through interrupt Wake up from SLEEP through WDT time-out
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000h	0000h	PC + 1(2)
STATUS	03h/83h	0001 1xxx	000? ?uuu(3)	uuu? ?uuu(3)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---- xxxx	---- uuuu	---- uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu(1)
ADTMRL	0Eh	0000 0000	0000 0000	uuuu uuuu
ADTMRH	0Fh	0000 0000	0000 0000	uuuu uuuu
I2CBUF	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
I2CCON	14h	0000 0000	0000 0000	uuuu uuuu
ADCAPL	15h	0000 0000	0000 0000	uuuu uuuu
ADCAPH	16h	0000 0000	0000 0000	uuuu uuuu
ADCON0	1Fh	0000 0010	0000 0010	uuuu uuuu
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	---- 1111	---- 1111	---- uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD	88h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PCON	8Eh	---- --0x	---- --uu	---- --uu
SLPCON	8Fh	0011 1111	0011 1111	uuuu uuuu
I2CADD	93h	0000 0000	0000 0000	uuuu uuuu
I2CSTAT	94h	--00 0000	--00 0000	--uu uuuu
PREFA	9Bh	0000 0000	0000 0000	uuuu uuuu
PREFB	9Ch	0000 0000	0000 0000	uuuu uuuu
CMCON	9Dh	0x00 0x00	0x00 0x00	uuuu uuuu
MISC	9Eh	0000 000x	0000 000x	uuuu uuuu
ADCON1	9Fh	0000 0000	0000 0000	uuuu uuuu

Legend: u=unchanged, x =unknown, - = unimplemented, reads as '0', ? = value depends on condition.

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: See Table 10-4 for reset value for specific condition.

10.6 Interrupts

The PIC14000 has several sources of interrupt:

- External interrupt from OSC1/PBTN pin
- I^2C port interrupt
- PORTC interrupt on change (pins RC<7:4> only)
- Timer0 overflow
- A/D timer overflow
- A/D converter capture event
- Programmable reference comparator interrupt

This section addresses the external and Timer0 interrupts only. Refer to the appropriate sections for description of the serial port, programmable reference and A/D interrupts.

INTCON records individual interrupt requests in flag bits. It also has individual and global enable bits. The peripheral interrupt flags reside in the PIR1 register. Peripheral interrupt enable interrupts are contained in the PIE1 register.

Global interrupt masking is controlled by GIE (INTCON<7>). Individual interrupts can be disabled through their corresponding mask bit in the INTCON register. GIE is cleared on reset to mask interrupts.

When an interrupt is serviced, the GIE is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h, the interrupt vector. For external interrupt events, such as the I^2C interrupt, the interrupt latency will be 3 or 4 instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for 1 or 2 cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit to allow polling.

The return from interrupt instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit to re-enable interrupts.

Note 1: The individual interrupt flags will be set by the specified condition even though the corresponding interrupt enable bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled).

Note 2: If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction). The events that would cause this to occur are:

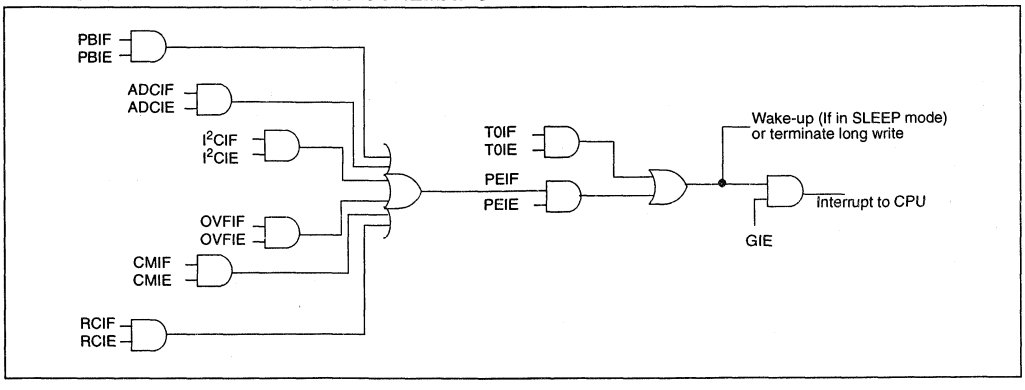
1. An instruction clears the GIE bit while an interrupt is acknowledged.
2. The program branches to the interrupt vector and executes the Interrupt Service Routine.
3. The interrupt service routine completes with the execution of the RETFIE instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GIE bit was cleared by the instruction, as shown in the following code:

```
LOOP: BCF    INTCON,GIE  ; Disable Global Interrupts
      BTFSC  INTCON,GIE  ; Global Interrupts Disabled?
      GOTO   LOOP        ; No, try again
      :                  ; Yes, continue with program
                         ;      flow
```

FIGURE 10-9: INTERRUPT LOGIC SCHEMATIC



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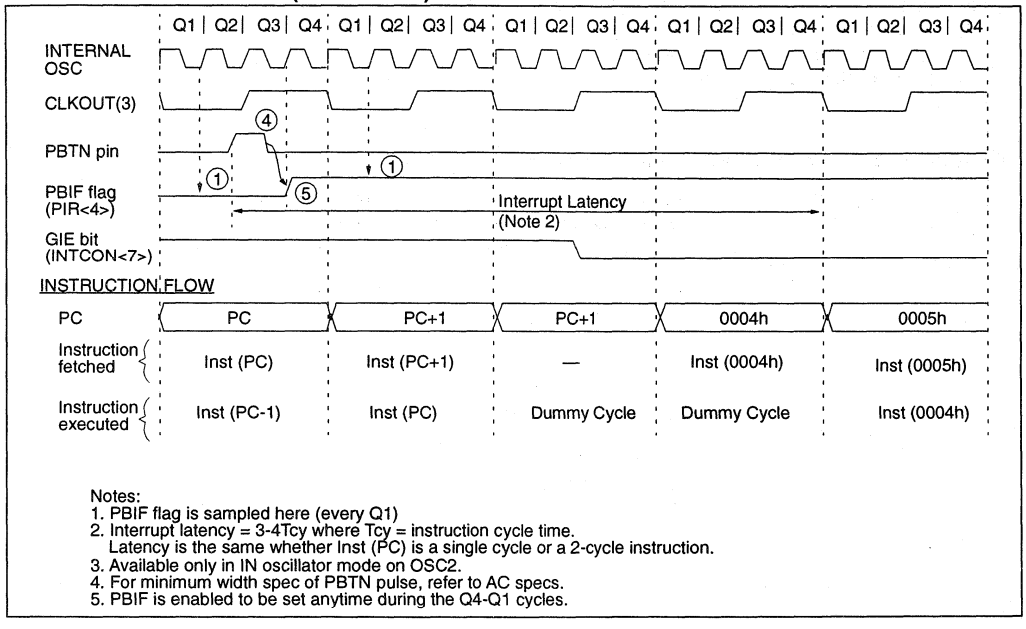
10.6.1 EXTERNAL INTERRUPT

An external interrupt can be generated via the OSC1/PBTN pin if IN (internal oscillator) mode is enabled. This interrupt is falling edge triggered. When a valid edge appears on OSC1/PBTN pin, PBIF (PIR1<4>) is set. This interrupt can be disabled by clearing PBIE (PIE1<4>). PBIF must be cleared in software in the interrupt service routine before re-enabling the interrupt. This interrupt can wake up the processor from SLEEP if PBIE bit is set (interrupt enabled) prior to going into SLEEP mode. The status of the GIE bit determines whether or not the processor branches to the interrupt vector following wake-up. The timing of the external interrupt is shown in Figure 10-10.

FIGURE 10-10: EXTERNAL (OSC1/PBTN) INTERRUPT TIMING



Notes:
1. PBIF flag is sampled here (every Q1)
2. Interrupt latency = 3-4Tcy where Tcy = instruction cycle time.
   Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. Available only in IN oscillator mode on OSC2.
4. For minimum width spec of PBTN pulse, refer to AC specs.
5. PBIF is enabled to be set anytime during the Q4-Q1 cycles.

10.6.2 TIMER0 INTERRUPT

An overflow (FFh → 00h) in Timer0 will set the T0IF (INTCON<2>) flag. Setting T0IE (INTCON<5>) enables the interrupt.

10.6.3 PORTC INTERRUPT ON CHANGE

An input change on PORTC<7:4> sets RCIF (PIR1<2>). Setting RCIE (PIE1<2>) enables the interrupt. For operation of PORTC, refer to Section 5.2.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RCIF interrupt flag may not be set.

10.6.4 CONTEXT SWITCHING DURING INTERRUPTS

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, for example, W register and Status register. Example 10-1 is an example that shows saving registers in RAM.

EXAMPLE 10-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF    W_TEMP           ;Copy W to TEMP register, could be any bank
SWAPF    STATUS,W         ;Swap status to be saved into W
BCF      STATUS,RP1       ;Change to bank zero, regardless of current bank
BCF      STATUS,RP0       ;
MOVWF    STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF    STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                          ;(sets bank to original state)
MOVWF    STATUS           ;Move W into STATUS register
SWAPF    W_TEMP,F         ;Swap W_TEMP
SWAPF    W_TEMP,W         ;Swap W_TEMP into W
```

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10.7 Watchdog Timer (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the IN oscillator used to generate the CPU and A/D clocks. That means that the WDT will run even if the clock has been stopped, for example, by execution of a SLEEP instruction. Refer to Section 10.8.1 for more information.

During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation.

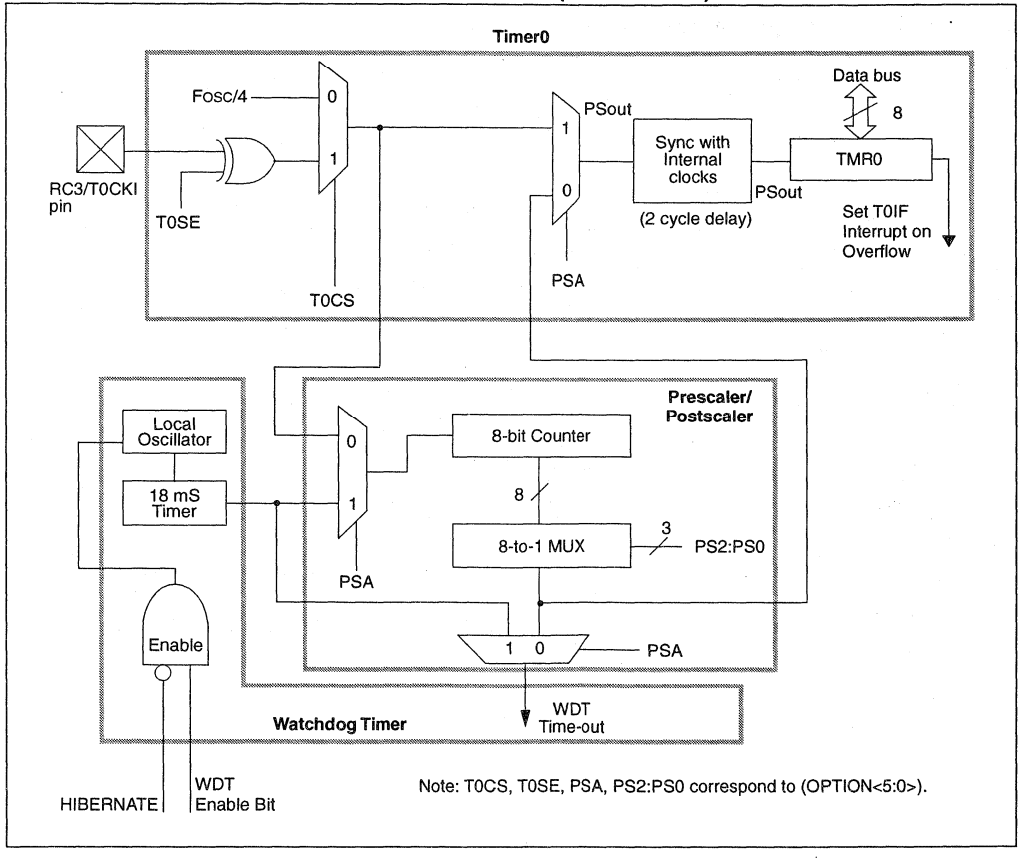
The WDT can be permanently disabled by programming the configuration bit WDTE as a '0'. Its oscillator can be shut down to conserve battery power by entering HIBERNATE Mode. Refer to Section 10.8.3 for more information on HIBERNATE mode.

CAUTION: Beware of disabling WDT if software routines require exiting based on WDT reset. For example, the MCU will not exit HIBERNATE mode based on WDT reset.

A block diagram of the watchdog timer is shown in Figure 10-11. It should be noted that a RESET generated by the WDT time-out does not drive $\overline{MCLR}$ low.

3

FIGURE 10-11: WATCHDOG TIMER BLOCK DIAGRAM (WITH TIMER0)



10.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, VDD and process variations (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION registers. Thus, time-out periods up to 2.3 seconds can be realized. The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{TO}$ bit in the status register will be cleared upon a watchdog timer time-out. The WDT time-out period (no prescaler) is measured and stored in calibration space at location 0FD2h.

10.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst-case conditions (minimum VDD, maximum temperature, maximum WDT prescaler) it may take several seconds before a WDT time-out occurs. Refer to Section 6.3 for prescaler switching considerations.

10.8 Power Management Options

The PIC14000 has several power management options to prolong battery lifetime. The SLEEP instruction halts the CPU and can turn off the on-chip oscillators. The CPU can be in SLEEP mode, yet the A/D converter can continue to run. Several bits are included in the SLPCON register (8Fh) to control power to analog modules.

TABLE 10-6: SUMMARY OF POWER MANAGEMENT OPTIONS

Function	Summary
CPU Clock	OFF during SLEEP/HIBERNATE mode, ON otherwise
Main Oscillator	ON if NOT in SLEEP mode. In SLEEP mode, controlled by OSCOFF bit, SLPCON<3>.
Watchdog Timer	Controlled by WDTE, 2007h<2> and HIBEN, SLPCON<7>
Temperature Sensor	Controlled by TEMPOFF, SLPCON<1>
Low-voltage Detector	Controlled by REFOFF, SLPCON<5>
Comparator and Programmable References	Controlled by CMOFF, SLPCON<2>
A/D Comparator	Controlled by ADOFF, SLPCON<0>
Programmable Current Source	Controlled by ADOFF, SLPCON<0> and ADCON1<7:4>
Slope Reference Voltage Divider	Controlled by ADOFF, SLPCON<0>
Level Shift Networks	Controlled by LSOFF, SLPCON<4>
Bandgap Reference	Controlled by REFOFF, SLPCON<5>
Voltage Regulator Control	Always ON. Does not consume power if unconnected.
Power On Reset	Always ON, except in SLEEP/HIBERNATE mode

Note: Refer to analog specs for individual peripheral operating currents.

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10.8.1 SLEEP MODE

The SLEEP mode is entered by executing a SLEEP instruction.

If SLEEP mode is enabled, the WDT will be cleared but keep running. The $\overline{PD}$ bit in the STATUS register is cleared, the $\overline{TO}$ bit is set, and on-chip oscillators are shut off, except the WDT RC oscillator, which continues to run. The I/O ports maintain the status they had before the SLEEP command was executed (driving high, low, or high-impedance).

It is an option while in SLEEP mode to leave the on-chip oscillator running. This option allows an A/D conversion to continue while the CPU is in SLEEP mode. The CPU clocks are stopped in this condition to preserve power. The operation of the on-chip oscillator during SLEEP is controlled by OSCOFF (SLPCON<3>). Clearing this bit to '0' allows the oscillator to continue to run. This bit is only active in SLEEP mode.

For lowest power consumption in this mode, all I/O pins should be either at VDD or VSS with no external circuitry drawing current from the I/O pin. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid leakage currents caused by floating inputs. The $\overline{MCLR}$ pin must be at a logic high level (VIH). The contribution from any on-chip pull-up resistors should be considered.

10.8.2 WAKE-UP FROM SLEEP

The PIC14000 can wake up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin
2. Watchdog Timer time-out (if WDT is enabled)
3. Interrupt from OSC1/PBTN pin
4. RC<7:4> port change
5. I^2C (serial port) start/stop bit detect interrupt.
6. Wake-up on programmable reference comparator interrupt.
7. A/D conversion complete (comparator trip) interrupt.
8. A/D timer overflow interrupt.

An external reset on $\overline{MCLR}$ pin causes a device reset. The other wake-up events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused a wake-up).

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set. Wake-up occurs regardless of the state of bit GIE. If bit GIE is clear, the device continues execution at the instruction after the SLEEP instruction. If bit GIE is set, the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake from SLEEP.

10.8.3 HIBERNATE MODE

HIBERNATE mode is an extension of SLEEP mode with the following additions.

- WDT is forced off
- Weak pull-ups on RC<5:0> are disabled
- Some input buffers are gated-off (refer to Section 5.0)

The HIBERNATE mode is entered by executing a SLEEP instruction with HIBEN (SLPCON<7>) bit set.

The PIC14000 wakes up from HIBERNATE mode via all the same mechanisms as SLEEP mode, except for WDT time-out. HIBERNATE mode allows power consumption to be reduced to a minimum.

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FIGURE 10-12: SLPCON REGISTER

8Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLPCON	HIBEN	—	REFOFF	LSOFF	OSCOFF	CMOFF	TEMPOFF	ADOFF
Read/Write	R/W	U	R/W	R/W	R/W	R/W	R/W	R/W
POR value 3Fh	0	0	1	1	1	1	1	1

Bit	Name	Function
B7	HIBEN	Hibernate Mode Select 1 = Hibernate mode enable 0 = Normal operating mode
B6	–	Unimplemented. Read as '0'
B5	REFOFF	References Power Control (bandgap reference, low voltage detector, bias generator) 1 = The references are off 0 = The references are on
B4	LSOFF	Level Shift Network Power Control 1 = The level shift network is off. The RA1/AN1, RD5/AN5 inputs can continue to function as either analog or digital. 0 = The level shift network is on. The signals at the RA1/AN1, RD5/AN5 inputs are level shifted by approximately 0.5V.
B3	OSCOFF	Main Oscillator Power Control 1 = The main oscillator is disabled during SLEEP mode 0 = The main oscillator is running during SLEEP mode for A/D conversions to continue
B2	CMOFF	Programmable Reference and Comparator Power Control 1 = The programmable reference and comparator circuits are off 0 = The programmable reference and comparator circuits are on
B1	TEMPOFF	On-chip Temperature Sensor Power Control 1 = The temperature sensor is off 0 = The temperature sensor is on
B0	ADOFF	A/D Module Power Control (comparator, programmable current source, slope reference voltage divider) 1 = The A/D module power is off 0 = The A/D module power is on

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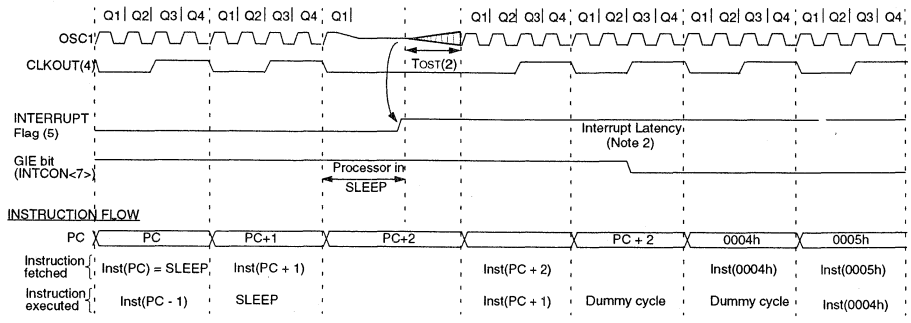
FIGURE 10-13: WAKE-UP FROM SLEEP AND HIBERNATE THROUGH INTERRUPT



Note 1: HS oscillator mode assumed.
2: TOST = 1024 TOSC (drawing not to scale). This delay will be 8 TOSC for IN osc mode.
3: GIE = 1 assumed. In this case after wake up processor jumps to interrupt routine. If GIE = 0, execution will continue in line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.
5: Refer to Section 10.8 for sources.

3

10.9 Code Protection

The code in the program memory can be protected by programming the code protect bits. When code protected, the contents of the program memory cannot be read out. In code-protected mode, the configuration word (2007h) will not be scrambled, allowing reading of all configuration bits.

10.10 In-Circuit Serial Programming

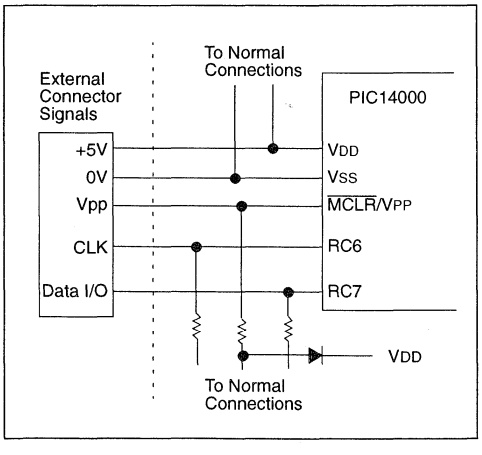
PIC14000 can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RC6/SCL and RC7/SDA pins low while raising the $\overline{MCLR}$ (VPP) pin from VIL to VIH. RC6 then becomes the programming clock and RC7 becomes the programmed data. Both RC6 and RC7 are Schmitt trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device. For complete details about serial programming, please refer to the *PIC16C6X/7X Programming Specifications* (Literature #DS30228).

A typical in-system serial programming connection is shown in Figure 10-14.

FIGURE 10-14: TYPICAL IN-SYSTEM SERIAL PROGRAMMING CONNECTION



NOTES:

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11.0 ELECTRICAL CHARACTERISTICS FOR PIC14000 ABSOLUTE MAXIMUM RATINGS †

Ambient temperature under bias ..... -55°C to+ 125°C

Storage Temperature ..... -65°C to +150°C

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.5V to V_{DD} +0.6V

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +6.0 V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2) ..... 0 to +14 V

Total power Dissipation (Note 1) ..... 1.0 W

Maximum Current out of V_{SS} pin 300mA

Maximum Current into V_{DD} pin 250mA

Input clamp current, I_{IK} (V_I <0 or V_I> V_{DD}) ..... ±20mA

Output clamp current, I_{OK} (V_O <0 or V_O>V_{DD}) ..... ±20mA

Maximum Output Current sunk by any I/O pin 25mA

Maximum Output Current sourced by any I/O pin 25mA

Maximum Current sunk by PORTA, PORTC, and PORTD(combined) 200mA

Maximum Current sourced by PORTA, PORTC, and PORTE (combined) 200mA

Maximum Current sunk by PORTC and PORTD (combined) 200mA

Maximum Current sourced by PORTC and PORTD (combined) 200mA

Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OI} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

11.1 DC Characteristics: PIC14000

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD = 2.7V to 6.0V				
Characteristic	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.7	—	6.0	V	IN or HS at Fosc ≤ 4 MHz
		4.5	—	5.5	V	HS at Fosc > 4 MHz
RAM Data Retention Voltage (Note 1)	VDR	—	1.5	—	V	Device in SLEEP mode
VDD start voltage to guarantee Power-On Reset	VPOR	—	VSS	—	V	See section on power-on reset for details
VDD rise rate to guarantee Power-On Reset	SVDD	0.05*	—	—	V/ms	See section on power-on reset for details
Operating Current in SLEEP Mode (Note 2)						
During A/D conversion: all analog on and internal oscillator active	IPD1	—	TBD	900	µA	VDD = 3.0V
	IPD1	—	TBD	1250	µA	VDD = 4.0V
Comparator interrupt enabled: level-shift, programmable reference, and comparator active	IPD2	—	75	100	µA	VDD = 3.0V, CMOFF = 0, LSOFF = 0, REFOFF = 0
	IPD2	—	95	125	µA	VDD = 4.0V, CMOFF = 0, LSOFF = 0, REFOFF = 0
All analog off, WDT on (Note 5)	IPD3	—	7.5	20	µA	VDD = 3.0V
	IPD3	—	10.5	28	µA	VDD = 4.0V
All analog off, WDT off (Hibernate mode) (Note 5)	IPD4	—	0.9	12	µA	VDD = 3.0V
	IPD4	—	1.5	16	µA	VDD = 4.0V
Operating Supply Current (Note 2, 4)						
Internal oscillator mode	IDD	—	2.2	TBD	mA	Fosc = 4 MHz, VDD = 5.5V
		—	1.1	TBD	mA	Fosc = 4 MHz, VDD = 3.0V
HS oscillator mode		—	2.4	TBD	mA	Fosc = 4 MHz, VDD = 5.5V
		—	1.2	TBD	mA	Fosc = 4 MHz, VDD = 3.0V
		—	10	TBD	mA	Fosc = 20 MHz, VDD = 5.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD.
MCLR = VDD; WDT enabled/disabled as specified.

3: Measured with all inputs at rails, no DC loads. IPD1 measured with internal oscillator active.

4: IDD values of individual analog module cannot be tested independently but are characterized.

5: Worst-case IPD conditions with all configuration bits unprogrammed. Programming configuration bits may reduce IPD.

PRELIMINARY

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11.2 DC Characteristics: PIC14000

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in Section 11.1.				
Characteristic	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL					
Schmitt Trigger mode		VSS	—	0.2VDD	V	
SMBus mode (RC7, RC6, RD0, RD1)		VSS	—	0.6	V	SMBus bit, MISC<3> = 1
$\overline{MCLR}$, OSC1 (in IN mode)		Vss	—	0.2VDD	V	
OSC1 (in HS mode)		Vss	—	0.3VDD	V	
Input High Voltage						
I/O ports	VIH		—			
Schmitt Trigger mode		0.85 VDD	—	VDD	V	
SMBus mode (RC7, RC6, RD0, RD1)		1.4V	—	VDD	V	SMBus bit, MISC<3> = 1
PORTC<5:0> weak pull-up current	IPURC	50	200	†400	µA	VDD = 5V, VPIN = VSS
Input Leakage Current (Notes 1,2)						
I/O ports, CDAC	IIL			±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$				±5	µA	Vss ≤ VPIN ≤ VDD
OSC1				±5	µA	Vss ≤ VPIN ≤ VDD
Output Low Voltage						
I/O ports	VOL	—	—	0.6	V	IOL = 8.5mA, VDD-4.5V, -40°C to +85°C
OSC2		—	—	0.6	V	IOL = 1.6mA, VDD-4.5V, -40°C to +85°C
Output High Voltage						
I/O ports (Note 2)	VOH	VDD-0.7	—	—	V	IOH = -3.0mA, VDD=4.5V, -40°C to +85°C
RC6, RC7, RD0, RD1 (except I^2C mode)		2.4	—	—	V	IOH = -2.0mA, VDD=4.5V, -40°C to +85°C
OSC2		VDD-0.7	—	—	V	IOH = -1.3mA, VDD=4.5V, -40°C to +85°C
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	
All I/O pins except OSC2 (in IN mode)	CIO			50	pF	
SCL, SDA in I^2C mode	Cb			400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as coming out of the pin.

PRELIMINARY

11.3 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. Tcc:st (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase subscripts (pp) and their meanings:

pp			
ck	CLKOUT	osc	OSC1
di	SDI	t0	T0CKI
io	I/O port		
mc	$\overline{MCLR}$		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:st (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

PRELIMINARY

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11.4 Timing Diagrams and Specifications

FIGURE 11-1: EXTERNAL CLOCK TIMING

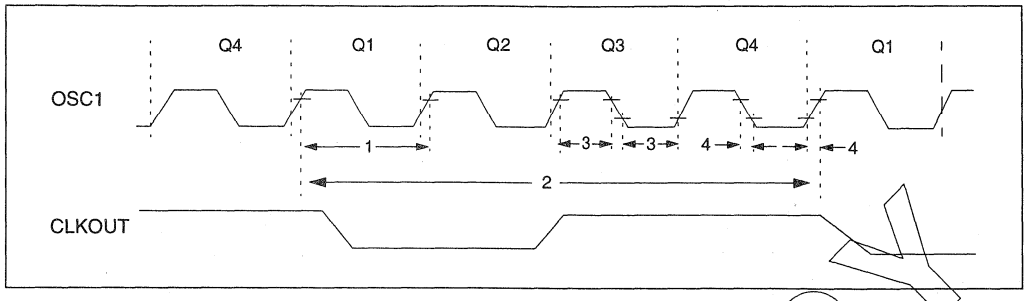


TABLE 11-1: EXTERNAL CLOCK TIMING REQUIREMENTS

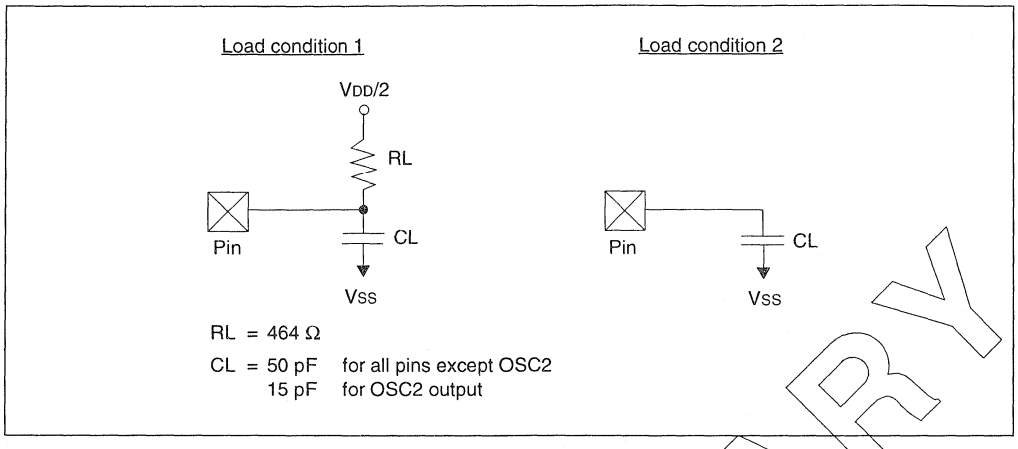
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency (Note 1)	DC DC	— —	4 20	MHz MHz	HS osc mode (PIC14000-04) HS osc mode (PIC14000-20)
		Oscillator Frequency (Note 1)	4 4	— —	4 20	MHz MHz	HS osc mode (PIC14000-04) HS osc mode (PIC14000-20)
1	TOSC	External CLKIN Period (Note 1)	250 50	— —	— —	ns ns	HS osc mode (PIC14000-04) HS osc mode (PIC14000-20)
		Oscillator Period (Note 1)	250 50	— —	250 250	ns ns	HS osc mode (PIC14000-04) HS osc mode (PIC14000-20)
2	TCY	Instruction Cycle Time (Note 1)	200	—	DC	ns	TCY = 4/FOSC
3	TOSL, TOSH	Clock in (OSC1) High or Low Time	10	—	—	ns	HS oscillator
4	TOSR, TOSF	Clock in (OSC1) Rise or Fall Time	—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

PRELIMINARY

FIGURE 11-2: LOAD CONDITIONS



PRELIMINARY

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FIGURE 11-3: CLKOUT AND I/O TIMING

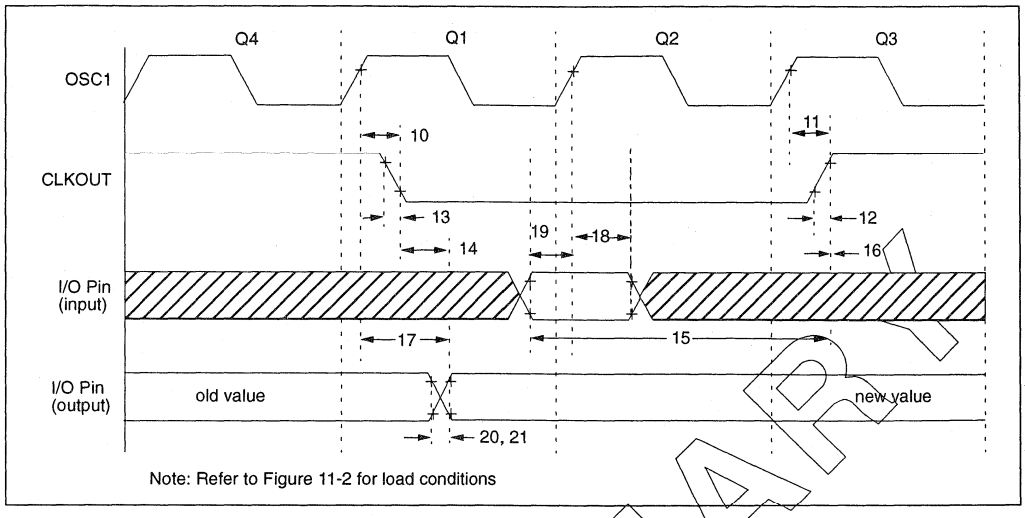


TABLE 11-2: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30	ns	Note 1
12	TckR	CLKOUT rise time	—	5	15	ns	Note 1
13	TckF	CLKOUT fall time	—	5	15	ns	Note 1
14	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5TCY+20	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT ↑	0.25 TCY+25	—	—	ns	Note 1
16	TckH2iol	Port in hold after CLKOUT ↑	0	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	80 - 100	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TioR	Port output rise time	—	10	25	ns	
21	TioF	Port output fall time	—	10	25	ns	
22††	Tinp	PBTN pin high or low time	20	—	—	ns	IN mode only
23††	Trbp	RC<7:4> change INT high or low time	20	—	—	ns	

* These parameters are characterized but not tested.

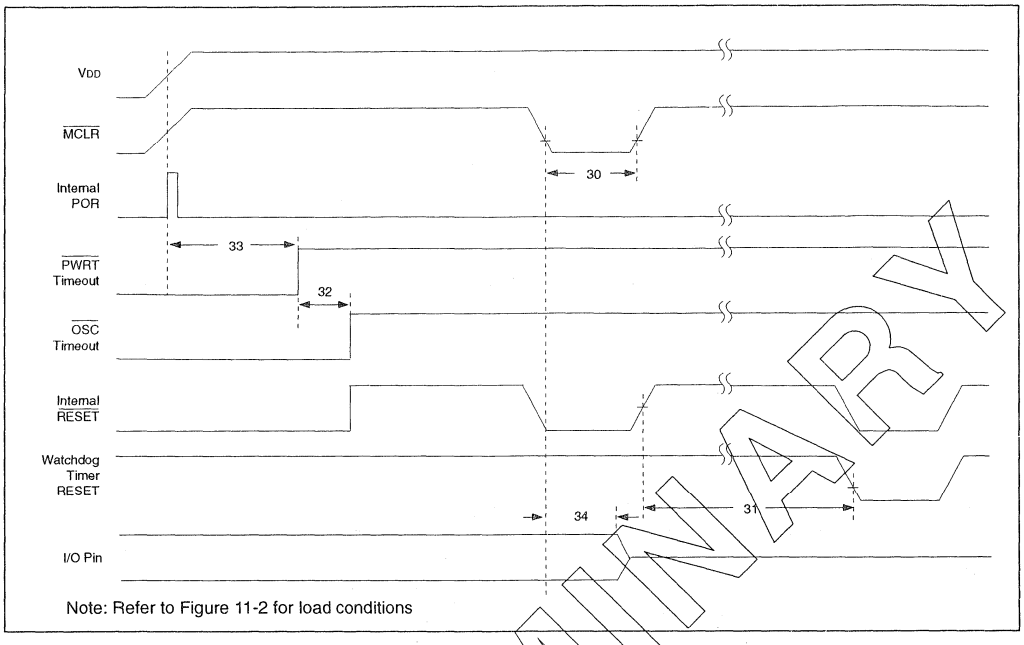
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in IN Mode where CLKOUT output is 4 x TOSC

PRELIMINARY

FIGURE 11-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER (HS MODE) AND POWER-UP TIMER TIMING



Note: Refer to Figure 11-2 for load conditions

TABLE 11-3: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100	—	—	ns	VDD = 5V, -40°C to +85°C
31	TWDT	Watchdog Timer Timeout Period (No Prescaler)	7*	18	33*	ms	VDD = 5V, -40°C to +85°C
	ss(WDT)	Supply Sensitivity	—	-12.6	—	%/V	TA = 25°C
	tc(WDT)	Temperature Coefficient	—	0.5	—	%/°C	VDD = 5V
32	TOST	Oscillation Start-up Timer Period		1024 TOSC		ms	TOSC = OSC1 period
				8 TOSC		ms	IN osc mode
33	TPWRT	Power up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +85°C
34	TIOZ	I/O High Impedance from MCLR Low			100	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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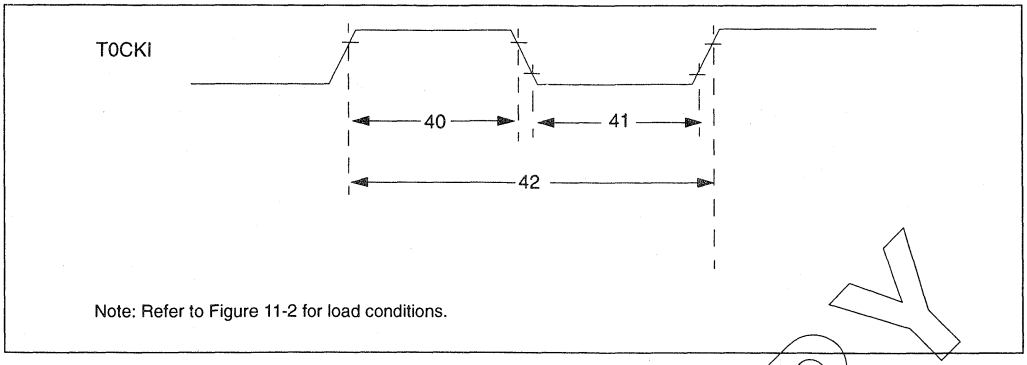
FIGURE 11-5: TIMER0 CLOCK TIMINGS



Note: Refer to Figure 11-2 for load conditions.

TABLE 11-4: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		TCY + 40* / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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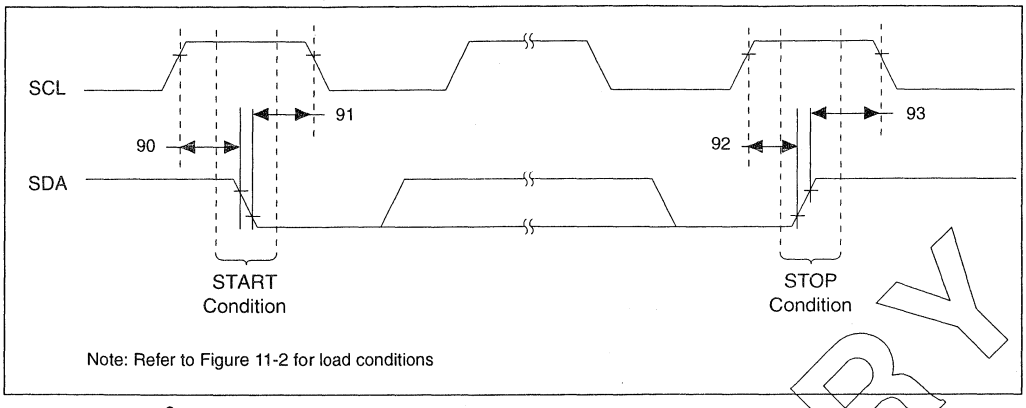
FIGURE 11-6: I²C BUS START/STOP BITS TIMING



Note: Refer to Figure 11-2 for load conditions

TABLE 11-5: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 KHZ mode	4700	—	—	ns	Only relevant for repeated START condition
			400 KHz mode	600	—	—		
91	THD:STA	START condition Hold time	100 KHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 KHz mode	600	—	—		
92	TSU:STO	STOP condition Setup time	100 KHZ mode	4700	—	—	ns	
			400 KHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 KHz mode	4000	—	—	ns	
			400 KHz mode	600	—	—		

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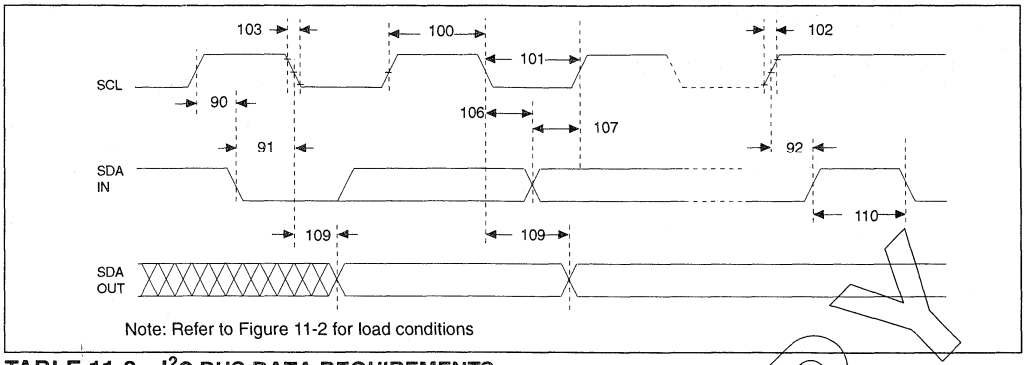
FIGURE 11-7: I^2C BUS DATA TIMING



Note: Refer to Figure 11-2 for load conditions

TABLE 11-8: I^2C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC14000 must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC14000 must operate at a minimum of 10 MHz
			I^2C Module	1.5 TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC14000 must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC14000 must operate at a minimum of 10 MHz
			I^2C Module	1.5 TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20+0.1 C_b	300	ns	C_b is specified to be from 10-400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20+0.1 C_b	300	ns	C_b is specified to be from 10-400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	C_b	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of STARTs or STOPs.

2: A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement tSU:DAT≥250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tSU:DAT=1000+250=1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

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11.5 DC and AC Characteristics Graphs and Tables for PIC14000

FIGURE 11-9: TYPICAL I_{PD4} vs V_{DD} AT 25°C

TO BE DETERMINED.

FIGURE 11-10: TYPICAL I_{PD3} vs V_{DD} AT 25°C

TO BE DETERMINED.

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FIGURE 11-11: V_{TH} (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN HS MODE) vs V_{DD}

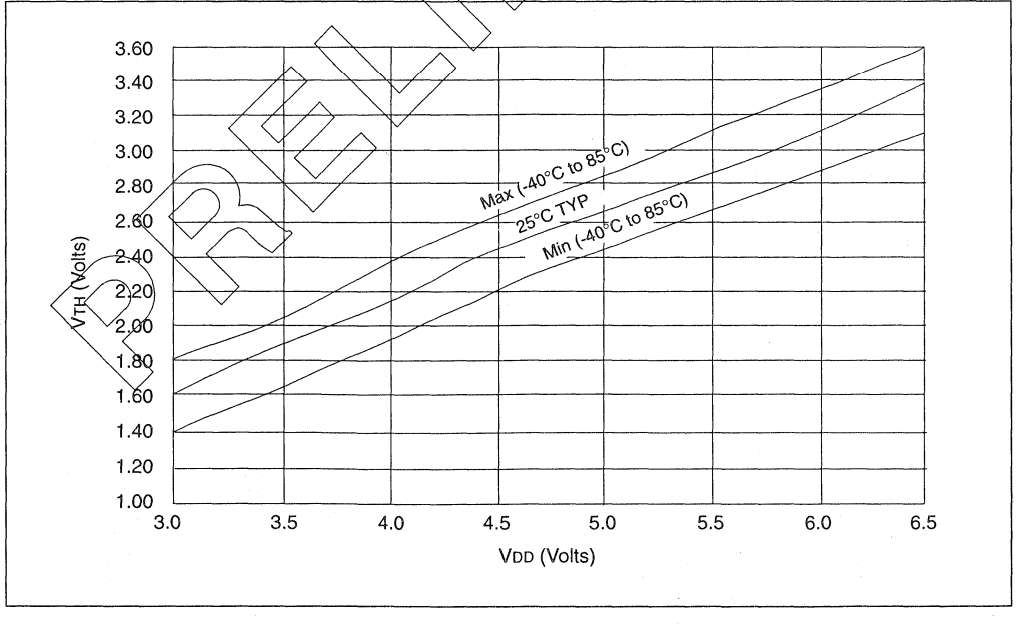

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FIGURE 11-12: TYPICAL OPERATING SUPPLY CURRENT vs FREQ (EXT CLOCK, 25°C)

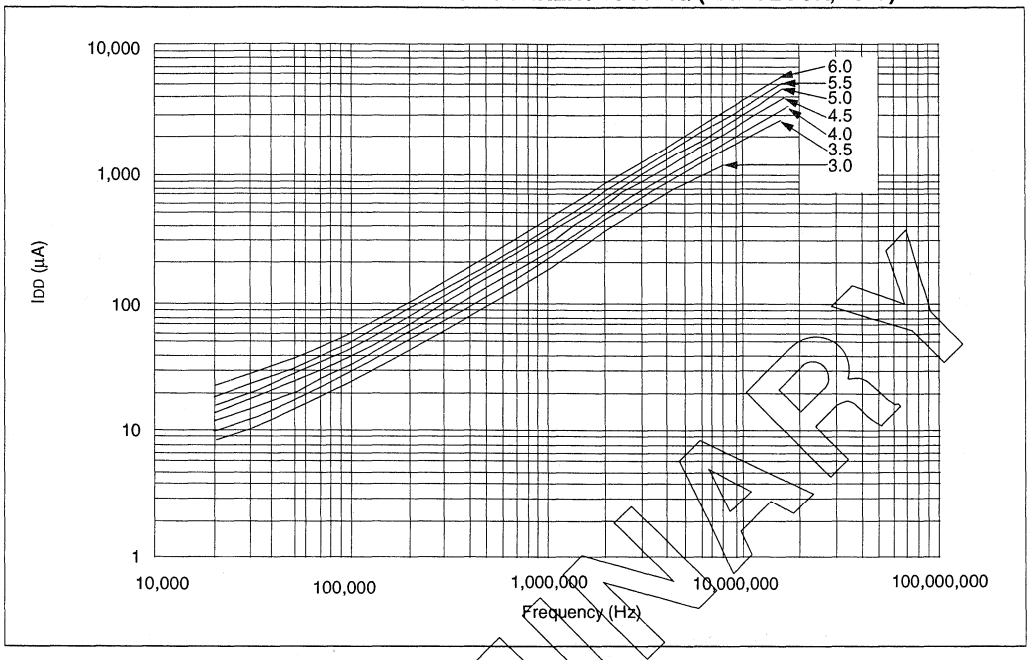

FIGURE 11-13: MAXIMUM OPERATING SUPPLY CURRENT vs FREQ (EXT CLOCK, -40° TO +85°C)

TO BE DETERMINED.

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FIGURE 11-14: MAXIMUM I_{PD1} VS FREQ (EXT CLOCK, -40° TO +85°C)

TO BE DETERMINED.

FIGURE 11-15: WATCHDOG TIMER TIME-OUT PERIOD (T_{WDT}) VS. TEMPERATURE (TYPICAL)

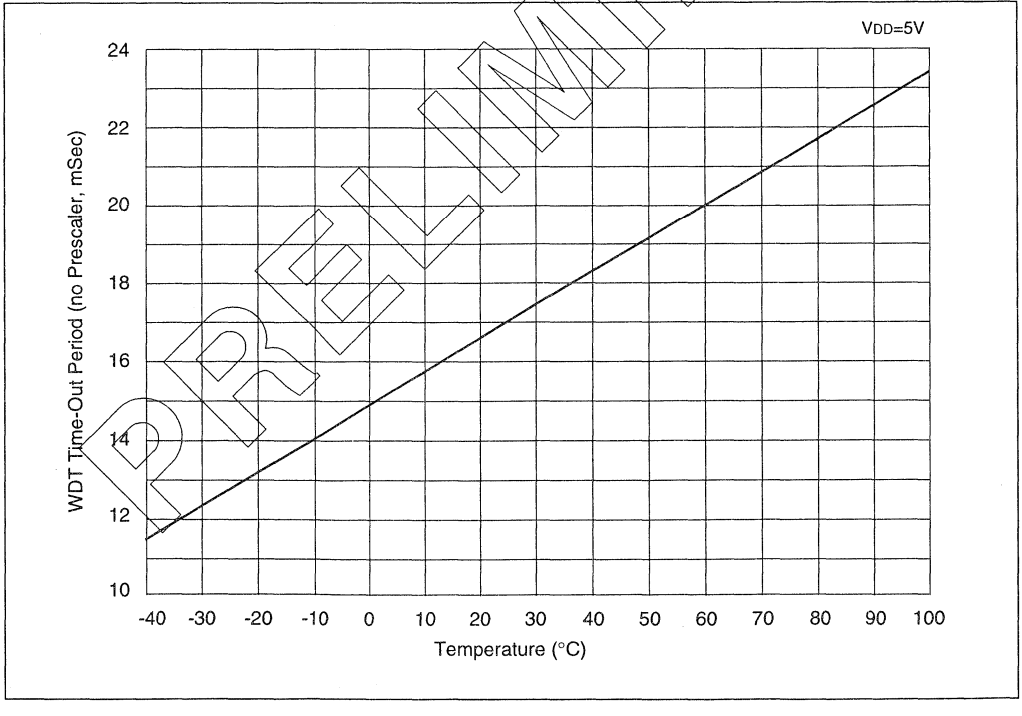

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FIGURE 11-16: WDT TIMER TIME-OUT PERIOD VS VDD

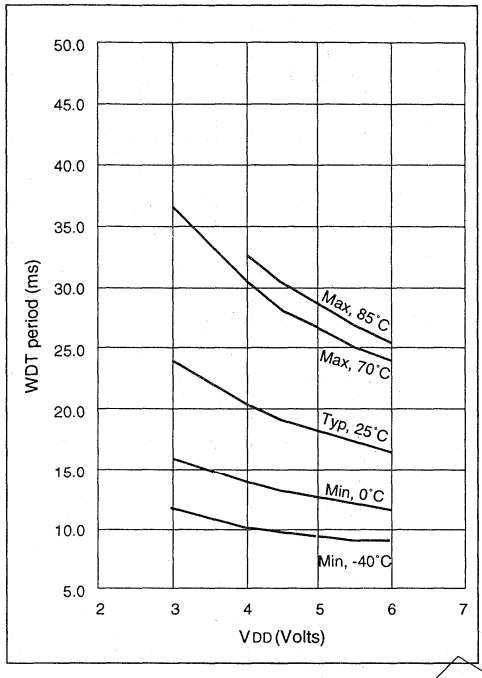


FIGURE 11-17: TRANSCONDUCTANCE (GM) OF HS OSCILLATOR VS VDD

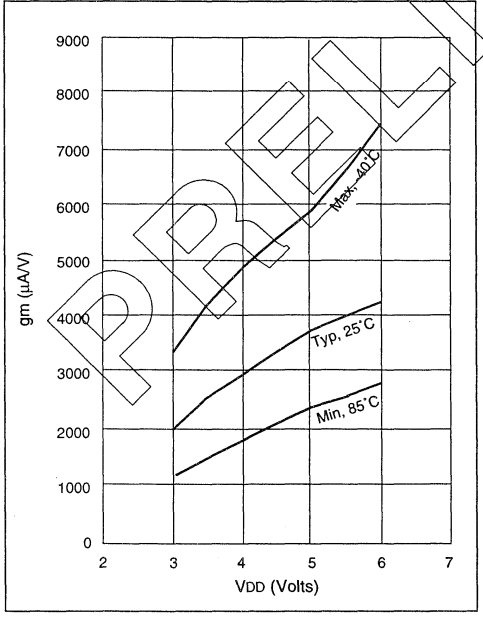


FIGURE 11-18: IOH VS VOH, VDD = 3V*

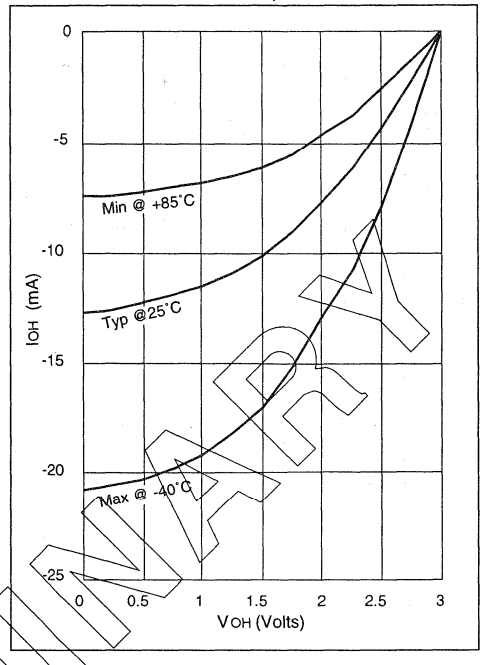
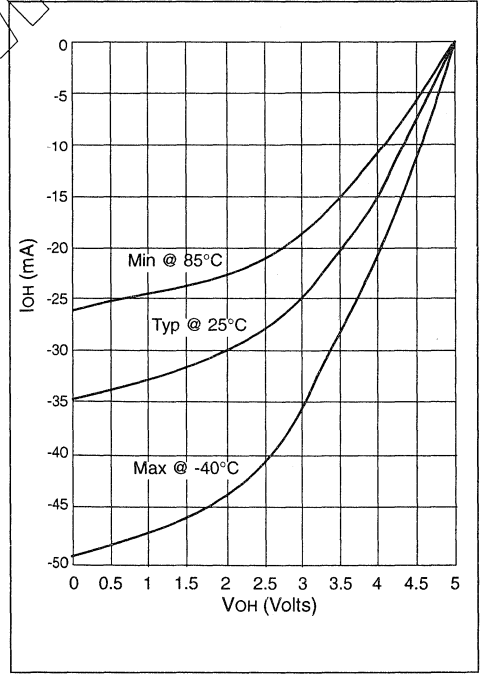


FIGURE 11-19: IOH VS VOH, VDD = 5V*



*NOTE: All pins except RC6, RC7, RD0, RD1,OSC2

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FIGURE 11-20: IOL vs VOL, VDD = 3V*

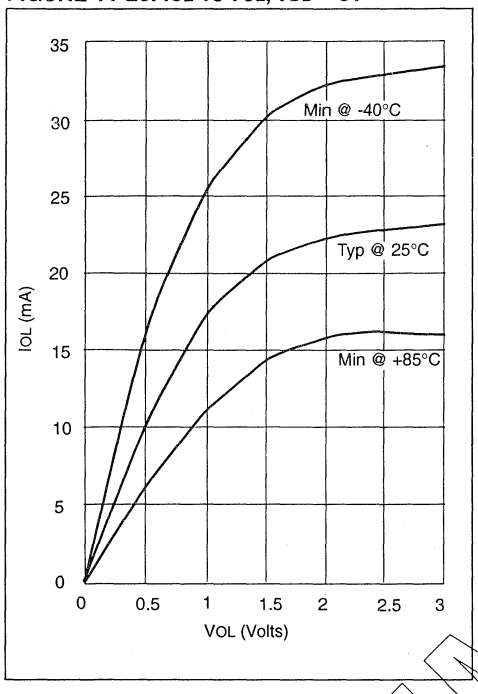
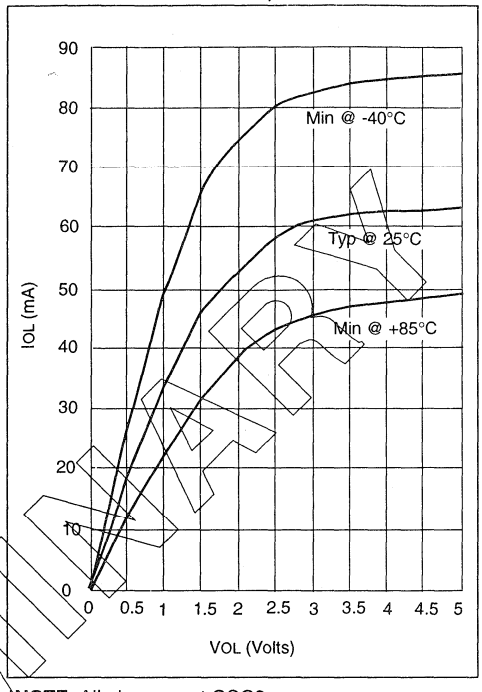


FIGURE 11-21: IOL vs VOL, VDD = 5V*



*NOTE: All pins except OSC2

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12.0 ANALOG SPECIFICATIONS: PIC14000-04 (COMMERCIAL, INDUSTRIAL)

Standard Operating Conditions (unless otherwise stated)

Operating Temperature: -40°C ≤ TA ≤ +85°C for industrial
0°C ≤ TA ≤ +70°C for commercial

VDD range: 2.7V (min) to 6.0V (max) unless otherwise stated.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions	Notes
Bandgap Voltage Reference							
Output Voltage	vo(vref)	1.14	1.19	1.24	V		
Turn-on Settling Time to < 0.1%	ton(vref)	—	1	10	ms	REFOFF bit in SLPCON register → 0	1
Temperature Coefficient	tc(vref)	—	±50	—	ppm/°C	Measured from 25°C to -40°C, +85°C	1
Temperature Coefficient	tc(vref)	—	±20	—	ppm/°C	Measured from 25°C to 0°C, +70°C	1
Supply Sensitivity	ss(vref)	—	0.04	—	%/V	From VDDmin to VDDmax	1
Operating Current (on)	idd(vref)	—	20	30	µA	REFOFF = 0	2
Operating Current (off)	idd(vref)	—	0	—	µA	REFOFF = 1	2
Programmable Current Source							
Output Current	io(cdac)					CDAC pin = 0V	3
		18.75	33.75	48.75	µA	ADCON1<7:4> = 1111b (full-scale)	
		1.25	2.25	3.25	µA	ADCON1<7:4> = 0001b (1 LSB)	
		-0.5	0	0.5	µA	ADCON1<7:4> = 0000b (zero-scale)	
Resolution	res(cdac)	1.25	2.25	3.25	µA	1 LSB	
Relative accuracy (linearity error)	racc(cdac)	-1/2		+1/2	lsb	CDAC = 0V	
Turn-on Settling Time to < 0.1% (reference start-up)	ton(cdac)	—	1	10	ms	Bias generator (reference) turn-on time (REFOFF 1 → 0)	1
Turn-on Settling Time to < 0.1% (reference already on and stable)	ton(cdac)	—	1	10	µs	REFOFF = 0 (constant), ADCON1<7:4> 0000b → 1111b	1
Temperature Coefficient	tc(cdac)	—	±0.1	—	%/°C	Measured from 25°C to Tmin, Tmax	1
Supply Sensitivity	ss(cdac)	—	0.2	—	%/V	From VDDmin to VDDmax	1
Output Voltage Sensitivity	vs(cdac)	-0.1	-0.01	–	%/V	CDAC pin voltage = 0V to VDD - 1.4V	
Output Voltage Range	vo(cdac)	0	—	VDD-1.4	V		
Operating Current (A/D on)	idd(cdac)	—	50	70	µA	ADCON1<7:4> = 1111b	2
Operating Current (A/D off)	idd(cdac)	—	0	—	µA	REFOFF = 1, ADOFF = 1	2
Temperature Sensor							
Output Voltage	vo(temp)	0.92	1.05	1.18	V	TA = 25°C	
Supply Sensitivity	ss(temp)	—	0.2	—	%/V	From VDDmin to VDDmax	1
Temperature Coefficient	KTC	3.2	3.65	4.1	mV/°C	Measured from 25°C to Tmax. Includes ± 2°C temperature calibration tolerance	

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Standard Operating Conditions (unless otherwise stated)

Operating Temperature: -40°C ≤ TA ≤ +85°C for industrial
0°C ≤ TA ≤ +70°C for commercial

VDD range: 2.7V (min) to 6.0V (max) unless otherwise stated.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions	Notes
Temperature Sensor (continued)							
Output Linearity	lin(temp)	—	TBD	—			1
Operating Current (sensor on)	idd(temp)	—	150	250	µA	TEMPOFF = 0	2
Operating Current (sensor off)	idd(temp)	—	0	—	µA	TEMPOFF = 1	2
Slope Reference Voltage Divider							
Output Voltage (SREFHI)	voh(sref)	1.14	1.19	1.24	V		
Output Voltage (SREFLO)	vol(sref)	0.10	0.13	0.16	V		
Slope Reference Calibration Factor	KREF	0.09	0.126	0.16		TA = 25°C, VDD = 5V	
KREF Supply Sensitivity	ss(KREF)	—	0.02	—	%/V	From VDDmin to VDDmax	1
KREF Temperature Coefficient	tc(KREF)	—	20	—	ppm/°C	From Tmin to Tmax	1
Operating Current (A/D on)	idd(sref)	—	55	85	µA	ADOFF = 0	2
Operating Current (A/D off)	idd(sref)	—	0	—	µA	ADOFF = 1	2
A/D Comparator							
Input Offset Voltage	ioff(adc)	-10	2	10	mV	Measured over common-mode range	
Input Common Mode Voltage Range	cmr(adc)	0	—	VDD-1.4	V		
Differential Voltage Gain	gain(adc)	—	100	—	dB		1
Common Mode Rejection Ratio	cmrr(adc)	—	80	—	dB	VDD = 5V, TA = 25°C, over common-mode range	1
Power Supply Rejection Ratio	psrr(adc)	—	70	—	dB	TA = 25°C, VDDmin to VDDmax	1
Operating Current (A/D on)	idd(adc)	—	40	65	µA	ADOFF = 0	2
Operating Current (A/D off)		—	0	—	µA	ADOFF = 1	2
Programmable Reference(s)							
Upper Range						TA = 25°C	
Output Voltage	vo(pref)	0.627	0.792	0.957	V	PREFx<7:0> = 7Fh (127 decimal), max	
		0.418	0.528	0.638	V	PREFx<7:0> = 50h (80 decimal), min	
Coarse Resolution	resc(pref)	38.0	48.0	58.0	mV	PREFx<2:0> = constant	
Fine Resolution	resf(pref)	4.0	5.0	6.0	mV	PREFx<7:3> = constant	
Middle Range						TA = 25°C	
Output Voltage	vo(pref)	0.414	0.523	0.632	V	PREFx<7:0> = 4F (79 decimal), max	
		0.380	0.480	0.580	V	PREFx<7:0> = 00h (default), mid-point	
		0.342	0.432	0.522	V	PREFx<7:0> = C8h (200 decimal), min	
Coarse Resolution	resc(pref)	3.8	4.8	5.8	mV	PREFx<2:0> = constant	
Fine Resolution	resf(pref)	0.38	0.46	0.54	mV	PREFx<7:3> = constant	1

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Standard Operating Conditions (unless otherwise stated)

Operating Temperature: -40°C ≤ TA ≤ +85°C for industrial
0°C ≤ TA ≤ +70°C for commercial

VDD range: 2.7V (min) to 6.0V (max) unless otherwise stated.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions	Notes
Programmable Reference(s) (continued)							
Lower Range						TA = 25°C	
Output Voltage	vo(pref)	0.304	0.384	0.464	V	PREFx<7:0> = D7h (215 decimal), max	
		0.114	0.144	0.174	V	PREFx<7:0> = F8h (248 decimal), min	
Coarse Resolution	resc(pref)	38.0	48.0	58.0	mV	PREFx<2:0> = constant	
Fine Resolution	resf(pref)	4.0	5.0	6.0	mV	PREFx<7:3> = constant	
Relative accuracy (linearity error)	racc(pref)	-1/2	—	+1/2	lsb	lsb = resolution within selected range	
Settling Time to < ±1/2 LSB	ts(pref)	—	1	10	µS	PREFx<7:0> transition from 7Fh to FFh	1
Temperature Coefficient	tc(pref)	—	0.39	—	%/°C	From Tmin to Tmax	1
Supply Sensitivity	ss(pref)	—	0.2	—	%/V	From VDDmin to VDDmax	1
Operating Current (on)	idd(pref)	—	5	10	µA	CMOFF = 0	2
Operating Current (off)	idd(pref)	—	0	—	µA	CMOFF = 1	2
Low-Voltage Detector							
Detect Voltage	v-(lvd)	2.43	2.55	2.67	V	Decreasing VDD	
Release Voltage	v+(lvd)	2.48	2.60	2.72	V	Increasing VDD	
Hysteresis	vhys(lvd)	35	55	75	mV	Between detect and release trip points	
Operating Current (on)	idd(lvd)	—	15	25	µA	REFOFF = 0	2
Operating Current (off)	idd(lvd)	—	0	—	µA	REFOFF = 1	2
Internal Oscillator							
Frequency Range	fosc(in)	3.0	4.0	5.0	MHz		
Temperature Coefficient	tc(in)	—	-0.04	—	%/°C	From Tmin to Tmax	1
Supply Sensitivity	ss(in)	—	0.8	—	%/V	From VDDmin to VDDmax	1
Jitter	jit(in)	—	100	—	ppm	±3 sigma from mean	1
Start-up Time	tsu(in)	—	8	—	Tcycs	At Power-On Reset and exit from SLEEP	4
Operating Current (oscillator on)	idd(in)	—	300	500	µA		2
Operating Current (oscillator off)	idd(in)	—	0	—	µA	SLEEP mode, OSCOFF = 1	2
Voltage Regulator Control Output							
Regulation Voltage	vo(reg)	5.2	5.9	6.6	V	Measured with Ivreg = 10µA at TA = 25°C	
Temperature Coefficient	tc(vreg)	—	-0.2	—	%/°C	From Tmin to Tmax	1
Operating Current (Recommended)	idd(vreg)	1	–	10	µA	Determined by external components	
Operating Current		—	0	—		If VREG pin is open	

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Standard Operating Conditions (unless otherwise stated)							
Operating Temperature: -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial							
VDD range: 2.7V (min) to 6.0V (max) unless otherwise stated.							
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	**Notes**
Programmable Reference Comparator(s)							
Input Offset Voltage	ioff(comp)	-10	3	10	mV	Tested at 0.5V common-mode voltage	
Input Common Mode Voltage Range	cmr(comp)	0	—	VDD-1.4	V		1
Differential Voltage Gain	gain(comp)	—	80	—	dB		1
Common Mode Rejection Ratio	cmrr(comp)	—	60	—	dB	VDD = 5V, TA = 25°C, over common-mode range	1
Power Supply Rejection Ratio	psrr(comp)	—	55	—	dB	TA = 25°C, VDDmin to VDDmax	1
Operating Current (on)	idd(comp)	—	10	20	µA	CMOFF = 0	2
Operating Current (off)	idd(comp)	—	0	—	µA	CMOFF = 1	2
Level-Shift Network(s)							
Input Current (RA1/RD5 pin)	iin(lvs)	-3.4	-4.8	-6.2	µA	TA = 25°C, RA1/RD5 = 0V (SUM pin is open)	
Output Voltage	vo(lvs)	0.37	0.46	0.55	V	TA = 25°C, RA1/RD5 = 0V, (SUM pin is open)	
Zeroing Mismatch Error	zm(lvs)	—	0.02	—	%		1
Output Voltage Temperature Coefficient	tc(lvs)	—	0.39	—	%/°C	From Tmin to Tmax	1
Output Voltage Supply Sensitivity	ss(lvs)	—	0.2	—	%/V	From VDDmin to VDDmax	1
Operating Current (network on)	idd(lvs)	—	5	15	µA	LSOFF = 0	2
Operating Current (network off)	idd(lvs)	—	0	—	µA	LSOFF = 1	2

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Standard Operating Conditions (unless otherwise stated)							
Operating Temperature: -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial							
VDD range: 2.7V (min) to 6.0V (max) unless otherwise stated.							
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	**Notes**
Calibration Accuracy						All parameters calibrated at VDD = 5V, TA = 25°C unless noted.	3, 5
				Accuracy			
Parameter	**Sym.**	**Resolution**	**Units**	**Typ**	**Max**	**Conditions**	**Notes**
Slope Reference Ratio	KREF	0.015%	—	.02%	—		
Bandgap Reference Voltage	KBG	10	µV	.01%	—		
Temperature Sensor Output Voltage	VTHERM	20	µV	.02%	—		
Temperature Sensor Slope Coefficient	KTC	0.33	µV/°C	6.7%	—	Calibrated at 25°C and Tmax	
Internal Oscillator Frequency	FOSC	10.0	kHz	0.14%	—		
Watchdog Timer Time-out Period	TWDT	1	ms	0.5 ms	—		

Notes for the analog specifications:

Note 1: This parameter is characterized but not tested.

Note 2: IDD values of individual analog module cannot be tested independently but are characterized.

Note 3: Calibration temp accuracy is ± 1°C typical, ± 2°C max.

Note 4: Guaranteed by design.

Note 5: Refer to AN621 for further information on calibration parameters and accuracy.

Calculations:

Temperature coefficients are calculated as:

tc = (value @TMAX - value @TMIN) / ((TMAX-TMIN) * Average(value @TMAX,value @TMIN))

Temperature coefficient for the internal temperature sensor is calculated as:

tc sensor = (sensor voltage @ TMAX - sensor voltage @ 25°C) / (TMAX - 25°C)

Temperature coefficients for the bandgap reference and programmable current source are calculated as the larger TC from 25°C to either TMIN or TMAX

Supply sensitivities are calculated as:

ss = (value@VDDMAX - value@VDDMIN)/((VDDMAX - VDDMIN)* Average(value@VDDMAX, value@VDDMIN))

Programmable current source output sensitivity is calculated as:

vs = (value@(VDD - 1.4V) - value @ 0V)/(VDD - 1.4V) * Average(value@(VDD - 1.4V), value @ 0V)

PRELIMINARY

FIGURE 12-1: BANDGAP REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE (TYPICAL DEVICES SHOWN)

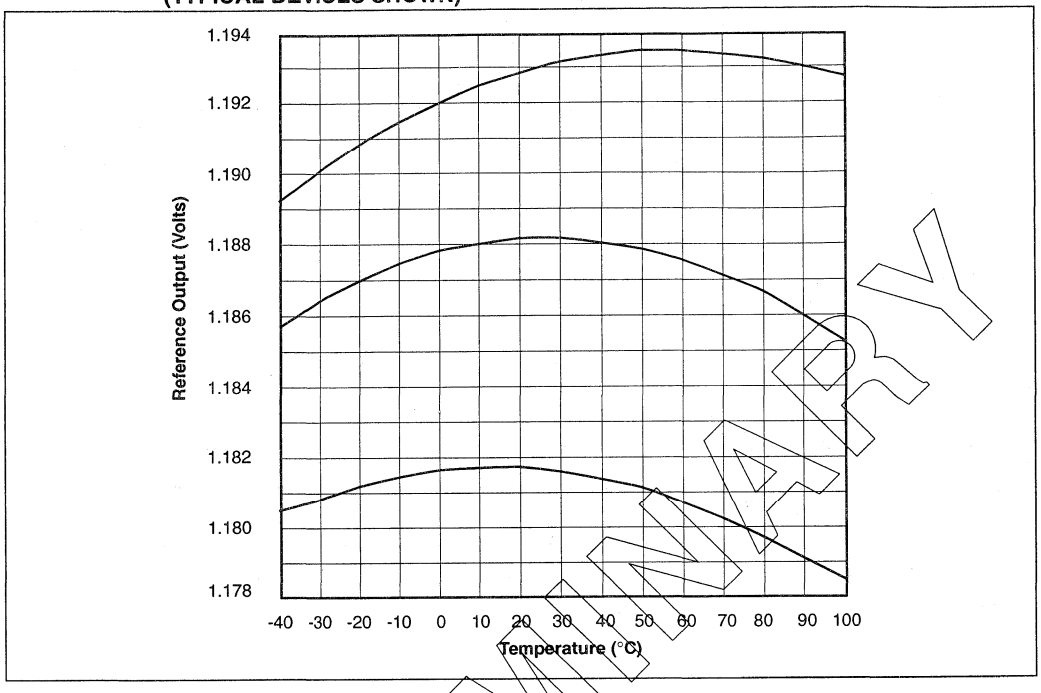
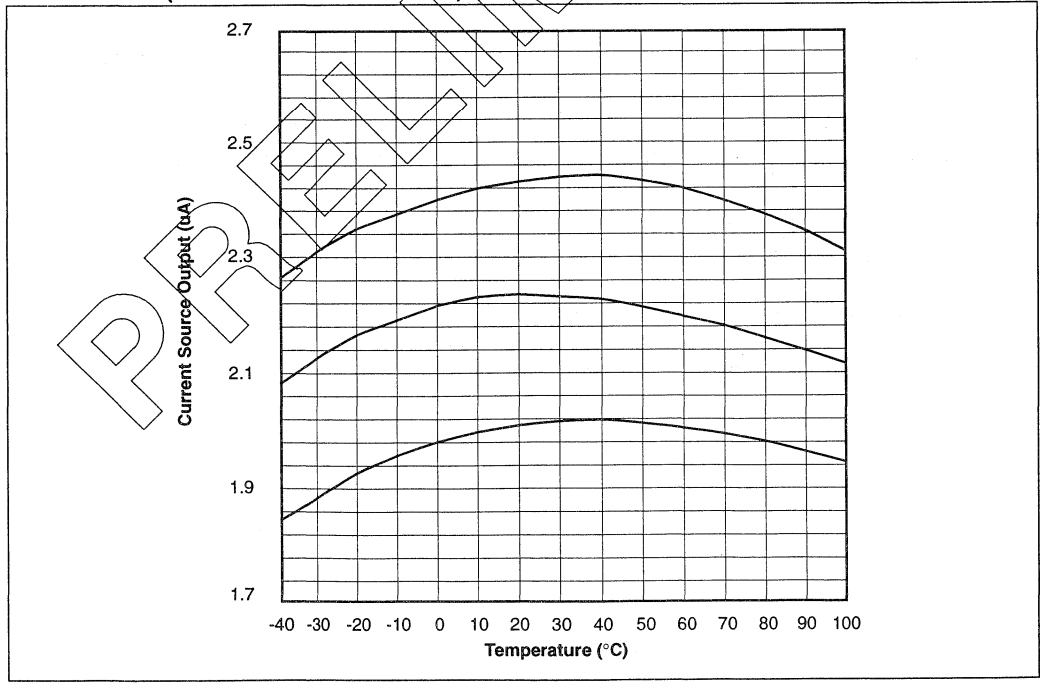


FIGURE 12-2: PROGRAMMABLE CURRENT SOURCE vs. TEMPERATURE (TYPICAL DEVICES SHOWN)



PRELIMINARY

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FIGURE 12-3: TEMPERATURE SENSOR OUTPUT VOLTAGE vs. TEMPERATURE (TYPICAL DEVICES SHOWN)

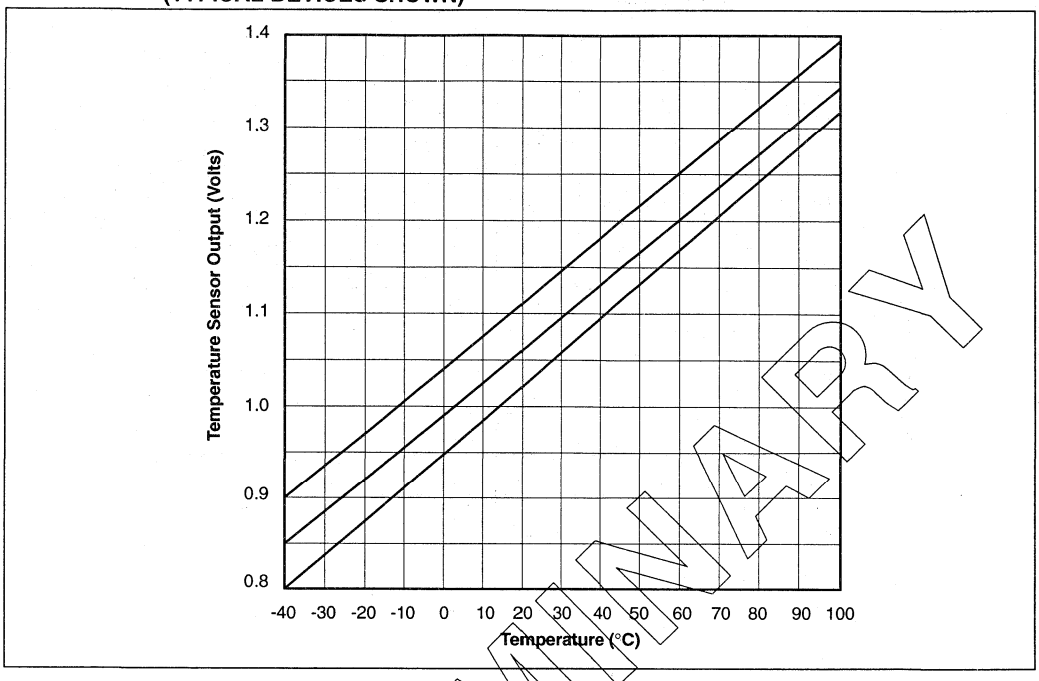
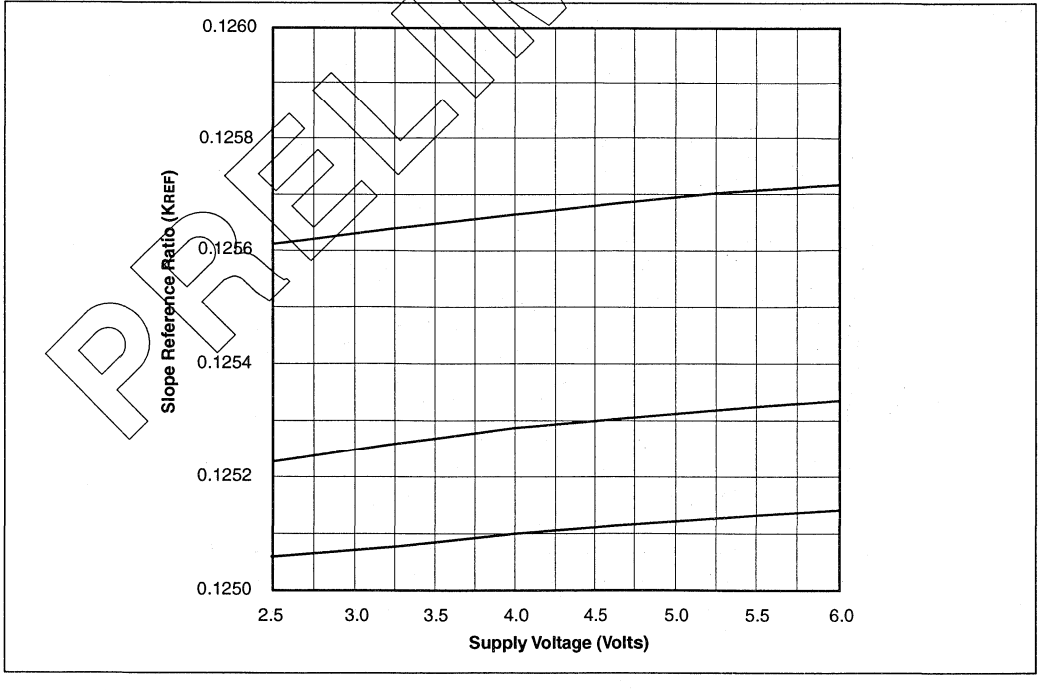


FIGURE 12-4: SLOPE REFERENCE RATIO (KREF) vs. SUPPLY VOLTAGE (TYPICAL DEVICES SHOWN)



PRELIMINARY

FIGURE 12-5: SLOPE REFERENCE RATIO (KREF) vs. TEMPERATURE (TYPICAL DEVICES SHOWN)

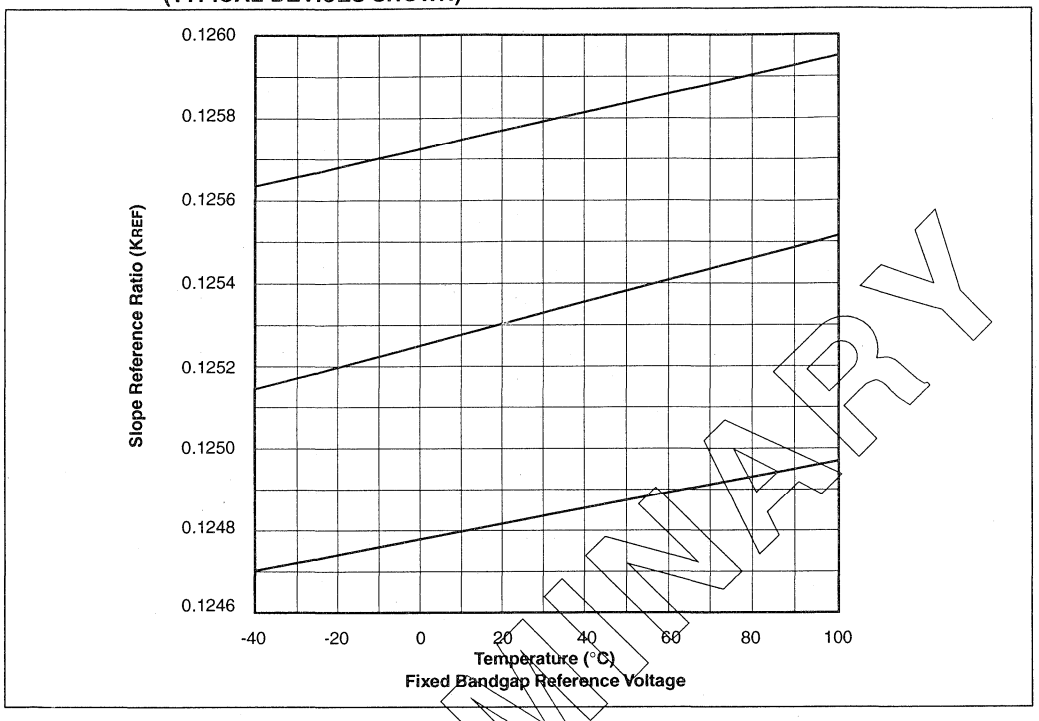
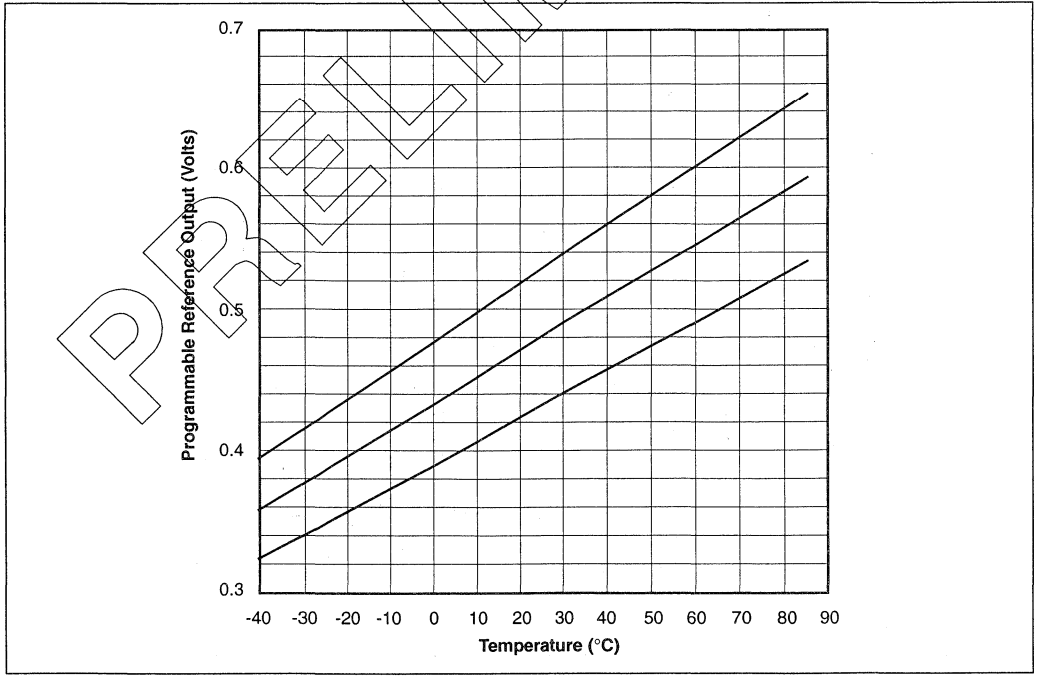


FIGURE 12-6: PROGRAMMABLE REFERENCE OUTPUT vs. TEMPERATURE (TYPICAL)



PRELIMINARY

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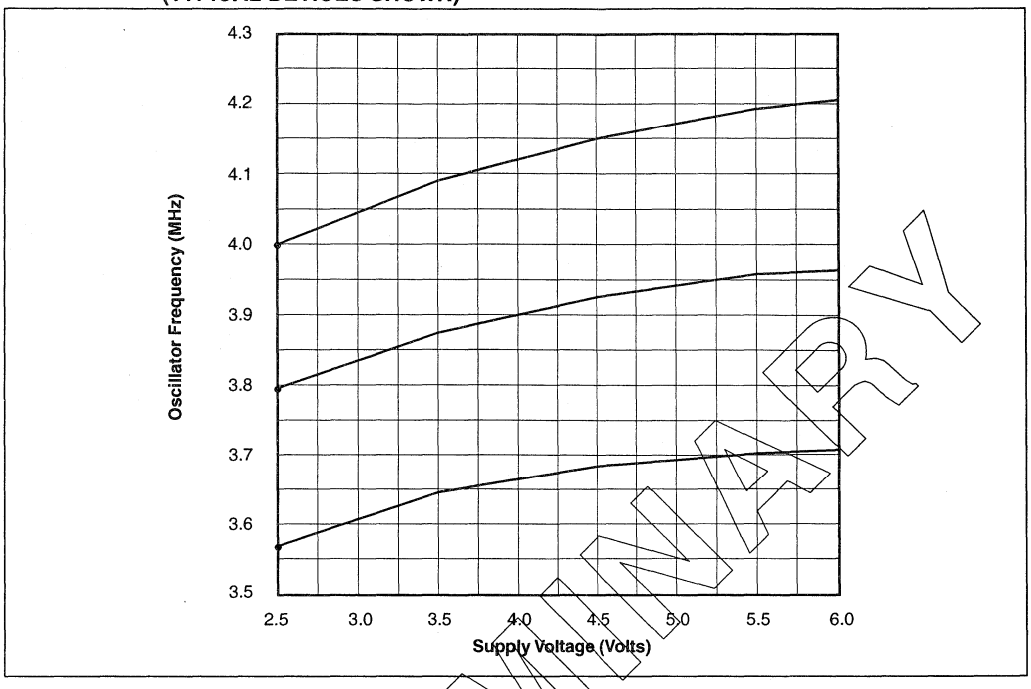
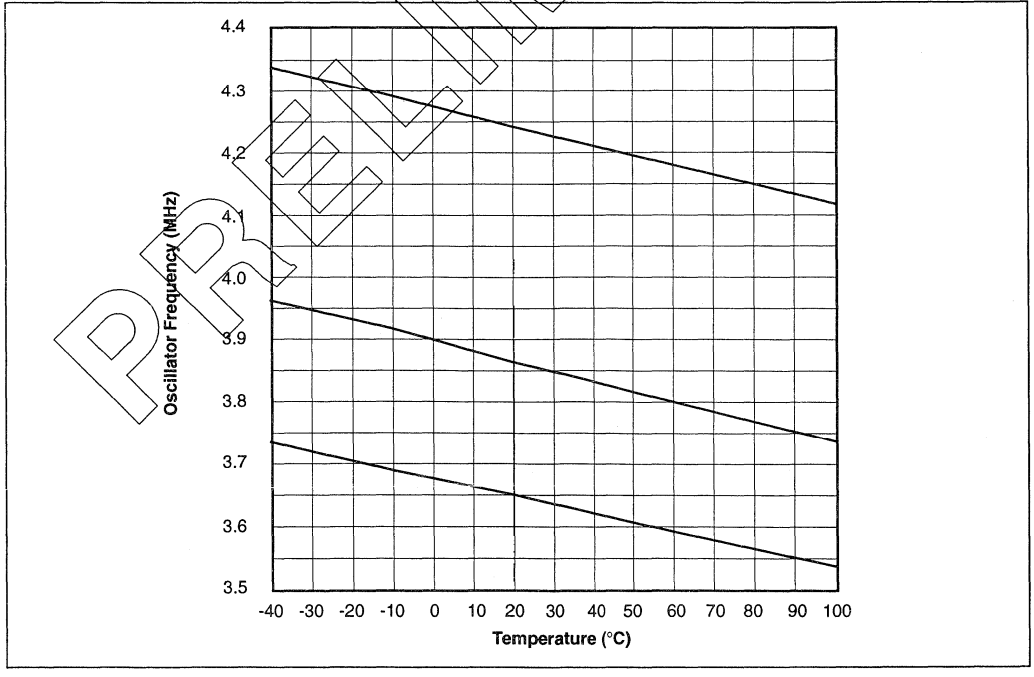
FIGURE 12-7: INTERNAL RC OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE (TYPICAL DEVICES SHOWN)



PRELIMINARY

FIGURE 12-8: INTERNAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE (TYPICAL DEVICES SHOWN)



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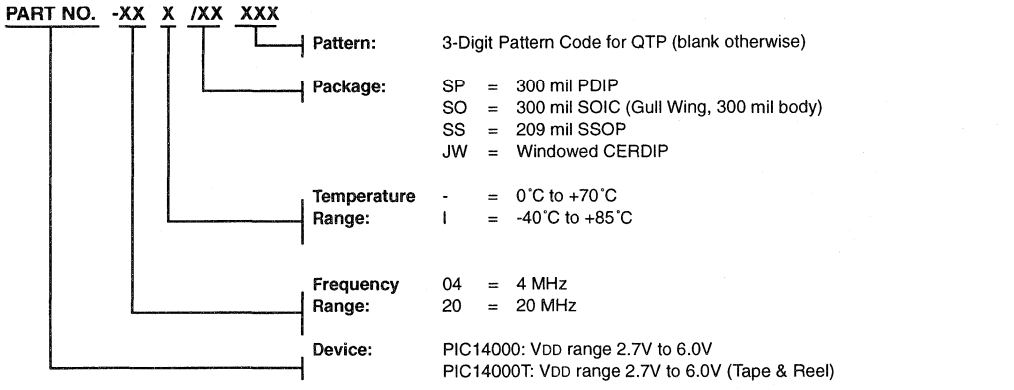
PIC14000 PRODUCT IDENTIFICATION SYSTEM

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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MICROCHIP

SECTION 4
PIC16C5X MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC16C5X EPROM/ROM-Based 8-Bit CMOS Microcontroller Series 4-1

4

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MICROCHIP

PIC16C5X

EPROM/ROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16C54
- PIC16CR54A
- PIC16C55
- PIC16C56
- PIC16C57

High-Performance RISC CPU Features:

- Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

Device	Pins	I/O	EPROM/ ROM	RAM
PIC16C54	18	12	512	25
PIC16CR54A	18	12	512	25
PIC16C55	28	20	512	24
PIC16C56	18	12	1K	25
PIC16C57	28	20	2K	72

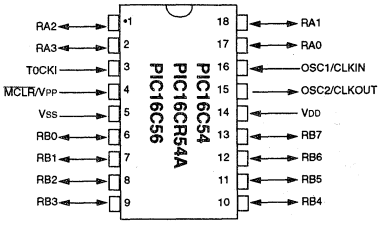
- 12-bit wide instructions
- 8-bit wide data path
- Seven or eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

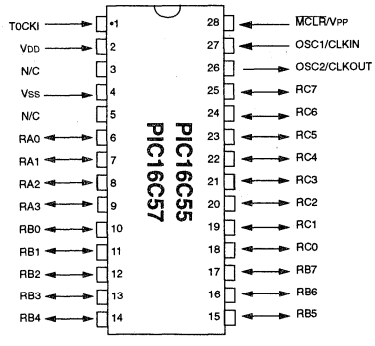
- 8-bit real time clock/counter (Timer0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power saving, low frequency crystal

Pin Diagrams

PDIP, SOIC, Windowed CERDIP



PDIP, SOIC, Windowed CERDIP



CMOS Technology:

- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide-operating voltage range:
  - EPROM Commercial/Industrial 2.5V to 6.25V
  - ROM Commercial/Industrial 2.0V to 6.25V
  - EPROM/ROM Automotive 2.5V to 6.0V
- Low-power consumption
  - < 2 mA typical @ 5.0V, 4 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - < 3 µA typical standby current (with WDT disabled) @ 3.0V, 0°C to 70°C

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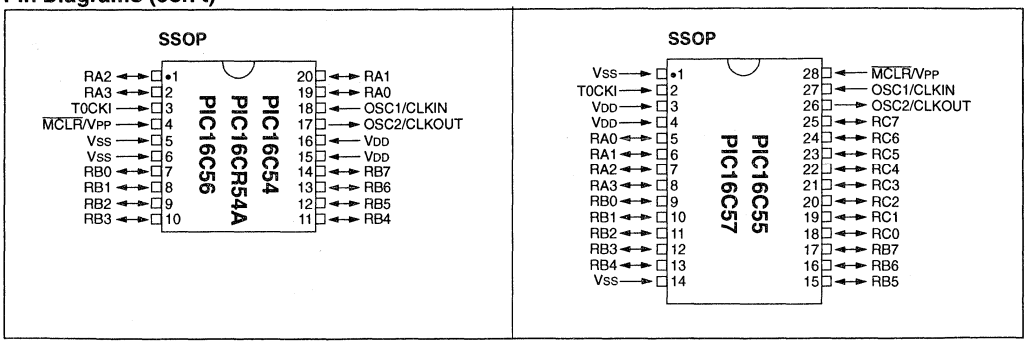
Pin Diagrams (con't)



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To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

To assist you in the use of this document, Appendix B contains a list of new information in this data sheet, while Appendix C contains information that has changed.

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1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EPROM/ROM-based CMOS microcontrollers. This family is pin and software compatible with the Enhanced PIC16C5X family of devices. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (200 ns) except for program branches which take two cycles. The PIC16C5X delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost-saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost effective One-Time-Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on AT class DOS/Windows-based machines.

1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through- hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

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TABLE 1-1: PIC16C5X FAMILY OF DEVICES

	Clock	Memory			Peripherals	Features		
	Maximum Frequency of Operation (MHz)	EPROM	ROM	RAM Data Memory (bytes)	Timer Module(s)	I/O Pins	Voltage Range (Volts)	Number of Instructions	Packages
PIC16C52	4	384	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC
PIC16C54	20	512	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C54A	20	512	—	25	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR54A	20	—	512	25	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C55	20	512	—	24	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C56	20	1K	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C57	20	2K	—	72	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16CR57B	20	—	2K	72	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C58A	20	2K	—	73	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR58A	20	—	2K	73	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP

Program Memory (x12 words)

All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

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2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are two device types, as indicated in the device number:

1. **C**, as in PIC16C54. These devices have EPROM program memory and operate over the standard voltage range.
2. **CR**, as in PIC16CR54A. These devices have ROM program memory and operate over the standard voltage range.

2.1 UV Erasable Devices

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE™ programmers both support programming of the PIC16C5X. Third party programmers also are available; refer to the *Third Party Guide* for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP SM) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C54/CR54A/C55 address 512 x 12 program memory, the PIC16C56 addresses 1K x 12, and the PIC16C57 addresses 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped into the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 and Table 3-2.

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FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM

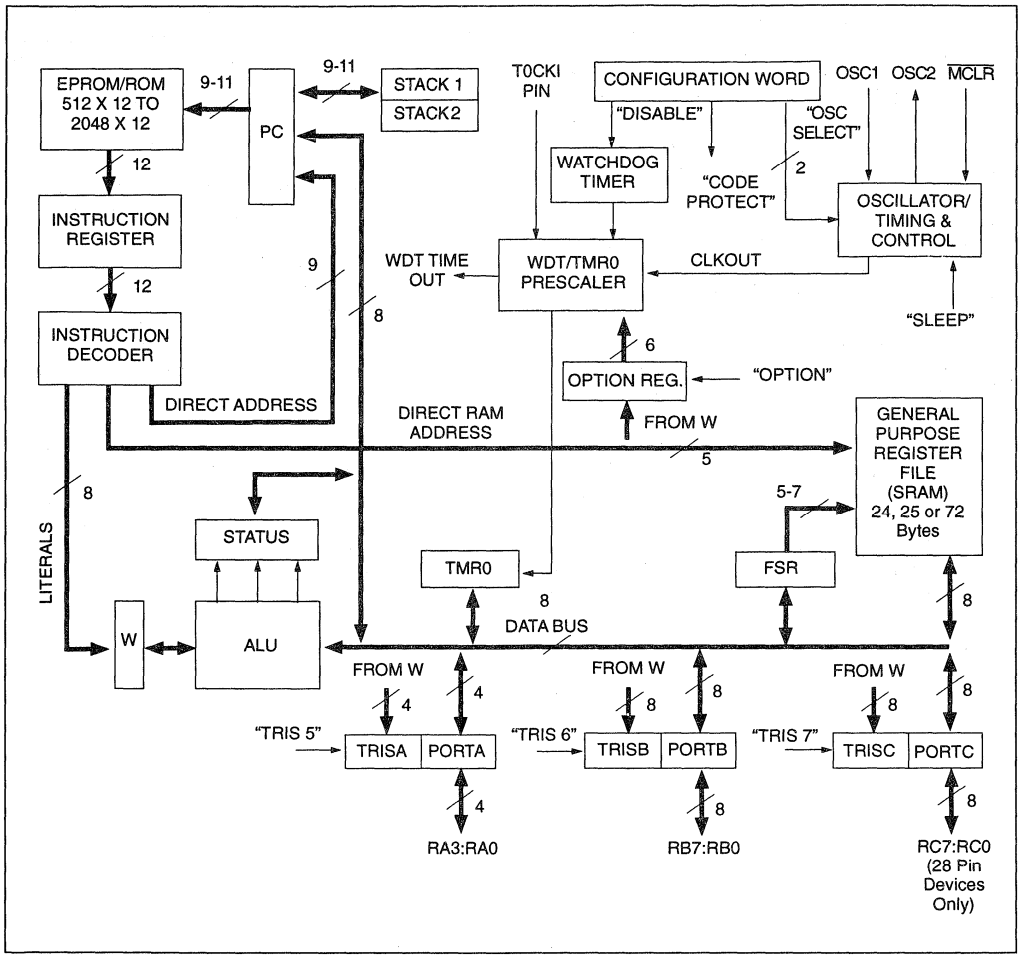

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TABLE 3-1: PIC16C54/CR54A/C56 PINOUT DESCRIPTION

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	20	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RB0	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL	
RB7	13	14	I/O	TTL	
T0CKI	3	3	I	ST	Clock input to Timer0. Must be tied to VSS or VDD, if not in use, to reduce current consumption.
$\overline{MCLR}$/VPP	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on $\overline{MCLR}$/VPP must not exceed VDD to avoid unintended entering of programming mode.
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.
VSS	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used,
TTL = TTL input, ST = Schmitt Trigger input

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TABLE 3-2: PIC16C55/C57 PINOUT DESCRIPTION

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	6	I/O	TTL	
RA2	8	7	I/O	TTL	
RA3	9	8	I/O	TTL	
RB0	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	10	I/O	TTL	
RB2	12	11	I/O	TTL	
RB3	13	12	I/O	TTL	
RB4	14	13	I/O	TTL	
RB5	15	15	I/O	TTL	
RB6	16	16	I/O	TTL	
RB7	17	17	I/O	TTL	
RC0	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	I/O	TTL	
RC2	20	20	I/O	TTL	
RC3	21	21	I/O	TTL	
RC4	22	22	I/O	TTL	
RC5	23	23	I/O	TTL	
RC6	24	24	I/O	TTL	
RC7	25	25	I/O	TTL	
T0CKI	1	2	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
$\overline{MCLR}$/VPP	28	28	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on $\overline{MCLR}$/VPP must not exceed VDD to avoid unintended entering of programming mode.
OSC1/CLKIN	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	2	3,4	P	—	Positive supply for logic and I/O pins.
Vss	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	—	—	—	Unused, do not connect

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used, TTL = TTL input,
ST = Schmitt Trigger input

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3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

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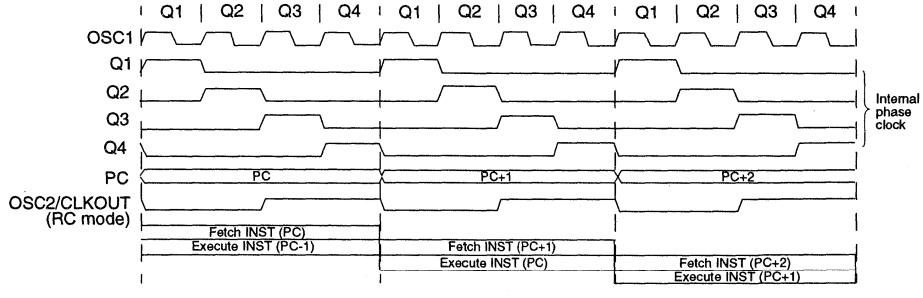
FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

```
1. MOVLW 55h
2. MOVWF PORTB
3. CALL  SUB_1
4. BSF   PORTA, BIT3
```

Fetch 1	Execute 1				
	Fetch 2	Execute 2			
		Fetch 3	Execute 3		
			Fetch 4	Flush	
				Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

4.1 Program Memory Organization

The PIC16C54, PIC16CR54A and PIC16C55 have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 4-1). The PIC16C56 has a 10-bit program counter capable of addressing a 1K x 12 program memory space (Figure 4-2). The PIC16C57 has an 11-bit program counter capable of addressing a 2K x 12 program memory space (Figure 4-3). Accessing a location above the physically implemented address will cause a wraparound.

The reset vector for the PIC16C54/CR54/C55 is at 1FFh, at 3FFh for the PIC16C56, and at 7FFh for the PIC16C57.

FIGURE 4-1: PIC16C54/CR54A/C55 PROGRAM MEMORY MAP AND STACK

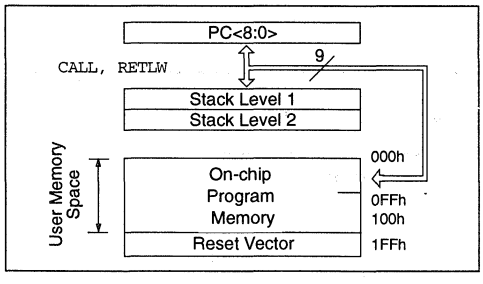


FIGURE 4-2: PIC16C56 PROGRAM MEMORY MAP AND STACK

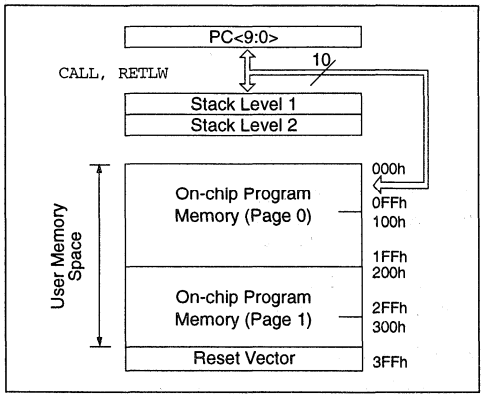
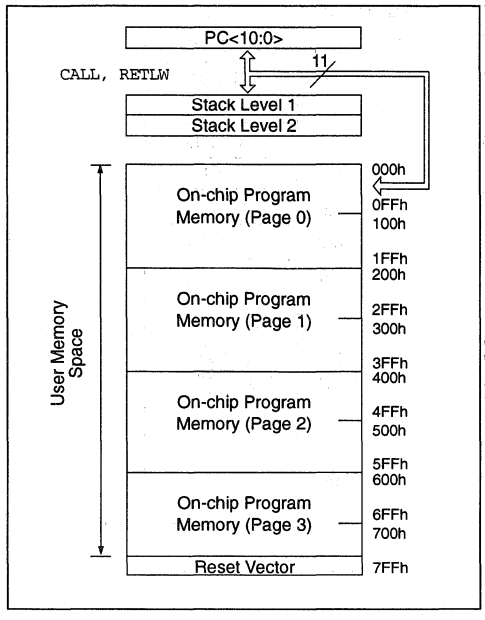


FIGURE 4-3: PIC16C57 PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54A and PIC16C56, the register file is composed of seven special function registers and 25 general purpose registers (Figure 4-4). For the PIC16C55, the register file is composed of eight special function registers and 24 general purpose registers (Figure 4-5). For the PIC16C57, up to 48 additional general purpose registers may be addressed using a banking scheme (Figure 4-6).

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the file select register FSR (Section 4.7).

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FIGURE 4-4: PIC16C54/CR54A/C56 REGISTER FILE MAP

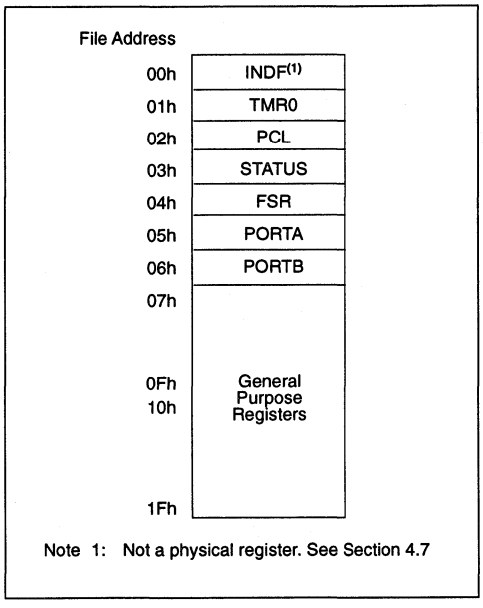


FIGURE 4-5: PIC16C55 REGISTER FILE MAP

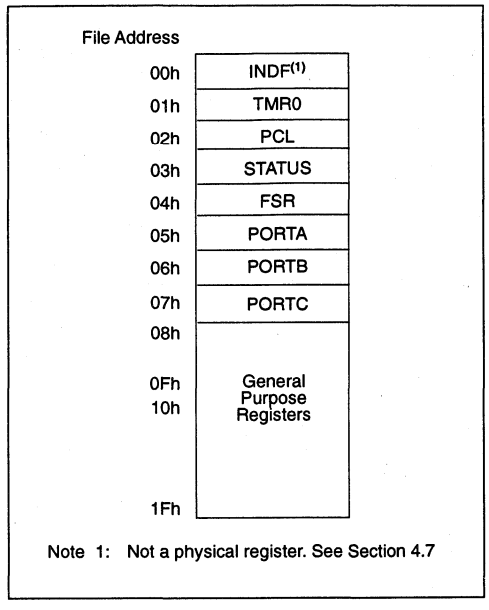
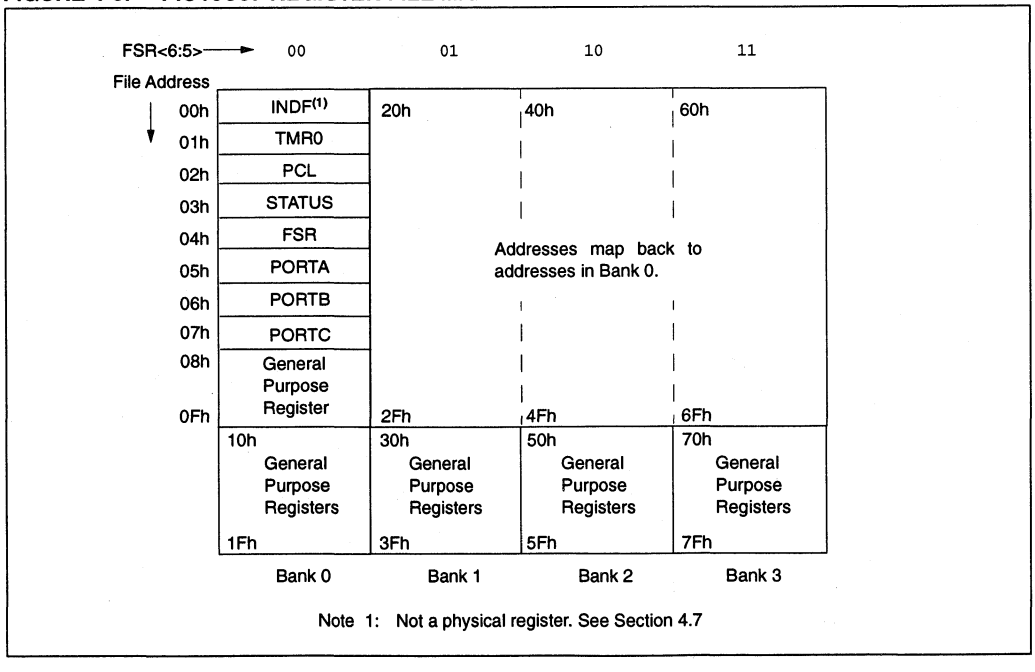


FIGURE 4-6: PIC16C57 REGISTER FILE MAP



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4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h(2)	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 7.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 for an explanation of how to access these bits.

2: File address 07h is a general purpose register on the PIC16C54/CR54A/C56.

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4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u uluu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions which do affect STATUS bits, see Section 13, Instruction Set Summary.

FIGURE 4-7: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **PA2**: This bit unused at this time.
Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA1:PA0**: Program page preselect bits (PIC16C56 and PIC16C57 only)
00 = Page 0 (000h - 1FFh) - PIC16C56 and PIC16C57
01 = Page 1 (200h - 3FFh) - PIC16C56 and PIC16C57
10 = Page 2 (400h - 5FFh) - PIC16C57
11 = Page 3 (600h - 7FFh) - PIC16C57
Each page is 512 bytes.
Using the PA1:PA0 bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: $\overline{TO}$: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: $\overline{PD}$: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF	**SUBWF**	**RRF or RLF**
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

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4.4 OPTION Register

The OPTION register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<5:0> bits.

FIGURE 4-8: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented.**

bit 5: **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 4-9, Figure 4-10 and Figure 4-11).

For the PIC16C56 and PIC16C57, a page number must be supplied as well. Bit5 of the STATUS register provides this to bit9 of the PC for the PIC16C56 (Figure 4-10). Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC for the PIC16C57 (Figure 4-11).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-9, Figure 4-10 and Figure 4-11).

Instructions where the PCL is the destination, or Modify PCL instructions, include `MOVWF PC`, `ADDWF PC`, and `BSF PC,5`.

For the PIC16C56 and PIC16C57, a page number again must be supplied. Bit5 of the STATUS register provides this to bit9 of the PC for the PIC16C56 (Figure 4-10). Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC for the PIC16C57 (Figure 4-11).

Note:	Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-9: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C54/CR54A/C55

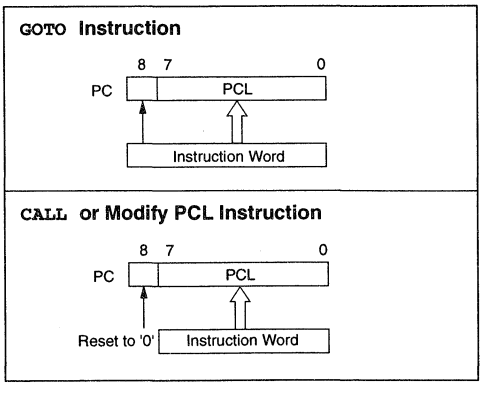


FIGURE 4-10: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56

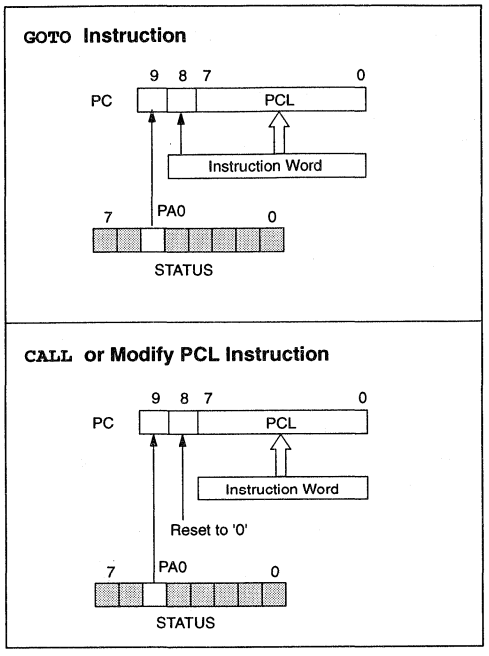
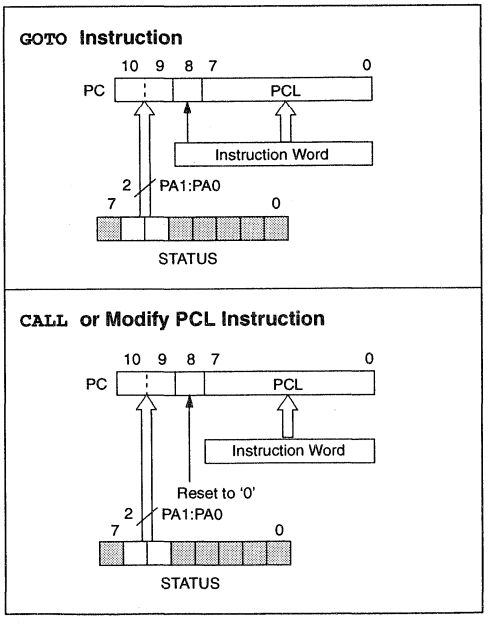


FIGURE 4-11: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57



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For the RETLW instruction, the PC is loaded with the Top Of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stacks. The stack has the same bit width as the device PC.

4.5.1 PAGING CONSIDERATIONS – PIC16C56/57

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS register will not be updated. Therefore, the next GOTO, CALL, or Modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA1:PA0).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxxh on page 0 (assuming that PA1:PA0 are clear).

To prevent this, the page preselect bits must be updated under program control.

4.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the reset vector).

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the reset vector location will automatically cause the program to jump to page 0.

If an inadequate RESET occurs (i.e., POR conditions are not met, a brown-out occurs, etc.), page preselect bits in the STATUS register may not be cleared. Therefore, it is good programming practice to clear the STATUS register (CLRF STATUS) at the reset vector and allow the PC to wrap around to 000h.

4.6 Stack

PIC16C5X devices have a 9-bit, 10-bit or 11-bit wide, two-level hardware push/pop stack (Figure 4-1, Figure 4-2 and Figure 4-3 respectively).

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2.

Note:	The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

4

4.7 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x10  ;initialize pointer
        movwf   FSR   ;  to RAM
NEXT    clrf    INDF  ;clear INDF register
        incf    FSR,F ;inc pointer
        btfsc   FSR,4 ;all done?
        goto    NEXT  ;NO, clear next
CONTINUE
        :             ;YES, continue
```

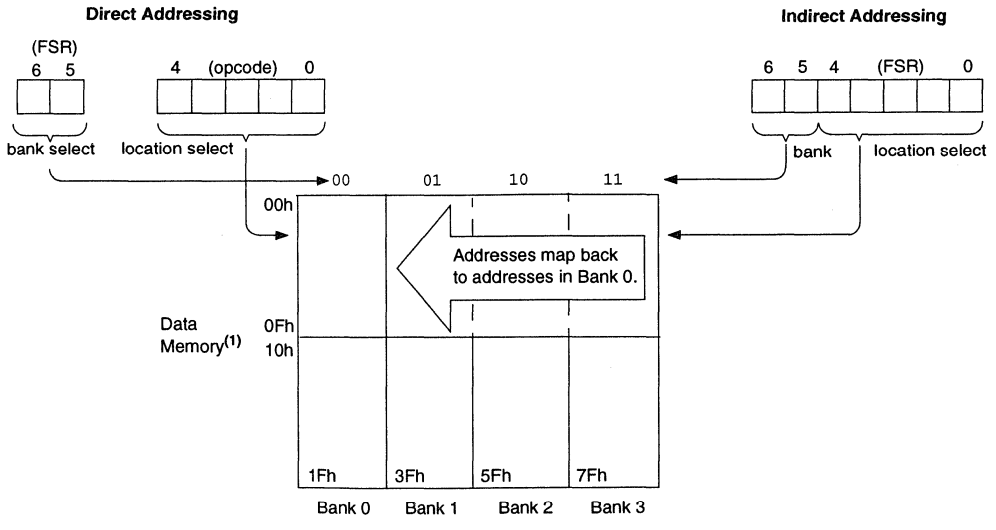
The FSR is either a 5-bit (PIC16C54/CR54A/C55/C56) or 7-bit (PIC16C57) wide register. It is used in conjunction with the INDF register to indirectly address the data memory area. The last two bits, FSR<6:5>, are also used on the PIC16C57 for direct addressing (Figure 4-12).

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C54/CR54A/C55/C56: Do not use banking. FSR<6:5> are unimplemented and read as '1's.

PIC16C57: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).

FIGURE 4-12: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Section 4.2.

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5.0 I/O PORTS

As with any other register, the I/O registers can be written and read under program control. However, read instructions (e.g., `MOVF PORTB,W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

5.1 PORTA

PORTA is a 4-bit I/O register. Only the low order 4 bits are used (RA3:RA0). Bits 7-4 are unimplemented and read as '0's.

5.2 PORTB

PORTB is an 8-bit I/O register (PORTB<7:0>).

5.3 PORTC

PIC16C55/C57: 8-bit I/O register.

PIC16C54/CR54A/C56:
General purpose register.

5.4 TRIS Registers

The output driver control registers are loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

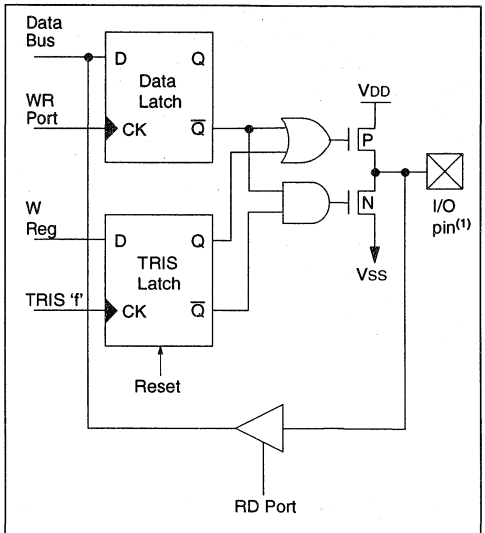
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h(1)	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented, read as '0',
– = unimplemented, read as '0', x = unknown, u = unchanged

Note 1: File address 07h is a general purpose register on the PIC16C54/CR54A/C56.

5.6 I/O Programming Considerations

5.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

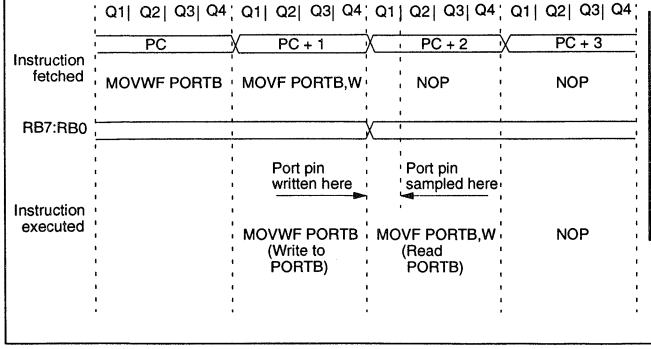
EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
;  PORTB<7:4> Inputs
;  PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                    PORT latch  PORT pins
;                    ----------  ----------
  BCF   PORTB, 7    ;01pp pppp   11pp pppp
  BCF   PORTB, 6    ;10pp pppp   11pp pppp
  MOVLW 03Fh        ;
  TRIS  PORTB       ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-2: SUCCESSIVE I/O OPERATION



This example shows a write to PORTB followed by a read from PORTB.

Data setup time = (0.25 TCY – TPD)

where: TCY = instruction cycle.

TPD = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

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6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module, while Figure 6-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-3 and Figure 6-4). The user can work around this by writing an adjusted value to the TMR0 register.

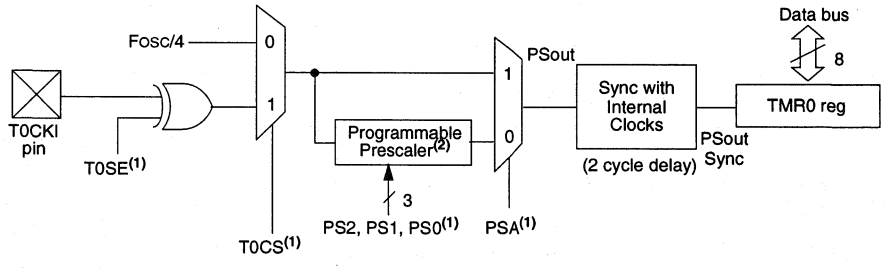
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

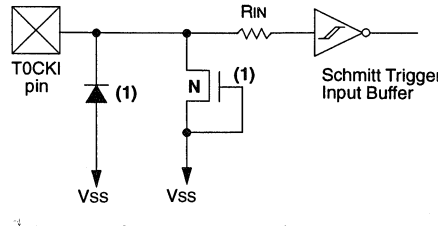
4

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-6).

FIGURE 6-2: ELECTRICAL STRUCTURE OF T0CKI PIN



Note 1: ESD protection circuits

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

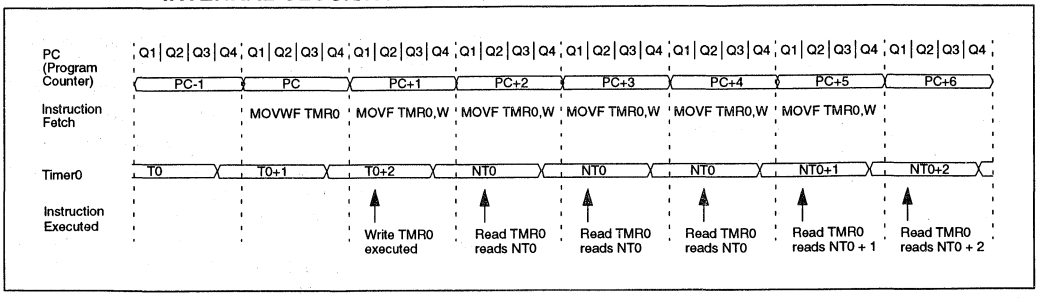


FIGURE 6-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

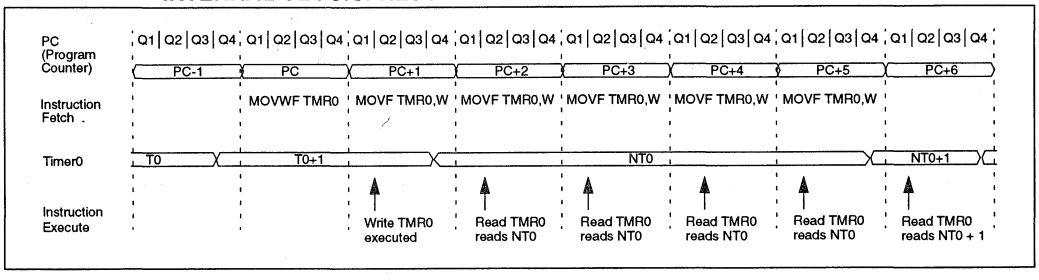


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
01	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded cells: Unimplemented bits,
- = unimplemented, x = unknown, u = unchanged,

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6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

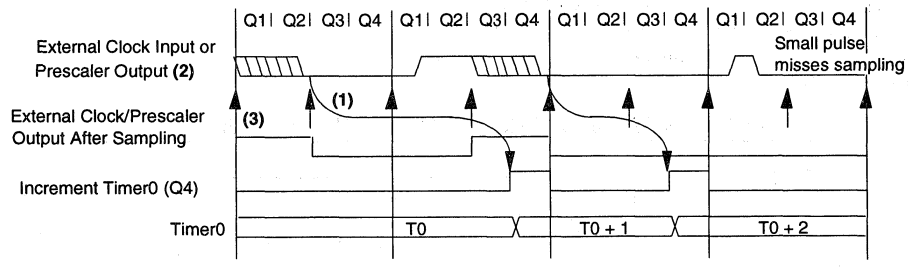
When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

4

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

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6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 6.1.2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

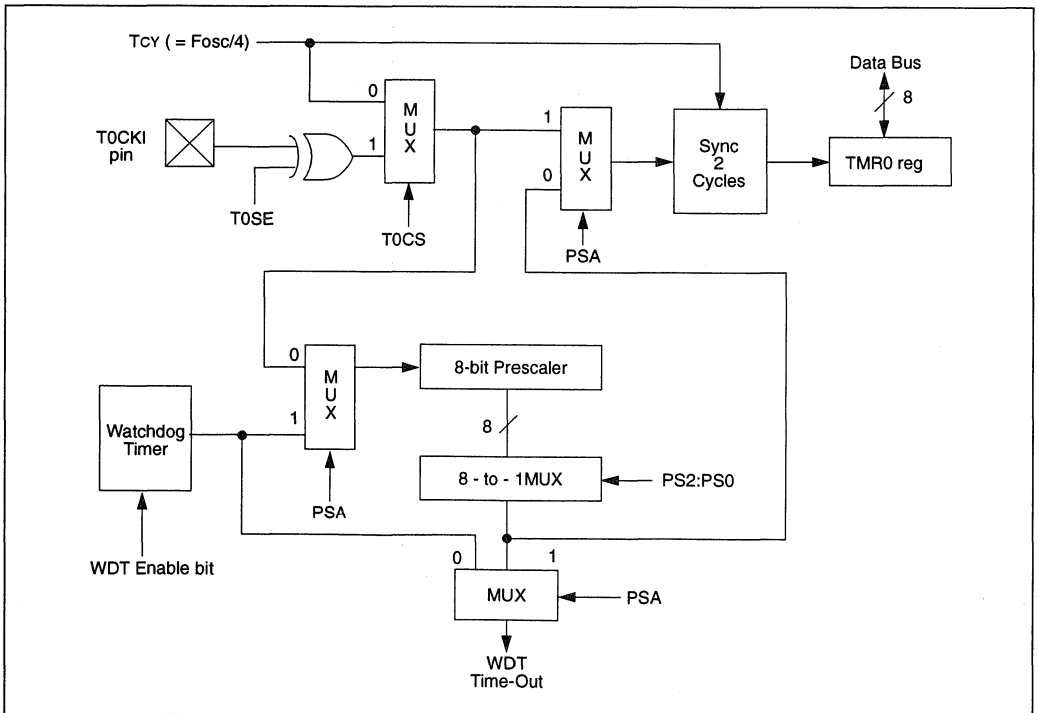
```
1. CLRWDT                ;Clear WDT
2. CLRF   TMR0           ;Clear TMR0 & Prescaler
3. MOVLW  '00xx1111'b;   ;These 3 lines (5, 6, 7)
4. OPTION                ; are required only if
                         ; desired
5. CLRWDT                ;PS<2:0> are 000 or 001
6. MOVLW  '00xx1xxx'b    ;Set Postscaler to
7. OPTION                ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                   ;Clear WDT and
                         ;prescaler
MOVLW   'xxxx0xxx'       ;Select TMR0, new
                         ;prescale value and
                         ;clock source
OPTION
```

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

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7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16C5X family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- Reset
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations

The PIC16C5X has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. With this timer on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

The PIC16C5X configuration word consists of 12 bits, 4 of which are implemented. Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type, one bit is the Watchdog Timer enable bit and one bit is the code protection bit (Figure 7-1).

OTP, QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" on the inside back cover).

4

FIGURE 7-1: CONFIGURATION WORD FOR PIC16C54/CR54A/C55/C56/C57

—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address(1): FFFh

bit 11-4: **Unimplemented:** Read as '0'.

bit 3: **CP:** Code protection bit
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (literature number DS30190) to determine how to access the configuration word.

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7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

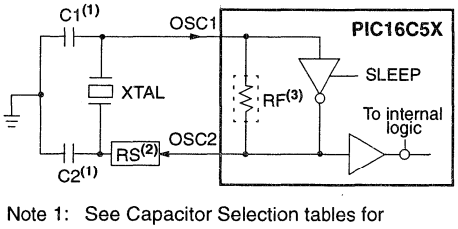
The PIC16C5X can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- RC: Resistor/Capacitor

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 7-2). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 7-3).

FIGURE 7-2: CRYSTAL OPERATION OR CERAMIC RESONATOR (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen (approx. value = 10 MΩ).

FIGURE 7-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

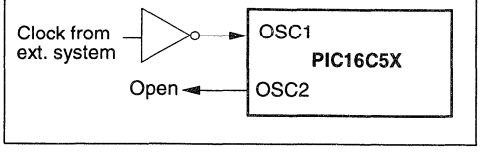


TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C54/55/56/57

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

PRELIMINARY

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C54/55/56/57

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

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7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 7-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 7-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

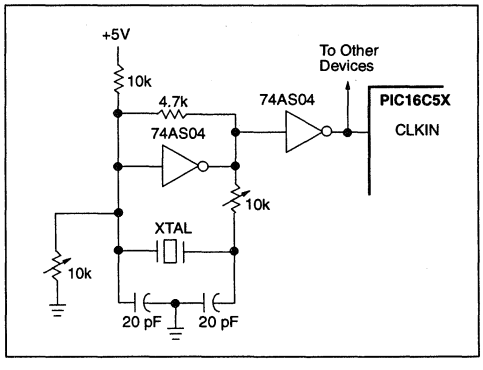
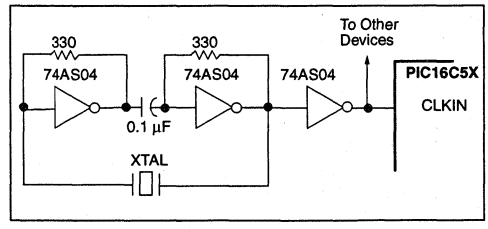


Figure 7-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



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7.2.4 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-6 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

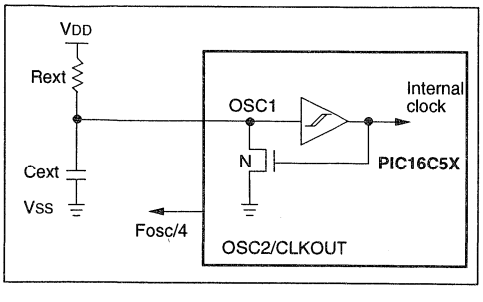
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by four, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

FIGURE 7-6: RC OSCILLATOR MODE



7.3 Reset

PIC16C5X devices may be reset in one of the following ways:

- Power-On Reset (POR)
- $\overline{MCLR}$ reset (normal operation)
- $\overline{MCLR}$ wake-up reset (from SLEEP)
- WDT reset (normal operation)
- WDT wake-up reset (from SLEEP)

Table 7-3 shows these reset conditions for the PCL and STATUS registers.

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-On Reset (POR), $\overline{MCLR}$ or WDT reset. A $\overline{MCLR}$ or WDT wake-up from SLEEP also results in a device reset, and not a continuation of operation before SLEEP.

The $\overline{TO}$ and $\overline{PD}$ bits (STATUS <4:3>) are set or cleared depending on the different reset conditions (Section 7.7). These bits may be used to determine the nature of the reset.

Table 7-4 lists a full description of reset states of all registers. Figure 7-7 shows a simplified block diagram of the on-chip reset circuit.

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TABLE 7-3: RESET CONDITIONS FOR SPECIAL REGISTERS

Condition	PCL Addr: 02h	STATUS Addr: 03h
Power-On Reset	1111 1111	0001 1xxx
$\overline{MCLR}$ reset (normal operation)	1111 1111	000u uuuu(1)
$\overline{MCLR}$ wake-up (from SLEEP)	1111 1111	0001 0uuu
WDT reset (normal operation)	1111 1111	0000 1uuu(2)
WDT wake-up (from SLEEP)	1111 1111	0000 0uuu

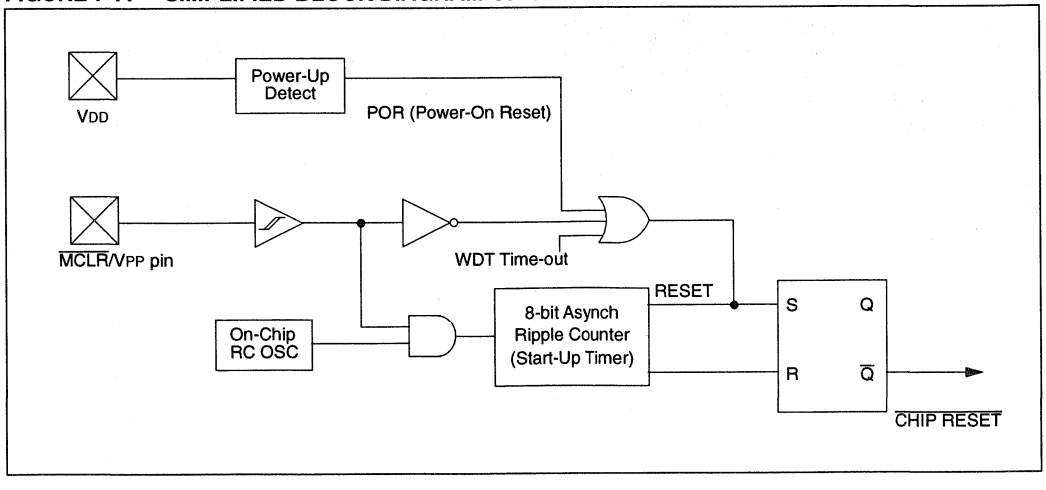
Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.
Note 1: $\overline{TO}$ and $\overline{PD}$ bits retain their last value until one of the other reset conditions occur.
2: The CLRWDT instruction will set the $\overline{TO}$ and $\overline{PD}$ bits.

TABLE 7-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	$\overline{MCLR}$ or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL(1)	02h	1111 1111	1111 1111
STATUS(1)	03h	0001 1xxx	000q quuu
FSR	04h	1xxx xxxx	1uuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC(2)	07h	xxxx xxxx	uuuu uuuu
General Purpose register files	08-7Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0',
q = see tables in Section 7.7 for possible values.
Note 1: See Table 7-3 for reset value for specific conditions.
2: General purpose register file on the PIC16C54/CR54A/C56.

FIGURE 7-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



7.4 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations. To use this feature, the user merely ties the $\overline{MCLR}$/VPP pin (Figure 7-8) to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 7-7.

The Power-On Reset circuit and the Device Reset Timer (Section 7.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

A power-up example where $\overline{MCLR}$ is not tied to VDD is shown in Figure 7-10. VDD is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset TDRT msec after $\overline{MCLR}$ goes high.

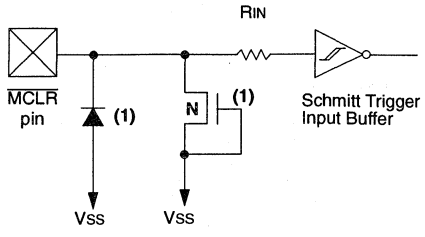
In Figure 7-11, the on-chip Power-On Reset feature is being used ($\overline{MCLR}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 7-12 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the $\overline{MCLR}$/VPP pin, and when the $\overline{MCLR}$/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 7-9).

Note:	When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

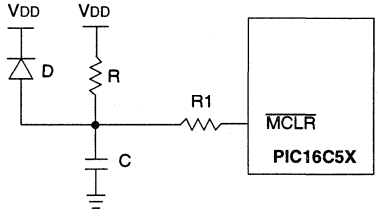
The POR circuit does not produce an internal reset when VDD declines.

FIGURE 7-8: ELECTRICAL STRUCTURE OF $\overline{MCLR}$/VPP PIN



Note 1: ESD protection circuits

FIGURE 7-9: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{MCLR}$/VPP pin is 5 μA). A larger voltage drop will degrade VIH level on $\overline{MCLR}$/VPP pin.
- R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to ESD or EOS.

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FIGURE 7-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD)

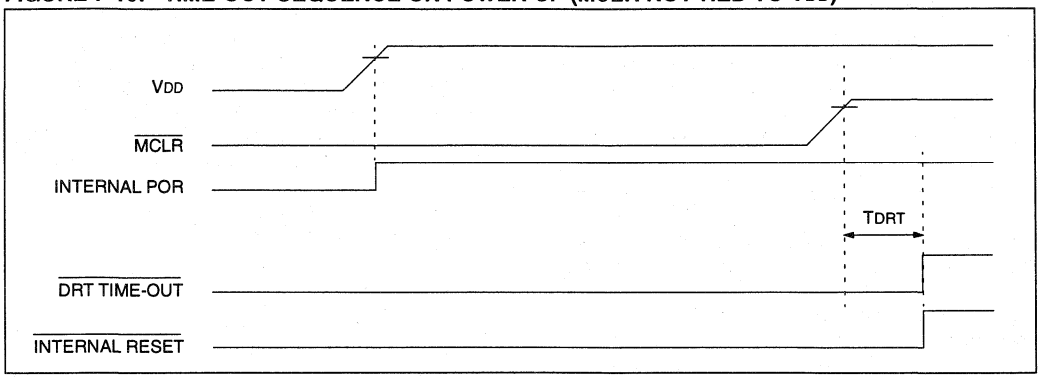


FIGURE 7-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME

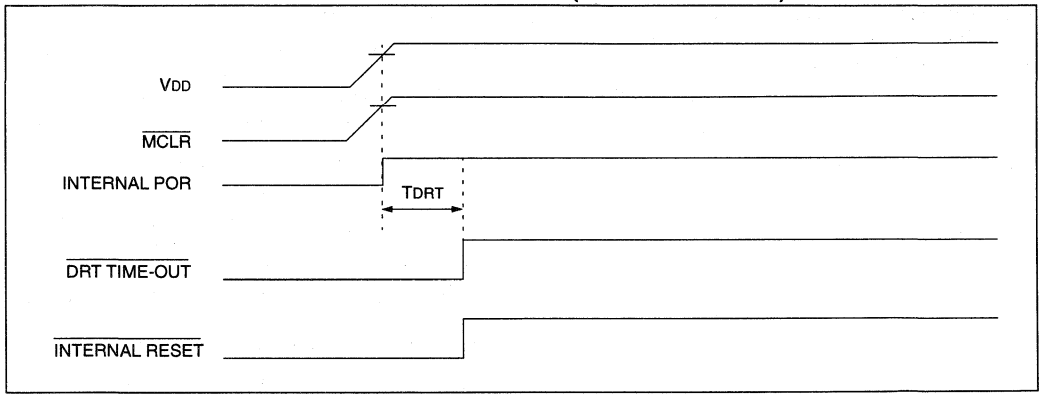
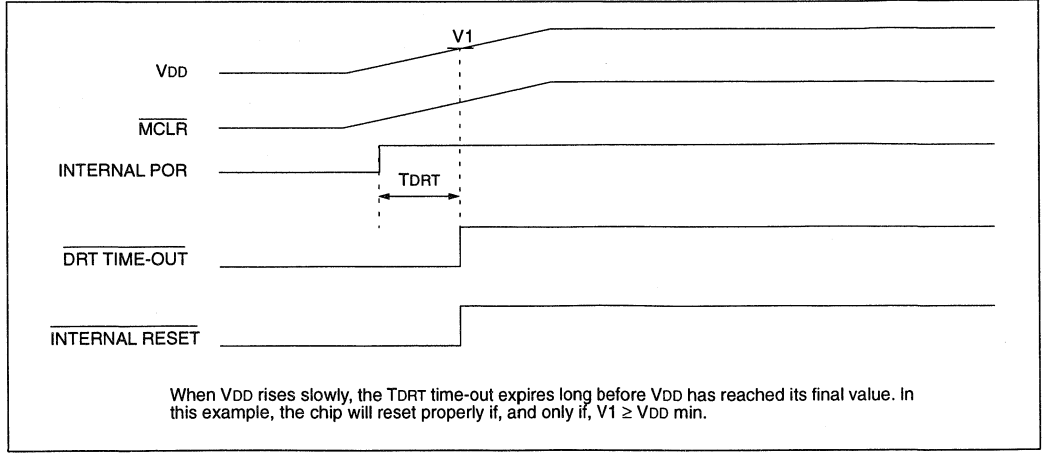


FIGURE 7-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME



When VDD rises slowly, the TDRT time-out expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ VDD min.

7.5 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides a fixed 18 ms nominal time-out on reset. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET for approximately 18 ms after the voltage on the $\overline{MCLR}$/VPP pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the $\overline{MCLR}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

7.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC16C5X Programming Specifications (DS30190) to determine how to access the configuration word.

7.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

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FIGURE 7-13: WATCHDOG TIMER BLOCK DIAGRAM

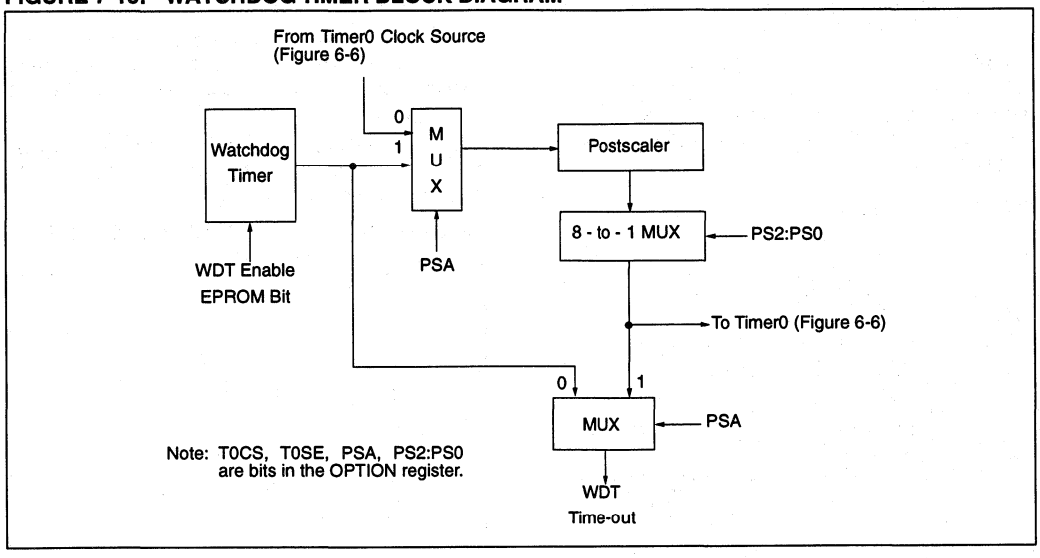

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TABLE 7-5: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded boxes = Not used by Watchdog Timer,
– = unimplemented, read as '0', u = unchanged

7.7 Time-Out Sequence and Power Down Status Bits (TO/PD)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) reset, or a $\overline{MCLR}$ or WDT wake-up reset.

TABLE 7-6: $\overline{TO}/\overline{PD}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-up (POR)
u	u	$\overline{MCLR}$ reset (normal operation)(1)
1	0	$\overline{MCLR}$ wake-up reset (from SLEEP)
0	1	WDT reset (normal operation)
0	0	WDT wake-up reset (from SLEEP)

Legend: u = unchanged
Note 1: The $\overline{TO}$ and $\overline{PD}$ bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$ and $\overline{PD}$ status bits.

These STATUS bits are only affected by events listed in Table 7-7.

TABLE 7-7: EVENTS AFFECTING $\overline{TO}/\overline{PD}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Time-out	0	u	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Legend: u = unchanged
A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 7-6 reflects the status of $\overline{TO}$ and $\overline{PD}$ after the corresponding event.

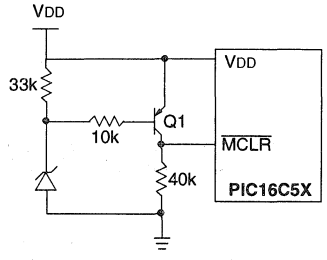
Table 7-3 lists the reset conditions for the special function registers, while Table 7-4 lists the reset conditions for all the registers.

7.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

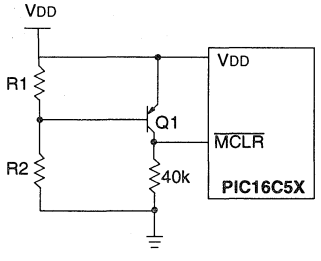
To reset PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built (Figure 7-14 and Figure 7-15).

FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

FIGURE 7-15: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

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7.9 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

7.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$/VPP pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or VSS and the $\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC).

7.9.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. An external reset input on $\overline{MCLR}$/VPP pin.
2. A Watchdog Timer time-out reset (if WDT was enabled).

Both of these events cause a device reset. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of device reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes..

Note: Microchip does not recommend code protecting windowed devices.

7.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower four bits of the ID locations and always program the upper eight bits as '1's.

Note: Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

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NOTES:

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8.0 ELECTRICAL CHARACTERISTICS - PIC16C54/55/56/57

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0V to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0V to +14V

Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)

Total Power Dissipation (1) ..... 800 mW

Max. Current out of V_{SS} pin ..... 150 mA

Max. Current into V_{DD} pin ..... 50 mA

Max. Current into an input pin (T0CKI only) ..... ±500 µA

Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Max. Output Current sunk by any I/O pin ..... 25 mA

Max. Output Current sourced by any I/O pin ..... 20 mA

Max. Output Current sourced by a single I/O port (PORTA, B or C) ..... 40 mA

Max. Output Current sunk by a single I/O port (PORTA, B or C) ..... 50 mA

Note 1: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4

TABLE 8-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS (RC, XT & 10) AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-RC	PIC16C5X-XT	PIC16C5X-10
RC	VDD: 3.0 V to 6.2 V IDD: 3.3 mA max. at 5. V IPD: 9 µA max. at 3.0 V, WDT dis Freq: 4 MHz max.	N/A	N/A
XT	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.6 µA typ. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 3.3 mA max. at 5.5V IPD: 9 µA max. at 3.0V, WDT dis Freq: 4 MHz max.	N/A
HS	VDD: 4.5V to 5.5V IDD: 9.0 mA typ. at 5.5V IPD: 0.6 µA typ. at 3.0V WDT dis Freq: 20 MHz max.	N/A	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 9 µA max. at 3.0V, WDT dis Freq: 10 MHz max.
LP	VDD: 2.5V to 6.25V IDD: 15 µA typ. at 3.0V IPD: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 15 µA typ. at 3.0V IPD: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 15 µA typ. at 3.0V IPD: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

TABLE 8-2: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS (HS, LP & JW) AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-HS	PIC16C5X-LP	PIC16C5X/JW
RC	N/A	N/A	VDD: 3.0V to 6.25V IDD: 3.3 mA max. at 5.5V IPD: 9 µA max. at 3.0V, WDT dis Freq: 4 MHz max.
XT	N/A	N/A	VDD: 3.0V to 6.25V IDD: 3.3 mA max. at 5.5V IPD: 9 µA max. at 3.0V, WDT dis Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 9 µA max. at 3.0V, WDT dis Freq: 20 MHz max.	N/A	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 9 µA max. at 3.0V, WDT dis Freq: 20 MHz max.
LP	VDD: 2.5V to 6.25V IDD: 15 µA typ. at 3.0V IPD: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 9 µA max. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 9 µA max. at 3.0V, WDT dis Freq: 40 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

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8.1 DC Characteristics: PIC16C5X-RC, XT, 10, HS, LP (Commercial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
PIC16C5X-RC		3.0		6.25	V	FOSC = DC to 4 MHz
PIC16C5X-XT		3.0		6.25	V	FOSC = DC to 4 MHz
PIC16C5X-10		4.5		5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HS		4.5		5.5	V	FOSC = DC to 20 MHz
PIC16C5X-LP		2.5		6.25	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP Mode
VDD Start Voltage to ensure Power-On Reset	VPOR		VSS		V	See Section 7.4 for details on Power-On Reset
VDD Rise Rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-On Reset
Supply Current(3)	IDD					
PIC16C5X-RC(4)			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XT			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HS			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
PIC16C5X-LP			15	32	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5)	IPD					
			4.0	12	µA	VDD = 3.0V, WDT enabled
			0.6	9	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
   a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
   b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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8.2 DC Characteristics: PIC16C5X-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +85°C				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
PIC16C5X-RCI		3.0		6.25	V	FOSC = DC to 4 MHz
PIC16C5X-XTI		3.0		6.25	V	FOSC = DC to 4 MHz
PIC16C5X-10I		4.5		5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HSI		4.5		5.5	V	FOSC = DC to 20 MHz
PIC16C5X-LPI		2.5		6.25	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-On Reset	VPOR		VSS		V	See Section 7.4 for details on Power-On Reset
VDD Rise Rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-On Reset
Supply Current(3)	IDD					
PIC16C5X-RCI(4)			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XTI			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10I			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HSI			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
PIC16C5X-LPI			19	40	µA	FOSC = 32 kHz, Vdd = 3.0V, WDT disabled
Power Down Current(5)	IPD					
			5.0	14	µA	VDD = 3.0V, WDT enabled
			0.6	12	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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8.3 DC Characteristics: PIC16C5X-RCE, XTE, 10E, HSE, LPE (Automotive)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40°C \le T_A \le +125°C$				
Characteristic	**Sym**	**Min**	**Typ (1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
PIC16C5X-RCE		3.25		6.0	V	FOSC = DC to 4 MHz
PIC16C5X-XTE		3.25		6.0	V	FOSC = DC to 4 MHz
PIC16C5X-10E		4.5		5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HSE		4.5		5.5	V	FOSC = DC to 16 MHz
PIC16C5X-LPE		2.5		6.0	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-On Reset	VPOR		VSS		V	See Section 7.4 for details on Power-On Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-On Reset
Supply Current(3)	IDD					
PIC16C5X-RCE(4)			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XTE			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10E			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HSE			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
			9.0	20	mA	FOSC = 16 MHz, VDD = 5.5V
PIC16C5X-LPE			25	55	µA	FOSC = 32 kHz, VDD = 3.25V, WDT disabled
Power Down Current(5)	IPD					
			5.0	22	µA	VDD = 3.25V, WDT enabled
			0.8	18	µA	VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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8.4 DC Characteristics: PIC16C5X-RC, XT, 10, HS, LP (Commercial) PIC16C5X-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 8.1, Section 8.2 and Section 8.3.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	PIC16C5X-RC only(4)
		VSS		0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
Input High Voltage	VIH					
I/O ports		0.45 VDD		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD		VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	PIC16C5X-RC only(4)
		0.7 VDD		VDD	V	PIC16C5X-XT, 10, HS, LP
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(2,3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5			µA	VPIN = VSS + 0.25V
			0.5	+5	µA	VPIN = VDD
T0CKI		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
Output High Voltage	VOH					
I/O ports(3)		VDD – 0.7			V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD – 0.7			V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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8.5 DC Characteristics: PIC16C5X-RC, XT, 10, HS, LP (Automotive)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C Operating Voltage VDD range is described in Section 8.1, Section 8.2 and Section 8.3.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		Vss		0.15 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		Vss		0.15 VDD	V	
T0CKI (Schmitt Trigger)		Vss		0.15 VDD	V	
OSC1 (Schmitt Trigger)		Vss		0.15 VDD	V	PIC16C5X-RC only(4)
		Vss		0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
Input High Voltage	VIH					
I/O ports		0.45 VDD		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD		VDD	V	VDD > 5.5 V
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	PIC16C5X-RC only(4)
		0.7 VDD		VDD	V	PIC16C5X-XT, 10, HS, LP
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current (2,3)	IIL					**For VDD ≤ 5.5 V**
I/O ports		−1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		−5			µA	VPIN = VSS + 0.25V
			0.5	+5	µA	VPIN = VDD
T0CKI		−3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		−3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
Output High Voltage	VOH					
I/O ports(3)		VDD − 0.7			V	IOH = −5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD − 0.7			V	IOH = −1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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8.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

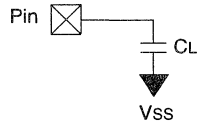
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 8-1: LOAD CONDITIONS - PIC16C54/55/56/57



CL = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

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8.7 Timing Diagrams and Specifications

FIGURE 8-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57

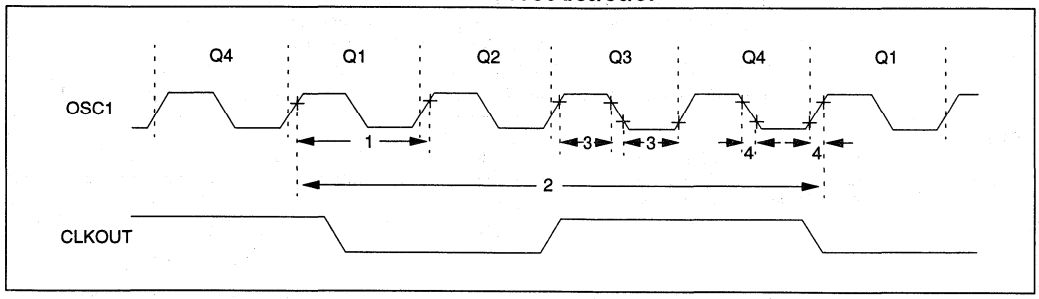

TABLE 8-3: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 8.1, Section 8.2 and Section 8.3

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4	MHz	RC osc mode
			DC	—	4	MHz	XT osc mode
			DC	—	10	MHz	10 MHz mode
			DC	—	20	MHz	HS osc mode (Com/Indust)
			DC	—	16	MHz	HS osc mode (Automotive)
			DC	—	40	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	10	MHz	10 MHz mode
			4	—	20	MHz	HS osc mode (Com/Indust)
			4	—	16	MHz	HS osc mode (Automotive)
			DC	—	40	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 8-3: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57 (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 8.1, Section 8.2 and Section 8.3

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
			100	—	—	ns	10 MHz mode
			50	—	—	ns	HS osc mode (Com/Indust)
			62.5	—	—	ns	HS osc mode (Automotive)
			25	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			100	—	250	ns	10 MHz mode
			50	—	250	ns	HS osc mode (Com/Indust)
			62.5	—	250	ns	HS osc mode (Automotive)
			25	—	—	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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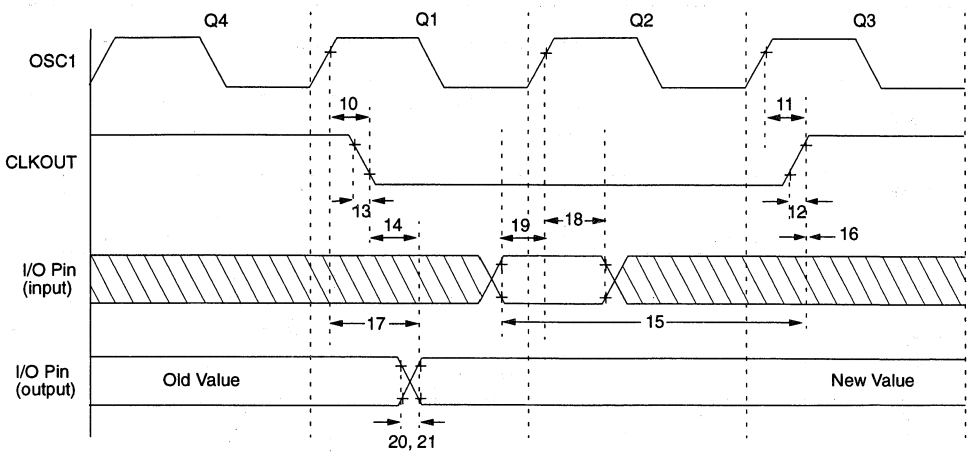
FIGURE 8-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

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TABLE 8-4: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 8.1, Section 8.2 and Section 8.3

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5	15**	ns
13	TckF	CLKOUT fall time(2)	—	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 8-1 for loading conditions.

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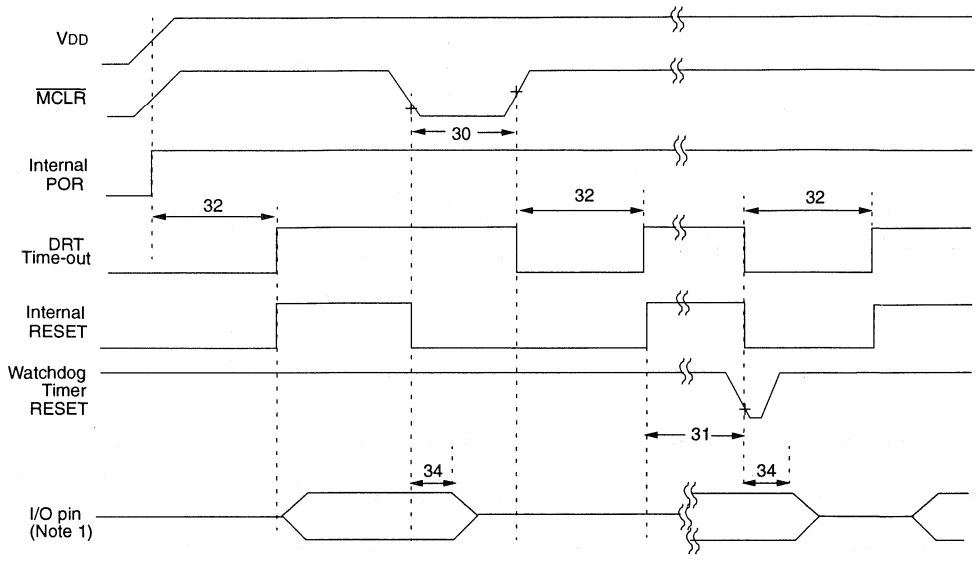
FIGURE 8-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 8-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 8.1, Section 8.2 and Section 8.3						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 8-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57

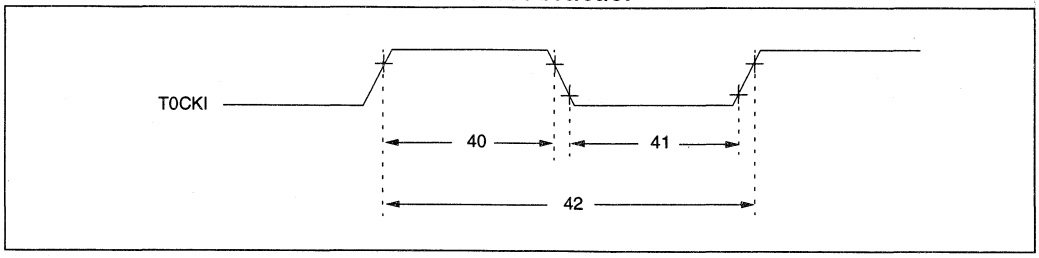

TABLE 8-6: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 8.1, Section 8.2 and Section 8.3

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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NOTES:

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9.0 DC AND AC CHARACTERISTICS - PIC16C54/55/56/57

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 9-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

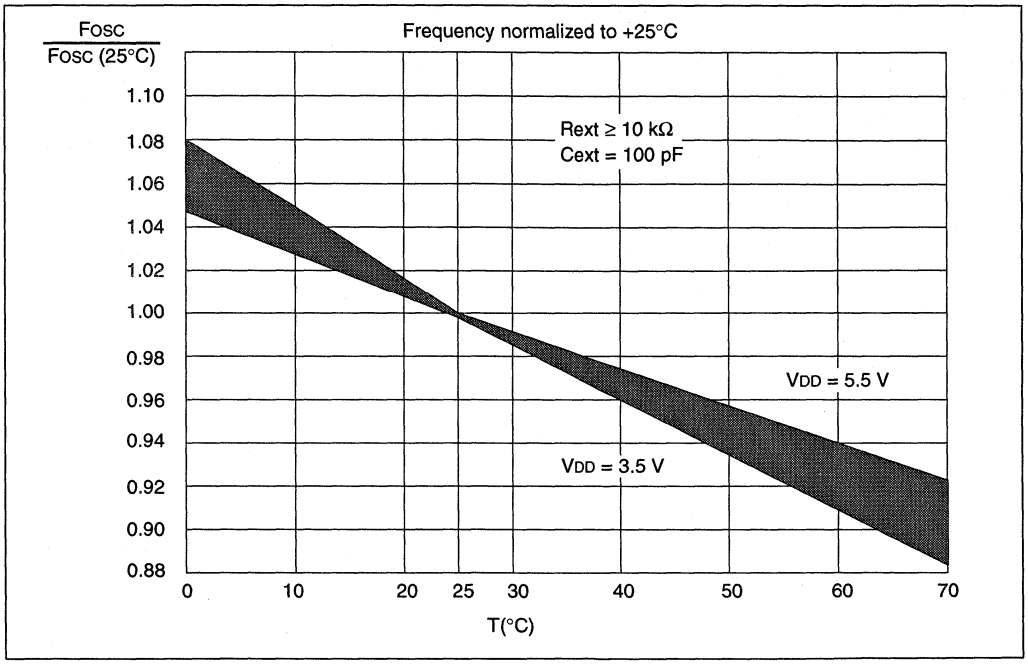

TABLE 9-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5 V.

FIGURE 9-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20pF

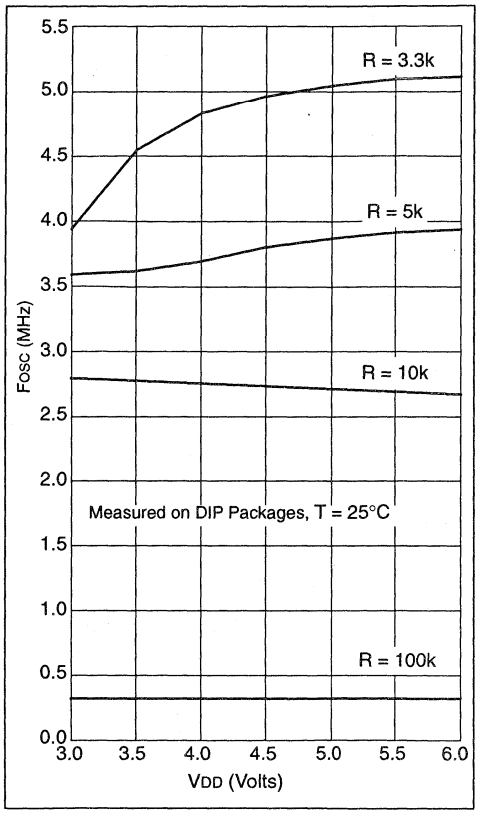

FIGURE 9-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF

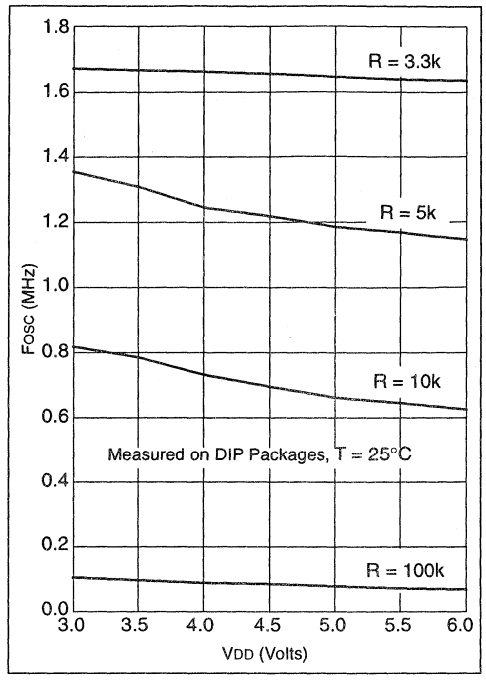

FIGURE 9-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF

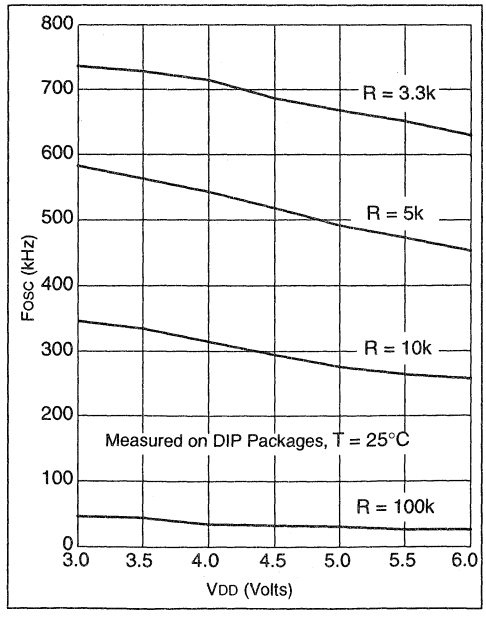

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FIGURE 9-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED

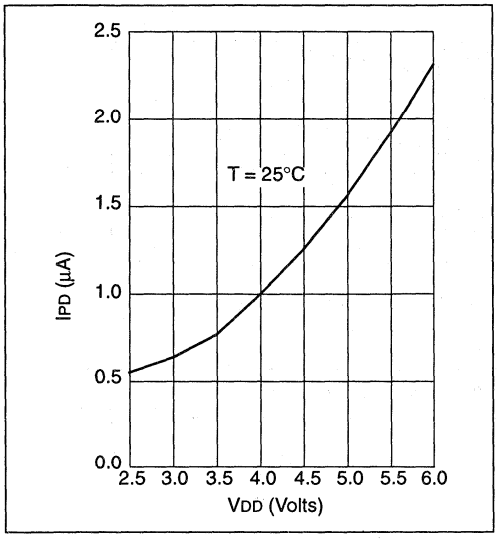


FIGURE 9-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED

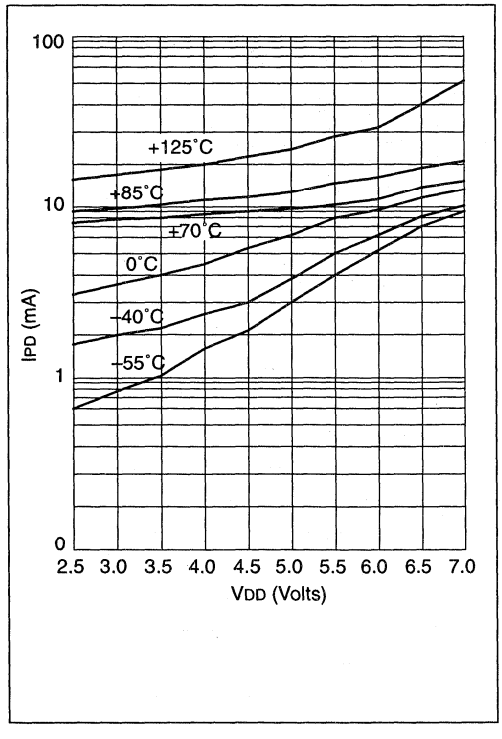


FIGURE 9-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED

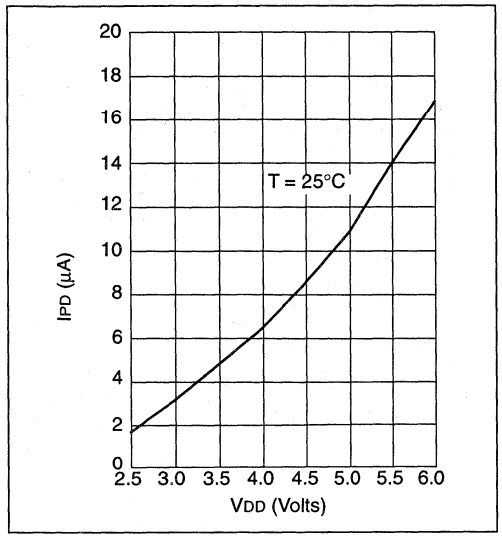
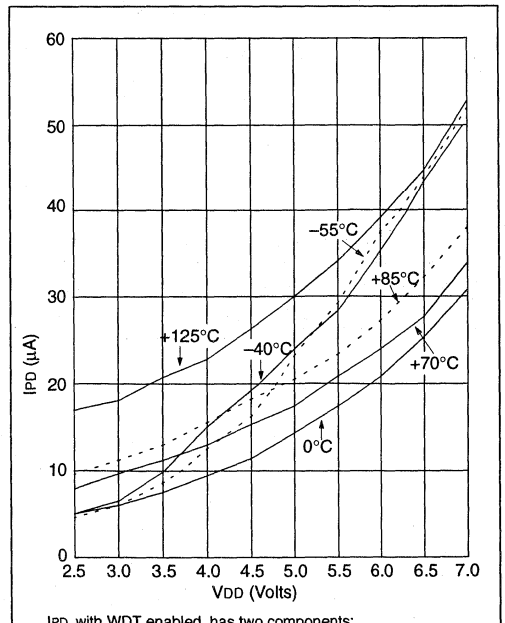


FIGURE 9-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components:

The leakage current which increases with higher temperature and the operating current of the WDT logic which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

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FIGURE 9-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

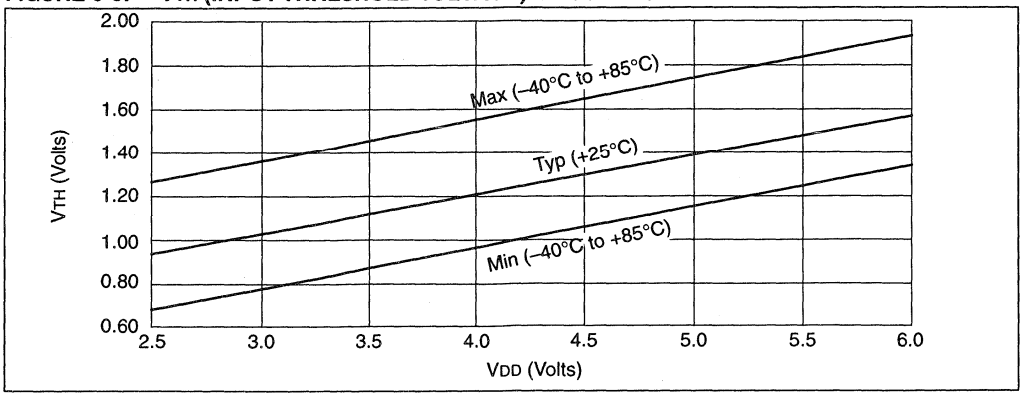
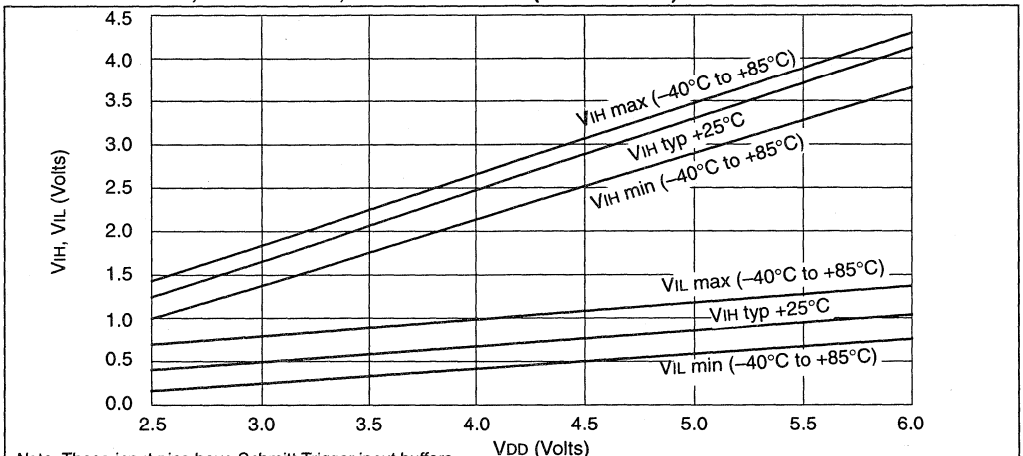


FIGURE 9-10: VIH, VIL OF $\overline{MCLR}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 9-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD

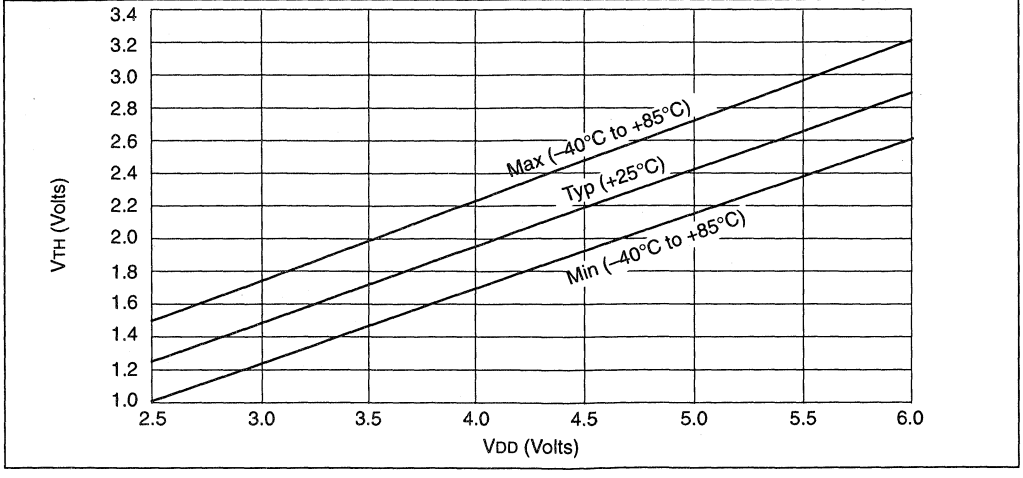


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FIGURE 9-12: TYPICAL IDD vs. FREQUENCY (EXTERNAL CLOCK, 25°C)

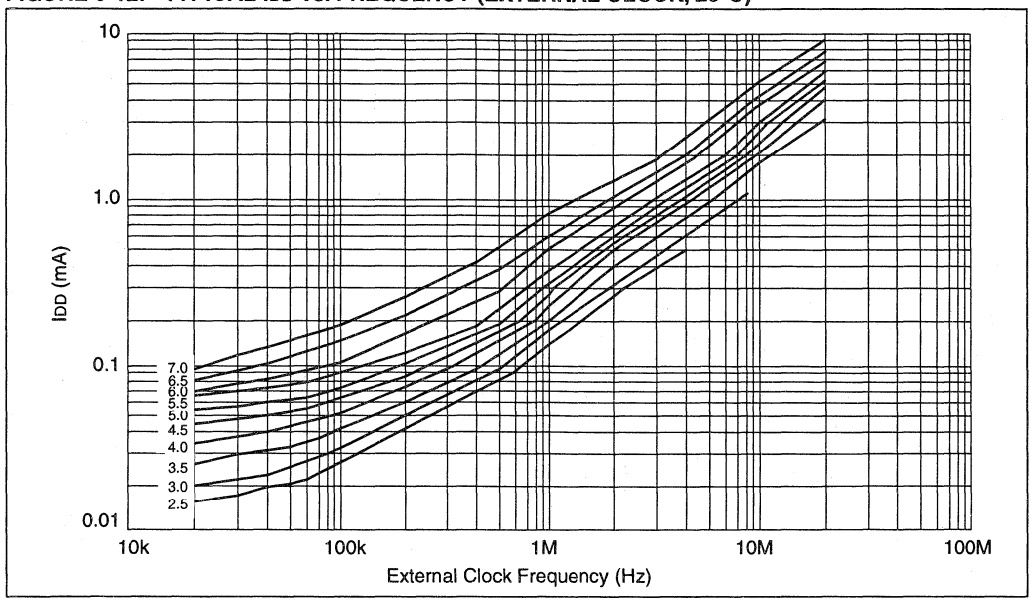

FIGURE 9-13: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK, –40°C TO +85°C)

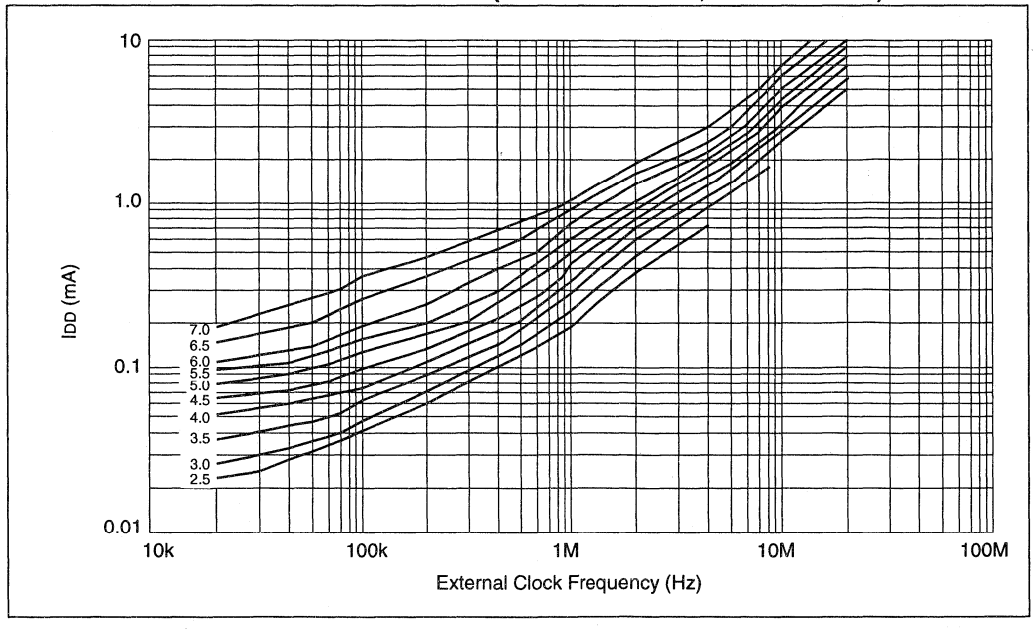

FIGURE 9-14: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK –55°C TO +125°C)

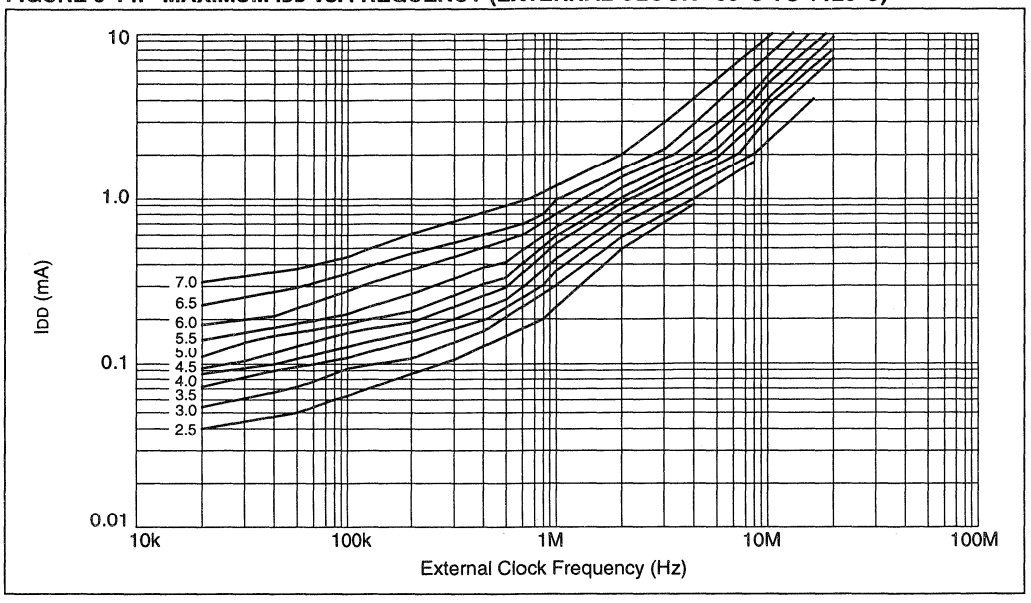

FIGURE 9-15: WDT TIMER TIME-OUT PERIOD vs. VDD

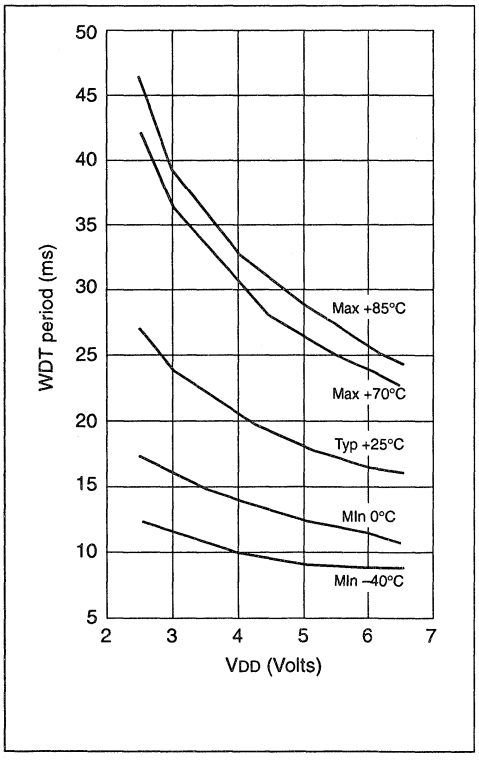

FIGURE 9-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

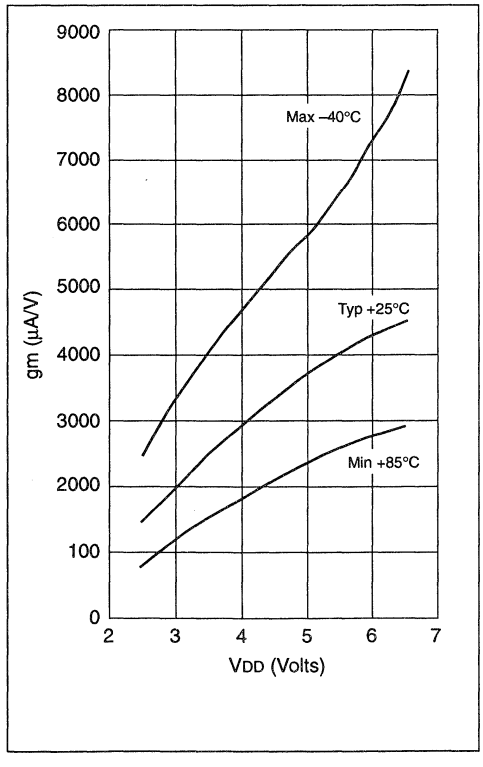

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FIGURE 9-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

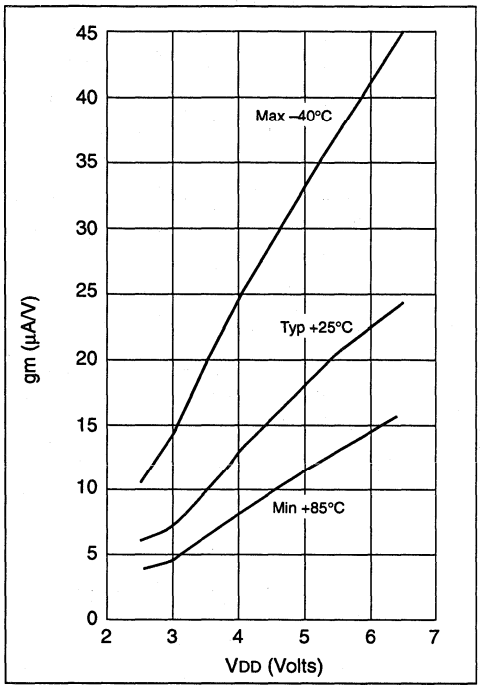

FIGURE 9-18: IOH vs. VOH, VDD = 3 V

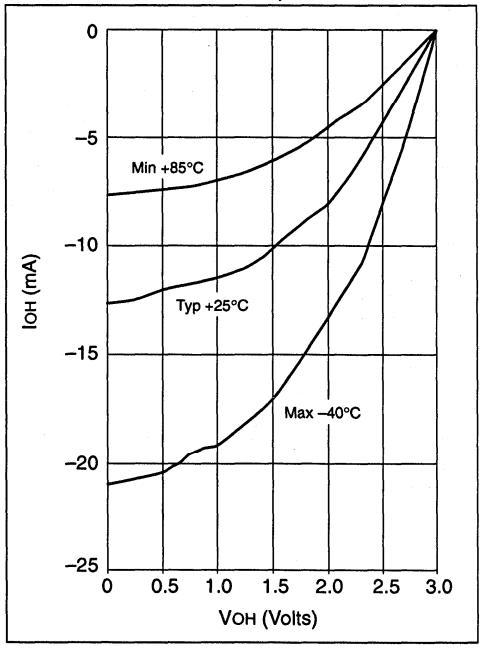

FIGURE 9-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

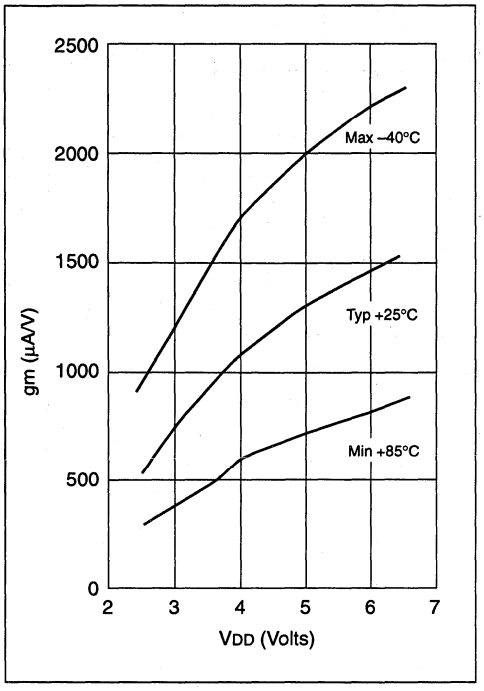

FIGURE 9-20: IOH vs. VOH, VDD = 5 V

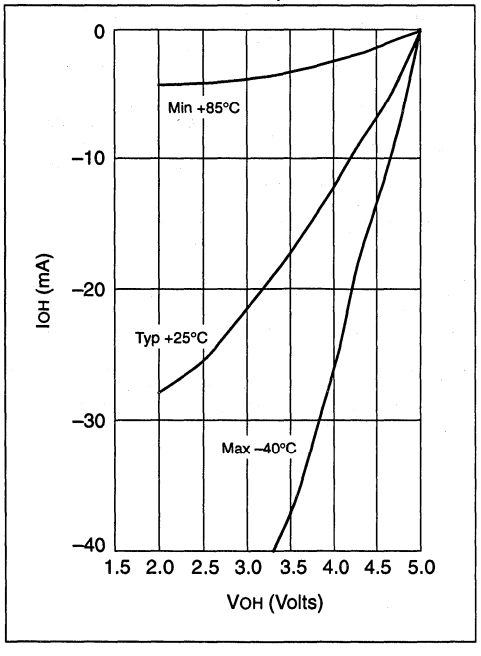

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FIGURE 9-21: IOL vs. VOL, VDD = 3 V

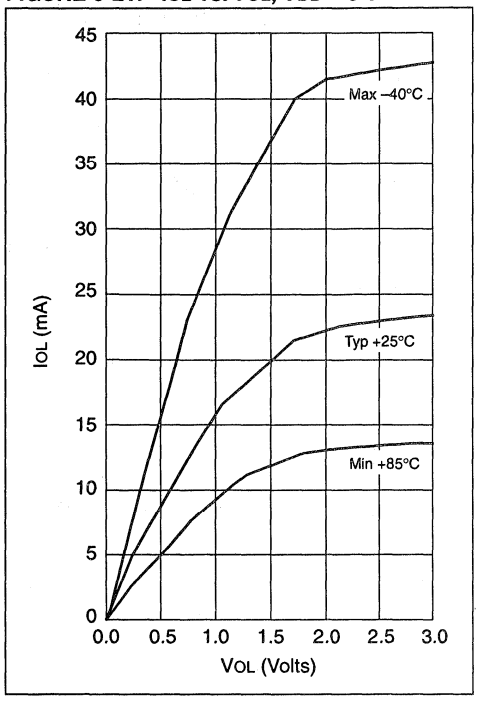

FIGURE 9-22: IOL vs. VOL, VDD = 5 V

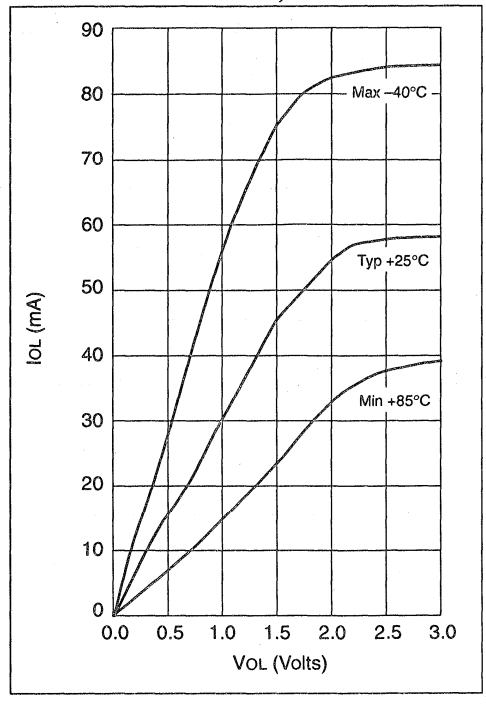

TABLE 9-2: INPUT CAPACITANCE FOR PIC16C54/56

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 9-3: INPUT CAPACITANCE FOR PIC16C55/57

Pin	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
$\overline{MCLR}$	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
T0CKI	4.5	3.5

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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10.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)
Total Power Dissipation (1) ..... 800 mW
Max. Current out of V_{SS} pin ..... 150 mA
Max. Current into V_{DD} pin ..... 50 mA
Max. Current into an input pin (T0CKI only) ..... ±500 µA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. Output Current sunk by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin ..... 20 mA
Max. Output Current sourced by a single I/O port (PORTA or B) ..... 40 mA
Max. Output Current sunk by a single I/O port (PORTA or B) ..... 50 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD}-V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100Ω should be used when applying a low level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 10-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR54A-04	PIC16CR54A-10	PIC16CR54A-20	PIC16LCR54A-04
RC	VDD: 2.5 V to 6.25 V IDD: 3.6 mA max at 6.0 V IPD: 6.0 µA max at 2.5 V, WDT dis Freq: 4 MHz max	N/A	N/A	N/A
XT	VDD: 2.5 V to 6.25 V IDD: 3.6 mA max at 6.0 V IPD: 6.0 µA max at 2.5 V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	VDD: 4.5 V to 5.5 V IDD: 10 mA max at 5.5 V IPD: 6.0 µA max at 2.5 V, WDT dis Freq: 10 MHz max	VDD: 4.5 V to 5.5 V IDD: 10 mA max at 5.5 V IPD: 6.0 µA max at 2.5 V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	VDD: 2.0 V to 6.25 V IDD: 20 µA max at 32 kHz, 2.0 V IPD: 6.0 µA max at 2.5 V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

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10.1 DC Characteristics: PIC16CR54A-04, 10, 20 (Commercial) PIC16CR54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
RC and XT options		2.5		6.25	V	
HS option		4.5		5.5	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
RC(4) and XT options			2.0	3.6	mA	FOSC = 4.0 MHz, VDD = 6.0V
			0.8	1.8	mA	FOSC = 4.0 MHz, VDD = 3.0V
			90	350	µA	FOSC = 200 kHz, VDD = 2.5V
HS option			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
Power-Down Current(5)	IPD					
Commercial						
			1.0	6.0	µA	VDD = 2.5V, WDT disabled
			2.0	8.0*	µA	VDD = 4.0V, WDT disabled
			3.0	15	µA	VDD = 6.0V, WDT disabled
			5.0	25	µA	VDD = 6.0V, WDT enabled
Power-Down Current(5)	IPD					
Industrial						
			1.0	8.0	µA	VDD = 2.5V, WDT disabled
			2.0	10*	µA	VDD = 4.0V, WDT disabled
			3.0	20*	µA	VDD = 4.0V, WDT enabled
			3.0	18	µA	VDD = 6.0V, WDT disabled
			5.0	45	µA	VDD = 6.0V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4

10.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Automotive)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C (automotive)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS options	VDD	 3.25 4.5		 6.0 5.5	 V V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD		 1.8 4.8 9.0	 3.3 10 20	 mA mA mA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V
Power-Down Current(5)	IPD		 5.0 0.8	 22 18	 µA µA	 VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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10.3 DC Characteristics: PIC16LCR54A-04 (Commercial) PIC16LCR54A-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.0		6.25	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD		10	20	µA	FOSC = 32 kHz, VDD = 2.0V
				70	µA	FOSC = 32 kHz, VDD = 6.0V
Power-Down Current(5) Commercial	IPD					
			1.0	6.0	µA	VDD = 2.5V, WDT disabled
			2.0	8.0*	µA	VDD = 4.0V, WDT disabled
			3.0	15	µA	VDD = 6.0V, WDT disabled
			5.0	25	µA	VDD = 6.0V, WDT enabled
Power-Down Current(5) Industrial	IPD					
			1.0	8.0	µA	VDD = 2.5V, WDT disabled
			2.0	10*	µA	VDD = 4.0V, WDT disabled
			3.0	20*	µA	VDD = 4.0V, WDT enabled
			3.0	18	µA	VDD = 6.0V, WDT disabled
			5.0	45	µA	VDD = 6.0V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4

10.4 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1 and Section 10.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	RC option only(4)
OSC1		VSS		0.15 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		2.0		VDD	V	VDD = 3.0V to 5.5V(5)
		0.6 VDD		VDD	V	Full VDD range(5)
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC option only(4)
OSC1		0.85 VDD		VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0		+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0			µA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports				0.5	V	IOL = 10 mA, VDD = 6.0V
OSC2/CLKOUT				0.5	V	IOL = 1.9 mA, VDD = 6.0V, RC option only
Output High Voltage(3)	VOH					
I/O ports		VDD –0.5			V	IOH = –4.0 mA, VDD = 6.0V
OSC2/CLKOUT		VDD –0.5			V	IOH = –0.8 mA, VDD = 6.0V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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10.5 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Automotive)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C Operating Voltage VDD range is described in Section 10.2.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		Vss		0.15 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		Vss		0.15 VDD	V	
T0CKI (Schmitt Trigger)		Vss		0.15 VDD	V	
OSC1 (Schmitt Trigger)		Vss		0.15 VDD	V	RC option only(4)
OSC1		Vss		0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD		VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC option only(4)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0			µA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage (3)	VOH					
I/O ports		VDD –0.7			V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7			V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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10.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

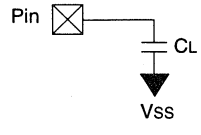
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{MCLR}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 10-1: LOAD CONDITIONS



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

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10.7 Timing Diagrams and Specifications

FIGURE 10-2: EXTERNAL CLOCK TIMING - PIC16CR54A

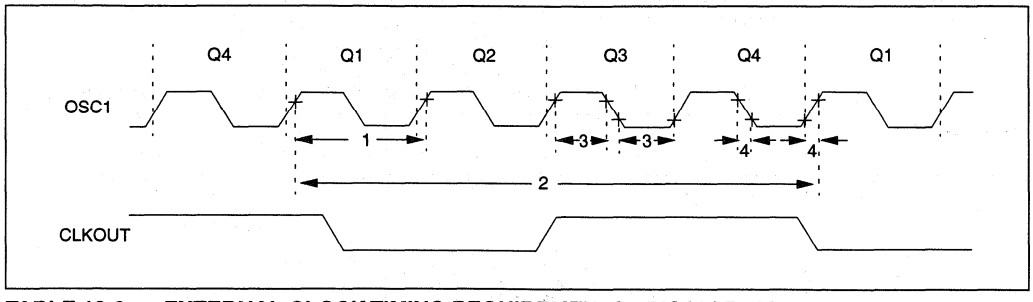

TABLE 10-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 10-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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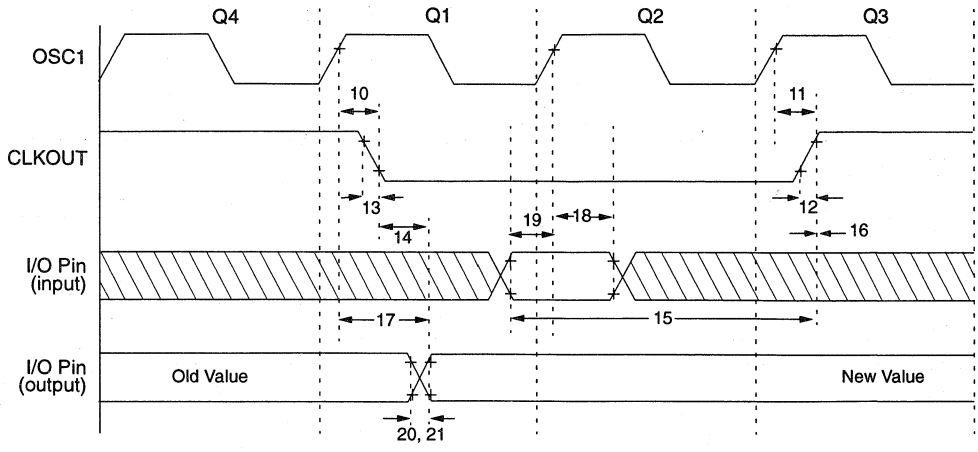
FIGURE 10-3: CLKOUT AND I/O TIMING - PIC16CR54A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

4

TABLE 10-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2iol	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

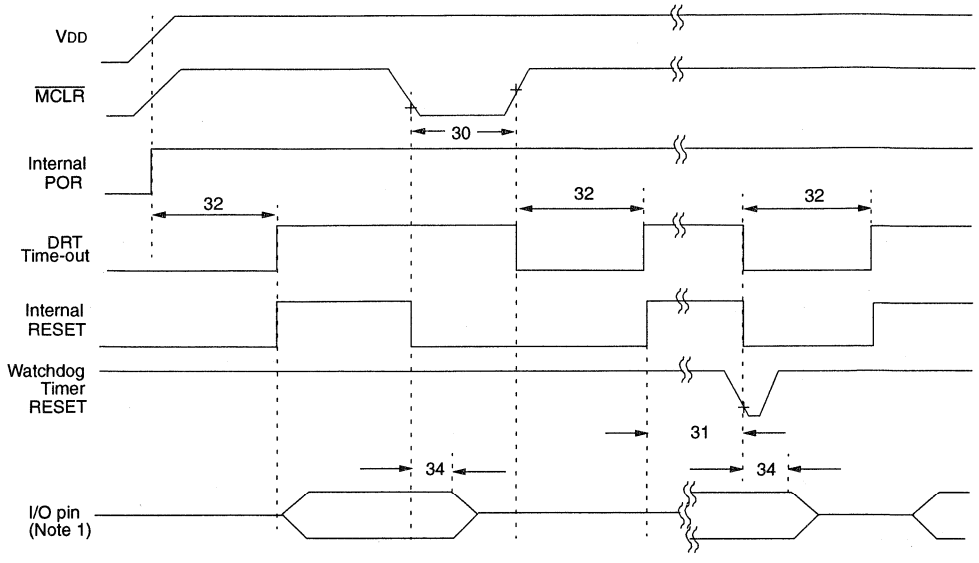
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 10-1 for loading conditions.

FIGURE 10-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 10-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
−40°C ≤ TA ≤ +85°C (industrial),
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	TioZ	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	1.0*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 10-5: TIMER0 CLOCK TIMINGS - PIC16CR54A

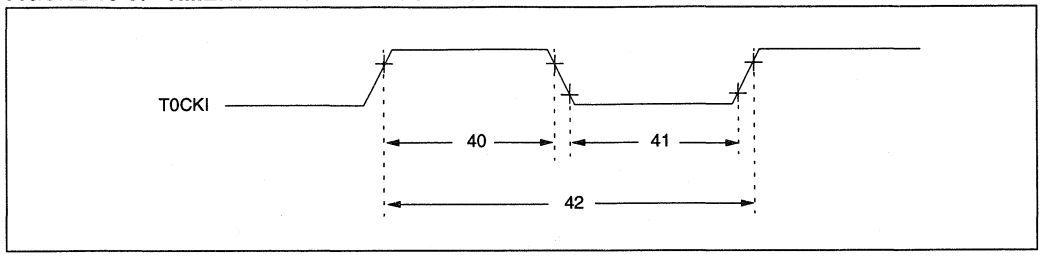

TABLE 10-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

4

NOTES:

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APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to proper value for processor used.
6. Remove any use of the ADDLW and SUBLW instructions.
7. Rewrite any code segments that use interrupts.

APPENDIX B: WHAT'S NEW

B.1 Format

The format of this data sheet has been changed to be consistent with other product families. This ensures that important topics are covered across all PIC16/17 families. Here is an overview list of new features:

- Data Sheet Structure / Outline
- Consistent Figures and Tables

B.2 Additions

Items that have been added to this data sheet are:

- PIC16CR54A data
- PIC16C5X-10 data
- PIC16C5X/JW package information

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APPENDIX C: WHAT'S CHANGED

Changes to this version of the PIC16C5X data sheet are:

- Correction of the 28-lead SSOP package pin-out
- Inclusion of errata sheet information

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NOTES:

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PIC16C54/55/56/57 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information (e.g., on pricing or delivery) refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Oscillator Type	Temperature Range	Package	Pattern

Device	PIC16C54, PIC16C54T[2] PIC16C55, PIC16C55T[2] PIC16C56, PIC16C56T[2] PIC16C57, PIC16C57T[2]	
Oscillator Type	RC	= Resistor Capacitor
	LP	= Low Power Crystal
	XT	= Standard Crystal/Resonator
	HS	= High Speed Crystal
	10	= 10 MHz Crystal
	b[1]	= No type for JW[3] devices
Temperature Range	b[1]	= 0°C to +70°C (Commercial)
	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Automotive)
Package	JW	= Windowed CERDIP
	P	= PDIP
	S	= Die in Waffle Pack
	SO	= SOIC (Gull Wing, 300 mil body)
	SP	= Skinny PDIP (28 pin, 300 mil body)
	SS	= SSOP (209 mil body)
Pattern	3-digit Pattern Code for QTP (blank otherwise)	

Examples:

a) PIC16C54 - XT/PXXX = "XT" oscillator, commercial temp., PDIP, QTP pattern.

b) PIC16C55 - XTI/SO = "XT" oscillator, industrial temp., SOIC (OTP device)

c) PIC16C55 /JW = Commercial temp. CERDIP with window.

d) PIC16C57 - RC/S = "RC" oscillator, commercial temp., dice in waffle pack.

Note 1: b = blank
2: T = in tape and reel - SOIC, SSOP packages only.
3: UV erasable devices are tested to all available voltage/frequency options. Erased devices are oscillator type RC. The user can select RC, LP, XT or HS oscillators by programming the appropriate configuration bits.

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PIC16CR54A PRODUCT IDENTIFICATION SYSTEM

To order or obtain information (e.g., on pricing or delivery) refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Oscillator Type	Temperature Range	Package	Pattern

Device	PIC16CR54A, PIC16CR54AT[2]	
Oscillator Type	RC	= Resistor Capacitor
	LP	= Low Power Crystal
	XT	= Standard Crystal/Resonator
	HS	= High Speed Crystal
	10	= 10 MHz Crystal
Temperature Range	b[1]	= 0°C to +70°C (Commercial)
	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Automotive)
Package	P	= PDIP
	S	= Die in Waffle Pack
	SO	= SOIC (Gull Wing, 300 mil body)
	SS	= SSOP (209 mil body)
Pattern	3-digit Pattern Code for ROM (blank otherwise)	

Examples:

a) PIC16CR54A - XT/P169 = "XT" oscillator, commercial temp., PDIP with ROM pattern 169.

b) PIC16CR54A - LP I/SO592 = "LP" oscillator, industrial temp., SOIC device with ROM code 592.

Note 1: b = blank
2: T = in tape and reel - SOIC, SSOP packages only.

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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MICROCHIP

SECTION 5
ENHANCED PIC16C5X MICROCONTROLLER PRODUCT SPECIFICATIONS

Enhanced PIC16C5X EPROM/ROM-Based 8-Bit CMOS Microcontroller Series 5-1
Enhanced PIC16LV5X EPROM-Based 8-Bit CMOS Microcontroller Series 5-121

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ENHANCED PIC16C5X

EPROM/ROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16C52
- PIC16C54A
- PIC16CR57B
- PIC16C58A
- PIC16CR58A

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

Device	Pins	I/O	EPROM/ ROM	RAM
PIC16C52	18	12	384	25
PIC16C54A	18	12	512	25
PIC16CR57B	28	20	2K	72
PIC16C58A	18	12	2K	73
PIC16CR58A	18	12	2K	73

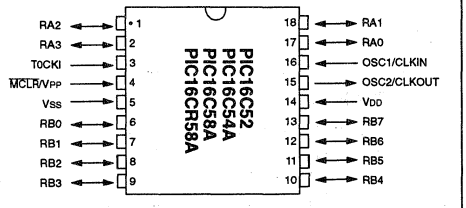
- 12-bit wide instructions
- 8-bit wide data path
- Seven or eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

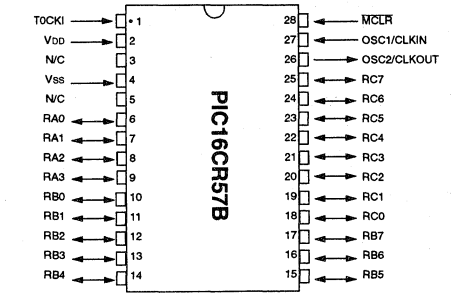
- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power saving, low frequency crystal

Pin Diagrams

PDIP, SOIC, Windowed CERDIP



PDIP, SOIC



CMOS Technology:

- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide-operating voltage range:
  - EPROM Commercial/Industrial 2.5V to 6.25V
  - ROM Commercial/Industrial 2.5V to 6.25V
  - EPROM Automotive 2.5V to 6.0V
- Low-power consumption
  - < 2 mA typical @ 5V, 4 MHz
  - 15 μA typical @ 3V, 32 kHz
  - < 0.6 μA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

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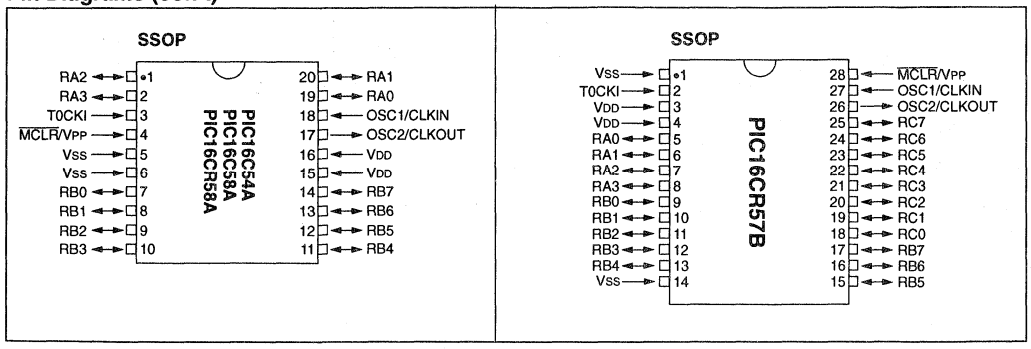
Pin Diagrams (con't)



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To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

To assist you in the use of this document, Appendix B contains a list of new information in this data sheet, while Appendix C contains information that has changed.

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1.0 GENERAL DESCRIPTION

The Enhanced PIC16C5X from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EPROM/ROM-based CMOS microcontrollers. This family is pin and software compatible with the PIC16C5X family of devices in a new enhanced process technology. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (200 ns) except for program branches which take two cycles. The Enhanced PIC16C5X delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The Enhanced PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

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TABLE 1-1: ENHANCED PIC16C5X FAMILY OF DEVICES

	Clock	Memory				Peripherals		Features		
	Maximum Frequency of Operation (MHz)	Program Memory (x12 words)	EPROM	ROM	RAM Data Memory (bytes)	Timer Module(s)	I/O Pins	Voltage Range (Volts)	Number of Instructions	Packages
PIC16C52	4	384	—	25		TMR0	12	2.5-6.25	33	18-pin DIP, SOIC
PIC16C54	20	512	—	25		TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C54A	20	512	—	25		TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR54A	20	—	512	25		TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C55	20	512	—	24		TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C56	20	1K	—	25		TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C57	20	2K	—	72		TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16CR57B	20	—	2K	72		TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C58A	20	2K	—	73		TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR58A	20	—	2K	73		TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP

Legend: Grayed boxes: devices NOT covered in this data sheet.
All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

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2.0 ENHANCED PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the Enhanced PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the Enhanced PIC16C5X family of devices, there are four device types, as indicated in the device number:

1. **C**, as in PIC16C54A. These devices have EPROM program memory and operate over the standard voltage range.
2. **LC**, as in PIC16LC54A. These devices have EPROM program memory and operate over an extended voltage range.
3. **CR**, as in PIC16CR54A. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16LCR54A. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE™ programmers both support programming of the Enhanced PIC16C5X. Third party programmers also are available; refer to the Third Party Guide for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP SM) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

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NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The igh performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200ns @ 20MHz) except for program branches.

The PIC16C52 address 384 x 12 of program memory, the PIC16C54A address 512 x 12 of program memory, and the PIC16CR57B and PIC16C58A/CR58A address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 and Table 3-2.

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FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM

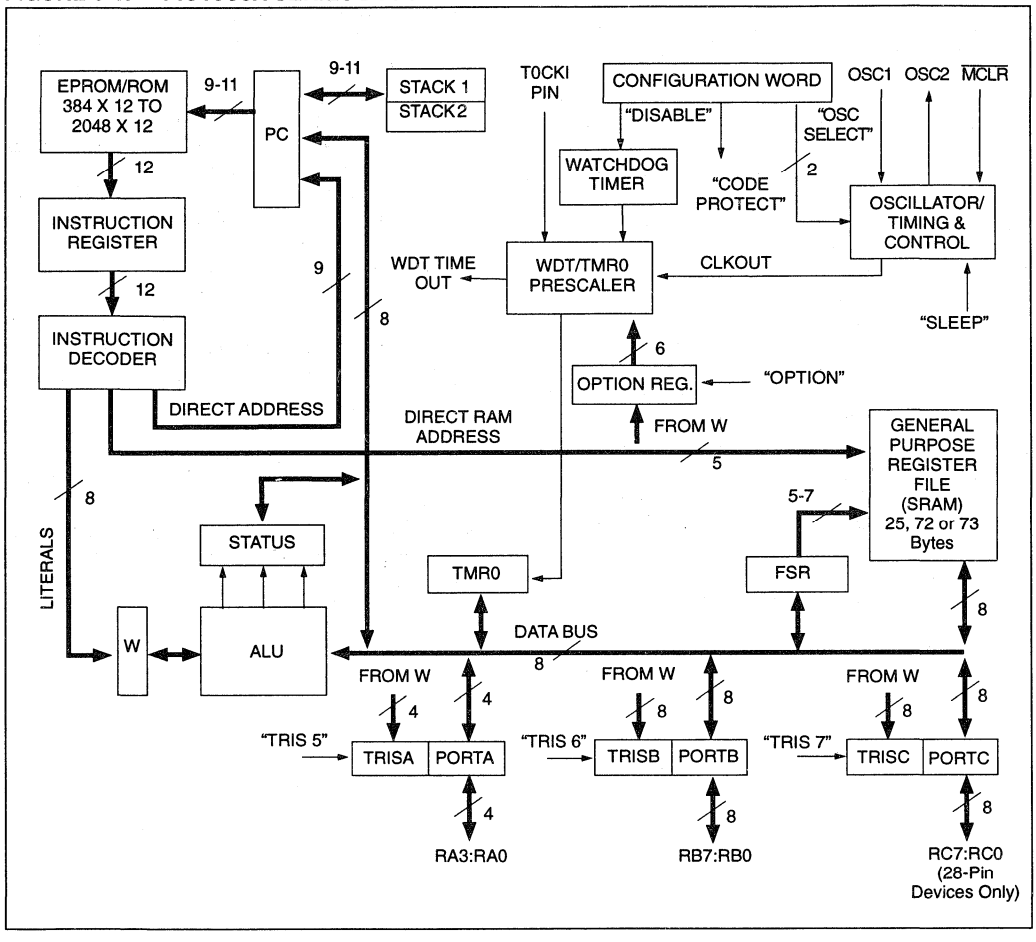

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TABLE 3-1: PINOUT DESCRIPTION - PIC16C52, PIC16C54A, PIC16C58A, PIC16CR58A

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	20	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RB0	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL	
RB7	13	14	I/O	TTL	
T0CKI	3	3	I	ST	Clock input to Timer0. Must be tied to VSS or VDD, if not in use, to reduce current consumption.
$\overline{MCLR}$/VPP	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the $\overline{MCLR}$/VPP pin must not exceed VDD to avoid unintended entering of programming mode.
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.
VSS	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used, TTL = TTL input,
ST = Schmitt Trigger input

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TABLE 3-2: PINOUT DESCRIPTION - PIC16CR57B

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	6	I/O	TTL	
RA2	8	7	I/O	TTL	
RA3	9	8	I/O	TTL	
RB0	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	10	I/O	TTL	
RB2	12	11	I/O	TTL	
RB3	13	12	I/O	TTL	
RB4	14	13	I/O	TTL	
RB5	15	15	I/O	TTL	
RB6	16	16	I/O	TTL	
RB7	17	17	I/O	TTL	
RC0	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	I/O	TTL	
RC2	20	20	I/O	TTL	
RC3	21	21	I/O	TTL	
RC4	22	22	I/O	TTL	
RC5	23	23	I/O	TTL	
RC6	24	24	I/O	TTL	
RC7	25	25	I/O	TTL	
T0CKI	1	2	I	ST	Clock input to Timer0. Must be tied to VSS or VDD if not in use to reduce current consumption.
$\overline{MCLR}$	28	28	I	ST	Master clear (reset) input. This pin is an active low reset to the device.
OSC1/CLKIN	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	2	3,4	P	—	Positive supply for logic and I/O pins.
VSS	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	—	—	—	Unused, do not connect

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used,
TTL = TTL input, ST = Schmitt Trigger input

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3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

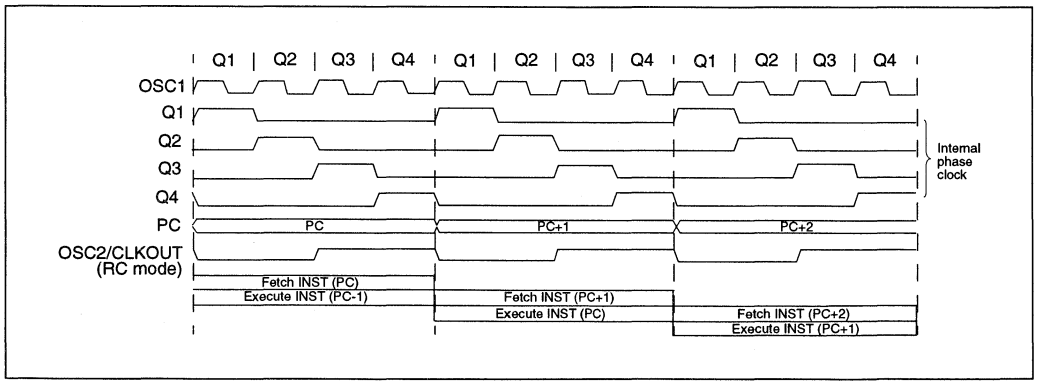
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

```
1. MOVLW 55H
2. MOVWF PORTB
3. CALL  SUB_1
4. BSF   PORTA, BIT3
```

Fetch 1	Execute 1					
	Fetch 2	Execute 2				
		Fetch 3	Execute 3			
			Fetch 4	Flush		
				Fetch SUB_1	Execute SUB_1	

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

NOTES:

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4.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

4.1 Program Memory Organization

The PIC16C52 has a 9-bit Program Counter (PC) capable of addressing a 384 x 12 program memory space (Figure 4-2). The PIC16C54A has a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 4-1). The PIC16CR57B, PIC16C58A, and PIC16CR58A have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 4-3). Accessing a location above the physically implemented address will cause a wraparound.

The reset vector for the PIC16C52 is at 17FL. A NOP at the reset vector location will cause a restart at location 000h. The reset vector for the PIC16C54A is at 1FFh, for the PIC16CR57B, PIC16C58A, and PIC16CR58A at 7FFh.

FIGURE 4-1: PIC16C54A PROGRAM MEMORY MAP AND STACK

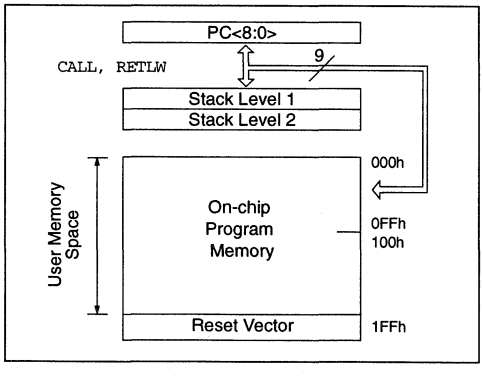


FIGURE 4-2: PIC16C52 PROGRAM MEMORY MAP AND STACK

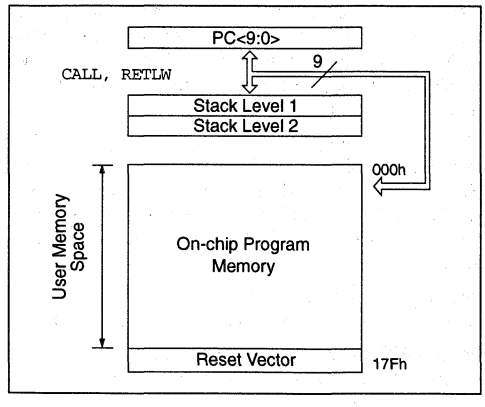
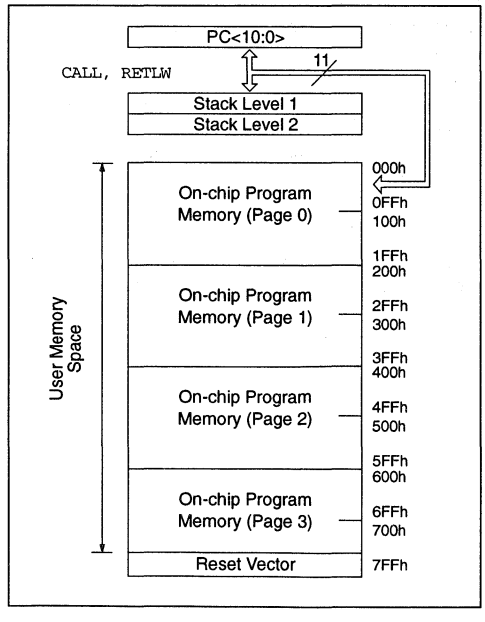


FIGURE 4-3: PIC16CR57B/C58A/CR58A PROGRAM MEMORY MAP AND STACK



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4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC16C52 and PIC16C54A, the register file is composed of 7 special function registers and 25 general purpose registers (Figure 4-4).

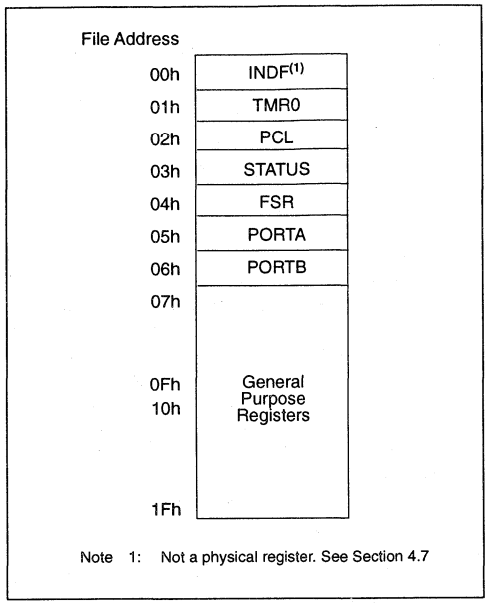
For the PIC16CR57B, the register file is composed of 8 special function registers, 24 general purpose registers and up to 48 additional general purpose registers that may be addressed using a banking scheme (Figure 4-5).

For the PIC16C58A and PIC16CR58A, the register file is composed of 7 special function registers, 25 general purpose registers and up to 48 additional general purpose registers that may be addressed using a banking scheme (Figure 4-6).

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the file select register FSR (Section 4.7).

FIGURE 4-4: PIC16C52, PIC16C54A REGISTER FILE MAP



Note 1: Not a physical register. See Section 4.7

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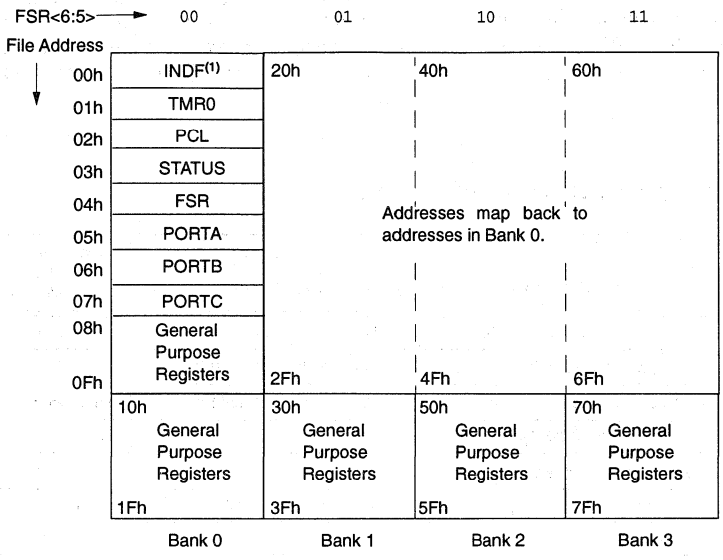
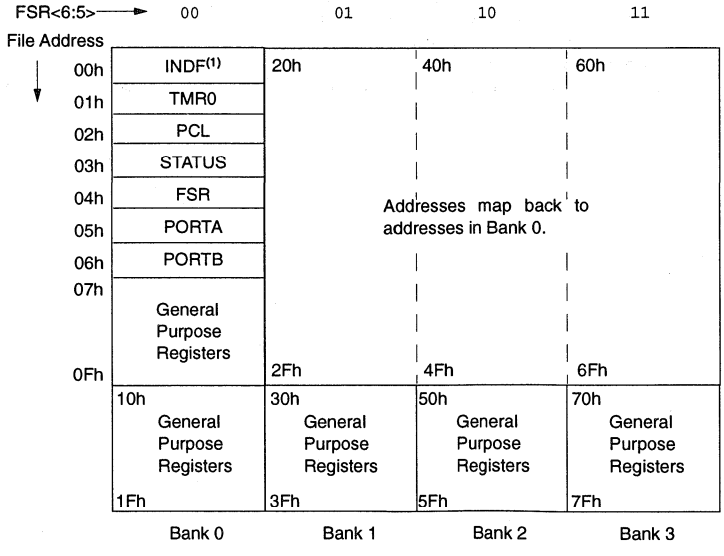
FIGURE 4-5: PIC16CR57B REGISTER FILE MAP



Note 1: Not a physical register. See Section 4.7

FIGURE 4-6: PIC16C58A/CR58A REGISTER FILE MAP



Note 1: Not a physical register. See Section 4.7

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4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h(2)	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, - = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 7.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 for an explanation of how to access these bits.

2: File address 07h is a general purpose register on the PIC16C52, PIC16C54A, PIC16C58A and PIC16CR58A.

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4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Section 13, Instruction Set Summary.

FIGURE 4-7: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **PA2**: This bit unused at this time.
Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA1:PA0**: Program page preselect bits (PIC16CR57B/C58A/CR58A)
00 = Page 0 (000h - 1FFh) - PIC16CR57B/C58A/CR58A
01 = Page 1 (200h - 3FFh) - PIC16CR57B/C58A/CR58A
10 = Page 2 (400h - 5FFh) - PIC16CR57B/C58A/CR58A
11 = Page 3 (600h - 7FFh) - PIC16CR57B/C58A/CR58A
Each page is 512 bytes.
Using the PA1:PA0 bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: $\overline{TO}$: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: $\overline{PD}$: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF	**SUBWF**	**RRF or RLF**
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

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4.4 OPTION Register

The OPTION register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<5:0> bits.

FIGURE 4-8: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented**.

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT (not implemented on PIC16C52)
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate (not implemented on PIC16C52)
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 4-9 and Figure 4-10).

For the PIC16CR57B, PIC16C58A, and PIC16CR58A, a page number must be supplied as well. Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC for the PIC16CR57B, PIC16C58A, and PIC16CR58A (Figure 4-10).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-9 and Figure 4-10).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC,5.

For the PIC16CR57B, PIC16C58A, and PIC16CR58A, a page number again must be supplied. Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC for the PIC16CR57B, PIC16C58A, and PIC16CR58A (Figure 4-10).

Note:	Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-9: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C52, PIC16C54A

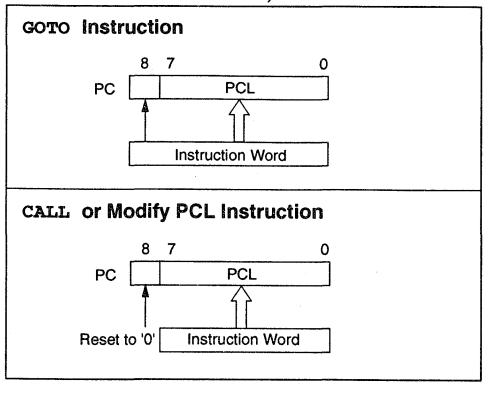
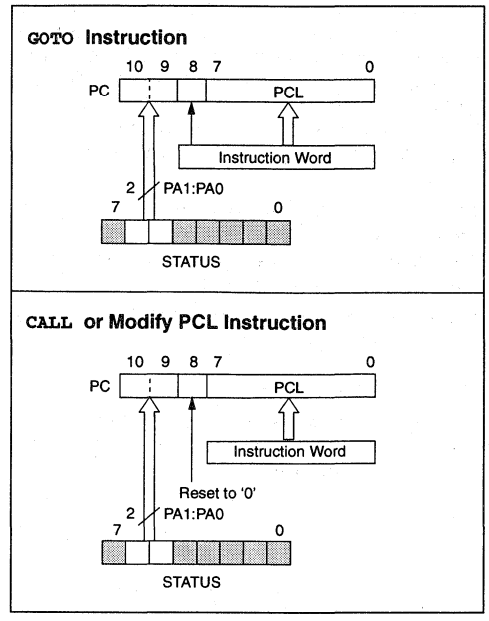


FIGURE 4-10: LOADING OF PC BRANCH INSTRUCTIONS - PIC16CR57B/C58A/CR58A



For the RETLW instruction, the PC is loaded with the Top Of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC.

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4.5.1 PAGING CONSIDERATIONS – PIC16CR57B/C58A/CR58A

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS register will not be updated. Therefore, the next GOTO, CALL, or Modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA1:PA0).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxxh on page 0 (assuming that PA1:PA0 are clear).

To prevent this, the page preselect bits must be updated under program control.

4.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the reset vector.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the reset vector location will automatically cause the program to jump to page 0.

4.6 Stack

PIC16C5X devices have a 9-bit, 10-bit or 11-bit wide, two-level hardware push/pop stack (Figure 4-1, Figure 4-2 and Figure 4-3 respectively).

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

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4.7 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x10    ;initialize pointer
        movwf   FSR     ; to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR,F   ;inc pointer
        btfsc   FSR,4   ;all done?
        goto    NEXT    ;NO, clear next
CONTINUE
        :               ;YES, continue
```

The FSR is either a 5-bit (PIC16C52, PIC16C54A), or 7-bit (PIC16CR57B, PIC16C58A, or PIC16CR58A) wide register. It is used in conjunction with the INDF register to indirectly address the data memory area. The last 2 bits, FSR<6:5>, are also used on the PIC16CR57B for direct addressing (Figure 4-11).

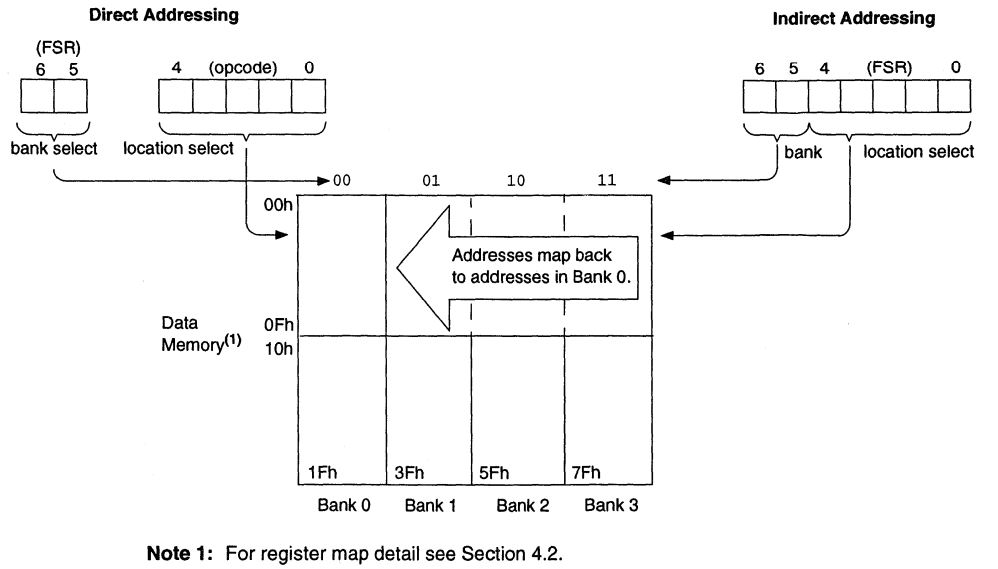
The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C52, PIC16C54A: Do not use banking. FSR<6:5> are unimplemented and read as '1's.

PIC16CR57B/C58A/CR58A: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).

5

FIGURE 4-11: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Section 4.2.

NOTES:

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5.0 I/O PORTS

As with any other register, the I/O registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB,W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

5.1 PORTA

PORTA is a 4-bit I/O register. Only the low order 4 bits are used (RA3:RA0). Bits 7-4 are unimplemented and read as '0's.

5.2 PORTB

PORTB is an 8-bit I/O register (PORTB<7:0>).

5.3 PORTC

PIC16CR57B: 8-bit I/O register.

PIC16C52/C54A/C58A/CR58A:
General purpose register.

5.4 TRIS Registers

The output driver control registers are loaded with the contents of the W register by executing the TRIS f instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

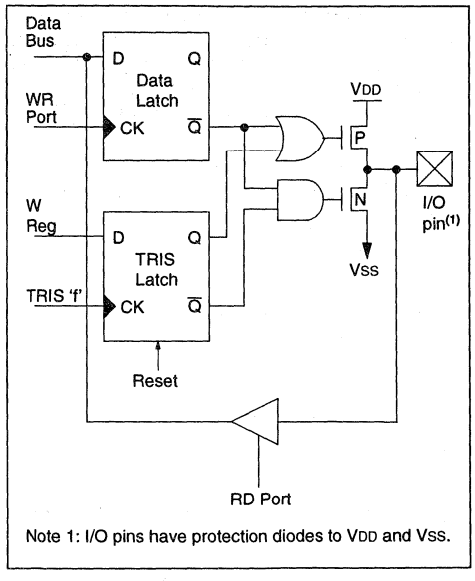
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to VDD and VSS.

5

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h(1)	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented, read as '0',
- = unimplemented, read as '0', x = unknown, u = unchanged

Note 1: File address 07h is a general purpose register on the PIC16C52/C54/C58A/CR58A.

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5.6 I/O Programming Considerations

5.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

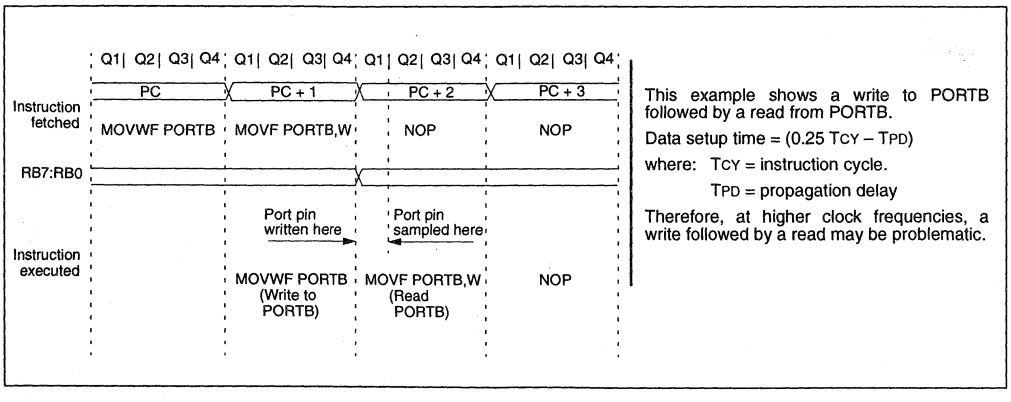
EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                    PORT latch  PORT pins
;                    ----------  ----------
  BCF   PORTB, 7    ;01pp pppp   11pp pppp
  BCF   PORTB, 6    ;10pp pppp   11pp pppp
  MOVLW 03Fh        ;
  TRIS  PORTB       ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-2: SUCCESSIVE I/O OPERATION



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6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module, while Figure 6-2 shows the electrical structure of the Timer0 input.

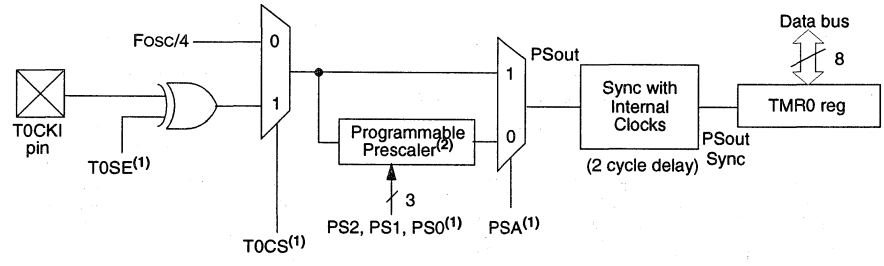
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-3 and Figure 6-4). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

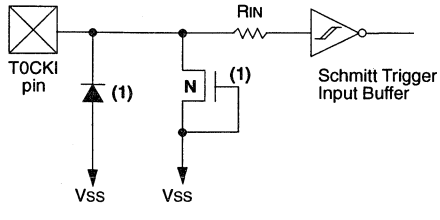
A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-6).

FIGURE 6-2: ELECTRICAL STRUCTURE OF T0CKI PIN



Note 1: ESD protection circuits

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

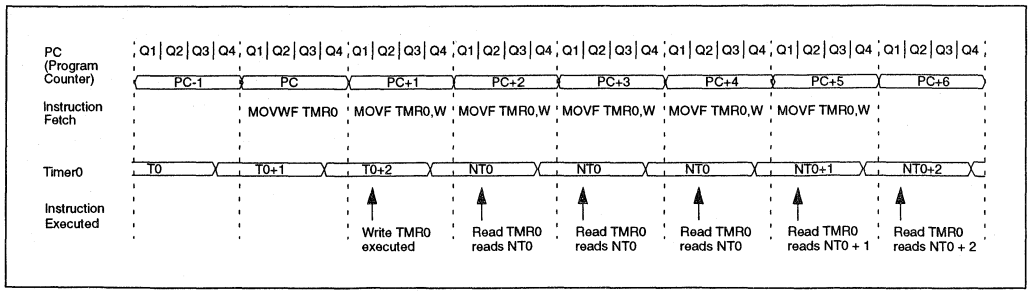


FIGURE 6-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

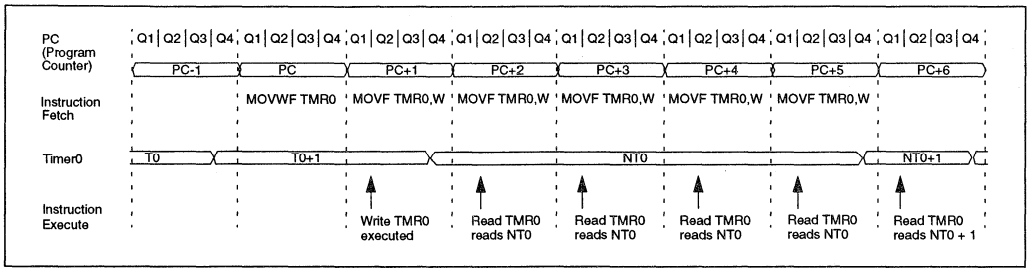


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
01	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded cells: Unimplemented bits,
- = unimplemented, x = unknown, u = unchanged,

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6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

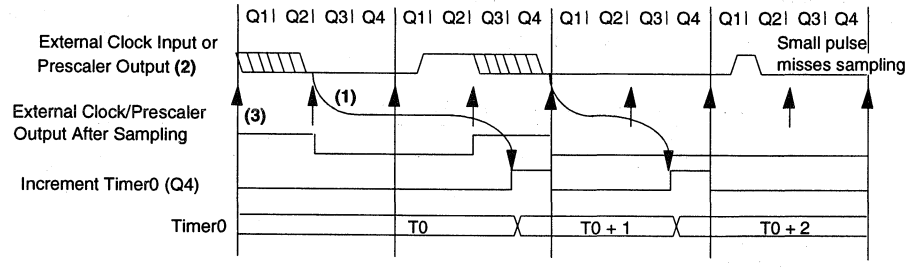
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

5

6.2 Prescaler (not implemented on PIC16C52)

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 6.1.2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

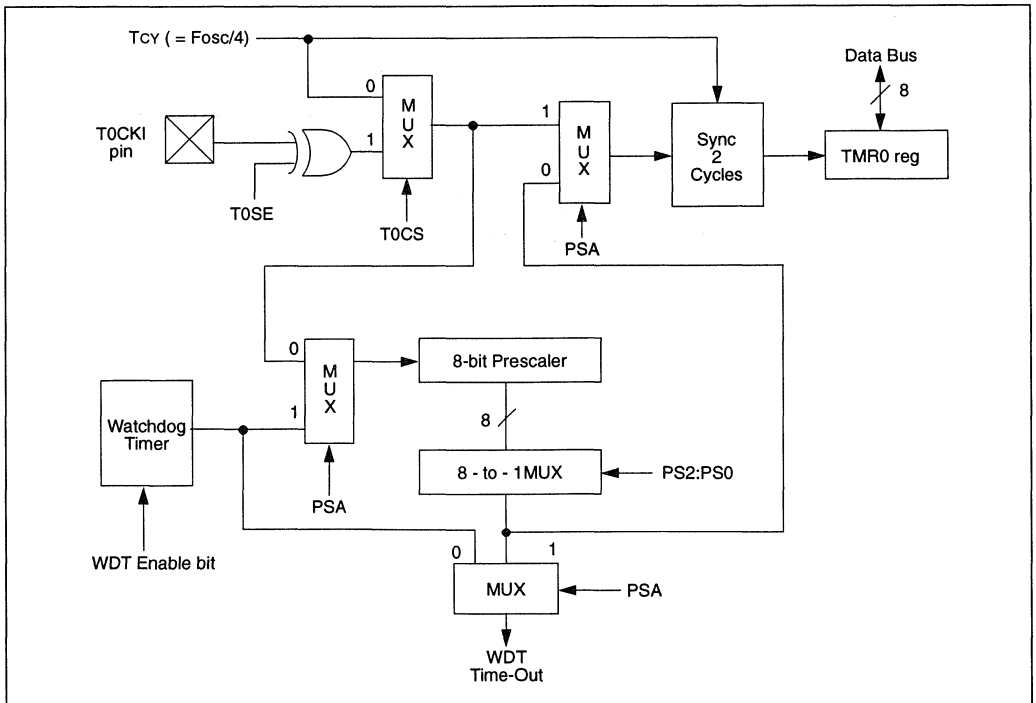
```
1. CLRWDT                ;Clear WDT
2. CLRF    TMR0          ;Clear TMR0 & Prescaler
3. MOVLW   '00xx1111'b;  ;These 3 lines (5, 6, 7)
4. OPTION                ; are required only if
                         ; desired
5. CLRWDT                ;PS<2:0> are 000 or 001
6. MOVLW   '00xx1xxx'b   ;Set Postscaler to
7. OPTION                ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                   ;Clear WDT and
                         ;prescaler
MOVLW    'xxxx0xxx'      ;Select TMR0, new
                         ;prescale value and
                         ;clock source
OPTION
```

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.
WDT not implemented on PIC16C52.

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7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16C5X family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- Reset
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) (not implemented on PIC16C52)
- SLEEP
- Code protection
- ID locations

Most PIC16C5X's have a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. With this timer on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

The PIC16C5X configuration word consists of 4 or 12 bits, depending on device configuration. Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. One bit is the code protection bit (Figure 7-1) for the PIC16C54A or PIC16C58A devices. Nine bits are code protection bits (Figure 7-2) for the PIC16CR57B or PIC16CR58B devices.

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" on the inside back cover).

5

FIGURE 7-1: CONFIGURATION WORD FOR PIC16C52/C54A/C58A

—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address(1): FFFh

bit 11-4: **Unimplemented:** Read as '0'

bit 3: **CP:** Code protection bit.
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit (not implemented on PIC16C52)
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (literature number DS30190) to determine how to access the configuration word.

FIGURE 7-2: CONFIGURATION WORD FOR PIC16CR57B/CR58A

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address(1): FFFh

bit 11-3: **CP:** Code protection bits
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (literature number DS30190) to determine how to access the configuration word.

7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

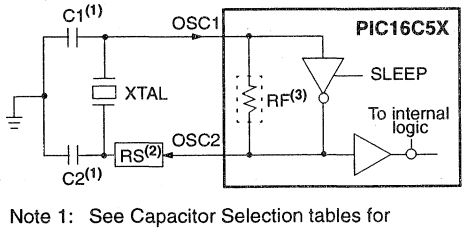
Most PIC16C5X's can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- RC: Resistor/Capacitor

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 7-3). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 7-4).

FIGURE 7-3: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen (approx. value = 10 MΩ).

FIGURE 7-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

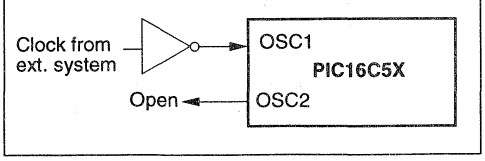


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TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - ENH. PIC16C5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - ENH. PIC16C5X

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

TABLE 7-3: CAPACITOR SELECTION FOR CERAMIC RESONATORS - ENH. PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
Data not available at this time.			

TABLE 7-4: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - ENH. PIC16CR5X

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15-33 pF	15-33 pF
	100 kHz	15-33 pF	15-33 pF
	200 kHz	15-30 pF	15-30 pF
XT	100 kHz	68-100 pF	68-100 pF
	200 kHz	15-30 pF	15-30 pF
	1 MHz	15-47 pF	15-47 pF
	2 MHz	15-47 pF	15-47 pF
	4 MHz	15-47 pF	15-47 pF
HS	4 MHz	15-47 pF	15-47 pF
	8 MHz	15-47 pF	15-47 pF
	20 MHz	15-47 pF	15-47 pF

Note 1: For VDD < 2.5V, C1 = C2 ≈ 15-33 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

PRELIMINARY

5

7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 7-5 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 7-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

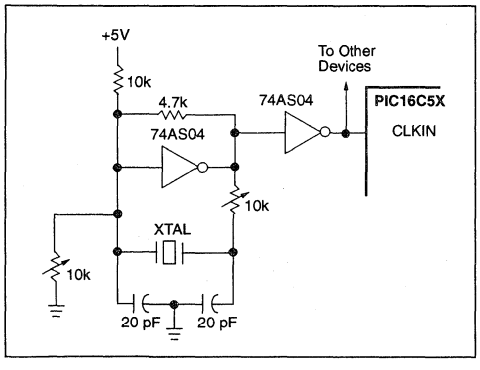
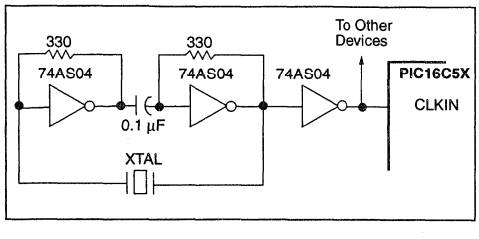


Figure 7-6 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



7.2.4 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-7 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

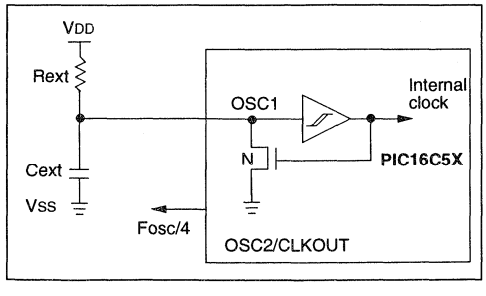
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

FIGURE 7-7: RC OSCILLATOR MODE



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7.3 Reset

PIC16C5X devices may be reset in one of the following ways:

- Power-On Reset (POR)
- $\overline{MCLR}$ reset (normal operation)
- $\overline{MCLR}$ wake-up reset (from SLEEP)
- WDT reset (normal operation)
- WDT wake-up reset (from SLEEP)

WDT not implemented on PIC16C52

Table 7-5 shows these reset conditions for the PCL and STATUS registers.

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-On Reset (POR), $\overline{MCLR}$ or WDT reset. A $\overline{MCLR}$ or WDT wake-up from SLEEP also results in a device reset, and not a continuation of operation before SLEEP.

The $\overline{TO}$ and $\overline{PD}$ bits (STATUS <4:3>) are set or cleared depending on the different reset conditions (Section 7.7). These bits may be used to determine the nature of the reset.

Table 7-6 lists a full description of reset states of all registers. Figure 7-8 shows a simplified block diagram of the on-chip reset circuit.

TABLE 7-5: RESET CONDITIONS FOR SPECIAL REGISTERS

Condition	PCL Addr: 02h	STATUS Addr: 03h
Power-On Reset	1111 1111	0001 1xxx
$\overline{MCLR}$ reset (normal operation)	1111 1111	000u uuuu(1)
$\overline{MCLR}$ wake-up (from SLEEP)	1111 1111	0001 0uuu
WDT reset (normal operation)	1111 1111	0000 1uuu(2)
WDT wake-up (from SLEEP)	1111 1111	0000 0uuu

Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.
Note 1: $\overline{TO}$ and $\overline{PD}$ bits retain their last value until one of the other reset conditions occur.
2: The CLRWDT instruction will set the $\overline{TO}$ and $\overline{PD}$ bits.

TABLE 7-6: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	$\overline{MCLR}$ or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL(1)	02h	1111 1111	1111 1111
STATUS(1)	03h	0001 1xxx	000q quuu
FSR	04h	1xxx xxxx	1uuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC(2)	07h	xxxx xxxx	uuuu uuuu
General Purpose register files	08-7Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0',
q = see tables in Section 7.7 for possible values.
Note 1: See Table 7-5 for reset value for specific conditions.
2: General purpose register file on the PIC16C52/C54/C56.

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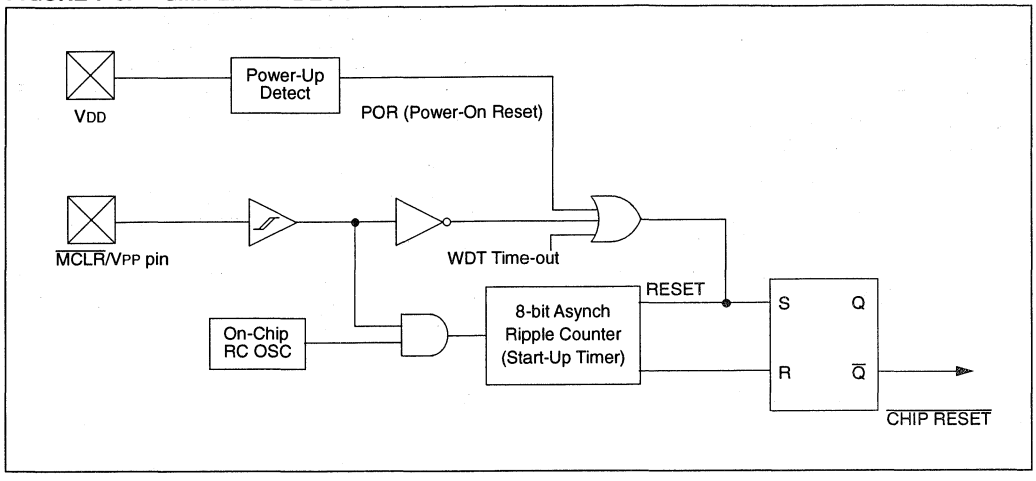
FIGURE 7-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



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7.4 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations. To use this feature, the user merely ties the $\overline{MCLR}$/VPP pin (Figure 7-9) to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 7-8.

The Power-On Reset circuit and the Device Reset Timer (Section 7.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

A power-up example where $\overline{MCLR}$ is not tied to VDD is shown in Figure 7-11. VDD is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset TDRT msec after $\overline{MCLR}$ goes high.

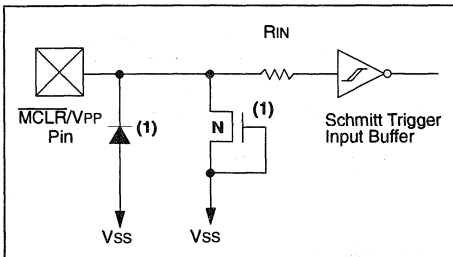
In Figure 7-12, the on-chip Power-On Reset feature is being used ($\overline{MCLR}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 7-13 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the $\overline{MCLR}$/VPP pin, and when the $\overline{MCLR}$/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 7-10).

Note:	When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

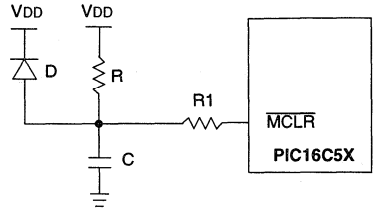
The POR circuit does not produce an internal reset when VDD declines.

FIGURE 7-9: ELECTRICAL STRUCTURE OF $\overline{MCLR}$/VPP PIN



Note 1: ESD protection circuits

FIGURE 7-10: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

5

FIGURE 7-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD)

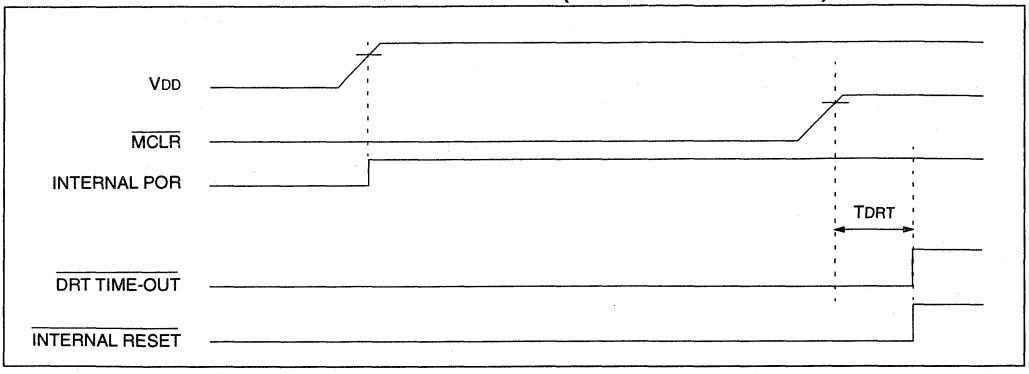


FIGURE 7-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD): FAST VDD RISE TIME

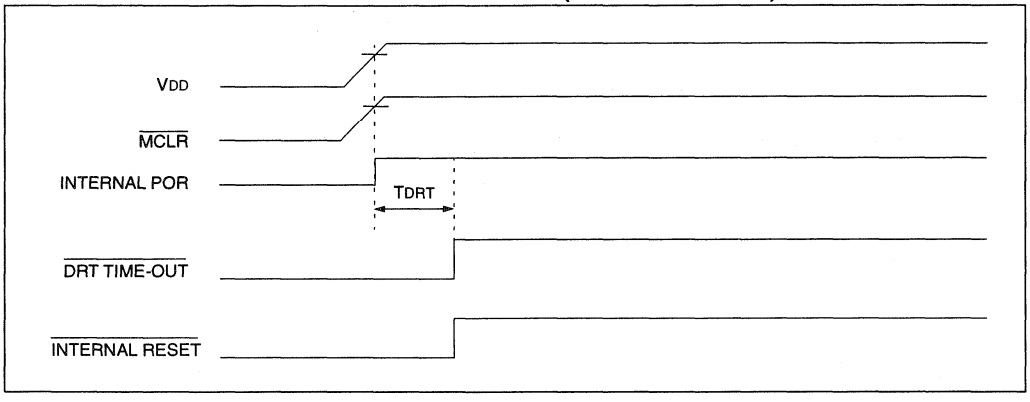
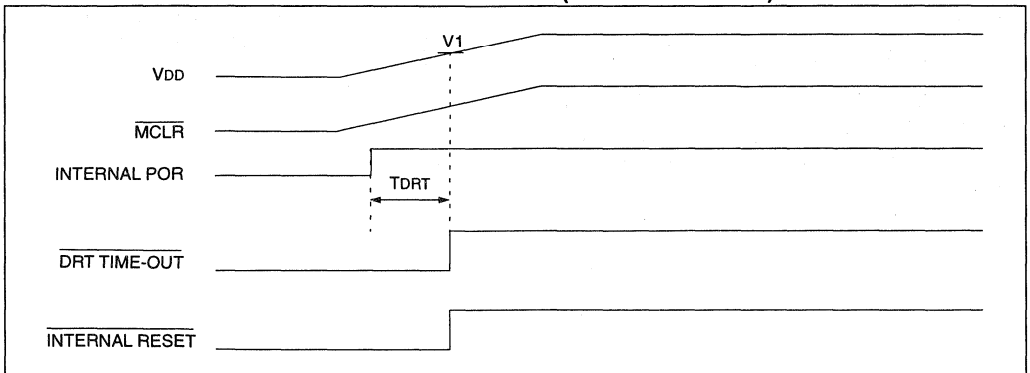


FIGURE 7-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD): SLOW VDD RISE TIME



When VDD rises slowly, the TDRT time-out expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ VDD min.

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7.5 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides a fixed 18 ms nominal time-out on reset. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the $\overline{MCLR}$/VPP pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the $\overline{MCLR}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

7.6 Watchdog Timer (WDT) (not implemented on PIC16C52)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC16C5X Programming Specifications (literature number DS30190) to determine how to access the configuration word.

7.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

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FIGURE 7-14: WATCHDOG TIMER BLOCK DIAGRAM

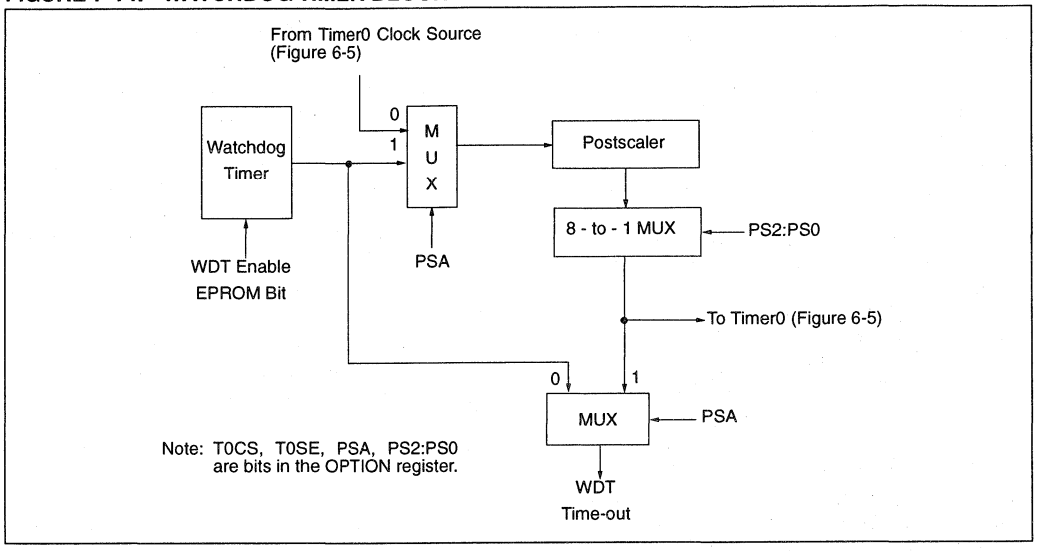

TABLE 7-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded boxes = Not used by Watchdog Timer,
– = unimplemented, read as '0', u = unchanged

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7.7 Time-Out Sequence and Power Down Status Bits (TO/PD)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) reset, or a $\overline{MCLR}$ or WDT wake-up reset.

TABLE 7-8: $\overline{TO}/\overline{PD}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-up (POR)
u	u	$\overline{MCLR}$ reset (normal operation)(1)
1	0	$\overline{MCLR}$ wake-up reset (from SLEEP)
0	1	WDT reset (normal operation)
0	0	WDT wake-up reset (from SLEEP)

Legend: u = unchanged
Note 1: The $\overline{TO}$ and $\overline{PD}$ bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$ and $\overline{PD}$ status bits.

These STATUS bits are only affected by events listed in Table 7-9.

TABLE 7-9: EVENTS AFFECTING $\overline{TO}/\overline{PD}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Time-out	0	u	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Legend: u = unchanged
A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 7-8 reflects the status of $\overline{TO}$ and $\overline{PD}$ after the corresponding event.

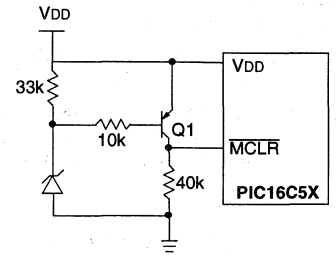
Table 7-5 lists the reset conditions for the special function registers, while Table 7-6 lists the reset conditions for all the registers.

7.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

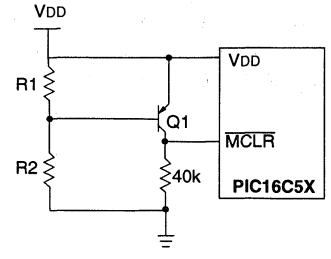
To reset PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-15 and Figure 7-16.

FIGURE 7-15: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

FIGURE 7-16: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

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7.9 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

7.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$/VPP pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or VSS and the $\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC).

7.9.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external reset input on $\overline{MCLR}$/VPP pin.
2. A Watchdog Timer time-out reset (if WDT was enabled).

Both of these events cause a device reset. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of device reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices.

7.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note:	Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

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8.0 ELECTRICAL CHARACTERISTICS - PIC16C52

Absolute Maximum Ratings†

Ambient Temperature under bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 V to +7.5 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 V to +14 V
Voltage on all other pins with respect to V_{SS} ..... −0.6 V to (V_{DD} + 0.6 V)
Total Power Dissipation(1) ..... 800 mW
Max. Current out of V_{SS} pin ..... 150 mA
Max. Current into V_{DD} pin ..... 50 mA
Max. Current into an input pin (T0CKI only) ..... ±500 µA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. Output Current sunk by any I/O pin ..... 10 mA
Max. Output Current sourced by any I/O pin ..... 10 mA
Max. Output Current sourced by a single I/O port (PORTA, B or C) ..... 10 mA
Max. Output Current sunk by a single I/O port (PORTA, B or C) ..... 10 mA

Note 1: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFORMATION

5

8.1 DC Characteristics: PIC16C52-04 (Commercial) PIC16C52-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0		6.25	V	FOSC = DC to 4 MHz
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP Mode
Supply Current(3,4)	IDD		1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5 V
Power Down Current(5)	IPD					
Commercial			0.6	9*	µA	VDD = 3.0 V
Industrial			0.6	12*	µA	VDD = 3.0 V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For RC option, does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

ADVANCE INFORMATION

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8.2 DC Characteristics: PIC16C52-04 (Commercial) PIC16C52-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 8.1.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	RC(4) option only
		VSS		0.3 VDD	V	XT option
Input High Voltage	VIH					
I/O ports		0.45 VDD		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0 V < VDD ≤ 5.5 V(5)
		0.36 VDD		VDD	V	VDD > 5.5 V
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC(4) option only
		0.7 VDD		VDD	V	XT option
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(2,3)	IIL					**For VDD ≤ 5.5 V**
I/O ports		–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5			µA	VPIN = VSS + 0.25 V
			0.5	+5	µA	VPIN = VDD
T0CKI		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, XT option
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 2.0 mA, VDD = 4.5 V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5 V, RC option
Output High Voltage	VOH					
I/O ports(3)		VDD – 0.7			V	IOH = –2.0 mA, VDD = 4.5 V
OSC2/CLKOUT		VDD – 0.7			V	IOH = –1.0 mA, VDD = 4.5 V, RC option

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C52 be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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8.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

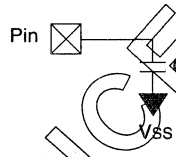
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 8-1: LOAD CONDITIONS - PIC16C52



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT mode when external clock is used to drive OSC1

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8.4 Timing Diagrams and Specifications

FIGURE 8-2: EXTERNAL CLOCK TIMING - PIC16C52

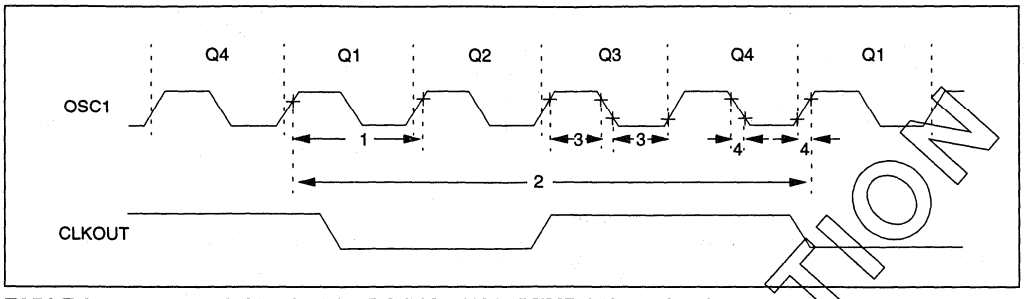

TABLE 8-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C52

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 8.1.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4	MHz	RC osc mode
			DC	—	4	MHz	XT osc mode
		Oscillator Frequency(2)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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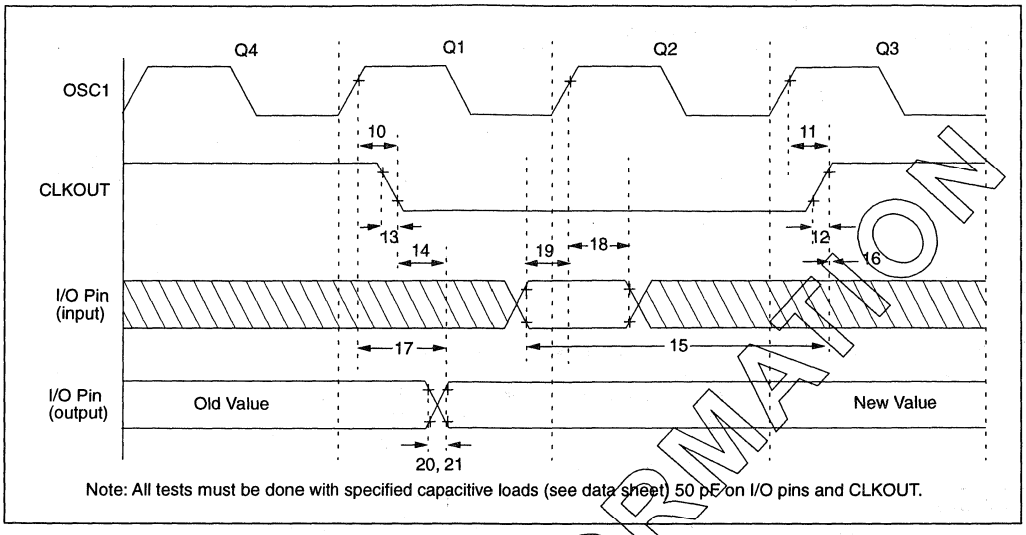
FIGURE 8-3: CLKOUT AND I/O TIMING - PIC16C52



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 8-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C52

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), -40°C ≤ TA ≤ +85°C (industrial), Operating Voltage VDD range is described in Section 8.1.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5	15**	ns
13	TckF	CLKOUT fall time(2)	—	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 8-1 for loading conditions.

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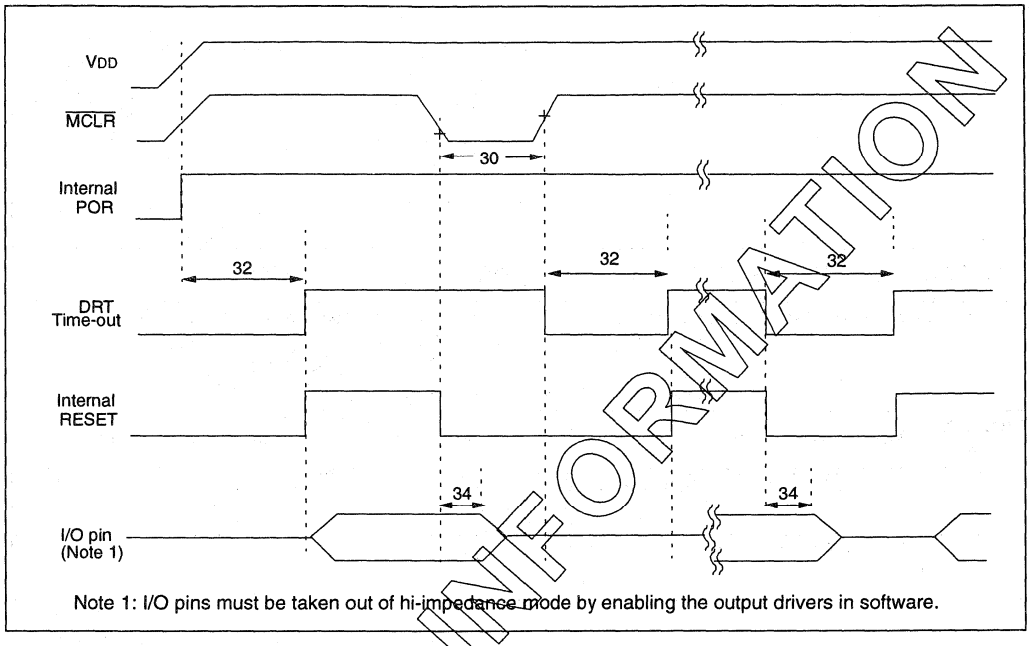
FIGURE 8-4: RESET AND DEVICE RESET TIMER TIMING - PIC16C52



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 8-3: RESET AND DEVICE RESET TIMER - PIC16C52

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), Operating Voltage VDD range is described in Section 8.1.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	MCLR Pulse Width (low)	100*	—	—	ns	VDD = 5 V
32	TDRT	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5 V (Commercial)
34	TioZ	I/O Hi-impedance from MCLR Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 8-5: TIMER0 CLOCK TIMINGS - PIC16C52

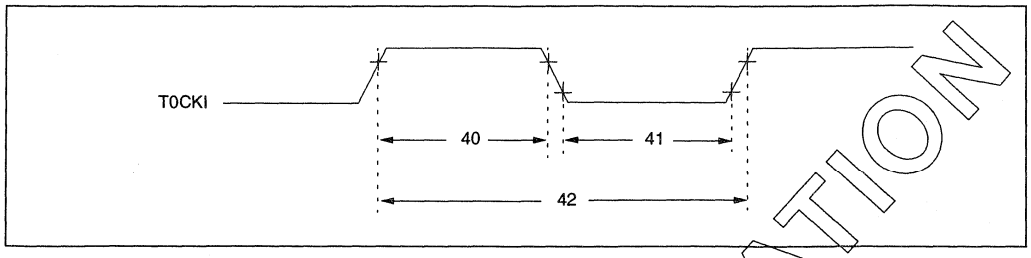

TABLE 8-4: TIMER0 CLOCK REQUIREMENTS - PIC16C52

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), Operating Voltage VDD range is described in Section 8.1.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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9.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings†

Ambient temperature under bias ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)
Total power dissipation (1) ..... 800 mW
Max. current out of V_{SS} pin ..... 150 mA
Max. current into V_{DD} pin ..... 100 mA
Max. current into an input pin (T0CKI only) ..... ±500 µA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 20 mA
Max. output current sourced by a single I/O port (PORTA or B) ..... 40 mA
Max. output current sunk by a single I/O port (PORTA or B) ..... 50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5

TABLE 9-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C54A-04	PIC16C54A-10	PIC16C54A-20	PIC16LC54A-04	PIC16C54A/JW
RC	VDD: 3.0V to 6.25V IDD: 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 2.4 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 8.0 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 16 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 8 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 10 MHz max.
LP	VDD: 3.0V to 6.25V IDD: 14 µA typ. at 32kHz, 3.0V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.25V IDD: 27 µA max. at 32kHz, 2.5V WDT dis IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.	VDD: 2.5V to 6.25V IDD: 27 µA max. at 32kHz, 2.5V WDT dis IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

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9.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT, RC and LP options		3.0		6.25	V	
HS option		4.5		5.5	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current(3)	IDD					
XT and RC(4) options			1.8	2.4	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option			2.4	8.0	mA	FOSC = 10 MHz, VDD = 5.5V
			4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V
LP option, Commercial			14		µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
LP option, Industrial			17		µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5)	IPD					
Commercial			4.0	12	µA	VDD = 3.0V, WDT enabled
			0.25	4.0	µA	VDD = 3.0V, WDT disabled
Industrial			5.0	14	µA	VDD = 3.0V, WDT enabled
			0.3	5.0	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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9.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Automotive)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C (automotive)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT and RC options		3.5		5.5	V	
HS option		4.5		5.5	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current(3)	IDD					
XT and RC(4) options			1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
Power Down Current(5)	IPD					
XT and RC options			5.0	22	µA	VDD = 3.5V, WDT enabled
			0.8	18	µA	VDD = 3.5V, WDT disabled
HS option			4.0	22	µA	VDD = 3.5V, WDT enabled
			0.25	18	µA	VDD = 3.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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9.3 DC Characteristics: PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial) PIC16LC54A-04E (Automotive)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT and RC options		3.0		6.25	V	
LP options		2.5		6.25	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current(3)	IDD					
XT and RC(4) options			0.5		mA	FOSC = 4.0 MHz, VDD = 5.5V
LP option, Commercial			11	27	µA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
LP option, Industrial			14	35	µA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
Power Down Current(5)	IPD					
Commercial			2.5	12	µA	VDD = 2.5V, WDT enabled
			0.25	4.0	µA	VDD = 2.5V, WDT disabled
Industrial			3.5	14	µA	VDD = 2.5V, WDT enabled
			0.3	5.0	µA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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9.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I (Industrial) PIC16C54A-04E, 10E, 20E (Automotive)

DC Characteristics
All Pins Except
Power Supply Pins

Standard Operating Conditions (unless otherwise specified)
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
−40°C ≤ TA ≤ +85°C (industrial)
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 9.1, Section 9.2 and Section 9.3.

Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	RC option only(4)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.2 VDD+1V		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V(5)
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC option only(4)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		-5.0		+5.0	µA	VPIN = VSS +0.25V(2)
			0.5	+3.0	µA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5		µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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9.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

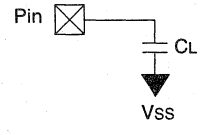
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{MCLR}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 9-1: LOAD CONDITIONS - PIC16C54A



CL = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

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9.6 Timing Diagrams and Specifications

FIGURE 9-2: EXTERNAL CLOCK TIMING - PIC16C54A

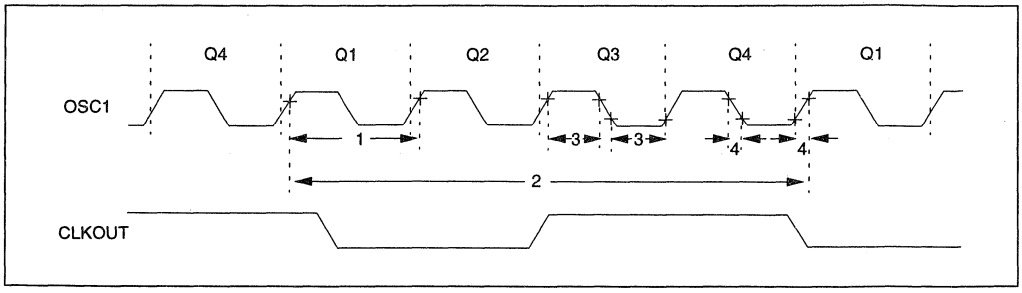

TABLE 9-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 9.1, Section 9.2 and Section 9.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4	—	4.0	MHz	HS osc mode (04)
			4	—	10	MHz	HS osc mode (10)
			4	—	20	MHz	HS osc mode (20)
			5	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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TABLE 9-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 9.1, Section 9.2 and Section 9.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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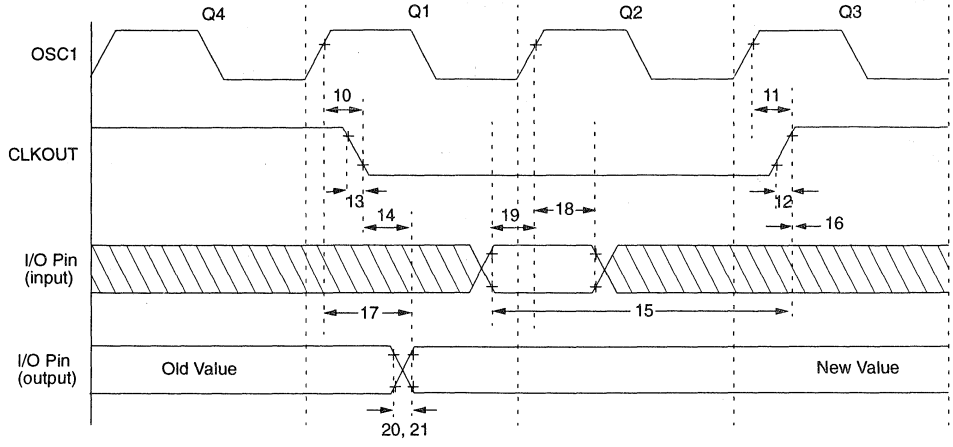
FIGURE 9-3: CLKOUT AND I/O TIMING - PIC16C54A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 9-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
−40°C ≤ TA ≤ +85°C (industrial),
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 9.1, Section 9.2 and Section 9.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2iol	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 9-1 for loading conditions.

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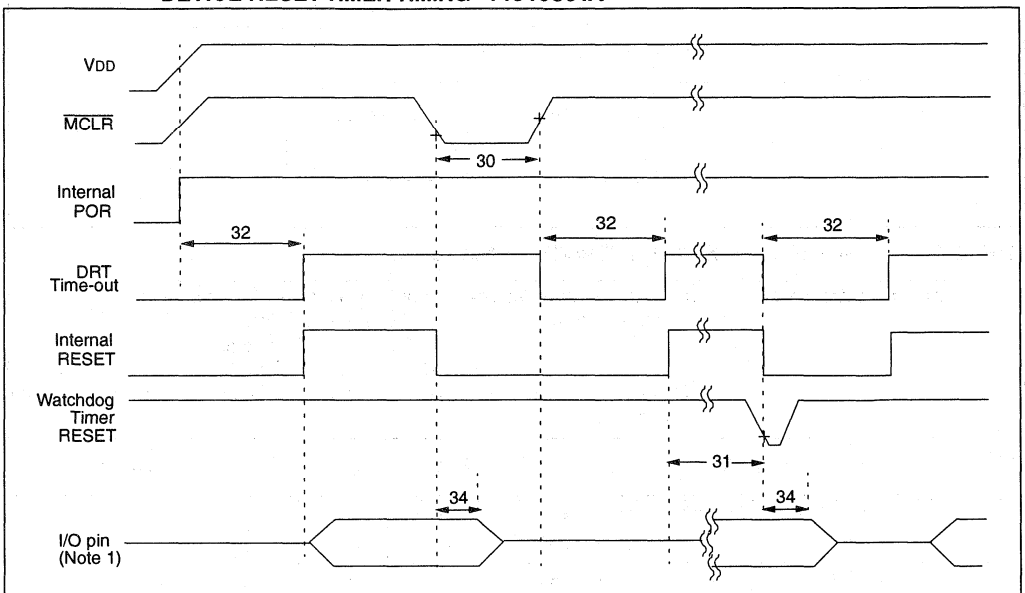
FIGURE 9-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 9-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 9.1, Section 9.2 and Section 9.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 9-5: TIMER0 CLOCK TIMINGS - PIC16C54A

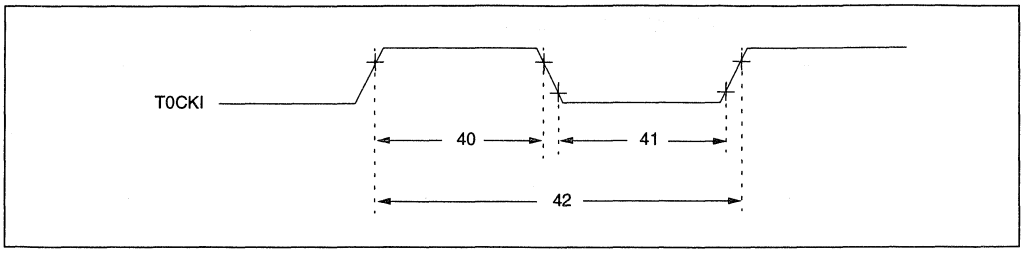


TABLE 9-5: TIMER0 CLOCK REQUIREMENTS - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 9.1, Section 9.2 and Section 9.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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10.0 ELECTRICAL CHARACTERISTICS - PIC16CR57B

Absolute Maximum Ratings†

Ambient Temperature under bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)
Total Power Dissipation (1) ..... 800 mW
Max. Current out of V_{SS} pin ..... 150 mA
Max. Current into V_{DD} pin ..... 100 mA
Max. Current into an input pin (T0CKI only) ..... ±500 µA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. Output Current sunk by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin ..... 20 mA
Max. Output Current sourced by a single I/O port
  PORTA ..... 50 mA
  PORTB or C ..... 100 mA
Max. Output Current sunk by a single I/O port
  PORTA ..... 50 mA
  PORTB or C ..... 100 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100Ω should be used when applying a low level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

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TABLE 10-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR57B-04	PIC16CR57B-10	PIC16CR57B-20	PIC16LCR57B-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
XT	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	VDD: 4.5V to 5.5V IDD: 10 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 10 MHz max	VDD: 4.5V to 5.5V IDD: 20 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	VDD: 2.5V to 6.25V IDD: 32 µA max at 32 kHz, 2.5V IPD: 4.0 µA max at 2.5V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

PRELIMINARY

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10.1 DC Characteristics: PIC16CR57B-04, 10, 20 (Commercial) PIC16CR57B-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
RC and XT options		3.0		6.25	V	
HS option		4.5		5.5	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
RC(4) and XT options			1.9	2.5	mA	FOSC = 4 MHz, VDD = 5.5V
HS option			2.5	8.0	mA	FOSC = 10 MHz, VDD = 5.5V
			4.7	17	mA	FOSC = 20 MHz, VDD = 5.5V
Power-Down Current(5)	IPD					
Commercial			4.0	12	µA	VDD = 3.0V, WDT enabled
			0.25	4.0	µA	VDD = 3.0V, WDT disabled
Industrial			5.0	14	µA	VDD = 3.0V, WDT enabled
			0.3	5.0	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

PRELIMINARY

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10.2 DC Characteristics: PIC16CR57B-04E, 10E, 20E (Automotive)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C (automotive)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS options	VDD	 3.25 4.5		 6.0 5.5	 V V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD		 1.9 4.8 9.0	 3.3 10 20	 mA mA mA	 FOSC = 4 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V
Power-Down Current(5)	IPD		 5.0 0.8	 22 18	 µA µA	 VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

PRELIMINARY

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10.3 DC Characteristics: PIC16LCR57B-04 (Commercial) PIC16LCR57B-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5		6.25	V	LP option
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
Commercial			12	28	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Industrial			15	37	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power-Down Current(5)	IPD					
Commercial			4.0	12	µA	VDD = 2.5V, WDT enabled
			0.25	4.0	µA	VDD = 2.5V, WDT disabled
Industrial			5.0	14	µA	VDD = 2.5V, WDT enabled
			0.3	5.0	µA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

PRELIMINARY

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10.4 DC Characteristics: PIC16CR57B-04, 10, 20, PIC16LCR57B-04 (Commercial) PIC16CR57B-04I, 10I, 20I, PIC16LCR57B-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1 and Section 10.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	RC option only(4)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD		VDD	V	VDD > 5.5V
$\overline{MCLR}$ (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC option only(4)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0		+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$		–5.0			µA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage(3)	VOH					
I/O ports		VDD –0.7			V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7			V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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10.5 DC Characteristics: PIC16CR57B-04E, 10E, 20E (Automotive)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40°C \le T_A \le +125°C$ Operating Voltage V_{DD} range is described in Section 10.2.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	V_{IL}					
I/O ports		V_{SS}		0.2 V_{DD}	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		V_{SS}		0.15 V_{DD}	V	
T0CKI (Schmitt Trigger)		V_{SS}		0.15 V_{DD}	V	
OSC1 (Schmitt Trigger)		V_{SS}		0.15 V_{DD}	V	RC option only(4)
OSC1		V_{SS}		0.3 V_{DD}	V	XT, HS and LP options
Input High Voltage	V_{IH}					
I/O ports		0.45 V_{DD}		V_{DD}	V	For all V_{DD}(5)
		2.0		V_{DD}	V	$4.0V < V_{DD} \le 5.5V$(5)
		0.36 V_{DD}		V_{DD}	V	$V_{DD} > 5.5V$
$\overline{MCLR}$ (Schmitt Trigger)		0.85 V_{DD}		V_{DD}	V	
T0CKI (Schmitt Trigger)		0.85 V_{DD}		V_{DD}	V	
OSC1 (Schmitt Trigger)		0.85 V_{DD}		V_{DD}	V	RC option only(4)
OSC1		0.7 V_{DD}		V_{DD}	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	V_{HYS}	0.15V_{DD}*			V	
Input Leakage Current(3)	I_{IL}					**For $V_{DD} \le 5.5V$**
I/O ports		–1.0		+1.0	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at hi-impedance
$\overline{MCLR}$		–5.0			µA	$V_{PIN} = V_{SS} + 0.25\ V$(2)
			0.5	+5.0	µA	$V_{PIN} = V_{DD}$(2)
T0CKI		–3.0	0.5	+3.0	µA	$V_{SS} \le V_{PIN} \le V_{DD}$
OSC1		–3.0	0.5	+3.0	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, XT, HS and LP options
Output Low Voltage	V_{OL}					
I/O ports				0.6	V	I_{OL} = 8.7 mA, V_{DD} = 4.5V
OSC2/CLKOUT				0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, RC option only
Output High Voltage(3)	V_{OH}					
I/O ports		V_{DD} –0.7			V	I_{OH} = –5.4 mA, V_{DD} = 4.5V
OSC2/CLKOUT		V_{DD} –0.7			V	I_{OH} = –1.0 mA, V_{DD} = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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10.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

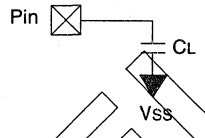
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 10-1: LOAD CONDITIONS



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

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10.7 Timing Diagrams and Specifications

FIGURE 10-2: EXTERNAL CLOCK TIMING - PIC16CR57B

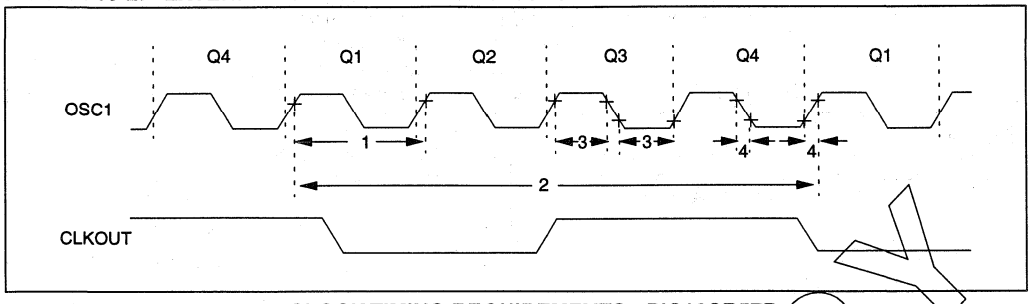

TABLE 10-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR57B

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
−40°C ≤ TA ≤ +85°C (industrial),
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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TABLE 10-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR57B (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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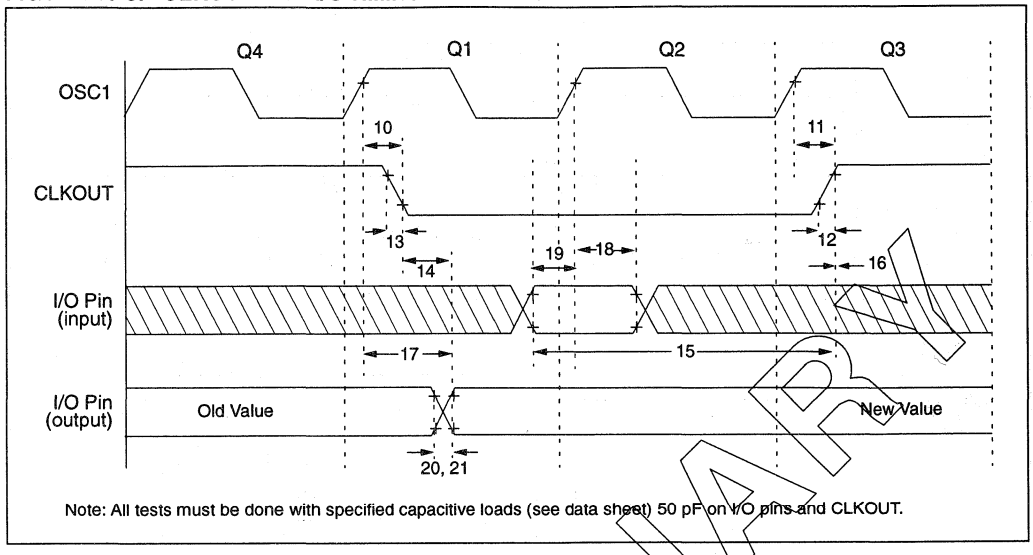
FIGURE 10-3: CLKOUT AND I/O TIMING - PIC16CR57B



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 10-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR57B

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
-40°C ≤ TA ≤ +85°C (industrial),
-40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.
** These parameters are design targets and are not tested. No characterization data available at this time.
Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
3: See Figure 10-1 for loading conditions.

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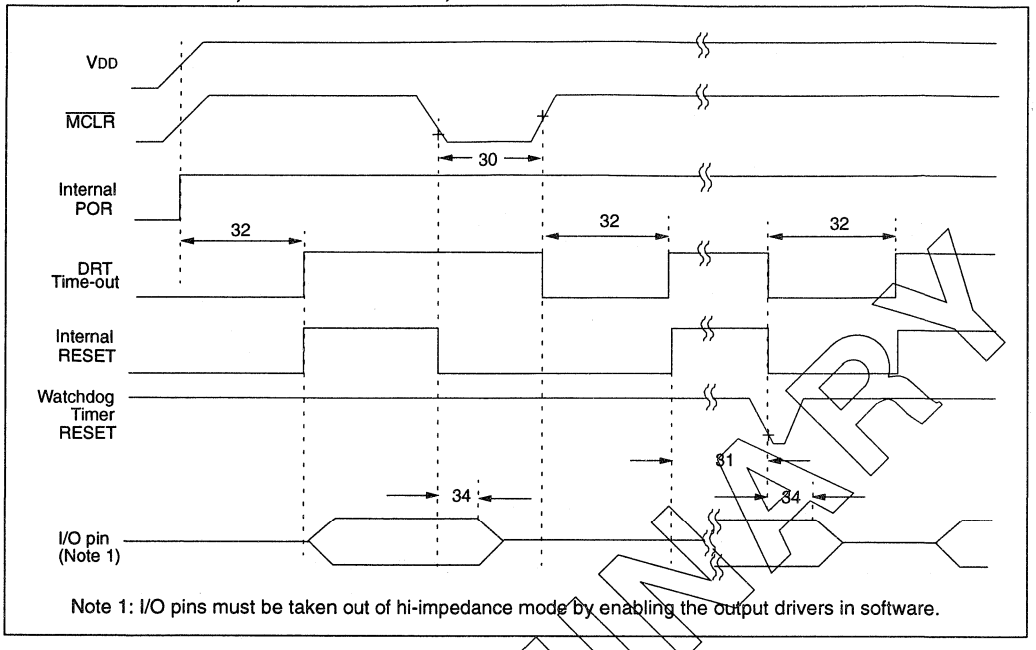
FIGURE 10-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR57B



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 10-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR57B

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
−40°C ≤ TA ≤ +85°C (industrial),
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	1.0*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 10-5: TIMER0 CLOCK TIMINGS - PIC16CR57B

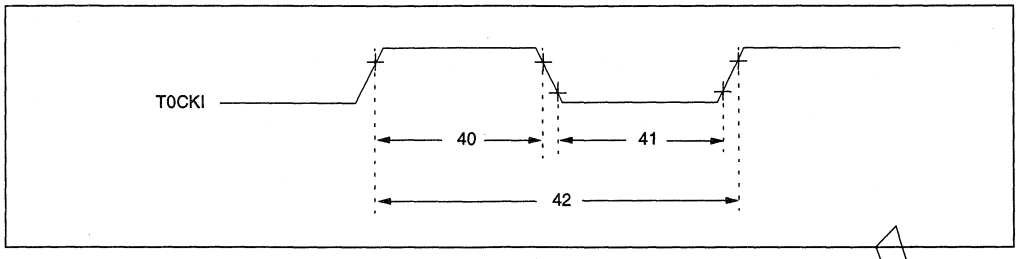

TABLE 10-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR57B

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or TCY + 40* / N	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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NOTES:

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11.0 ELECTRICAL CHARACTERISTICS - PIC16C58A

Absolute Maximum Ratings†

Ambient Temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)
Total Power Dissipation(1) ..... 800 mW
Max. Current out of V_{SS} pin ..... 150 mA
Max. Current into V_{DD} pin ..... 100 mA
Max. Current into an input pin (T0CKI only) ..... ±500 µA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. Output Current sunk by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin ..... 20 mA
Max. Output Current sourced by a single I/O port
PORTA ..... 50 mA
PORTB ..... 100 mA
Max. Output Current sunk by a single I/O port
PORTA ..... 50 mA
PORTB ..... 100 mA

Note 1: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 11-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C58A-04	PIC16C58A-10	PIC16C58A-20	PIC16LC58A-04	PIC16C58A/JW
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 1.9 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 8.0 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 20 MHz max.
LP	VDD: 3.0V to 6.25V IDD: 15 µA typ. at 32kHz, 3.0V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.25V IDD: 28 µA max. at 32kHz, 2.5V WDT dis IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.	VDD: 2.5V to 6.25V IDD: 28 µA max. at 32kHz, 2.5V WDT dis IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

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11.1 DC Characteristics: PIC16C58A-04, 10, 20 (Commercial) PIC16C58A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT, RC and LP options		3.0		6.25	V	
HS option		4.5		5.5	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current(3)	IDD					
XT and RC(4) options			1.9	2.5	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option			2.5	8.0	mA	FOSC = 10 MHz, VDD = 5.5V
			4.7	17	mA	FOSC = 20 MHz, VDD = 5.5V
LP option, Commercial			15		µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
LP option, Industrial			18		µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5)	IPD					
Commercial			4.0	12	µA	VDD = 3.0V, WDT enabled
			0.25	4.0	µA	VDD = 3.0V, WDT disabled
Industrial			5.0	14	µA	VDD = 3.0V, WDT enabled
			0.3	5.0	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

5

11.2 DC Characteristics: PIC16C58A-04E, 10E, 20E (Automotive)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C (automotive)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT and RC options		3.5		5.5	V	
HS option		4.5		5.5	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current(3)	IDD					
XT and RC(4) options			1.9	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
Power Down Current(5)	IPD					
XT and RC options			5.0	22	µA	VDD = 3.5V, WDT enabled
			0.8	18	µA	VDD = 3.5V, WDT disabled
HS option			4.0	22	µA	VDD = 3.5V, WDT enabled
			0.25	18	µA	VDD = 3.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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11.3 DC Characteristics: PIC16LC58A-04 (Commercial) PIC16LC58A-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT and RC options		3.0		6.25	V	
LP options		2.5		6.25	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current(3)	IDD					
XT and RC(4) options			0.5		mA	FOSC = 4.0 MHz, VDD = 5.5V
LP option, Commercial			12	28	µA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
LP option, Industrial			15	37	µA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
Power Down Current(5)	IPD					
Commercial			2.5	12	µA	VDD = 2.5V, WDT enabled
			0.25	4.0	µA	VDD = 2.5V, WDT disabled
Industrial			3.5	14	µA	VDD = 2.5V, WDT enabled
			0.3	5.0	µA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

5

11.4 DC Characteristics: PIC16C58A-04, 10, 20, PIC16LC58A-04 (Commercial) PIC16C58A-04I, 10I, 20I, PIC16LC58A-04I (Industrial) PIC16C58A-04E, 10E, 20E (Automotive)

DC Characteristics All Pins Except Power Supply Pins

Standard Operating Conditions (unless otherwise specified)
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
−40°C ≤ TA ≤ +85°C (industrial)
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.

Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	RC option only(4)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.2 VDD+1V		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V(5)
$\overline{MCLR}$ (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC option only(4)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$		-5.0			µA	VPIN = VSS +0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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11.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

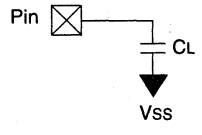
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 11-1: LOAD CONDITIONS - PIC16C58A



CL = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

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11.6 Timing Diagrams and Specifications

FIGURE 11-2: EXTERNAL CLOCK TIMING - PIC16C58A

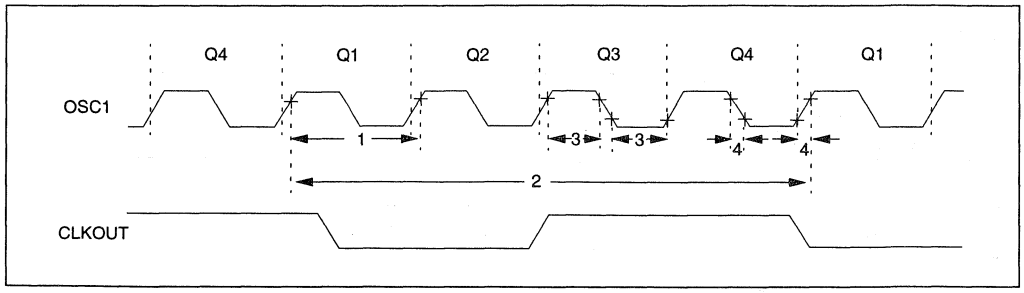

TABLE 11-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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TABLE 11-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C58A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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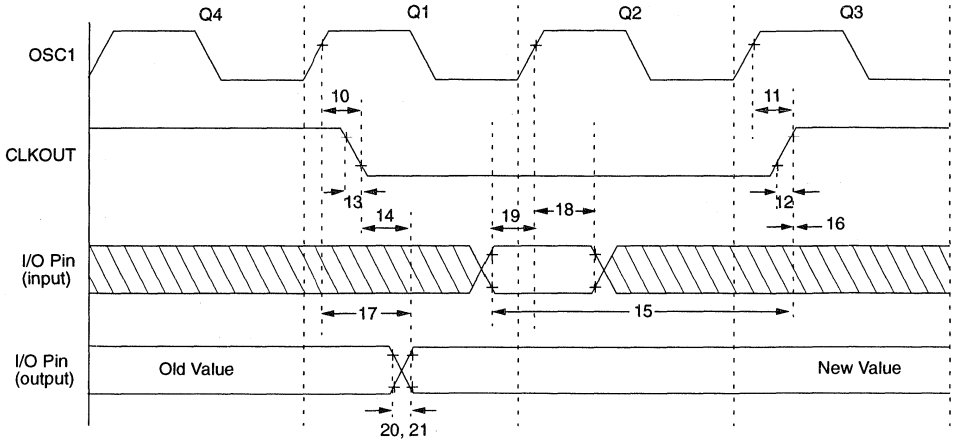
FIGURE 11-3: CLKOUT AND I/O TIMING - PIC16C58A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 11-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5	15**	ns
13	TckF	CLKOUT fall time(2)	—	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 11-1 for loading conditions.

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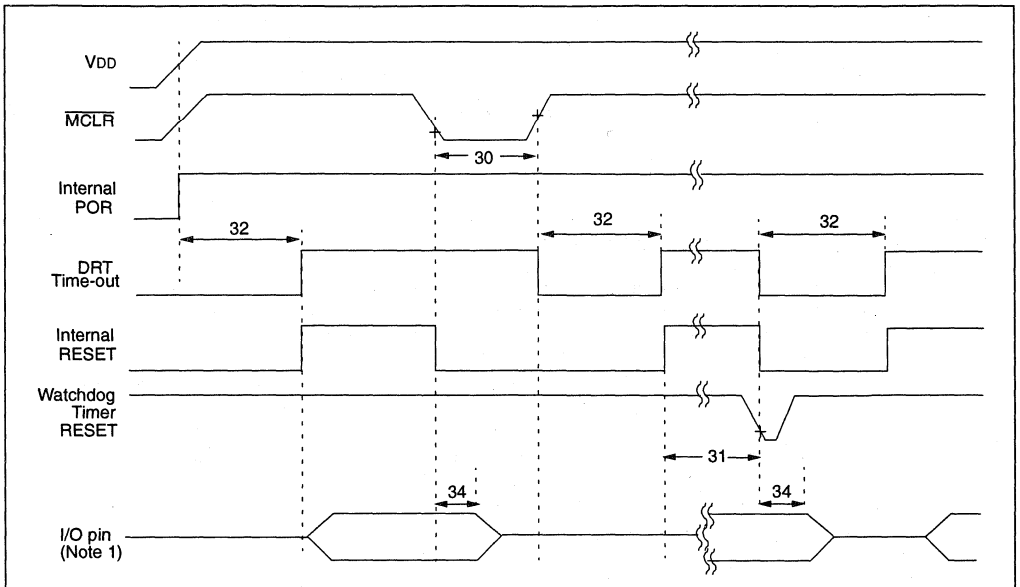
FIGURE 11-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C58A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

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TABLE 11-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C58A

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 11-5: TIMER0 CLOCK TIMINGS - PIC16C58A

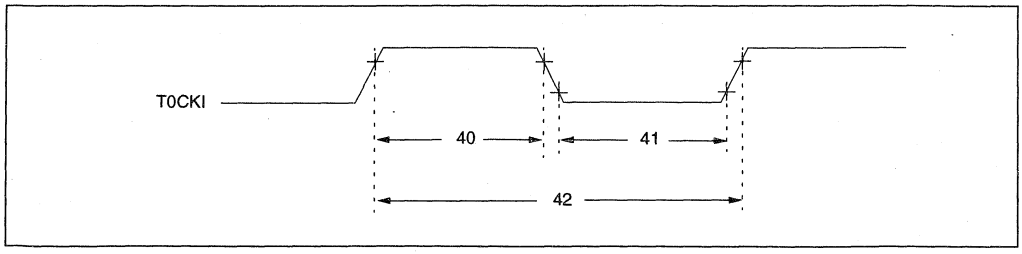

TABLE 11-5: TIMER0 CLOCK REQUIREMENTS - PIC16C58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −40°C ≤ TA ≤ +85°C (industrial), −40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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12.0 ELECTRICAL CHARACTERISTICS - PIC16CR58A

Absolute Maximum Ratings†

Ambient Temperature under bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14V

Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)

Total Power Dissipation (1) ..... 800 mW

Max. Current out of V_{SS} pin ..... 150 mA

Max. Current into V_{DD} pin ..... 100 mA

Max. Current into an input pin (T0CKI only) ..... ±500 µA

Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output Clamp Current, I_{OK} (V_O < 0 or V_O> V_{DD}) ..... ±20 mA

Max. Output Current sunk by any I/O pin ..... 25 mA

Max. Output Current sourced by any I/O pin ..... 20 mA

Max. Output Current sourced by a single I/O port

PORTA ..... 50 mA

PORTB ..... 100 mA

Max. Output Current sunk by a single I/O port

PORTA ..... 50 mA

PORTB ..... 100 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100Ω should be used when applying a low level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 12-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR58A-04	PIC16CR58A-10	PIC16CR58A-20	PIC16LCR58A-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
XT	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	VDD: 4.5V to 5.5V IDD: 8.0 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 10 MHz max	VDD: 4.5V to 5.5V IDD: 17 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	VDD: 2.5V to 6.25V IDD: 28 µA max at 32 kHz, 2.5V IPD: 4.0 µA max at 2.5V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

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12.1 DC Characteristics: PIC16CR58A-04, 10, 20 (Commercial) PIC16CR58A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS option	VDD	 3.0 4.5		 6.25 5.5	 V V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD		 1.9 2.5 4.7	 2.5 8.0 17	 mA mA mA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
Power-Down Current(5) Commercial Industrial 	IPD		 4.0 0.25 5.0 0.3	 12 4.0 14 5.0	 µA µA µA µA	 VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

5

12.2 DC Characteristics: PIC16CR58A-04E, 10E, 20E (Automotive)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C (automotive)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS options	VDD	 3.25 4.5		 6.0 5.5	 V V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD		 1.9 4.8 9.0	 3.3 10 20	 mA mA mA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V
Power-Down Current(5)	IPD		 5.0 0.8	 22 18	 µA µA	 VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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12.3 DC Characteristics: PIC16LCR58A-04 (Commercial) PIC16LCR58A-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5		6.25	V	LP option
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
Commercial			12	28	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Industrial			15	37	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power-Down Current(5)	IPD					
Commercial			4.0	12	µA	VDD = 2.5V, WDT enabled
			0.25	4.0	µA	VDD = 2.5V, WDT disabled
Industrial			5.0	14	µA	VDD = 2.5V, WDT enabled
			0.3	5.0	µA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

5

12.4 DC Characteristics: PIC16CR58A-04, 10, 20, PIC16LCR58A-04 (Commercial) PIC16CR58A-04I, 10I, 20I, PIC16LCR58A-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 12.1 and Section 12.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	RC option only(4)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD		VDD	V	For all VDD(5)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD		VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC option only(4)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0		+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0			µA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage(3)	VOH					
I/O ports		VDD –0.7			V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7			V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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12.5 DC Characteristics: PIC16CR58A-04E, 10E, 20E (Automotive)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40°C \le T_A \le +125°C$ Operating Voltage V_{DD} range is described in Section 12.2.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	V_{IL}					
I/O ports		V_{SS}		0.2 V_{DD}	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		V_{SS}		0.15 V_{DD}	V	
T0CKI (Schmitt Trigger)		V_{SS}		0.15 V_{DD}	V	
OSC1 (Schmitt Trigger)		V_{SS}		0.15 V_{DD}	V	RC option only(4)
OSC1		V_{SS}		0.3 V_{DD}	V	XT, HS and LP options
Input High Voltage	V_{IH}					
I/O ports		0.45 V_{DD}		V_{DD}	V	For all V_{DD}(5)
		2.0		V_{DD}	V	$4.0V < V_{DD} \le 5.5V$(5)
		0.36 V_{DD}		V_{DD}	V	$V_{DD} > 5.5V$
$\overline{MCLR}$ (Schmitt Trigger)		0.85 V_{DD}		V_{DD}	V	
T0CKI (Schmitt Trigger)		0.85 V_{DD}		V_{DD}	V	
OSC1 (Schmitt Trigger)		0.85 V_{DD}		V_{DD}	V	RC option only(4)
OSC1		0.7 V_{DD}		V_{DD}	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	V_{HYS}	0.15V_{DD}*			V	
Input Leakage Current(3)	I_{IL}					**For $V_{DD} \le 5.5V$**
I/O ports		−1.0		+1.0	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at hi-impedance
$\overline{MCLR}$		−5.0			µA	$V_{PIN} = V_{SS} + 0.25V$(2)
			0.5	+5.0	µA	$V_{PIN} = V_{DD}$(2)
T0CKI		−3.0	0.5	+3.0	µA	$V_{SS} \le V_{PIN} \le V_{DD}$
OSC1		−3.0	0.5	+3.0	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, XT, HS and LP options
Output Low Voltage	V_{OL}					
I/O ports				0.6	V	I_{OL} = 8.7 mA, V_{DD} = 4.5V
OSC2/CLKOUT				0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, RC option only
Output High Voltage(3)	V_{OH}					
I/O ports		V_{DD} −0.7			V	I_{OH} = −5.4 mA, V_{DD} = 4.5V
OSC2/CLKOUT		V_{DD} −0.7			V	I_{OH} = −1.0 mA, V_{DD} = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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12.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

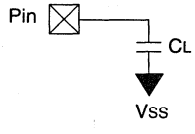
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{MCLR}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 12-1: LOAD CONDITIONS



CL = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

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12.7 Timing Diagrams and Specifications

FIGURE 12-2: EXTERNAL CLOCK TIMING - PIC16CR58A

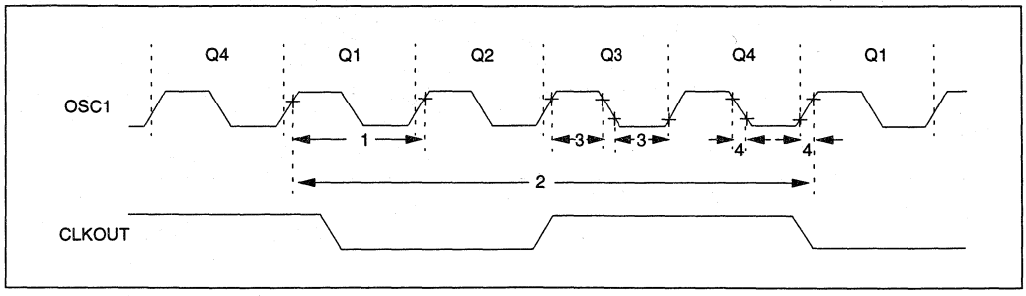

TABLE 12-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

5

TABLE 12-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR58A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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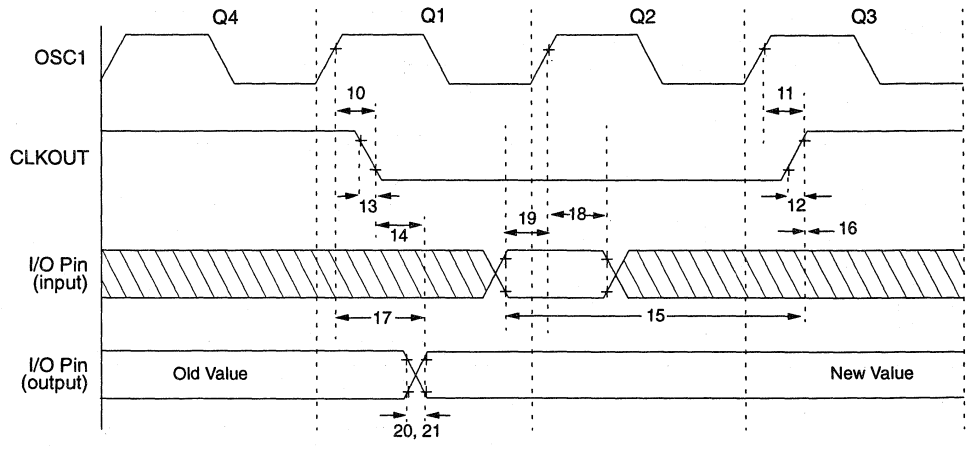
FIGURE 12-3: CLKOUT AND I/O TIMING - PIC16CR58A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 12-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR58A

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
−40°C ≤ TA ≤ +85°C (industrial),
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2iol	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

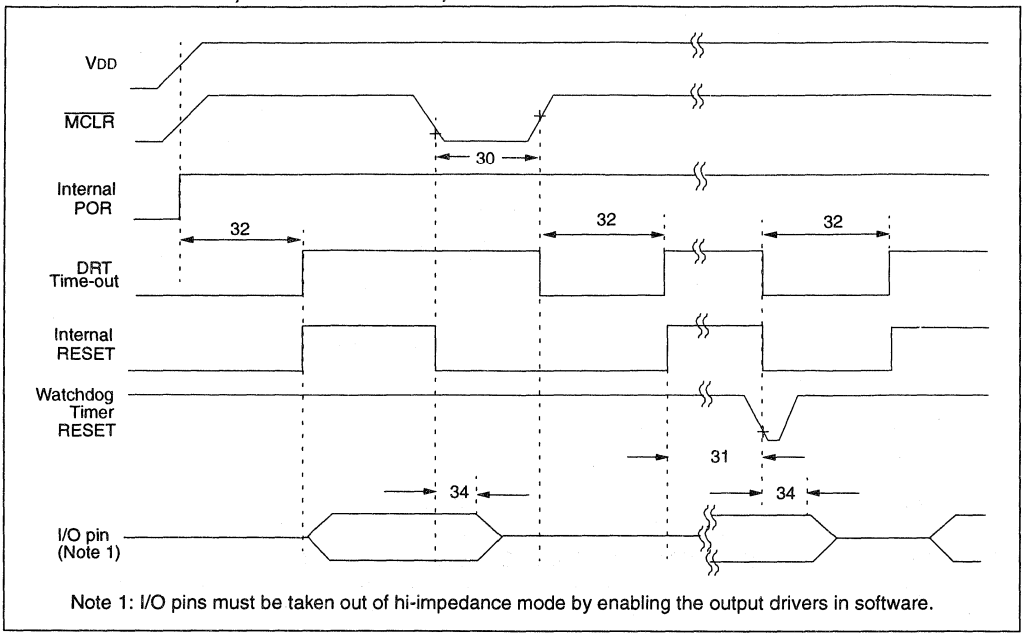
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 12-1 for loading conditions.

FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR58A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR58A

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
−40°C ≤ TA ≤ +85°C (industrial),
−40°C ≤ TA ≤ +125°C (automotive)
Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	TioZ	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	1.0*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16CR58A

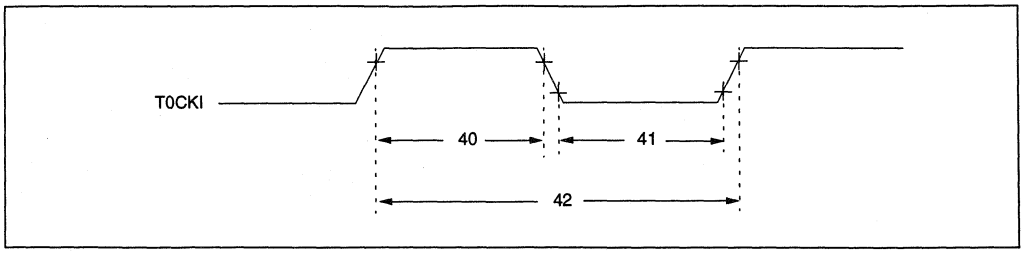

TABLE 12-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), –40°C ≤ TA ≤ +125°C (automotive) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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NOTES:

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13.0 DC AND AC CHARACTERISTICS - ALL ENH. PIC16C5X

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 13-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

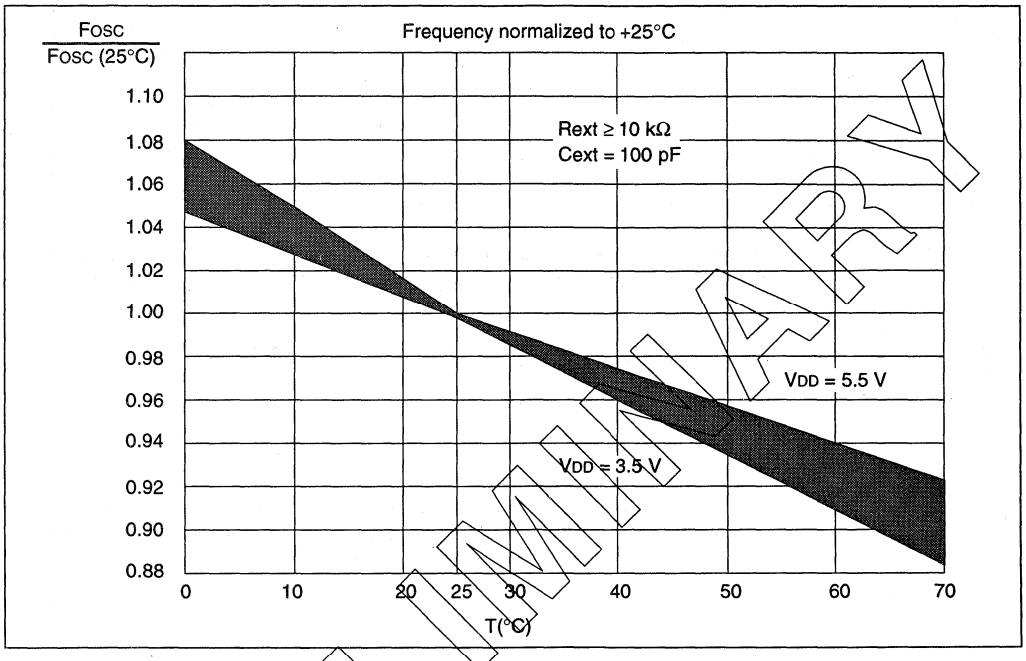

TABLE 13-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5 V.

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FIGURE 13-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20PF

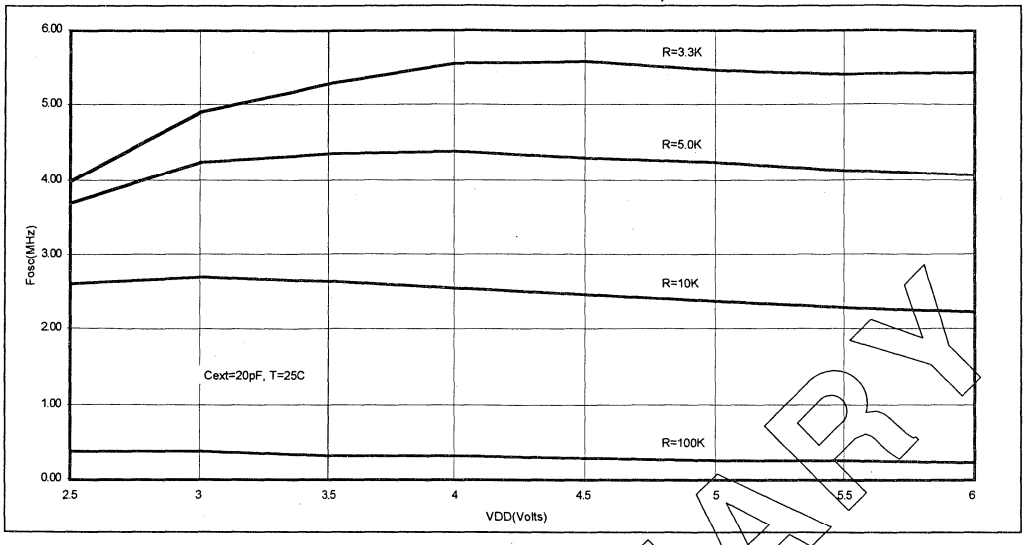

FIGURE 13-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 PF

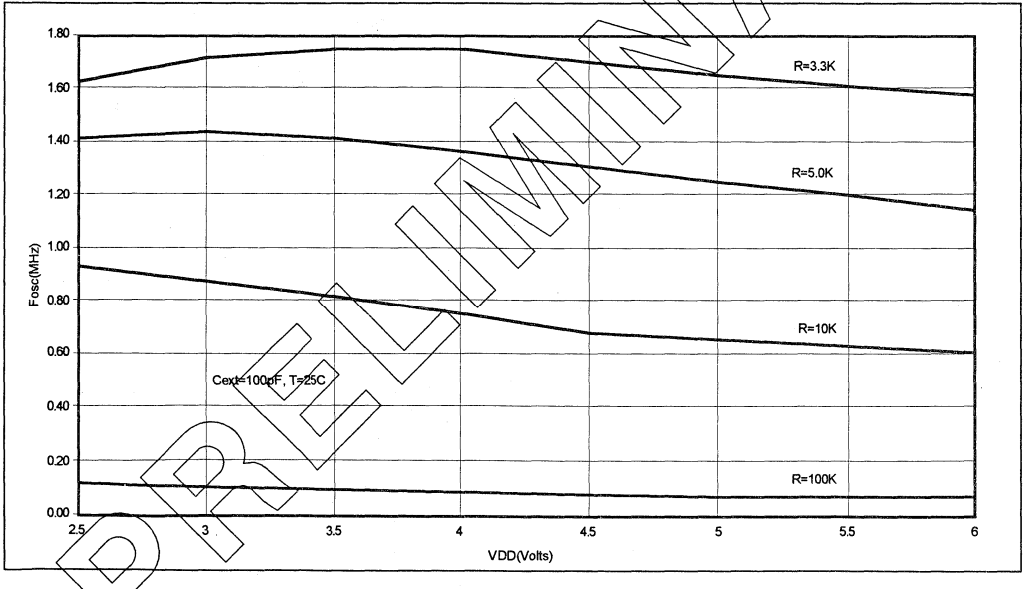

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FIGURE 13-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF

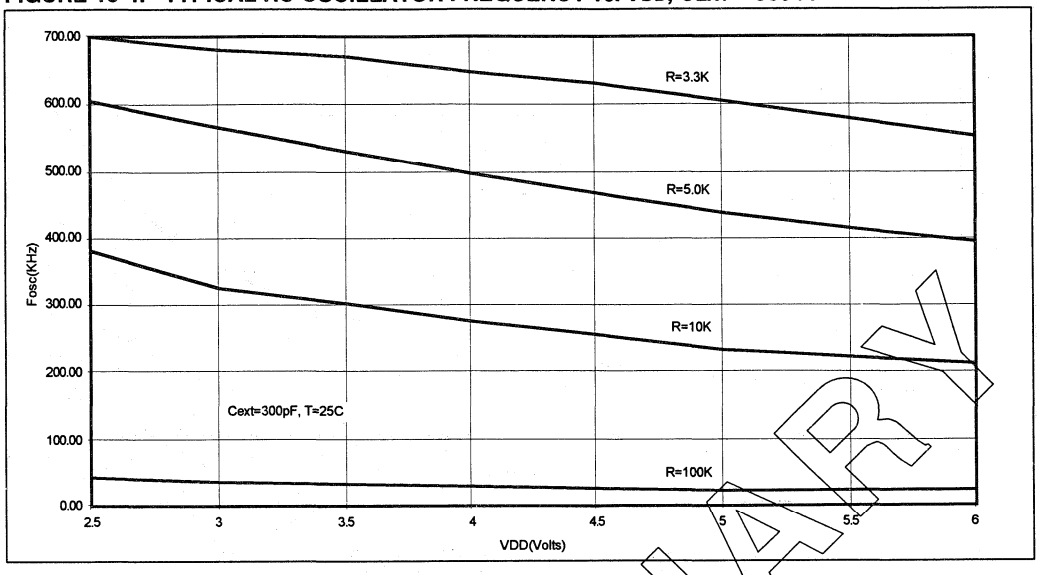

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FIGURE 13-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)

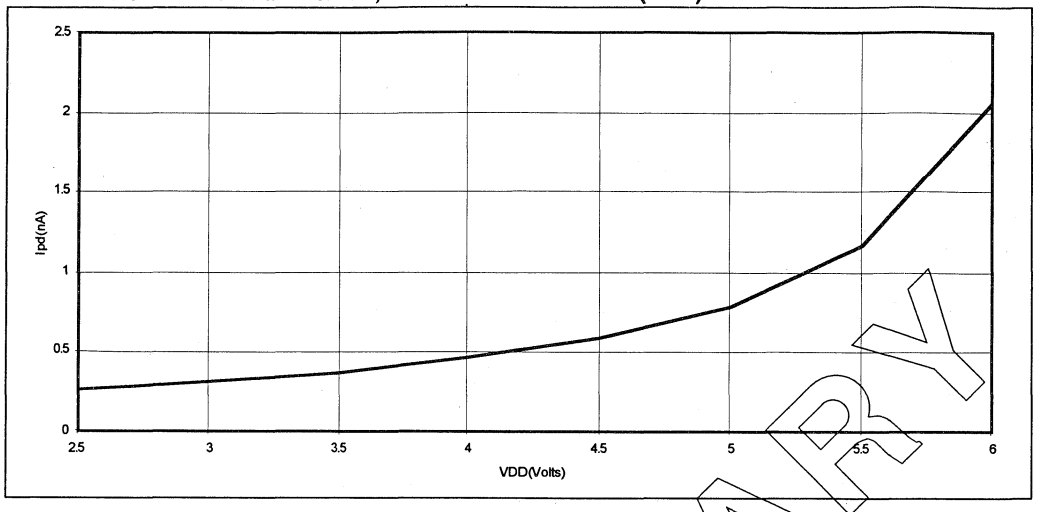

FIGURE 13-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED (-40°C TO +85°C)

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FIGURE 13-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

FIGURE 13-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED (-40°C TO +85°C)

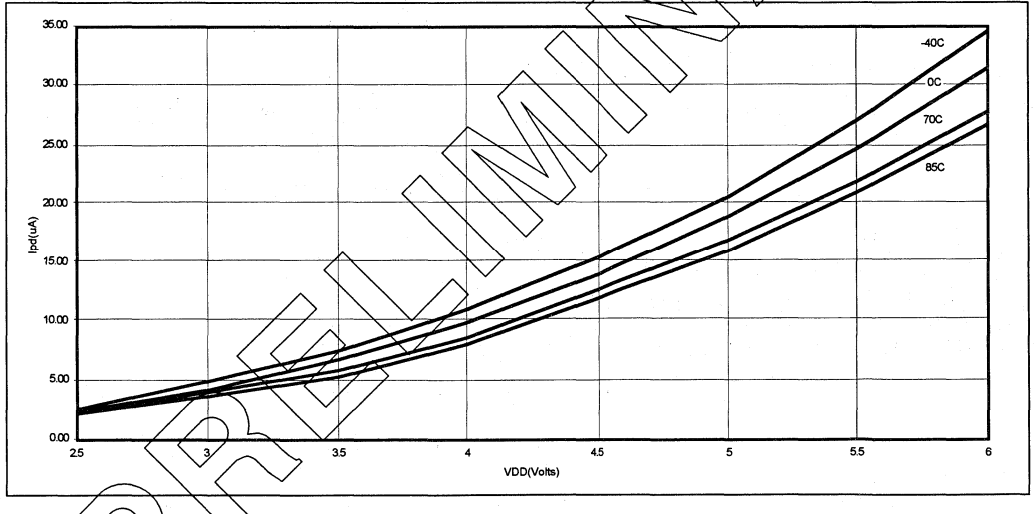

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FIGURE 13-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

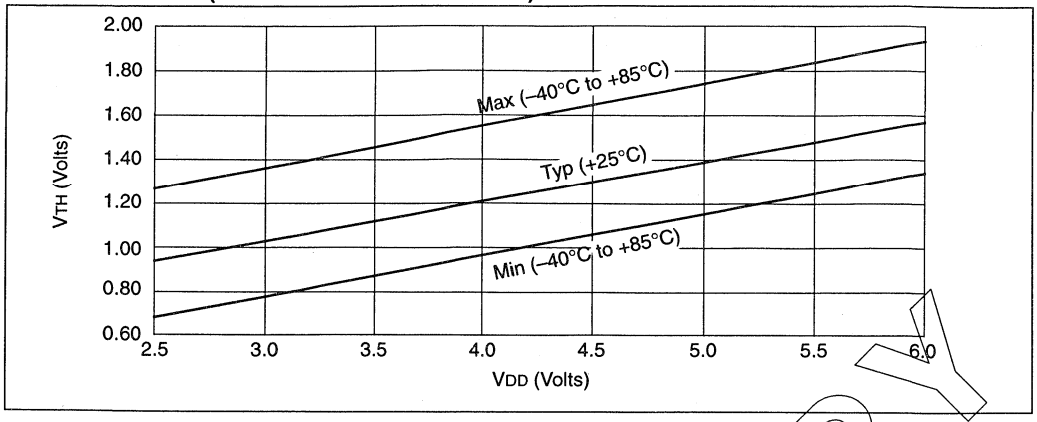
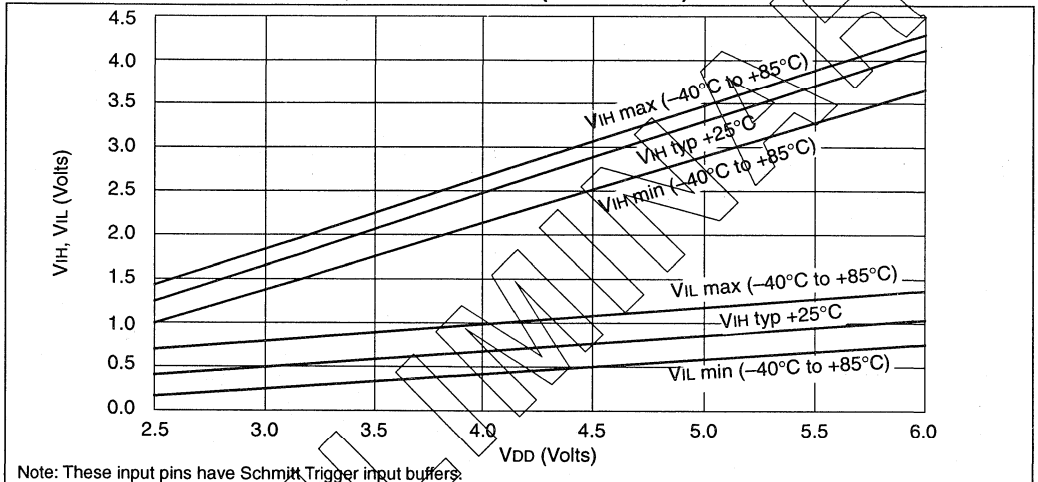


FIGURE 13-10: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 13-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD

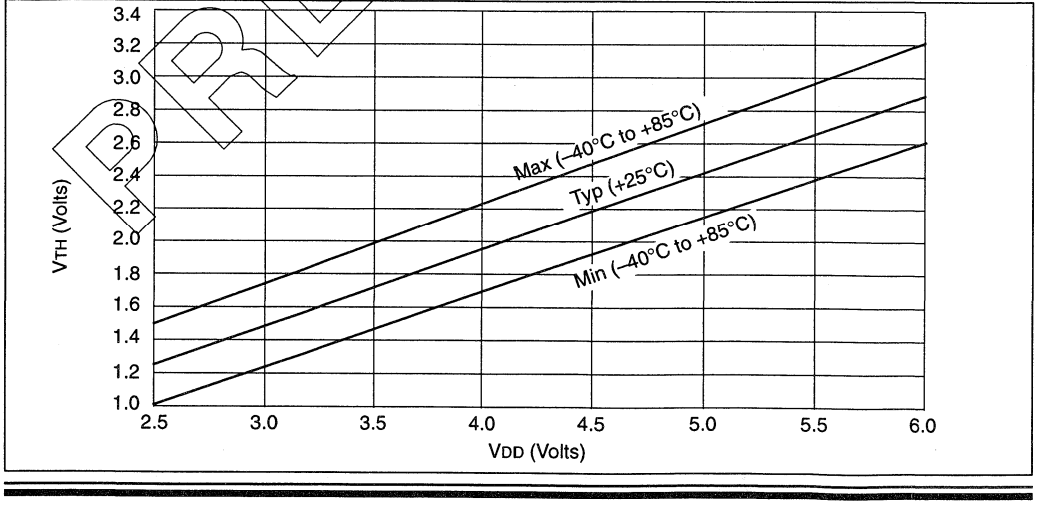


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FIGURE 13-12: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20PF, 25°C)

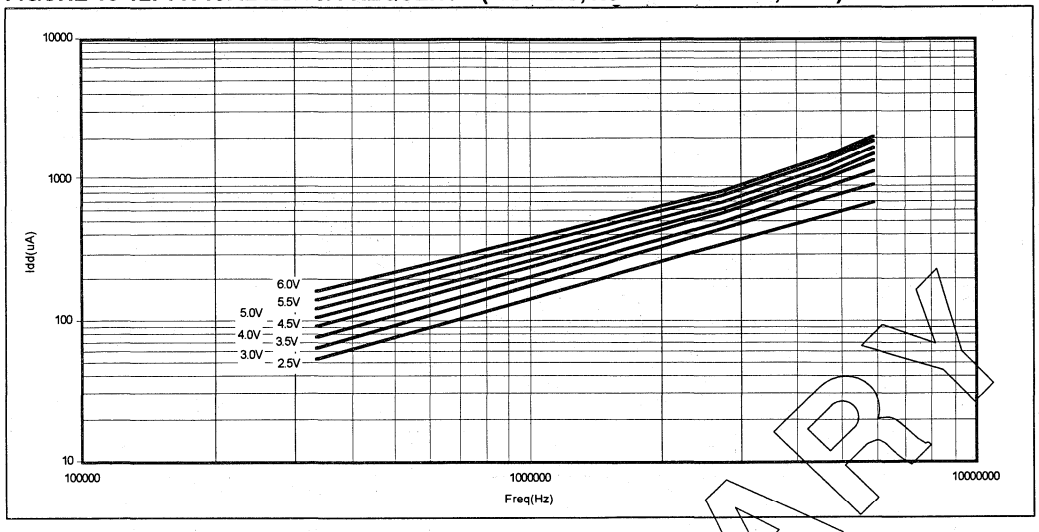

FIGURE 13-13: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20PF, -40°C TO +85°C)

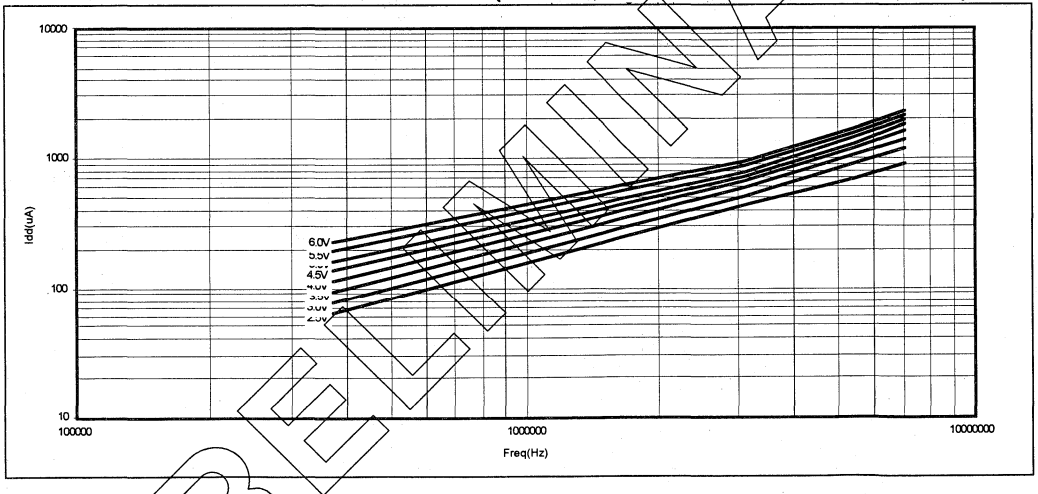

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FIGURE 13-14: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100PF, 25°C)

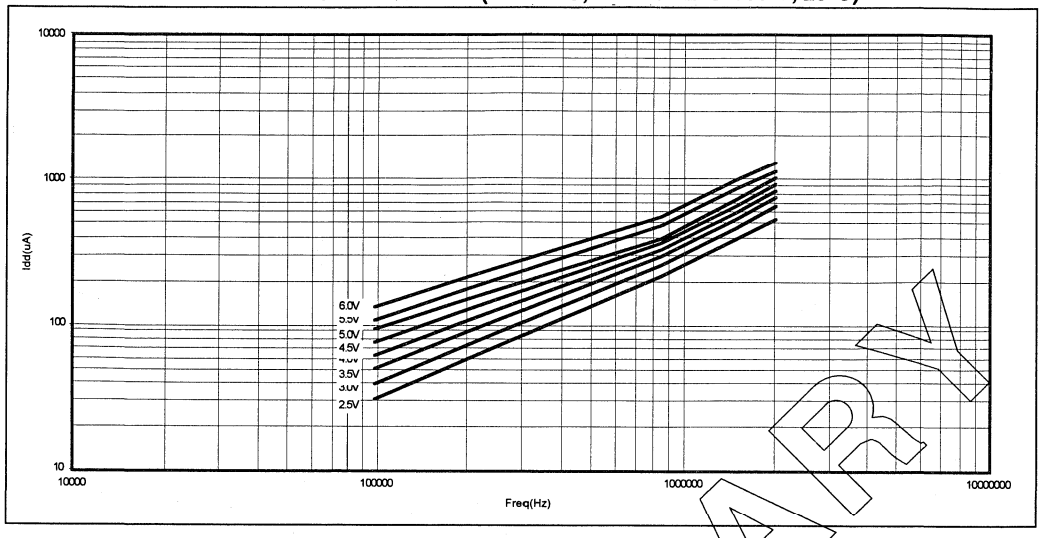

FIGURE 13-15: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100PF, -40°C TO +85°C)

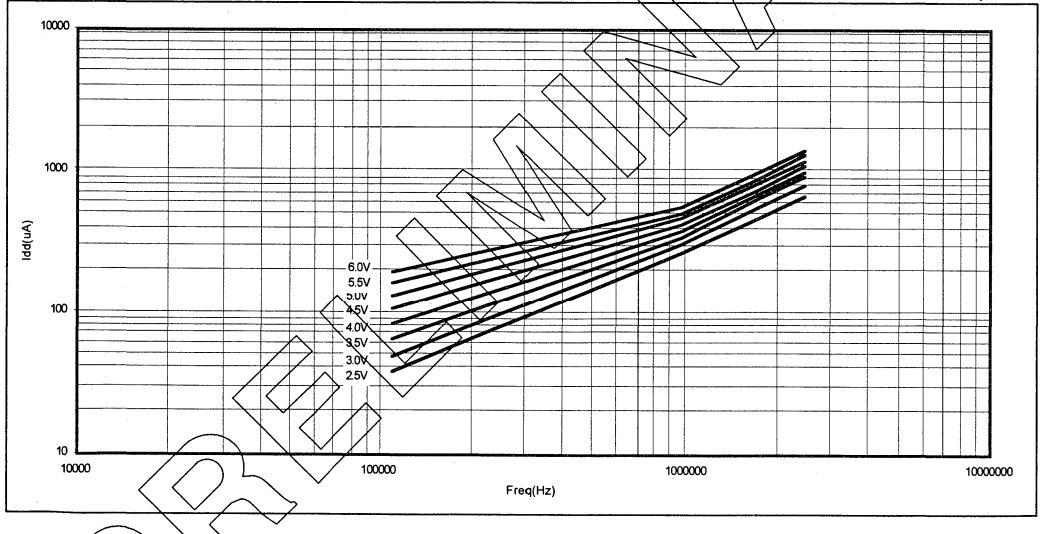

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FIGURE 13-16: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300PF, 25°C)

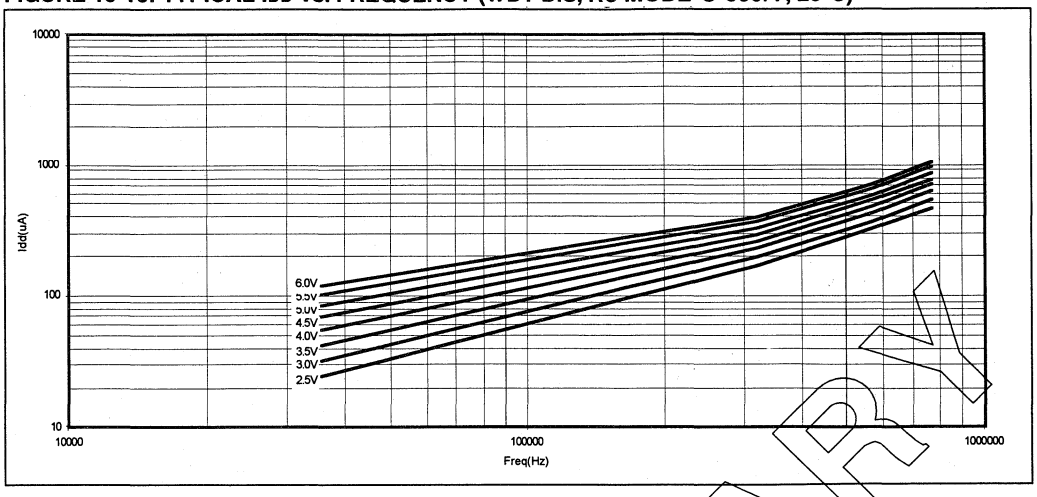

FIGURE 13-17: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300PF, -40°C TO +85°C)

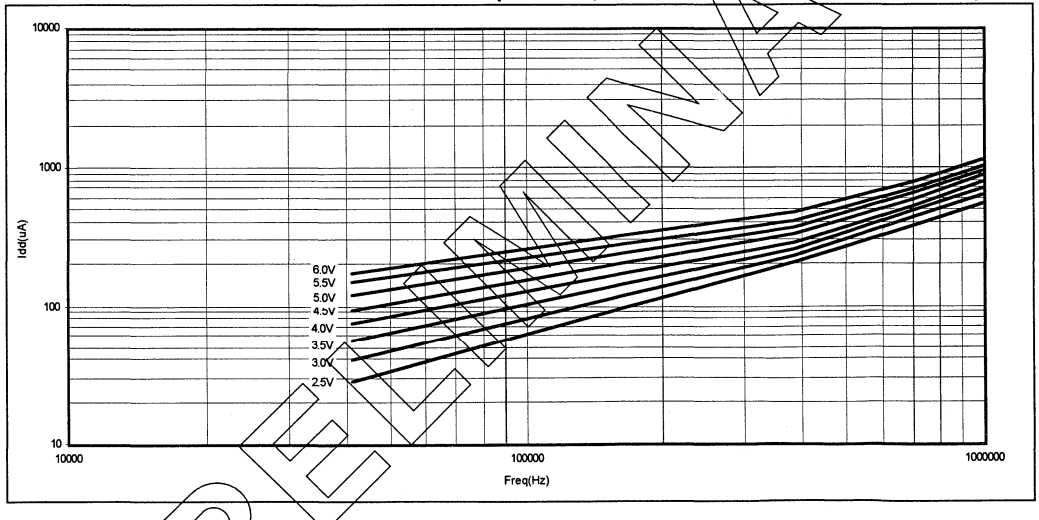

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FIGURE 13-18: WDT TIMER TIME-OUT PERIOD vs. VDD

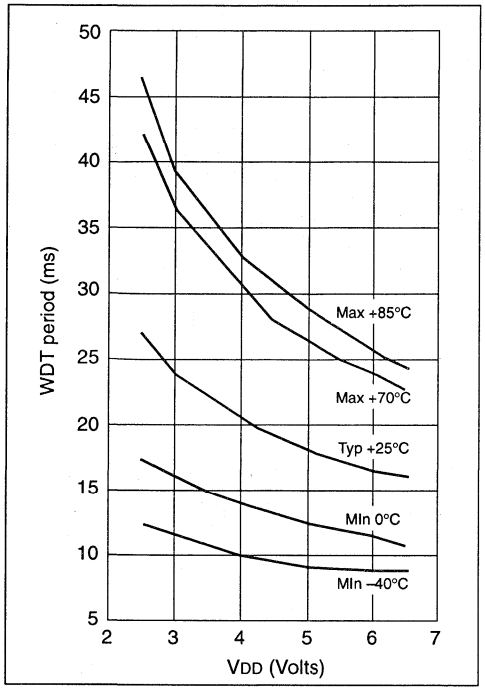

TABLE 13-2: INPUT CAPACITANCE FOR PIC16C54A/C58A

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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FIGURE 13-19: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

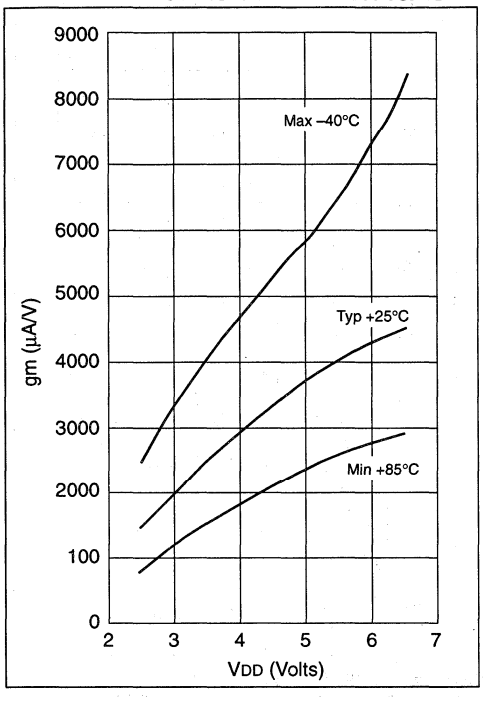

FIGURE 13-20: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

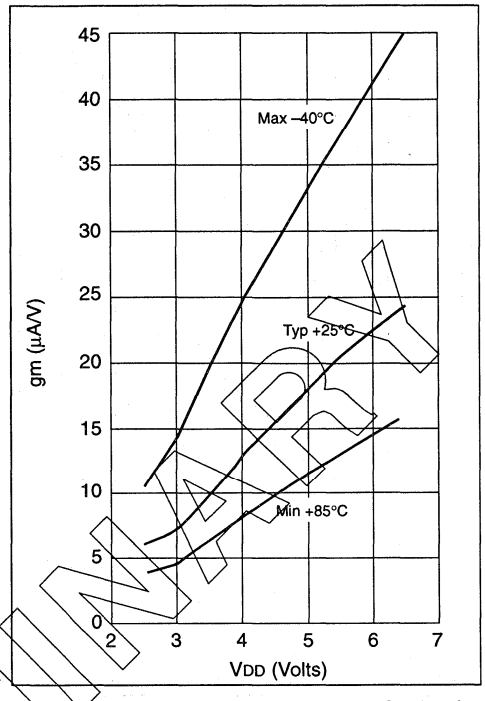

FIGURE 13-21: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

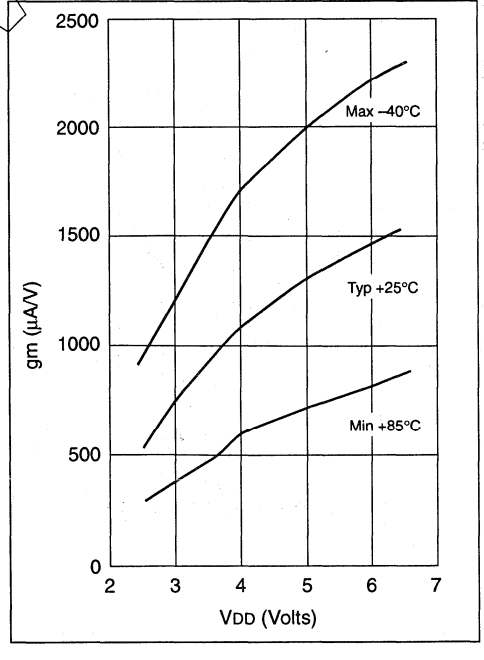

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FIGURE 13-22: IOH vs. VOH, VDD = 3 V

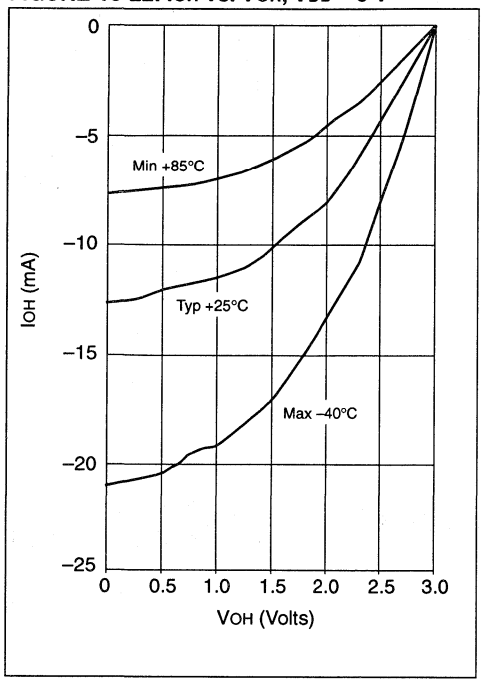


FIGURE 13-23: IOH vs. VOH, VDD = 5 V

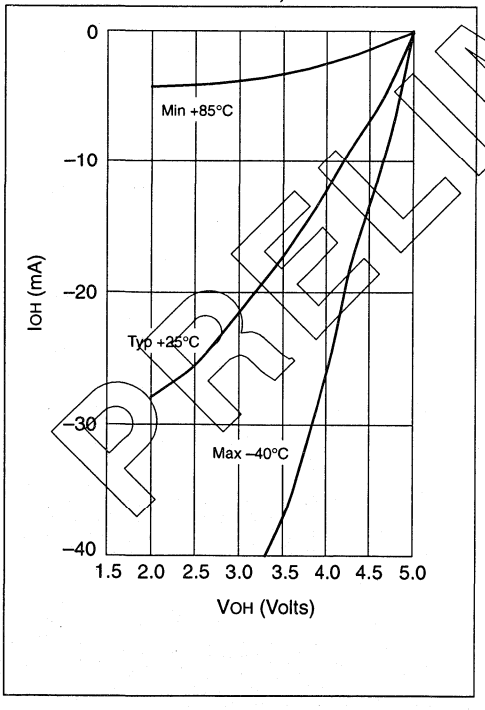


FIGURE 13-24: IOL vs. VOL, VDD = 3 V

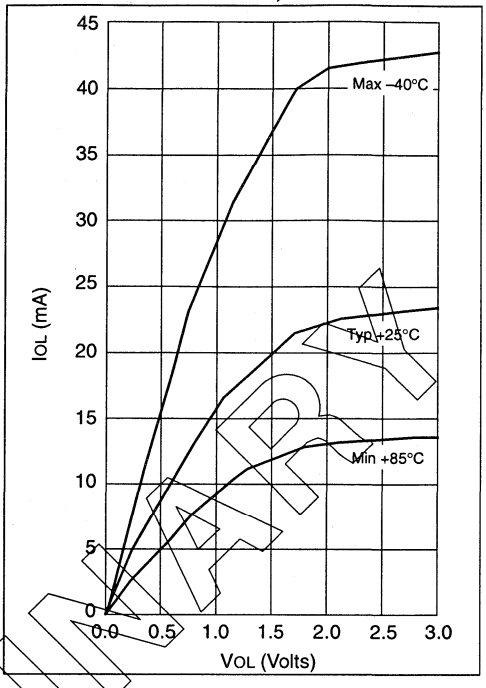
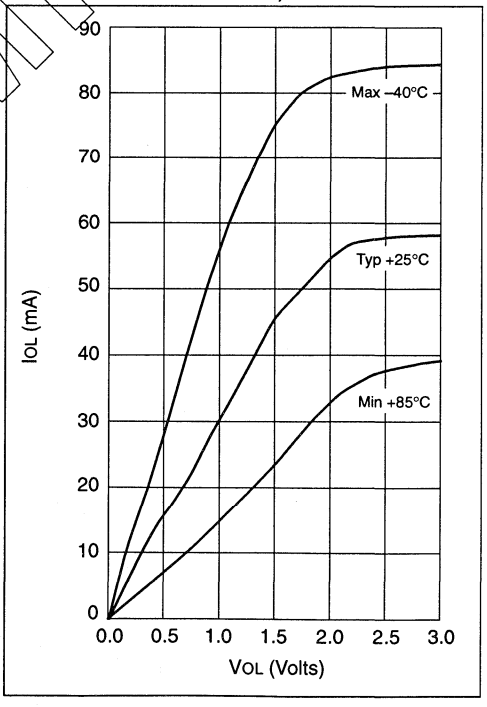


FIGURE 13-25: IOL vs. VOL, VDD = 5 V



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APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to proper value for processor used.
6. Remove any use of the ADDLW and SUBLW instructions.
7. Rewrite any code segments that use interrupts.

APPENDIX B: WHAT'S NEW

B.1 Format

The format of this data sheet has been changed to be consistent with other product families. This ensures that important topics are covered across all PIC16/17 families. Here is an overview list of new features:

- Data Sheet Structure / Outline
- Consistent Figures and Tables

B.2 Additions

Items that have been added to this data sheet are:

- PIC16CR54A, PIC16CR54B, PIC16CR55, PIC16CR56, PIC16CR57B and PIC16CR58B data
- PIC16C5X-10 data
- PIC16C5X/JW package information

B.3 Deletions

Items that have been deleted from this data sheet are:

- PIC16CR54A, PIC16CR54B, PIC16CR55, PIC16CR56, PIC16CR57A and PIC16CR58B data

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APPENDIX C: WHAT'S CHANGED

Changes to this version of the PIC16C5XA data sheet are:

- Correction of the 28-lead SSOP package pin-out
- Inclusion of errata sheet information

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ENHANCED PIC16C5X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Frequency Range	Temperature Range	Package	Pattern

Device	PIC16C5X[2], PIC16C5XT[3] PIC16LC5X[2], PIC16LC5XT[3] PIC16CR5X[2], PIC16CR5XT[3] PIC16LCR5X[2], PIC16LCR5XT[3]	
Frequency Range	04 10 20 b[1]	= 4 MHz = 10 MHz = 20 MHz = No type for JW[4] devices
Temperature Range	b[1] I E	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial) = -40°C to +125°C (Automotive)
Package	JW P SO SP SS	= Windowed CERDIP = PDIP = SOIC (Gull Wing, 300 mil body) = Skinny PDIP (28 pin, 300 mil body) = SSOP (209 mil body)
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)	

Examples:

a) PIC16C54A -04/P 301 = Commercial temp., PDIP package, 4MHz, normal VDD limitis, QTP pattern #301.

b) PIC16LC58A - 04I/SO = Industrial temp., SOIC package, 4MHz, Extended VDD limits.

c) PIC16CR57B - 10E/P355 = ROM program memory, Automotive temp., PDIP package, 10MHz, normal VDD limits.

Note 1: b = blank
2: C = Standard VDD range
LC = Extended VDD range
CR = ROM Version, Standard VDD range
LCR = ROM Version, Extended VDD range
3: T = in tape and reel - SOIC, SSOP packages only.
4: UV erasable devices are tested to all available voltage/frequency options. Erased devices are oscillator type 04. The user can select 04, 10 or 20 oscillators by programmng the appropriate configuration bits.

5

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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NOTES:

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ENHANCED PIC16LV5X

EPROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16LV54A
- PIC16LV58A

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (2 µs) except for program branches which are two-cycle
- Operating speed: DC - 2 MHz clock input
  DC - 2 µs instruction cycle

Device	Pins	I/O	EPROM	RAM
PIC16LV54A	18	12	512	25
PIC16LV58A	18	12	2K	73

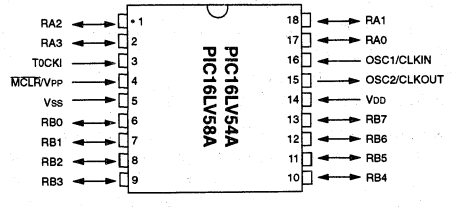
- 12-bit wide instructions
- 8-bit wide data path
- Seven special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

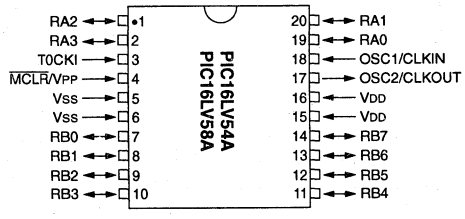
- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - LP: Power saving, low frequency crystal

Pin Diagrams

PDIP, SOIC, Windowed CERDIP



SSOP



CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range:
  - EPROM Commercial/Industrial 2.0V to 3.8V
- Low-power consumption
  - < 1 mA typical @ 3V, 2 MHz
  - 10 µA typical @ 2V, 32 kHz
  - < 0.6 µA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

5

1.0 GENERAL DESCRIPTION

The Enhanced PIC16LV5X from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EPROM-based CMOS microcontrollers. This family is pin and software compatible with the PIC16LV5X family of devices in a new enhanced process technology. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (2 μs) except for program branches which take two cycles. The Enhanced PIC16LV5X delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The Enhanced PIC16LV5X products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are three oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective One-Time-Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The Enhanced PIC16LV5X products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The Enhanced PIC16LV5X series fits perfectly in applications such as low-power remote transmitters/receivers and pointing devices. The EPROM technology makes customizing application programs (transmitter codes, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the Enhanced PIC16LV5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

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TABLE 1-1: ENHANCED PIC16LV5X FAMILY OF DEVICES

	Clock	Memory		Peripherals		Features		
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (words)	RAM Data Memory (bytes)	Timer Module(s)	I/O Pins	Voltage Range (Volts)	Number of Instructions	Packages
PIC16LV54A	2	512	25	TMR0	12	2.0-3.8	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16LV58A	2	2K	73	TMR0	12	2.0-3.8	33	18-pin DIP, SOIC; 20-pin SSOP

Legend: All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

5

2.0 ENHANCED PIC16LV5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the Enhanced PIC16LV5X Product Identification System at the back of this data sheet to specify the correct part number.

For the Enhanced PIC16LV5X family of devices, there is one device type, as indicated in the device number:

1. **LV**, as in PIC16LV54A. These devices have EPROM program memory and operate over the standard voltage range of 2.0 to 3.8 volts.

2.1 UV Erasable Devices

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE™ programmers both support programming of the Enhanced PIC16LV5X. Third party programmers also are available; refer to the Third Party Guide for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP^{SM}) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

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3.0 ARCHITECTURAL OVERVIEW

This section provides information on the architecture of the Enhanced PIC16LV5X. For information on operation of the peripherals, electrical specifications, etc., please refer to the Enhanced PIC16C5X data sheet.

FIGURE 3-1: ENHANCED PIC16LV5X SERIES BLOCK DIAGRAM

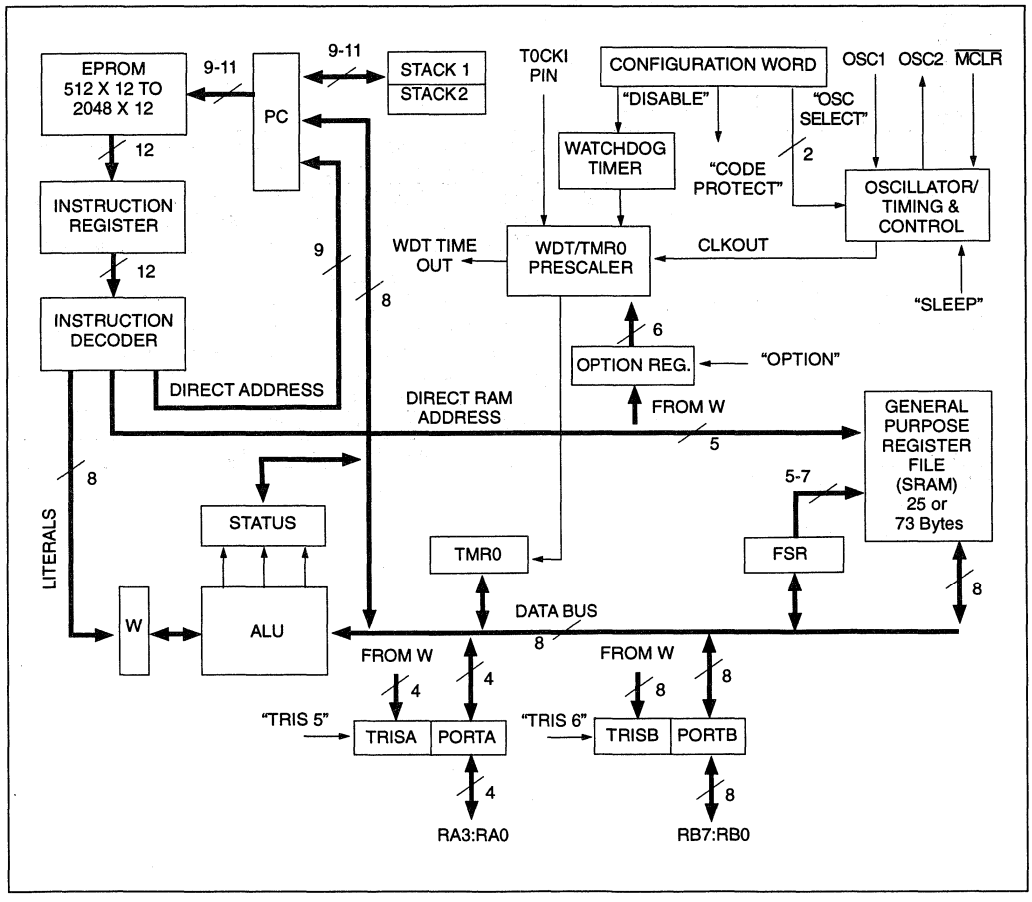

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TABLE 3-1: PINOUT DESCRIPTION - PIC16LV54A, PIC16LV58A

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	20	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RB0	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL	
RB7	13	14	I/O	TTL	
T0CKI	3	3	I	ST	Clock input to Timer0. Must be tied to VSS or VDD, if not in use, to reduce current consumption.
$\overline{MCLR}$/VPP	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the $\overline{MCLR}$/VPP pin must not exceed VDD to avoid unintended entering of programming mode.
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.
VSS	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used, TTL = TTL input,
ST = Schmitt Trigger input

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4.0 MEMORY ORGANIZATION

FIGURE 4-1: PIC16LV54A PROGRAM MEMORY MAP AND STACK

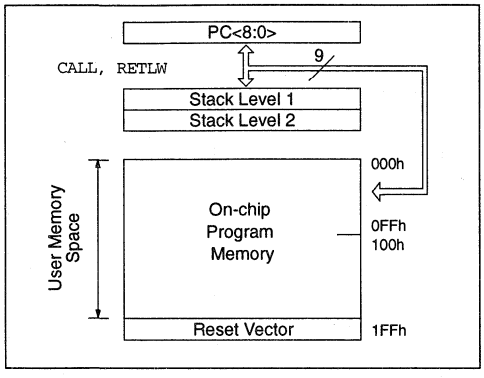


FIGURE 4-2: PIC16LV58A PROGRAM MEMORY MAP AND STACK

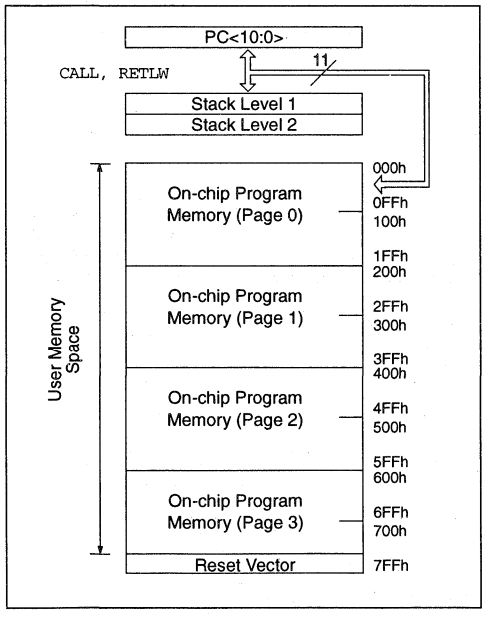
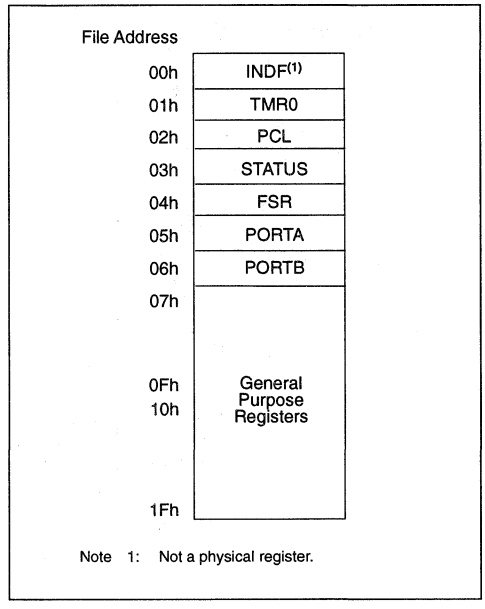


FIGURE 4-3: PIC16LV54A REGISTER FILE MAP



Note 1: Not a physical register.

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FIGURE 4-4: PIC16LV58A REGISTER FILE MAP

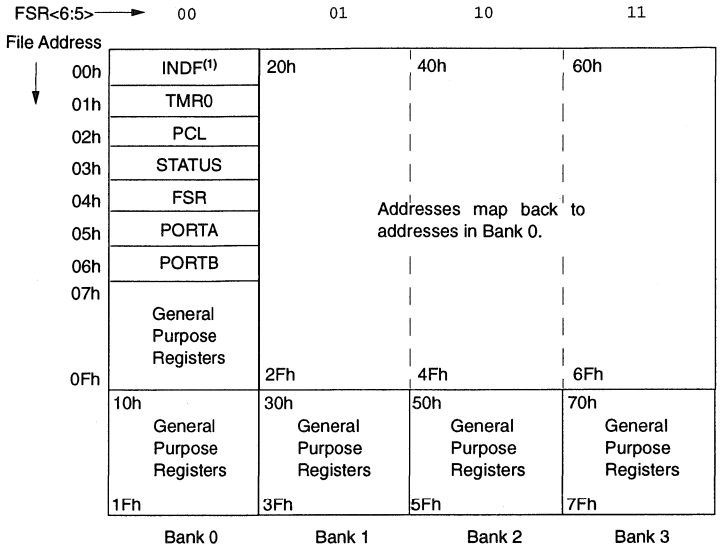

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, - = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 of the Enhanced PIC16C5X data sheet (DS30236B) for an explanation of how to access these bits.

2: File address 07h is a general purpose register on the PIC16LV54A and PIC16LV58A.

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5.0 ELECTRICAL CHARACTERISTICS - PIC16LV5XA

Absolute Maximum Ratings†

Ambient temperature under bias ..... -20°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)
Total power dissipation (1) ..... 800 mW
Max. current out of V_{SS} pin ..... 150 mA
Max. current into V_{DD} pin ..... 100 mA
Max. current into an input pin (T0CKI only) ..... ±500 µA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 20 mA
Max. output current sourced by a single I/O port (PORTA or B) ..... 40 mA
Max. output current sunk by a single I/O port (PORTA or B) ..... 50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5

5.1 DC Characteristics: PIC16LV5XA-02 (Commercial) PIC16LV5XA-02 (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –20°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT, RC and LP options	VDD	2.0		3.8	V	
RAM Data Retention Voltage(2)	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current(3) XT and RC(4) options LP option, Commercial LP option, Industrial	IDD		 0.5 11 14	 27 35	 mA µA µA	 FOSC = 2.0 MHz, VDD = 3.0V FOSC = 32 kHz, VDD = 2.5V, WDT disabled FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power Down Current(5)(6) Commercial Industrial	IPD		 2.5 0.25 3.5 0.3	 12 4.0 14 5.0	 µA µA µA µA	 VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is entered or during initial power-up.

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5.2 DC Characteristics: PIC16LV5XA-02 (Commercial) PIC16LV5XA-02 (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) −20°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS		0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS		0.15 VDD	V	RC option only(4)
OSC1		VSS		0.3 VDD	V	XT and LP options
Input High Voltage	VIH					
I/O ports		0.2 VDD+1V		VDD	V	For all VDD(5)
MCLR (Schmitt Trigger)		0.85 VDD		VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD		VDD	V	RC option only(4)
OSC1		0.7 VDD		VDD	V	XT and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*			V	
Input Leakage Current(3)	IIL					
I/O ports		-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		-5.0		+5.0	µA	VPIN = VSS +0.25V(2)
			0.5	+3.0	µA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5		µA	VSS ≤ VPIN ≤ VDD, XT and LP options
Output Low Voltage	VOL					
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 3.8V
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 3.8V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7			V	IOH = -5.4 mA, VDD = 3.8V
OSC2/CLKOUT		VDD-0.7			V	IOH = -1.0 mA, VDD = 3.8V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16LV5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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5.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

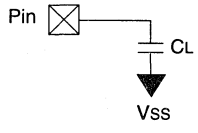
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 5-1: LOAD CONDITIONS - PIC16LV5XA



CL = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

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5.4 Timing Diagrams and Specifications

FIGURE 5-2: EXTERNAL CLOCK TIMING - PIC16LV5XA

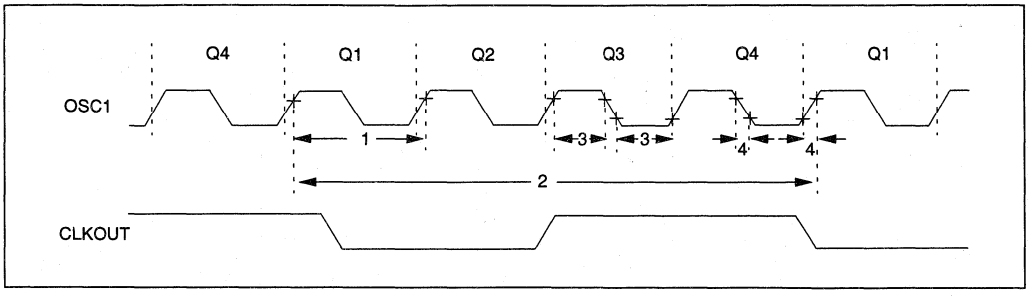


TABLE 5-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16LV5XA

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –20°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	2.0	MHz	RC osc mode
			DC	—	2.0	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	2.0	MHz	RC osc mode
			0.1	—	2.0	MHz	XT osc mode
			5	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(2)	500	—	—	ns	RC osc mode
			500	—	—	ns	XT osc mode
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	500	—	—	ns	RC osc mode
			500	—	10,000	ns	XT osc mode
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	50*	ns	LP oscillator

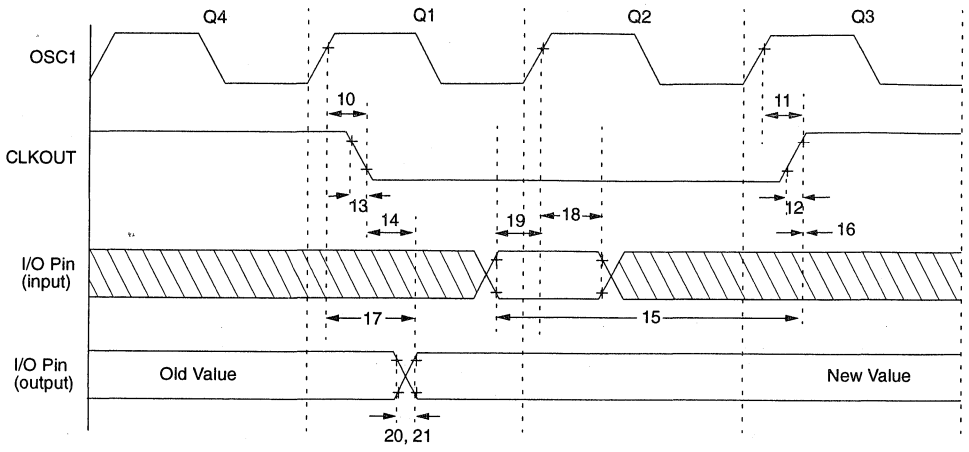
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 5-3: CLKOUT AND I/O TIMING - PIC16LV5XA



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 5-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16LV5XA

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), −20°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2iol	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 5-1 for loading conditions.

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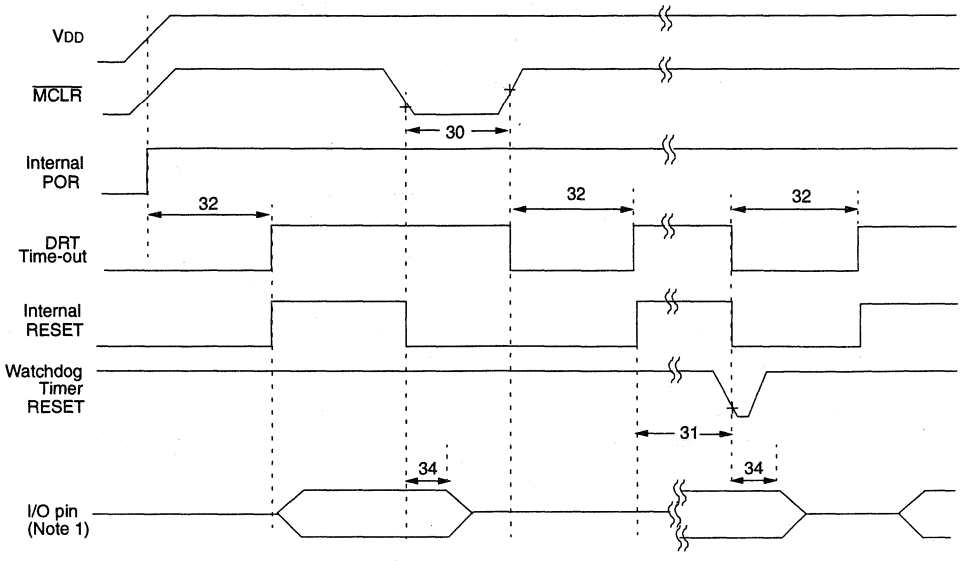
FIGURE 5-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16LV5XA



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

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TABLE 5-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16LV5XA

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –20°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100*	—	—	ns	VDD = 3.8V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	40*	ms	VDD = 3.8V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 3.8V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 5-5: TIMER0 CLOCK TIMINGS - PIC16LV5XA

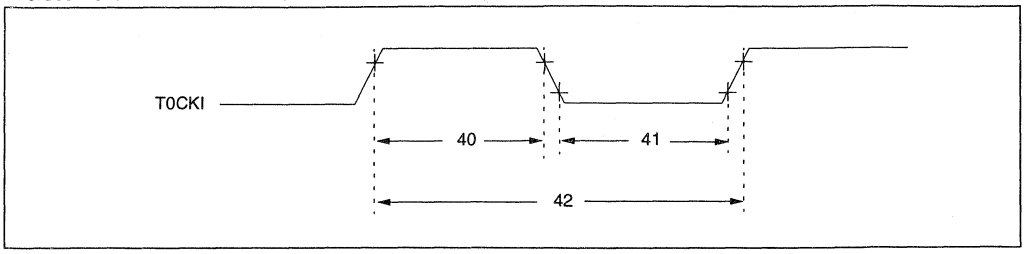

TABLE 5-4: TIMER0 CLOCK REQUIREMENTS - PIC16LV5XA

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), –20°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in the Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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6.0 DC AND AC CHARACTERISTICS - ENHANCED PIC16LV5X

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

Not available at this time.

ENHANCED PIC16LV5X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Frequency Range	Temperature Range	Package	Pattern

Device	PIC16LV5XA, PIC16LV5XAT(2)	
Frequency Range	02	= 2 MHz
Temperature Range	b(1)	= 0°C to +70°C (Commercial)
	I	= -20°C to +85°C (Industrial)
Package	P	= PDIP
	SO	= SOIC (Gull Wing, 300 mil body)
	SS	= SSOP (209 mil body)
Pattern	3-digit Pattern Code for QTP (blank otherwise)	

Examples:

a) PIC16LV54A -02/P 301 = Commercial temp., PDIP package, 2MHz, normal VDD limits, QTP pattern #301.

b) PIC16LV58A - 02I/SO = Industrial temp., SOIC package, 2 MHz, Extended VDD limits.

Note 1: b = blank
2: T = in tape and reel - SOIC, SSOP packages only.

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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MICROCHIP

SECTION 6
PIC16C55X MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC16C55X EPROM-Based 8-Bit CMOS Microcontroller 6-1

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PIC16C55X

EPROM-Based 8-Bit CMOS Microcontroller

Devices included in this data sheet:

- PIC16C554
- PIC16C556
- PIC16C558

High Performance RISC CPU:

- Only 35 instructions to learn
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle

Device	Program Memory	Data Memory
PIC16C554	512	80
PIC16C556	1K	80
PIC16C558	2K	128

- Interrupt capability
- 16 special function hardware registers
- 8-level deep hardware stack
- Direct, Indirect and Relative addressing modes

Peripheral Features:

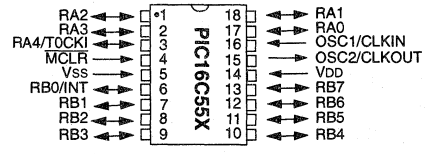
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

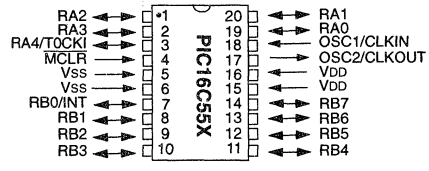
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation

Pin Diagrams

PDIP, SOIC, Windowed CERDIP



SSOP



Special Microcontroller Features (cont'd)

- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Four user programmable ID locations

CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range
  - 2.5V to 5.5V
- Commercial, industrial and automotive temperature range
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - < 1.0 µA typical standby current @ 3.0V

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To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error from the previous version of this data sheet (PIC16C55X Data Sheet, Literature Number DS40143A), please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

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1.0 GENERAL DESCRIPTION

The PIC16C55X are 18 and 20-Pin EPROM-based members of the versatile PIC16CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16C55X have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single-cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16C55X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC16C554 and PIC16C556 have 80 bytes of RAM. The PIC16C558 has 128 bytes of RAM. Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler.

PIC16C55X devices have special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake up the chip from SLEEP through several external and internal interrupts and reset.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock- up.

A UV-erasable CERDIP-packaged version is ideal for code development while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C55X mid-range microcontroller families.

A simplified block diagram of the PIC16C55X is shown in Figure 3-1.

The PIC16C55X series fit perfectly in applications ranging from motor control to low-power remote sensors. The EPROM technology makes customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16C55X very versatile.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to PIC16C55X family of devices (Appendix B).

The PIC16C55X family fills the niche for users wanting to migrate up from the PIC16C5X family and not needing various peripheral features of other members of the PIC16XX mid-range microcontroller family.

1.2 Development Support

The PIC16C55X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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TABLE 1-1: PIC16C55X FAMILY OF DEVICES

	Clock	Memory		Peripherals			Features	
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (x 14)	Data Memory (bytes)	Timer Module(s)	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Packages
PIC16C554	20	512	80	TMR0	3	13	2.5-5.5	18-pin DIP, SOIC; 20-pin SSOP
PIC16C556	20	1K	80	TMR0	3	13	2.5-5.5	18-pin DIP, SOIC; 20-pin SSOP
PIC16C558	20	2K	128	TMR0	3	13	2.5-5.5	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC16C55X Family devices use serial programming with clock pin RB6 and data pin RB7.

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2.0 PIC16C55X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in the PIC16C55X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® and PROMATE™ programmers both support programming of the PIC16C55X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C55X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C55X uses a Harvard architecture, in which, program and data are accessed from separate memories using separate busses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data words. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single-cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C554 addresses 512 x 14 on-chip program memory. The PIC16C556 addresses 1K x 14 program memory. The PIC16C558 addresses 2K x 14 program memory. All program memory is internal.

The PIC16C55X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped into the data memory. The PIC16C55X have an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C55X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C55X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit}}$ $\overline{\text{Borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

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FIGURE 3-1: BLOCK DIAGRAM

Device	Program Memory	Data Memory (RAM)
PIC16C554	512 x 14	80 x 8
PIC16C556	1K x 14	80 x 8
PIC16C558	2K x 14	128 x 8

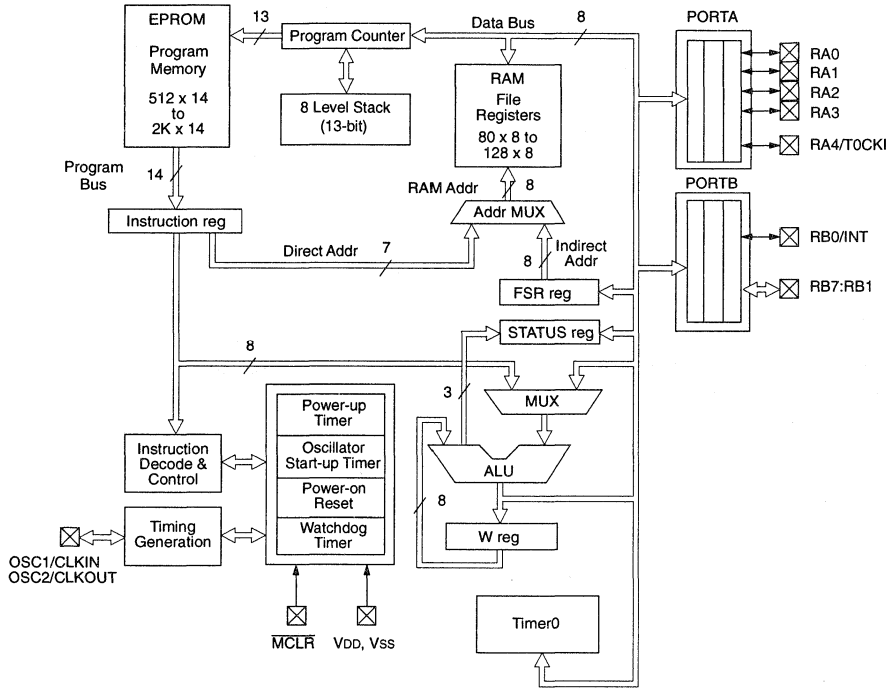

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TABLE 3-1: PIC16C55X PINOUT DESCRIPTION

Name	DIP SOIC Pin #	SSOP Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	I	ST/CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	19	I/O	ST	
RA1	18	20	I/O	ST	
RA2	1	1	I/O	ST	
RA3	2	2	I/O	ST	
RA4/T0CKI	3	3	I/O	ST	Can be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	7	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	Interrupt on change pin.
RB5	11	12	I/O	TTL	Interrupt on change pin.
RB6	12	13	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.
RB7	13	14	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.
VSS	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: O = output I/O = input/output P = power
— = Not used I = Input ST = Schmitt Trigger input
TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
Note 2: This buffer is a Schmitt Trigger input when used in serial programming mode.

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2.

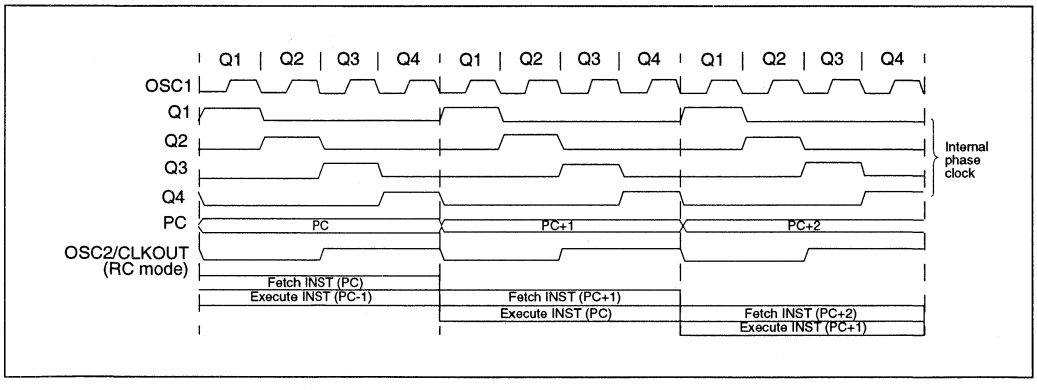
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

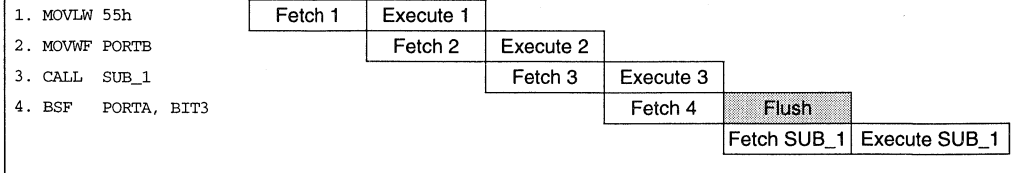
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C55X has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 512 x 14 (0000h - 01FFh) for the PIC16C554, 1K x 14 (0000h - 03FFh) for the PIC16C556 and 2K x 14 (0000h - 07FFh) for the PIC16C558 are physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 512 x 14 space (PIC16C554) or 1K x 14 space (PIC16C556) or 2K x 14 space (PIC16C558). The reset vector is at 0000h and the interrupt vector is at 0004h (Figure 4-1, Figure 4-2, Figure 4-3).

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C554

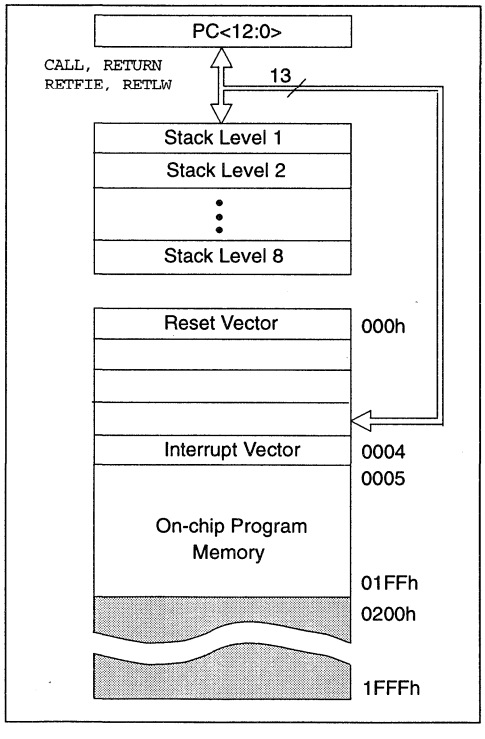


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C556

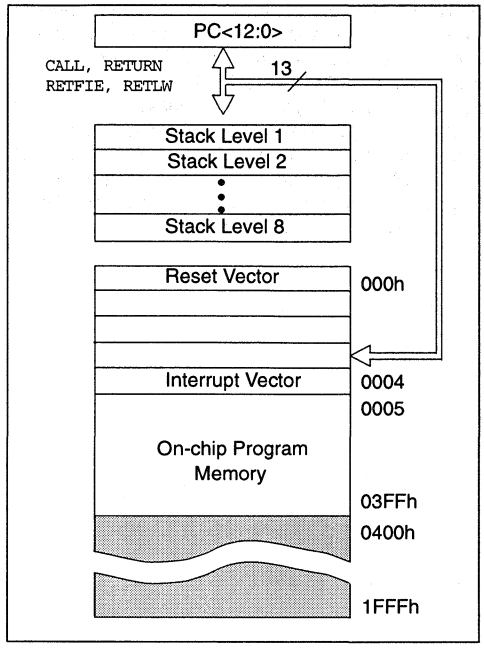
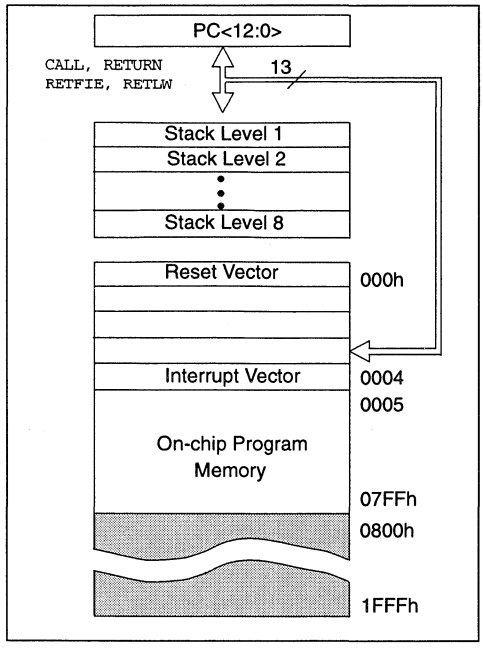


FIGURE 4-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C558



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4.2 Data Memory Organization

The data memory (Figure 4-4 and Figure 4-5) is partitioned into two Banks which contain the general purpose registers and the special function registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each Bank. Register locations 20-6Fh (Bank0) on the PIC16C554/556 and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16C558 are general purpose registers implemented as static RAM. Some special purpose registers are mapped in Bank 1.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 80 x 8 in the PIC16C554/556 and 128 x 8 in the PIC16C558. Each is accessed either directly or indirectly through the File Select Register, FSR (Section 4.4).

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FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C554/556

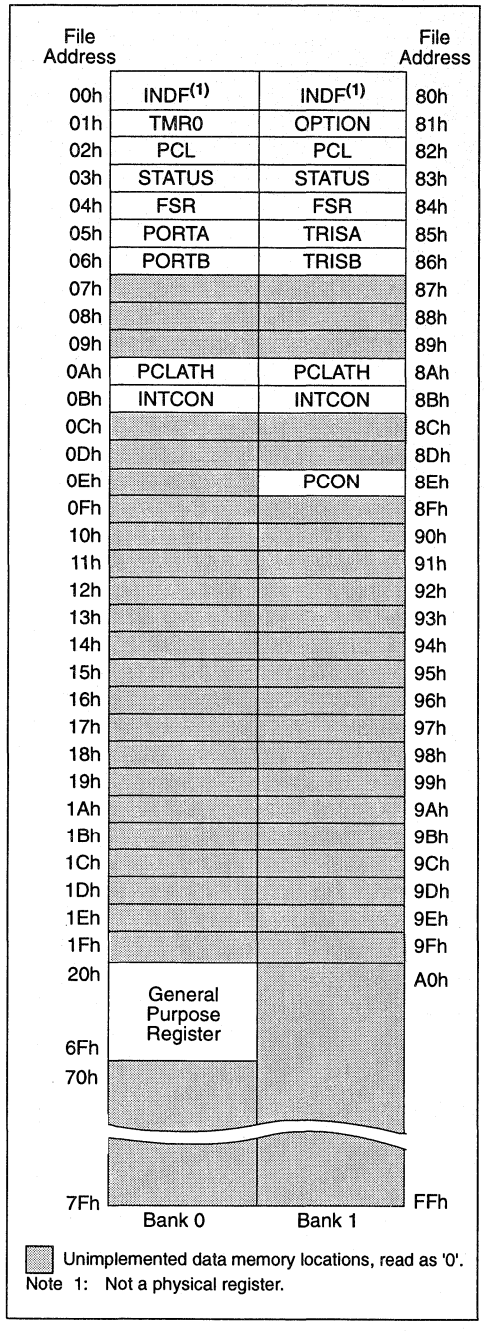
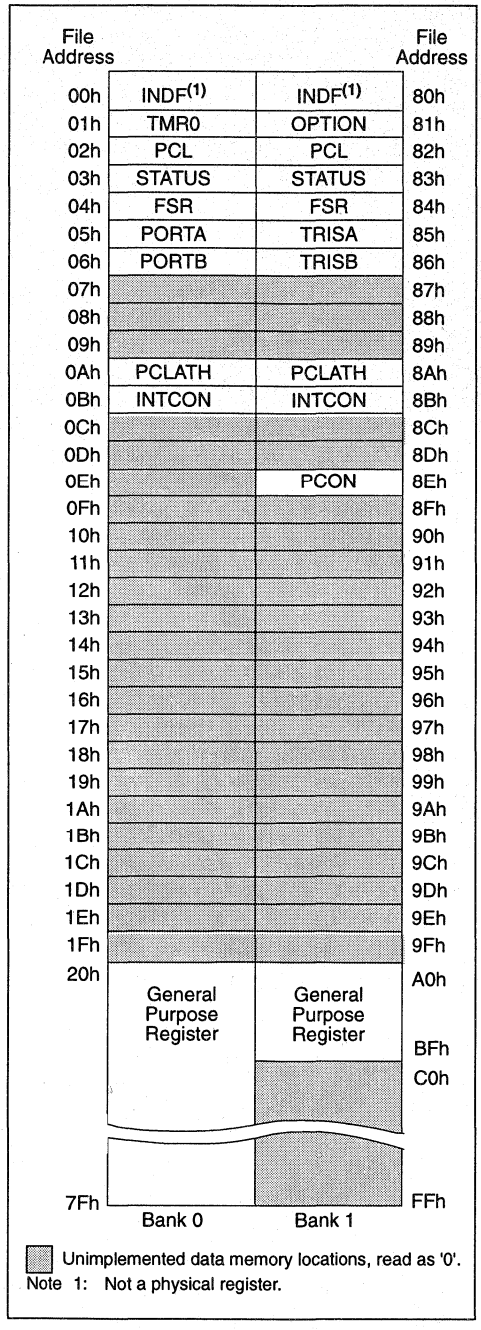


FIGURE 4-5: DATA MEMORY MAP FOR THE PIC16C558



6

4.2.2 SPECIAL FUNCTION REGISTERS

The special function registers are registers used by the CPU and Peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM.

The special function registers can be classified into two sets (core and peripheral). The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C55X

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other resets(1)
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module's Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP(2)	RP1(2)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	Unimplemented									—	—
08h	Unimplemented									—	—
09h	Unimplemented									—	—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
0Bh	INTCON	GIE	(3)	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
0Ch	Unimplemented									—	—
0Dh-1Eh	Unimplemented									—	—
1Fh	Unimplemented									—	—
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	—	—	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h	Unimplemented									—	—
88h	Unimplemented									—	—
89h	Unimplemented									—	—
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
8Bh	INTCON	GIE	(3)	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
8Ch	Unimplemented									—	—
8Dh	Unimplemented									—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	—	---- --0-	---- --u-
8Fh-9Eh	Unimplemented									—	—
9Fh	Unimplemented									—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) resets include $\overline{MCLR}$ reset and Watchdog Timer reset during normal operation.

Note 2: IRP & RPI bits are reserved, always maintain these bits clear.

Note 3: Bit 6 of INTCON register is reserved for future use. Always maintain this bit as clear.

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4.2.2.1 STATUS REGISTER

The STATUS register, shown in Figure 4-6, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as the destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the status register as `000uu1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect any status bits. For other instructions, not affecting any status bits, see the "Instruction Set Summary".

Note 1:	The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C55X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
Note 2:	The C and DC bits operate as a $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 4-6: STATUS REGISTER (ADDRESS 03H OR 83H)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset
- x = Unknown at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)
The IRP bit is reserved on the PIC16C55X, always maintain this bit clear.

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C55X, always maintain this bit clear.

bit 4: $\overline{TO}$: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: $\overline{PD}$: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

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4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT (PSA = 1).

FIGURE 4-7: OPTION REGISTER (ADDRESS 81H)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable and flag bits for all interrupt sources.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-8: INTCON REGISTER (ADDRESS 0BH OR 8BH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	—	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset
- x = Unknown at POR reset

bit 7: **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: — = Reserved for future use. Always maintain this bit clear.

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

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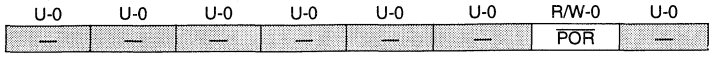
4.2.2.4 PCON REGISTER

The PCON register contains flag bits to differentiate between a Power-on Reset, an external $\overline{MCLR}$ reset or WDT reset. See Section 7.3 and Section 7.4 for detailed reset operation.

FIGURE 4-9: PCON REGISTER (ADDRESS 8Eh)



R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1: **$\overline{POR}$**: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = Power-on Reset occurred

bit 0: **Unimplemented:** Read as '0'

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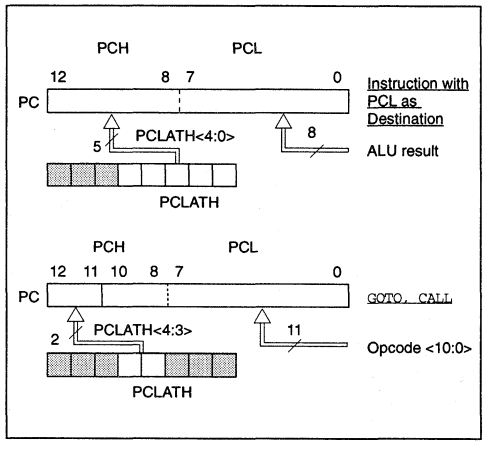
4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high bits (PC<12:8>) are not directly readable or writable and come from PCLATH. On any reset, the PC is cleared. Figure 4-10 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-10: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16C55X family has an 8 level deep x 13-bit wide hardware stack (Figure 4-1, Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or vectoring to an interrupt address.

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4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

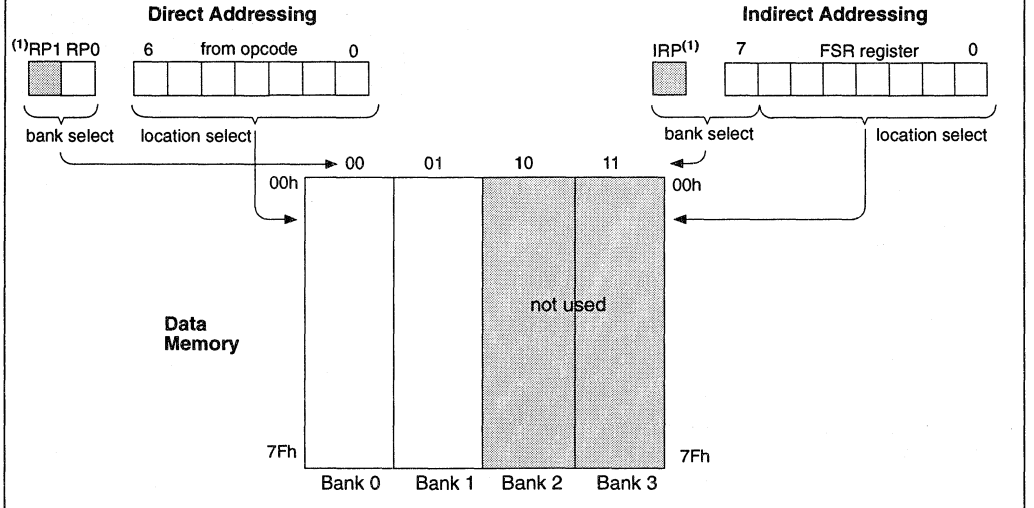
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-11. However, IRP is not used in the PIC16C55X.

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;no clear next
                        ;yes continue
CONTINUE:
```

FIGURE 4-11: DIRECT/INDIRECT ADDRESSING PIC16C55X



For memory map detail see Figure 4-4 and Figure 4-5.

Note 1: The RP1 and IRP bits are reserved, always maintain these bits clear.

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5.0 I/O PORTS

The PIC16C55X have two ports, PORTA and PORTB.

5.1 PORTA and TRISA Registers

PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. Port RA4 is multiplexed with the T0CKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as input or output.

A '1' in the TRISA register puts the corresponding output driver in a hi- impedance mode. A '0' in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Note: On reset, the TRISA register is set to all inputs.

FIGURE 5-1: BLOCK DIAGRAM OF PORT PINS RA<3:0>

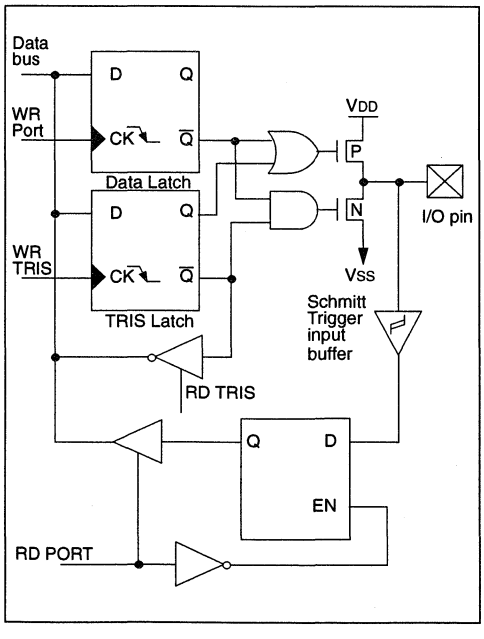
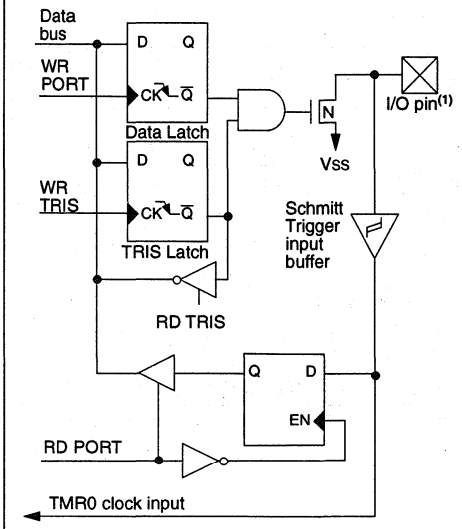


FIGURE 5-2: BLOCK DIAGRAM OF RA4 PIN



Note 1: I/O pin has protection diodes to Vss only.

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TABLE 5-1: PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0	bit0	ST	Input/output
RA1	bit1	ST	Input/output
RA2	bit2	ST	Input/output
RA3	bit3	ST	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: — = Unimplemented locations, read as '0'

Note: Note: Shaded bits are not used by PORTA.

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5.2 PORTB and TRISB Registers

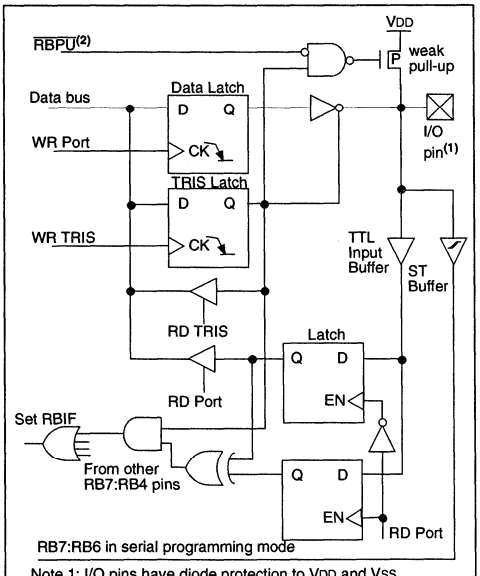
PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a high impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up (≈200 µA typical). A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBPU}}$ (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

FIGURE 5-3: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: I/O pins have diode protection to VDD and VSS.

Note 2: TRISB = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

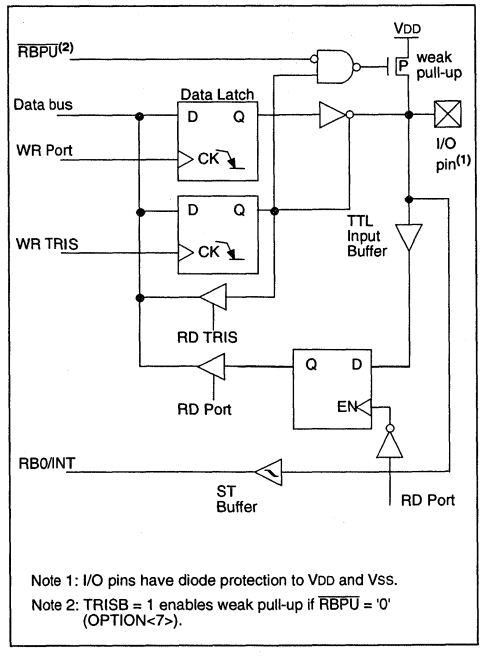
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552 in the Microchip *Embedded Control Handbook*.)

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-4: BLOCK DIAGRAM OF RB3:RB0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.

Note 2: TRISB = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

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TABLE 5-3: PORTB FUNCTIONS

Name	Bit #	Buffer Type	Function
RB0/INT	bit0	TTL/ST(1)	Input/output or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock pin.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data pin.

Legend: ST = Schmitt Trigger, TTL = TTL input
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
Note 2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Rests
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Note: Shaded bits are not used by PORTB.

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5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read modify write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-1 shows the effect of two sequential read-modify-write instructions (ex., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

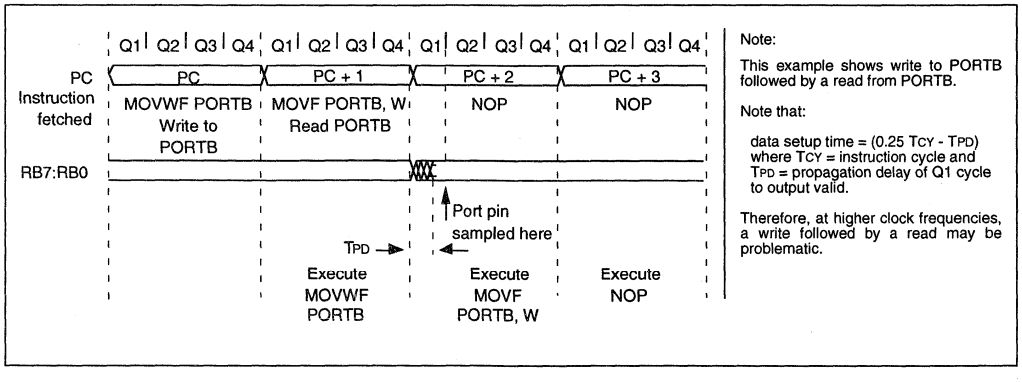
```
; Initial PORT settings:     PORTB<7:4> Inputs
;
;                            PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are not
; connected to other circuitry
;
;                            PORT latch  PORT pins
;                            ----------  ----------

    BCF  PORTB, 7          ; 01pp pppp   11pp pppp
    BCF  PORTB, 6          ; 10pp pppp   11pp pppp
    BSF  STATUS,RP0        ;
    BCF  TRISB, 7          ; 10pp pppp   11pp pppp
    BCF  TRISB, 6          ; 10pp pppp   10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused
; RB7 to be latched as the pin value (High).
```

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with an NOP or another instruction not accessing this I/O port.

6

FIGURE 5-5: SUCCESSIVE I/O OPERATION



NOTES:

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6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

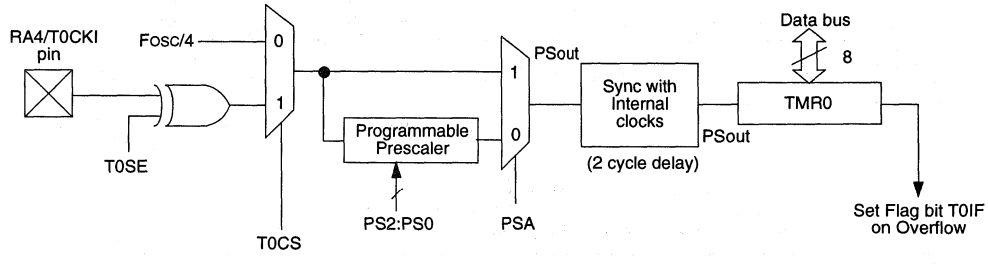
Counter mode is selected by setting the T0CS bit. In this mode Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the WatchdogTimer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

6.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits, T0SE, T0CS, PS2, PS1, PS0 and PSA are located in the OPTION register.
2: The prescaler is shared with Watchdog Timer (Figure 6-6)

FIGURE 6-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER

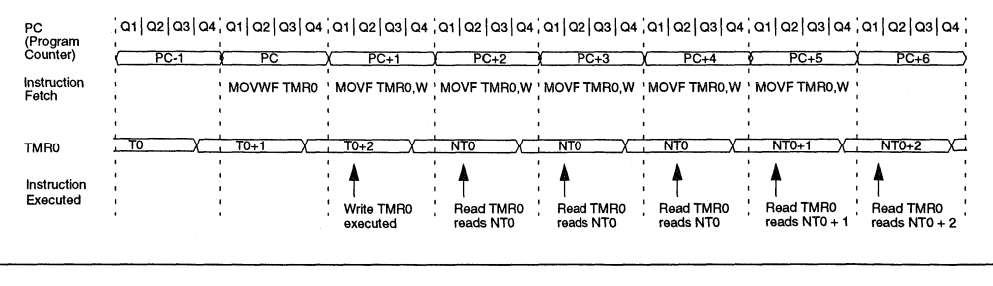


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

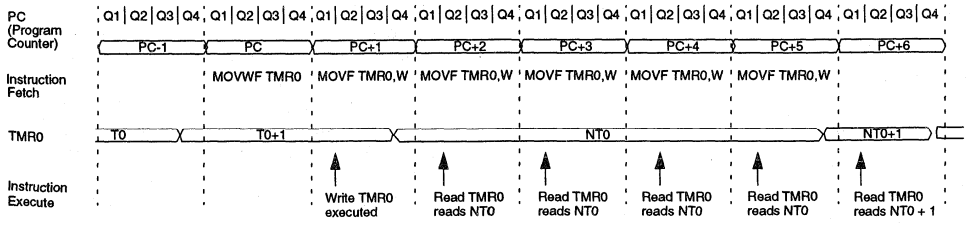
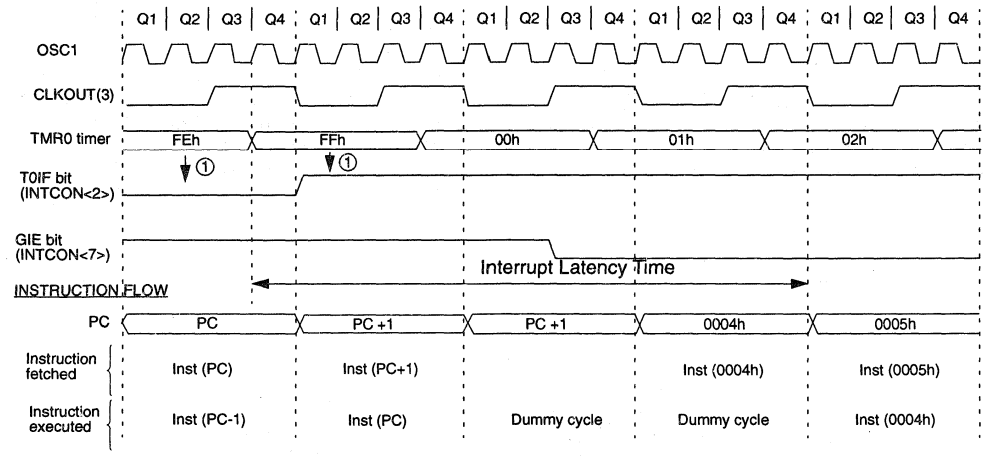


FIGURE 6-4: TIMER0 INTERRUPT TIMING



Note 1: T0IF interrupt flag is sampled here (every Q1).
2: Interrupt latency = 4Tcy, where Tcy = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.

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6.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

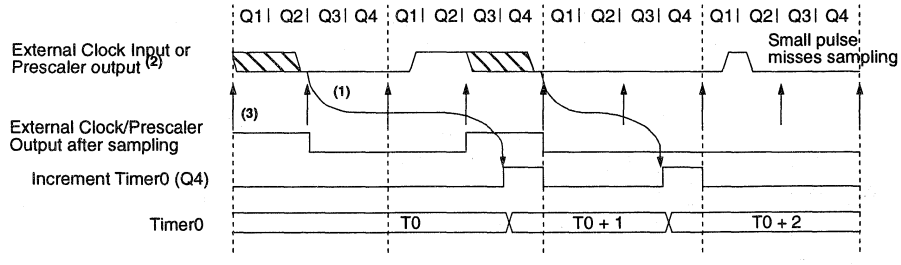
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

6

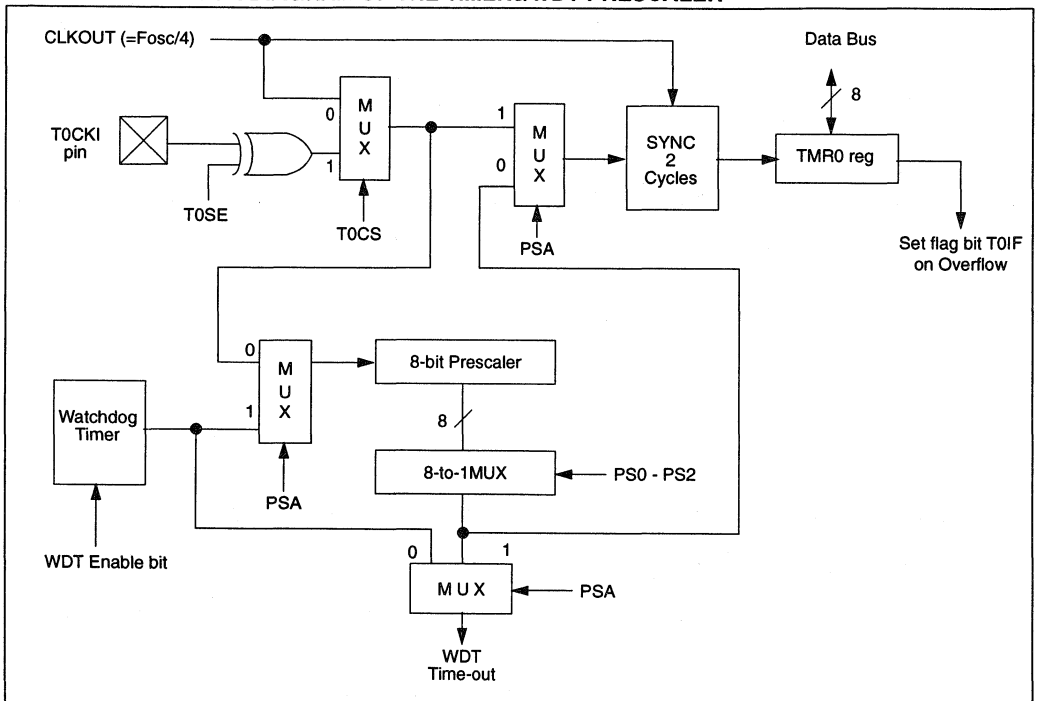
6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0SE, T0CS, PSA, PS0-PS2 are bits in the OPTION register.

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6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to WDT. Lines 5-7 are required only if the desired postscaler rate is 1:1 (PS<2:0> = 000) or 1:2 (PS<2:0> = 001).

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
 1. BCF     STATUS, RP0   ;Skip if already in
                          ; Bank 0
 2. CLRWDT                ;Clear WDT
 3. CLRF    TMR0          ;Clear TMR0 & Prescaler
 4. BSF     STATUS, RP0   ;Bank 1
 5. MOVLW   '00101111'b;  ;These 3 lines (5, 6, 7)
 6. MOVWF   OPTION        ; are required only if
                          ; desired PS<2:0> are
 7. CLRWDT                ; 000 or 001
 8. MOVLW   '00101xxx'b   ;Set Postscaler to
 9. MOVWF   OPTION        ; desired WDT rate
10. BCF     STATUS, RP0   ;Return to Bank 0
```

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 6-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                   ;Clear WDT and
                         ;prescaler
BSF     STATUS, RP0
MOVLW   b'xxxx0xxx'      ;Select TMR0, new
                         ;prescale value and
                         ;clock source
MOVWF   OPTION
BCF     STATUS, RP0
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	+	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: — = Unimplemented locations, read as '0'.
+ = Reserved for future use.

Note: Shaded bits are not used by TMR0 module.

NOTES:

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7.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC16C55X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

1. OSC selection
2. Reset
   Power-on Reset (POR)
   Power-up Timer (PWRT)
   Oscillator Start-Up Timer (OST)
3. Interrupts
4. Watchdog Timer (WDT)
5. SLEEP
6. Code protection
7. ID Locations
8. In-circuit serial programming

The PIC16C55X has a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two functions on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

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7.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h – 3FFFh), which can be accessed only during programming.

FIGURE 7-1: CONFIGURATION WORD

CP1	CP0	CP1	CP0	CP1	CP0	—	Reserved	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

CONFIG Address
REGISTER: 2007h

bit 13-8 **CP<1:0>:** Code protection bits(1)
5-4: 11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 7: **Unimplemented**: Read as '1'

bit 6: **Reserved:** Do not use

bit 3: **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

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7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

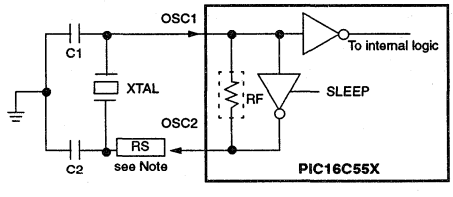
The PIC16C55X can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 7-2). The PIC16C55X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 7-3).

FIGURE 7-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 7-1 and Table 7-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 7-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

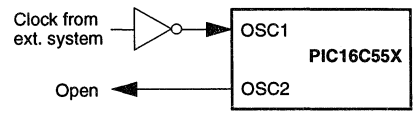


TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS (PRELIMINARY)

Ranges Characterized:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	22 - 100 pF 15 - 68 pF 15 - 68 pF	22 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF

Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

Resonators to be Characterized:		
455 kHz	Panasonic EFO-A455K04B	±0.3%
2.0 MHz	Murata Erie CSA2.00MG	±0.5%
4.0 MHz	Murata Erie CSA4.00MG	±0.5%
8.0 MHz	Murata Erie CSA8.00MT	±0.5%
16.0 MHz	Murata Erie CSA16.00MX	±0.5%

All resonators used did not have built-in capacitors.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR (PRELIMINARY)

Mode	Freq	OSC1	OSC2
LP	32 kHz 200 kHz	68 - 100 pF 15 - 30 pF	68 - 100 pF 15 - 30 pF
XT	100 kHz 2 MHz 4 MHz	68 - 150 pF 15 - 30 pF 15 - 30 pF	150 - 200 pF 15 - 30 pF 15 - 30 pF
HS	8 MHz 10 MHz 20 MHz	15 - 30 pF 15 - 30 pF 15 - 30 pF	15 - 30 pF 15 - 30 pF 15 - 30 pF

Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Crystals to be Characterized:		
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM
200 kHz	STD XTL 200.000 kHz	± 20 PPM
2.0 MHz	ECS ECS-20-S-2	± 50 PPM
4.0 MHz	ECS ECS-40-S-4	± 50 PPM
10.0 MHz	ECS ECS-100-S-4	± 50 PPM
20.0 MHz	ECS ECS-200-S-4	± 50 PPM

6

7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a pre-packaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 7-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 7-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

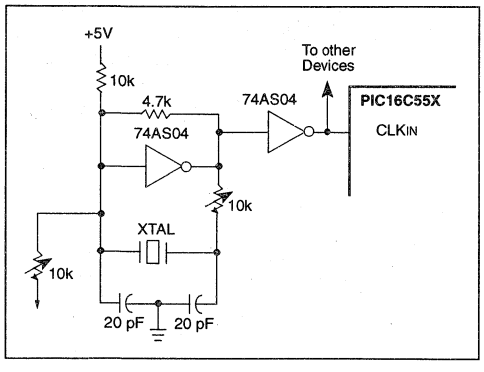
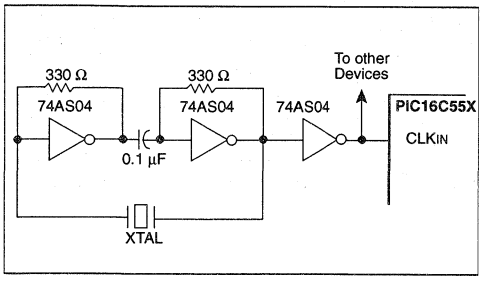


Figure 7-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



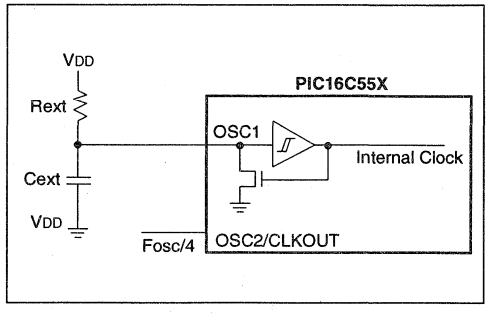
7.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 7-6 shows how the R/C combination is connected to the PIC16C55X. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kΩ and 100 kΩ.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

FIGURE 7-6: RC OSCILLATOR MODE



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7.3 Reset

The PIC16C55X differentiates between various kinds of reset:

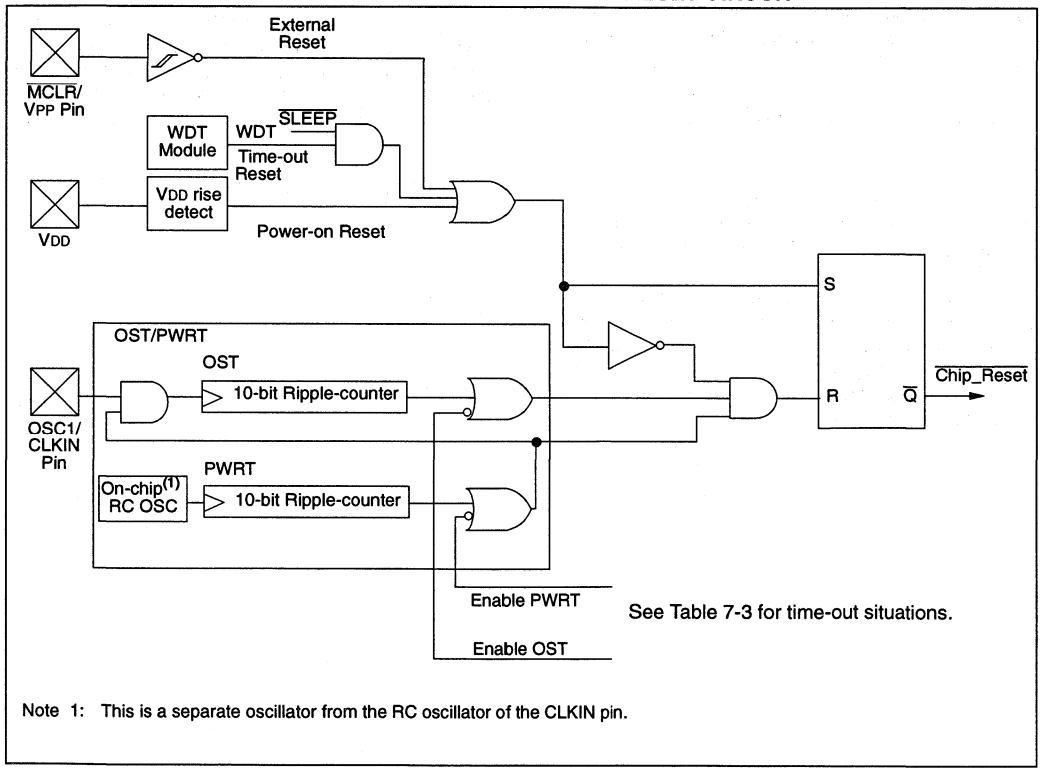
a) Power-on reset (POR)
b) $\overline{MCLR}$ reset during normal operation
c) $\overline{MCLR}$ reset during SLEEP
d) WDT reset (normal operation)
e) WDT wake-up (SLEEP)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on reset, on $\overline{MCLR}$ or WDT reset and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 7-4. These bits are used in software to determine the nature of the reset. See Table 7-6 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 7-7.

The $\overline{MCLR}$ reset path has a noise filter to detect and ignore small pulses. See Table 8-4 for pulse width specification.

FIGURE 7-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.

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7.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)

7.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.6 V – 1.8 V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce internal reset when VDD declines.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607 "Power-up Trouble Shooting".

7.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, $\overline{PWRTE}$ can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-Up Time delay will vary from chip to chip and due to VDD, temperature and process variation. See DC parameters for details.

7.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on power-on reset or wake-up from SLEEP.

7.4.4 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired, then OST is activated. The total time-out will vary based on oscillator configuration and $\overline{PWRTE}$ bit status. For example, in RC mode with $\overline{PWRTE}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 7-8, Figure 7-9 and Figure 7-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (see Figure 7-9). This is useful for testing purposes or to synchronize more than one PIC16C55X device operating in parallel.

Table 7-5 shows the reset conditions for some special registers, while Table 7-6 shows the reset conditions for all the registers.

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7.4.5 POWER CONTROL/STATUS REGISTER (PCON)

Bit1 is $\overline{POR}$ (Power-on-reset). It is a '0' on power-on-reset and unaffected otherwise. The user must write a '1' to this bit following a power-on-reset. On a subsequent reset if $\overline{POR}$ is '0', it will indicate that a power-on-reset must have occurred (V_{DD} may have gone too low).

TABLE 7-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1	
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	1024 Tosc
RC	72 ms	—	—

TABLE 7-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{TO}$	$\overline{PD}$	
0	1	1	Power-on-reset
0	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	1	WDT Reset
1	0	0	WDT Wake-up
1	1	1	$\overline{MCLR}$ reset during normal operation
1	1	0	$\overline{MCLR}$ reset during SLEEP

TABLE 7-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0-
$\overline{MCLR}$ reset during normal operation	000h	0001 1uuu	---- --u-
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	---- --u-
WDT reset	000h	0000 1uuu	---- --u-
WDT Wake-up	PC + 1	uuu0 0uuu	---- --u-
Interrupt Wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.
Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 7-6: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	• MCLR Reset during normal operation • MCLR Reset during SLEEP • WDT Reset	• Wake up from SLEEP through interrupt • Wake up from SLEEP through WDT time-out
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1(2)
STATUS	03h	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---x xxxx	---u uuuu	---u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000x	uuuu uuuu(1)
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
PCON	8Eh	---- --0-	---- --u-	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.
Note 1: One or more bits in INTCON will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: See Table 7-5 for reset value for specific condition.

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FIGURE 7-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

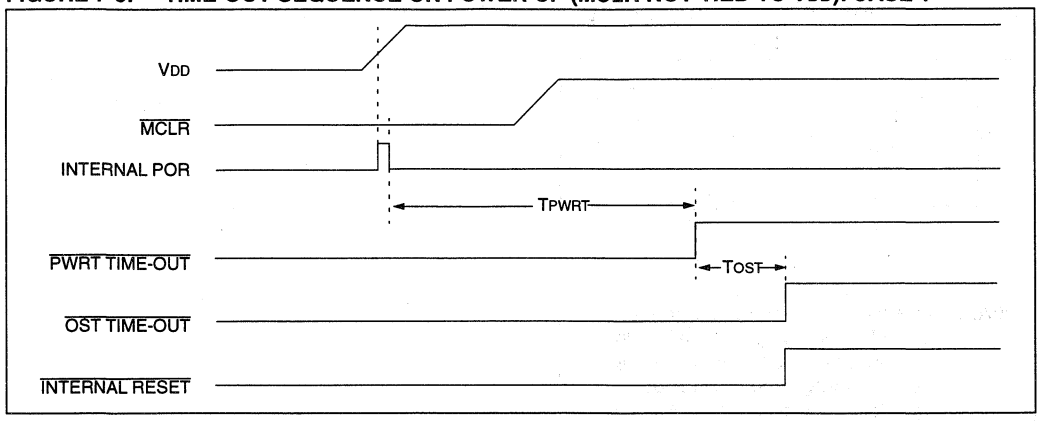

FIGURE 7-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

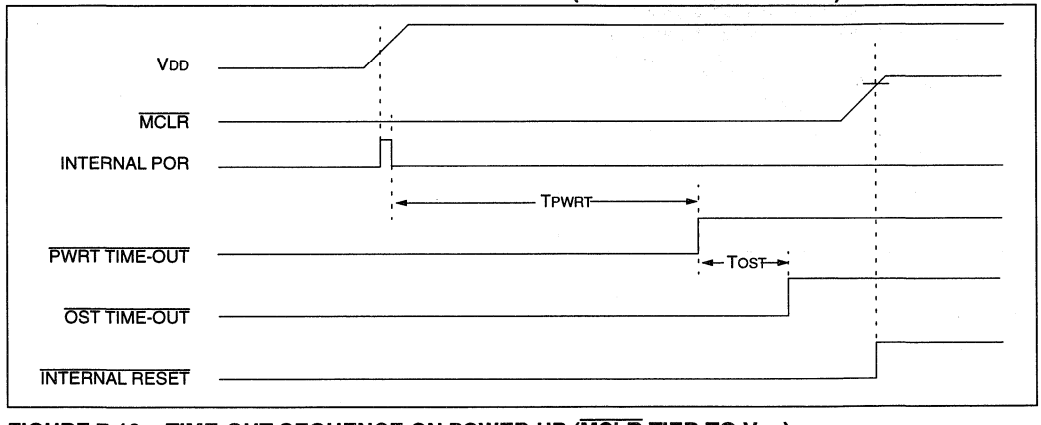

FIGURE 7-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

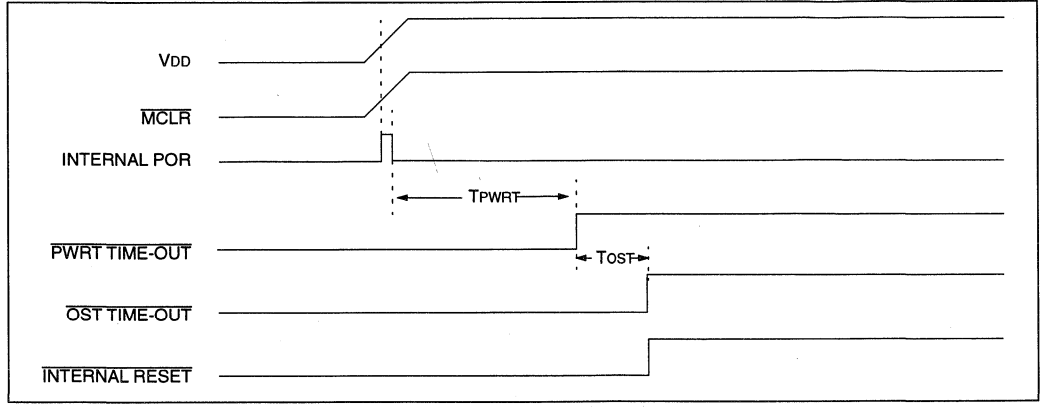

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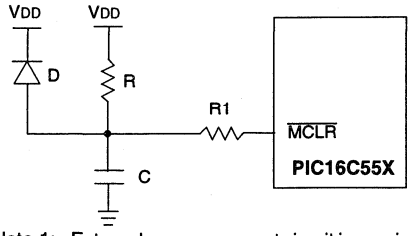
FIGURE 7-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External power-on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

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7.5 Interrupts

The PIC16C55X has 3 sources of interrupt:

- External interrupt RB0/INT
- TMR0 overflow interrupt
- PortB change interrupts (pins RB7:RB4)

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enables RB0/INT interrupts.

The INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid RB0/INT recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 7-13). The latency is the same for one or two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The CPU will execute a NOP in the cycle immediately following the instruction which clears the GIE bit. The interrupts which were ignored are still pending to be serviced when the GIE bit is set again.

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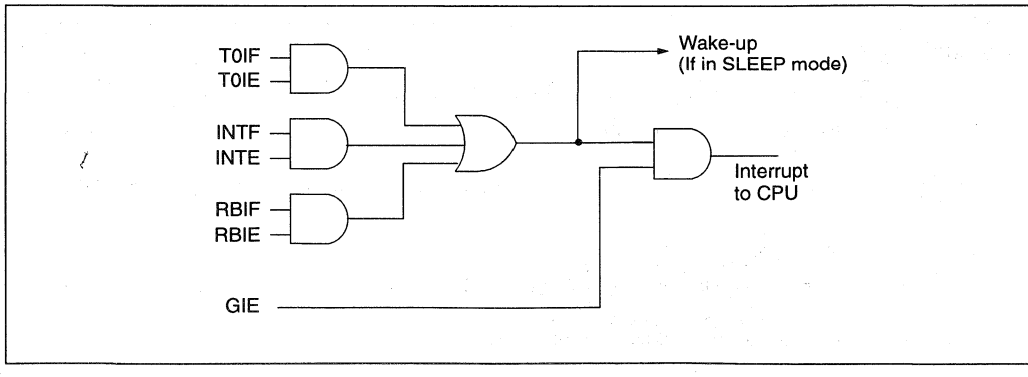
FIGURE 7-12: INTERRUPT LOGIC



7.5.1 RB0/INT INTERRUPT

An external interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION<6>) is set, or falling if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 7.8 for details on SLEEP and Figure 7-16 for timing of wake-up from SLEEP through RB0/INT interrupt.

7.5.2 TMR0 INTERRUPT

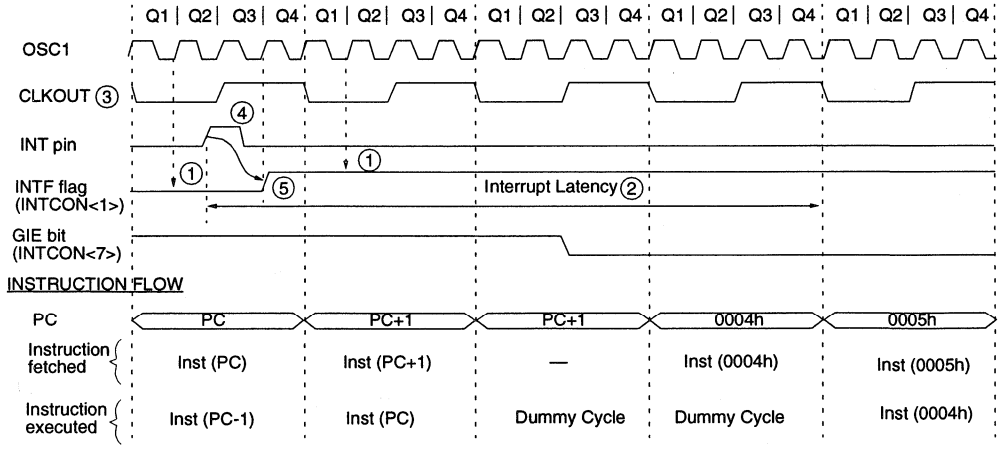
An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 6.0.

7.5.3 PORTB INTERRUPT

An input change on PORTB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB (Section 5.2).

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may get set.

FIGURE 7-13: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

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7.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, e.g. W register and STATUS register. This will have to be implemented in software.

Example 7-1 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 7-1:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

EXAMPLE 7-1: SAVING THE STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP          ;copy W to temp register,
                        ;could be in either bank
SWAPF   STATUS,W        ;swap status to be saved into W
BCF     STATUS,RP0      ;change to bank 0 regardless
                        ;of current bank
MOVWF   STATUS_TEMP     ;save status to bank 0
                        ;register
    :
    :   (ISR)
    :
SWAPF   STATUS_TEMP,W   ;swap STATUS_TEMP register
                        ;into W, sets bank to original
                        ;state
MOVWF   STATUS          ;move W into STATUS register
SWAPF   W_TEMP,F        ;swap W_TEMP
SWAPF   W_TEMP,W        ;swap W_TEMP into W
```

7.7 Watchdog Timer (WDT)

The watchdog timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 7.1).

7.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

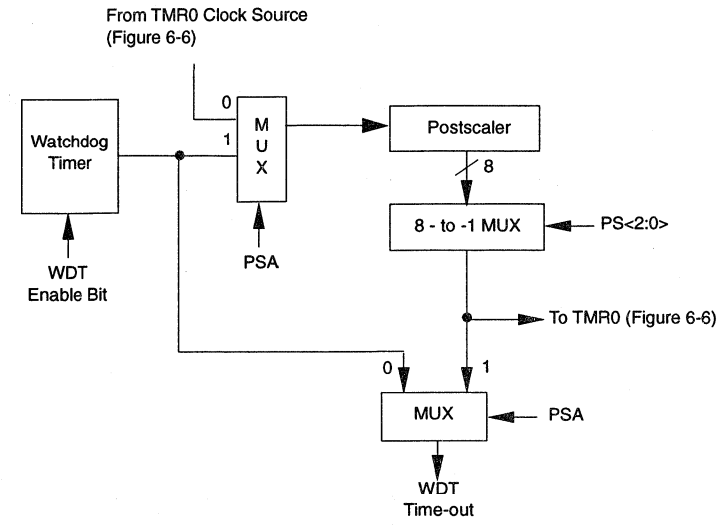
The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

7.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 7-14: WATCHDOG TIMER BLOCK DIAGRAM



Note: T0SE, T0CS, PSA, PS0-PS2 are bits in the OPTION register.

FIGURE 7-15: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	—	+	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.
— = Unimplemented location, read as '0'.
+ = Reserved for future use.

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7.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

Note: It should be noted that a RESET generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.

7.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from RB0/INT pin or RB Port change

The first event will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. $\overline{TO}$ bit is cleared if WDT Wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wakeup from sleep. The sleep instruction is completely executed.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

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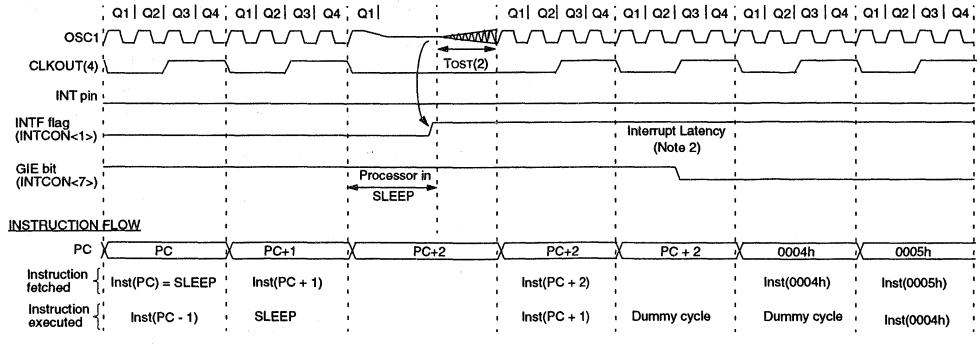
FIGURE 7-16: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

7.9 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

7.10 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. Only the least significant 4 bits of the ID locations are used.

7.11 In-Circuit Serial Programming

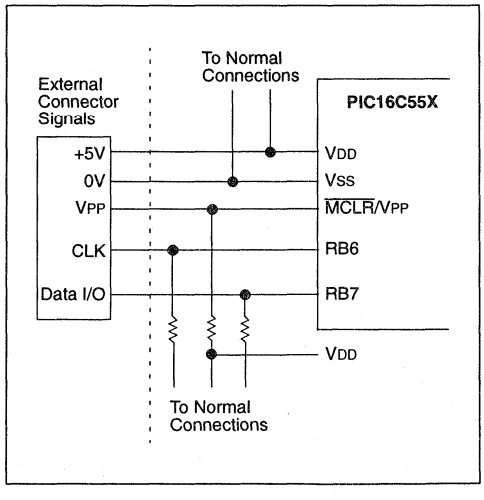
The PIC16C55X microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

A typical in-circuit serial programming connection is shown in Figure 7-17.

FIGURE 7-17: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



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8.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias ..... -40° to +125°C

Storage Temperature ..... -65° to +150°C

Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.6V to VDD +0.6V

Voltage on VDD with respect to VSS ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V

Total power Dissipation (Note 1) 1.0W

Maximum Current out of VSS pin ..... 300 mA

Maximum Current into VDD pin ..... 250 mA

Input Clamp Current, IIK (VI<0 or VI> VDD) ..... ±20 mA

Output Clamp Current, IOK (VO <0 or VO>VDD) ..... ±20 mA

Maximum Output Current sunk by any I/O pin ..... 25 mA

Maximum Output Current sourced by any I/O pin ..... 25 mA

Maximum Current sunk by PORTA and PORTB ..... 200 mA

Maximum Current sourced by PORTA and PORTB ..... 200 mA

Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ(VOl x IOL)

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 8-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C55X-04	PIC16C55X-20	PIC16LC55X-04	PIC16C55X/JW
RC	VDD: 3.0V to 5.5V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 4.0 MHz max.	VDD: 3.0V to 5.5V IDD: 1.4 mA typ. @3.0V IPD: 0.7 µA typ. @3.0V Freq: 4.0 MHz max.	VDD: 3.0V to 5.5V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz Max.
XT	VDD: 3.0V to 5.5V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 4.0 MHz max.	VDD: 3.0V to 5.5V IDD: 1.4 mA typ. @3.0V IPD: 0.7 µA typ. @3.0V Freq: 4.0 MHz max.	VDD: 3.0V to 5.5V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 9.0 mA typ. @5.5V IPD: 1.0 µA typ. @4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 20 MHz max.
LP	VDD: 3.0V to 5.5V IDD: 35 µA typ. @32 kHz, 3.0V IPD: 1.0 µA typ. @4.0 V Freq: 200 kHz maximum	Do not use in LP mode	VDD: 2.5V to 5.5V IDD: 32 µA max. @32 kHz, 3.0V IPD: 9.0 µA max. @3.0V Freq: 200 kHz max.	VDD: 2.5V to 5.5V IDD: 32 µA max. @32 kHz, 3.0V IPD: 9.0 µA Max. @3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that guarantees the specifications required.

8.1 DC CHARACTERISTICS: PIC16C55X-04 (Commercial, Industrial, Automotive) PIC16C55X-20 (Commercial, Industrial, Automotive)

Standard Operating Conditions (unless otherwise stated)
Operating temperature $-40°C \le T_A \le +85°C$ for industrial and
$0°C \le T_A \le +70°C$ for commercial and
$-40°C \le T_A \le +125°C$ for automotive

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0	-	5.5	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002	VDR	RAM Data Retention Voltage (Note 1)	–	1.5*	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	–	VSS	–	V	See section on power-on reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	–	–	V/ms	See section on power-on reset for details
D010	IDD	Supply Current (Note 2)	–	1.8	3.3	mA	XT and RC osc configuration FOSC = 4 MHz, VDD = 5.5V, WDT disabled (Note 4)
D010A			–	35	70	µA	LP osc configuration, PIC16C55X-04 only FOSC = 32 kHz, VDD = 4.0V, WDT disabled
D013			–	9.0	20	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V, WDT disabled
	ΔIWDT	WDT Current (Note 5)	–	6.0	20	µA	VDD = 4.0V
					25	µA	(+85°C to +125°C)
D020	IPD	Power Down Current (Note 3)	–	1.0	2.5	µA	VDD=4.0V, WDT disabled
					15	µA	(+85°C to +125°C)
	ΔIWDT	WDT Current (Note 5)	–	6.0	20	µA	VDD=4.0V (+85°C to +125°C)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins configured as input, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins configured as input and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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8.2 DC CHARACTERISTICS: PIC16LC55X-04 (Commercial, Industrial, Automotive)

Standard Operating Conditions (unless otherwise stated)
Operating temperature –40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial and
–40°C ≤ TA ≤ +125°C for automotive

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0 2.5	-	5.5 5.5	V	XT and RC osc configuration LP osc configuration
D002	VDR	RAM Data Retention Voltage (Note 1)	–	1.5*	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	–	VSS	–	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	–	–	V/ms	See section on Power-on Reset for details
D010	IDD	Supply Current (Note 2)	–	1.4	2.5	mA	XT and RC osc configuration FOSC = 2.0 MHz, VDD = 3.0V, WDT disabled (Note 4)
D010A			–	26	53	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
	ΔIWDT	WDT Current (Note 5)	–	6.0	15	µA	VDD = 3.0V
D020	IPD	Power Down Current (Note 3)	–	0.7	2	µA	VDD=3.0V, WDT disabled
	ΔIWDT	WDT Current (Note 5)	–	6.0	15	µA	VDD=3.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins configured as input, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins configured as input and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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8.3 DC CHARACTERISTICS: PIC16C55X (Commercial, Industrial, Automotive) PIC16LC55X (Commercial, Industrial, Automotive)

Standard Operating Conditions (unless otherwise stated)
Operating temperature –40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial and
–40°C ≤ TA ≤ +125°C for automotive
Operating voltage VDD range as described in DC spec Table 8-1 and Table 8-2

Param. No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	-	0.8V 0.15VDD	V	VDD = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	VSS		0.2VDD	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)	VSS	-	0.2VDD	V	Note1
D033		OSC1 (in XT* and HS)	VSS	-	0.3VDD	V	
		OSC1 (in LP*)	VSS	-	0.6VDD-1.0	V	
	VIH	**Input High Voltage**					
		I/O ports		-			
D040		with TTL buffer	2.0V	-	VDD	V	
D041		with Schmitt Trigger input	0.8VDD		VDD		
D042		$\overline{MCLR}$ RA4/T0CKI	0.8VDD	-	VDD	V	
D043		OSC1 (XT*, HS and LP*)	0.7VDD	-	VDD	V	
D043A		OSC1 (in RC mode)	0.9VDD				Note1
D070	IPURB	PORTB weak pull-up current	50	200	400	µA	VDD = 5.0V, VPIN = VSS
	IIL	**Input Leakage Current** (Notes 2, 3)					
		I/O ports (Except PORTA)			±1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D060		PORTA	-	-	±0.5	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D061		RA4/T0CKI	-	-	±1.0	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1, $\overline{MCLR}$	-	-	±5.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	**Output Low Voltage**					
D080		I/O ports	-	-	0.6	V	IOL=8.5 mA, VDD=4.5V, -40° to +85°C
			-	-	0.6	V	IOL=7.0 mA, VDD=4.5V, +125°C
D083		OSC2/CLKOUT	-	-	0.6	V	IOL=1.6 mA, VDD=4.5V, -40° to +85°C
		(RC only)	-	-	0.6	V	IOL=1.2 mA, VDD=4.5V, +125°C
	VOH	**Output High Voltage** (Note 3)					
D090		I/O ports (Except RA4)	VDD-0.7	-	-	V	IOH=-3.0 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	-	-	V	IOH=-2.5 mA, VDD=4.5V, +125°C
D092		OSC2/CLKOUT	VDD-0.7	-	-	V	IOH=-1.3 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	-	-	V	IOH=-1.0 mA,
		(RC only)					VDD=4.5V, +125°C
*	VOD	**Open-Drain High Voltage**			14*	V	RA4 pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C55X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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8.3 DC CHARACTERISTICS: PIC16C55X (Commercial, Industrial, Automotive) PIC16LC55X (Commercial, Industrial, Automotive) (Cont.)

		Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for automotive Operating voltage VDD range as described in DC spec Table 8-1 and Table 8-2					
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Unit**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	CIO	All I/O pins/OSC2 (in RC mode)			50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C55X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

8.4 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

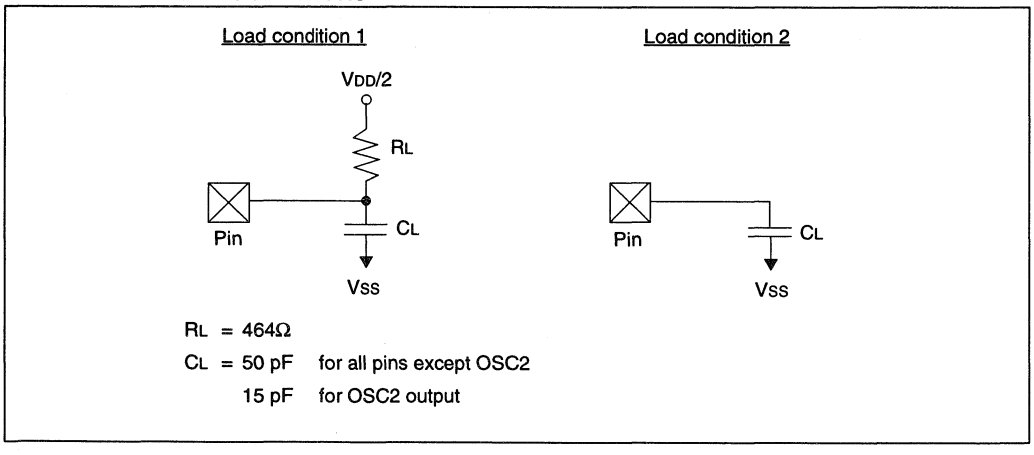
Lowercase subscripts (pp) and their meanings:

pp			
ck	CLKOUT	os	OSC1
io	I/O port	t0	T0CKI
mc	$\overline{\text{MCLR}}$		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-Impedance

FIGURE 8-1: LOAD CONDITIONS



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8.5 Timing Diagrams and Specifications

FIGURE 8-2: EXTERNAL CLOCK TIMING

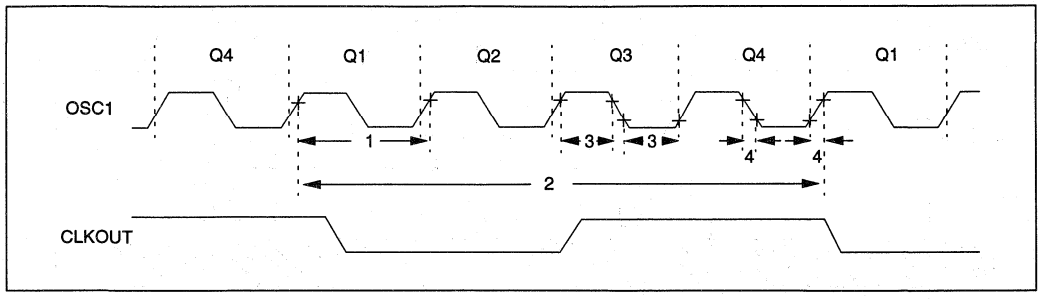

TABLE 8-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode, VDD=5.0V
			DC	—	20	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode, VDD=5.0V
			0.1	—	4	MHz	XT osc mode
			1	—	20	MHz	HS osc mode
			DC	–	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			50	—	—	ns	HS osc mode
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			50	—	1,000	ns	HS osc mode
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	1.0	Fos/4	DC	µs	TCY=FOS/4
3*	TosL, TosH	External Clock in (OSC1) High or Low Time	100*	—	—	ns	XT osc mode
			2*	—	—	µs	LP osc mode
			20*	—	—	ns	HS osc mode
4*	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	25*	—	—	ns	XT osc mode
			50*	—	—	ns	LP osc mode
			15*	—	—	ns	HS osc mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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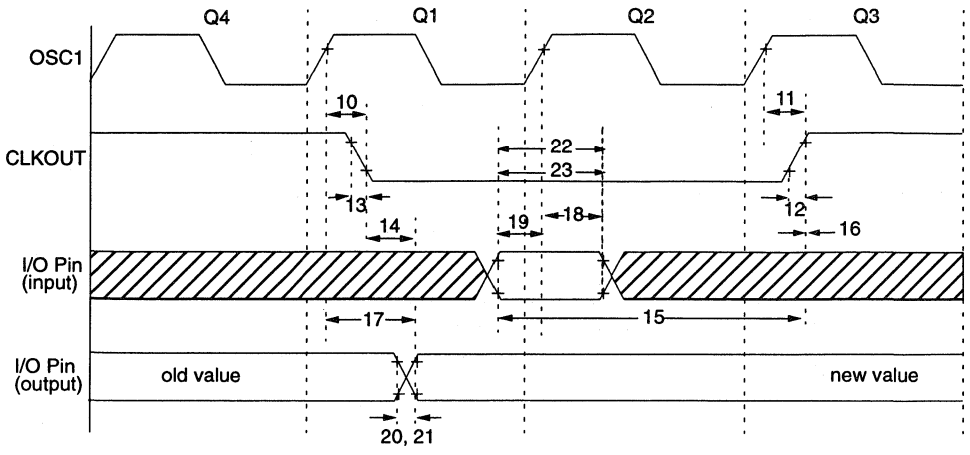
FIGURE 8-3: CLKOUT AND I/O TIMING



Note: All tests must be do with specified capacitance loads (Figure 8-1) 50 pF on I/O pins and CLKOUT

TABLE 8-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter #	Sym	Characteristic	Min	Typ†	Max	Units
10*	TosH2ckL	OSC1↑ to CLKOUT↓ (Note1)	— —	75 —	200 400	ns ns
11*	TosH2ckH	OSC1↑ to CLKOUT↑ (Note1)	— —	75 —	200 400	ns ns
12*	TckR	CLKOUT rise time (Note1)	— —	35 —	100 200	ns ns
13*	TckF	CLKOUT fall time (Note1)	— —	35 —	100 200	ns ns
14*	TckL2ioV	CLKOUT ↓ to Port out valid (Note1)	—	—	20	ns
15*	TioV2ckH	Port in valid before CLKOUT ↑ (Note1)	Tosc +200 ns Tosc +400 ns	— —	— —	ns ns
16*	TckH2iol	Port in hold after CLKOUT ↑ (Note1)	0	—	—	ns
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	— —	50	150 300	ns ns
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	— —	— —	ns ns
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns
20*	TioR	Port output rise time	— —	10 —	40 80	ns ns
21*	TioF	Port output fall time	— —	10 —	40 80	ns ns
22*	Tinp	RB0/INT pin high or low time	25 40	— —	— —	ns ns
23	Trbp	RB<7:4> change interrupt high or low time	Tcy	—	—	ns

* These parameters are characterized but not tested

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC

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FIGURE 8-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

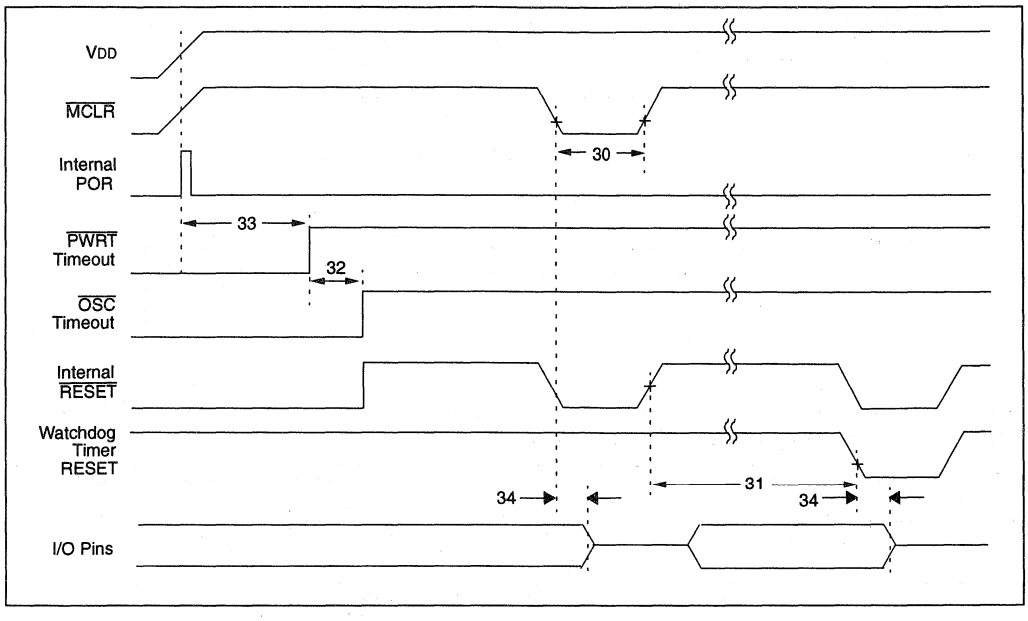


TABLE 8-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2000	—	—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 Tosc	—	—	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	TIOZ	I/O hi-impedance from MCLR low		—	2.0	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 8-5: TIMER0 CLOCK TIMING

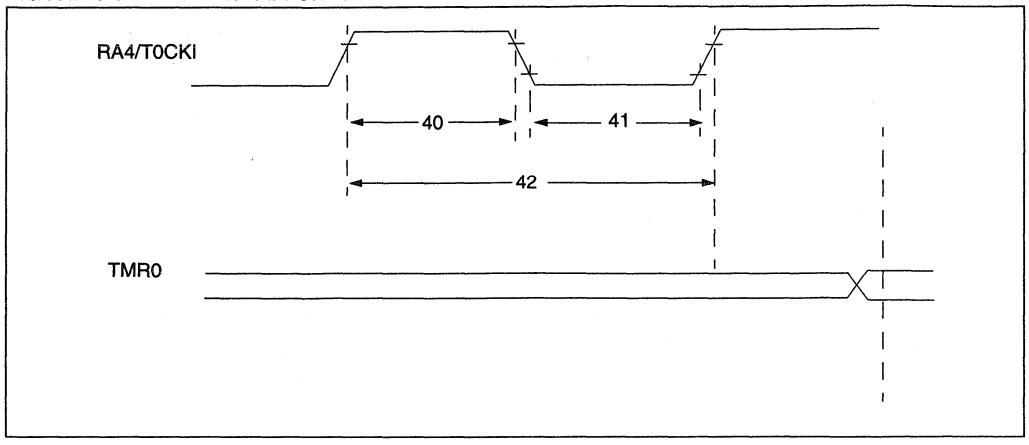


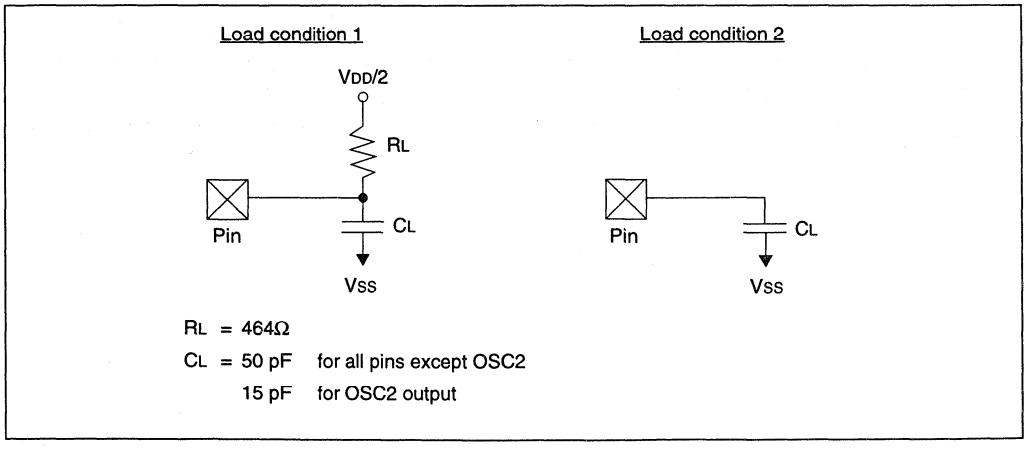
TABLE 8-5: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		TCY + 40* / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 8-6: LOAD CONDITIONS



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APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
3. Data memory paging is slightly redefined. STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revised. Three different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
14. FSR is made a full 8-bit register.
15. "In-circuit programming" is made possible. The user can program PIC16C55X devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-on-Reset ($\overline{POR}$) status bit.
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
18. PORTA inputs are now Schmitt Trigger inputs.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16C55X, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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PIC16C55X PRODUCT IDENTIFICATION SYSTEM

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NO. -XX X /XX XXX

Pattern:	3-Digit Pattern Code for QTP (blank otherwise)		
Package:	P	=	PDIP
	SO	=	SOIC (Gull Wing, 300 mil body)
	SS	=	SSOP (209 mil)
	JW*	=	Windowed CERDIP
Temperature Range:	-	=	0°C to +70°C
	I	=	–40°C to +85°C
	E	=	–40°C to +125°C
Frequency Range:	04	=	200kHz (LP osc)
	04	=	4 MHz (XT and RC osc)
	20	=	20 MHz (HS osc)
Device:	PIC16C55X :VDD range 3.0V to 5.5V		
	PIC16C55XT:VDD range 3.0V to 5.5V (Tape and Reel)		
	PIC16LC55X:VDD range 2.5V to 5.5V		
	PIC16LC55XT:VDD range 2.5V to 5.5V (Tape and Reel)		

Examples:

a) PIC16C554 - 04/P 301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern #301.

b) PIC16LC558- 04I/SO = Industrial temp., SOIC package, 200kHz, extended VDD limits.

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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NOTES:

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MICROCHIP

SECTION 7
PIC16C62X MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC16C62X EPROM-Based 8-Bit CMOS Microcontroller 7-1

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MICROCHIP

PIC16C62X

EPROM-Based 8-Bit CMOS Microcontroller

Devices included in this data sheet:

- PIC16C620
- PIC16C621
- PIC16C622

High Performance RISC CPU:

- Only 35 instructions to learn
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle

Device	Program Memory	Data Memory
PIC16C620	512	80
PIC16C621	1K	80
PIC16C622	2K	128

- Interrupt capability
- 16 special function hardware registers
- 8-level deep hardware stack
- Direct, Indirect and Relative addressing modes

Peripheral Features:

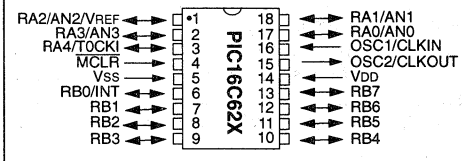
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (V_{REF}) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs can be output signals
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

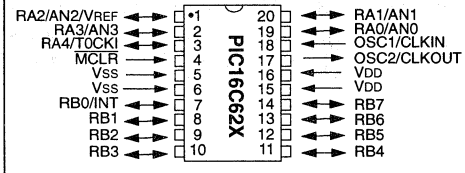
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation

Pin Diagrams

PDIP, SOIC, Windowed CERDIP



SSOP



Special Microcontroller Features (cont'd)

- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Four user programmable ID locations

CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range
  - 2.5V to 6.0V
- Commercial and industrial temperature range
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - < 1.0 µA typical standby current @ 3.0V

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To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error from the previous version of this data sheet (PIC16C62X Data Sheet, Literature Number DS30235E), please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

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1.0 GENERAL DESCRIPTION

The PIC16C62X are 18-Pin EPROM-based members of the versatile PIC16CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16C62X have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single-cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16C62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in its class.

The PIC16C620 and PIC16C621 have 80 bytes of RAM. The PIC16C622 has 128 bytes of RAM. Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16C62X add two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low-cost analog interface (e.g., battery chargers, threshold detectors, white goods controllers, etc).

PIC16C62X devices have special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake up the chip from SLEEP through several external and internal interrupts and reset.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock- up.

A UV-erasable CERDIP-packaged version is ideal for code development while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C62X mid-range microcontroller families.

A simplified block diagram of the PIC16C62X is shown in Figure 3-1.

The PIC16C62X series fit perfectly in applications ranging from battery chargers to low-power remote sensors. The EPROM technology makes customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16C62X very versatile.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to PIC16C62X family of devices (Appendix B).

1.2 Development Support

The PIC16C62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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TABLE 1-1: PIC16C62X FAMILY OF DEVICES

	Clock	Memory		Peripherals					Features		
	Maximum Frequency of Operation (MHz)	EPROM	Program Memory (x 14) / Data Memory (bytes)	Timer Module(s)	Comparator(s)	Internal Reference Voltage	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Brown-out Reset	Packages
PIC16C620	20	512	80	TMR0	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C621	20	1K	80	TMR0	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C622	20	2K	128	TMR0	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC16C62X Family devices use serial programming with clock pin RB6 and data pin RB7.

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2.0 PIC16C62X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in the PIC16C62X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® and PRO MATE™ programmers both support programming of the PIC16C62X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C62X uses a Harvard architecture, in which, program and data are accessed from separate memories using separate busses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single-cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C620 addresses 512 x 14 on-chip program memory. The PIC16C621 addresses 1K x 14 program memory. The PIC16C622 addresses 2K x 14 program memory. All program memory is internal.

The PIC16C62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C62X have an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

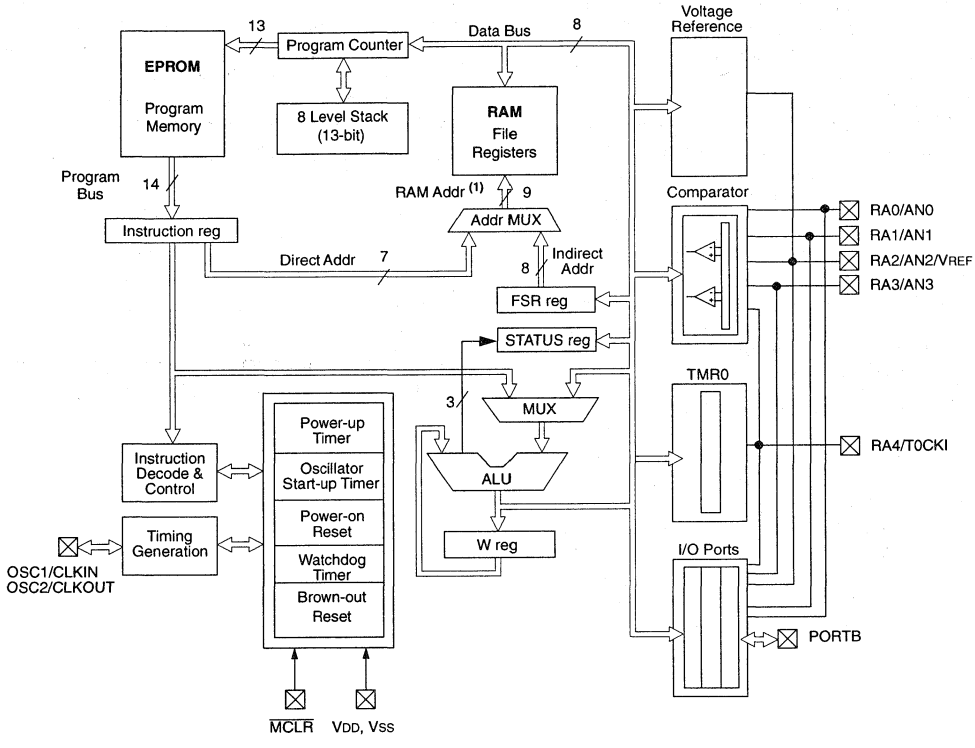
Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit}}$ $\overline{\text{Borrow}}$ out bit, respectively, bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

7

FIGURE 3-1: BLOCK DIAGRAM

Device	Program Memory	Data Memory (RAM)
PIC16C620	512 x 14	80 x 8
PIC16C621	1K x 14	80 x 8
PIC16C622	2K x 14	128 x 8



Note 1: Higher order bits are from the STATUS register.

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TABLE 3-1: PIC16C62X PINOUT DESCRIPTION

Name	DIP SOIC Pin #	SSOP Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	I	ST/CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0/AN0	17	19	I/O	ST	Analog comparator input
RA1/AN1	18	20	I/O	ST	Analog comparator input
RA2/AN2/VREF	1	1	I/O	ST	Analog comparator input or VREF output
RA3/AN3	2	2	I/O	ST	Analog comparator input /output
RA4/T0CKI	3	3	I/O	ST	Can be selected to be the clock input to the Timer0 timer/counter or a comparator output. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	7	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	Interrupt on change pin.
RB5	11	12	I/O	TTL	Interrupt on change pin.
RB6	12	13	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.
RB7	13	14	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.
VSS	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: O = output I/O = input/output P = power
— = Not used I = Input ST = Schmitt Trigger input
TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
Note 2: This buffer is a Schmitt Trigger input when used in serial programming mode.

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

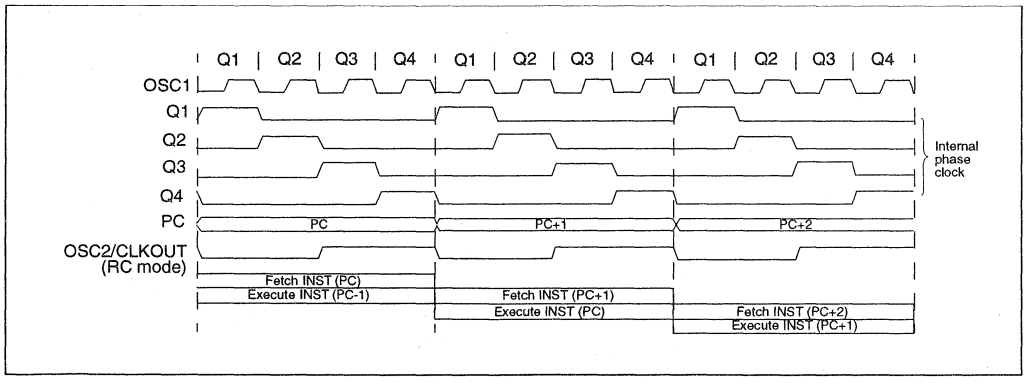
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

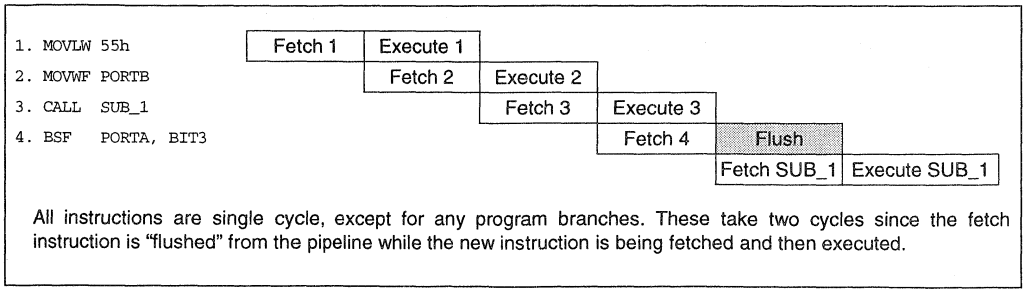
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C62X has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 512 x 14 (0000h - 01FFh) for the PIC16C620, 1K x 14 (0000h - 03FFh) for the PIC16C621 and 2K x 14 (0000h - 07FFh) for the PIC16C622 are physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 512 x 14 space (PIC16C620) or 1K x 14 space (PIC16C621) or 2K x 14 space (PIC16C622). The reset vector is at 0000h and the interrupt vector is at 0004h (Figure 4-1, Figure 4-2, Figure 4-3).

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C620

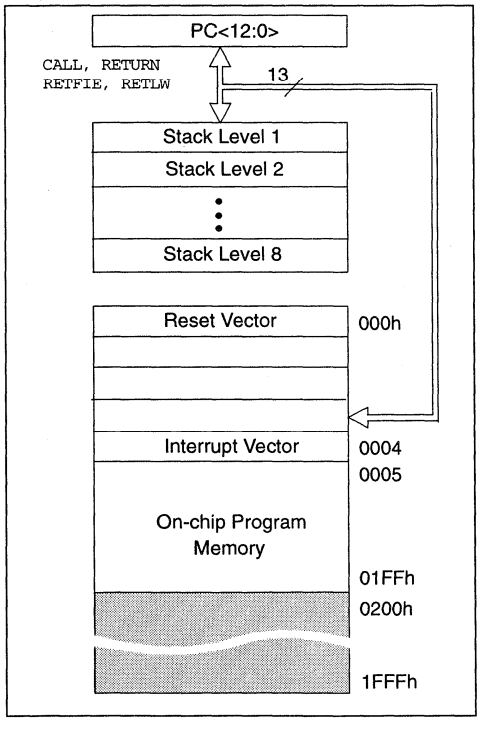


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C621

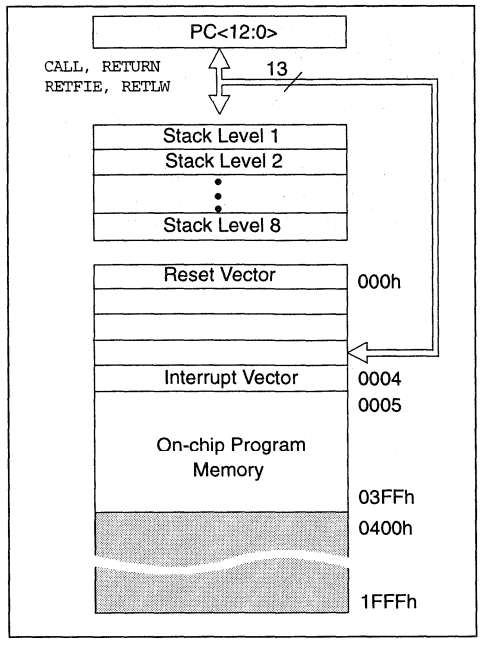
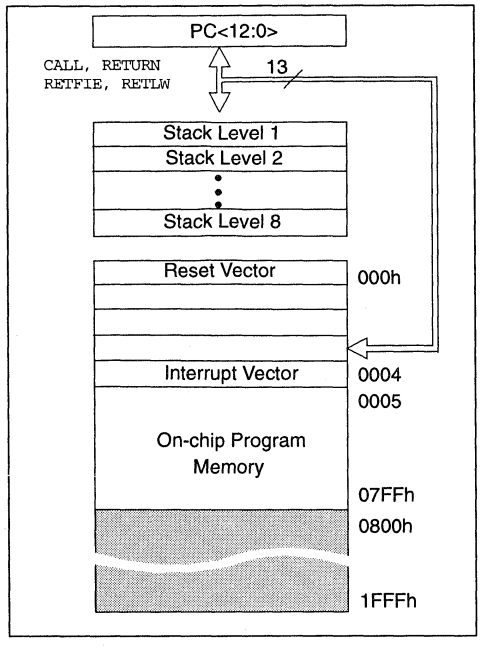


FIGURE 4-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C622



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4.2 Data Memory Organization

The data memory (Figure 4-4 and Figure 4-5) is partitioned into two Banks which contain the general purpose registers and the special function registers. Bank 0 is selected when the RP0 bit is cleared. Bank 1 is selected when the RP0 bit (STATUS <5>) is set. The Special Function Registers are located in the first 32 locations of each Bank. Register locations 20-6Fh (Bank0) on the PIC16C620/621 and 20-7Fh (Bank0) and A0-BFh (Bank1) on the PIC16C622 are general purpose registers implemented as static RAM. Some special purpose registers are mapped in Bank 1.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 80 x 8 in the PIC16C620/621 and 128 x 8 in the PIC16C622. Each is accessed either directly or indirectly through the File Select Register FSR (Section 4.4).

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FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C620/621

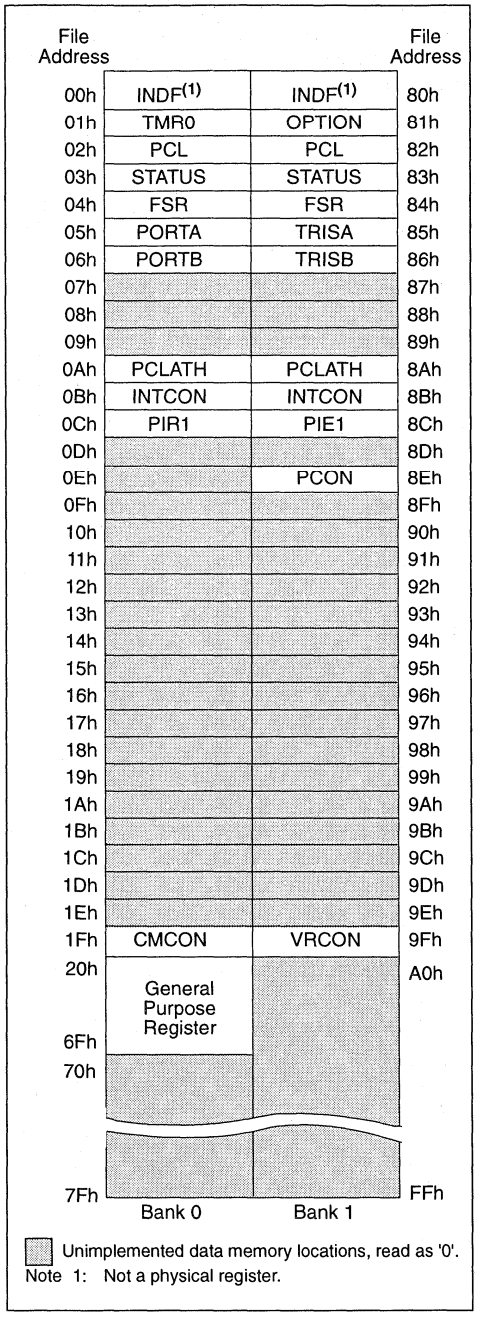
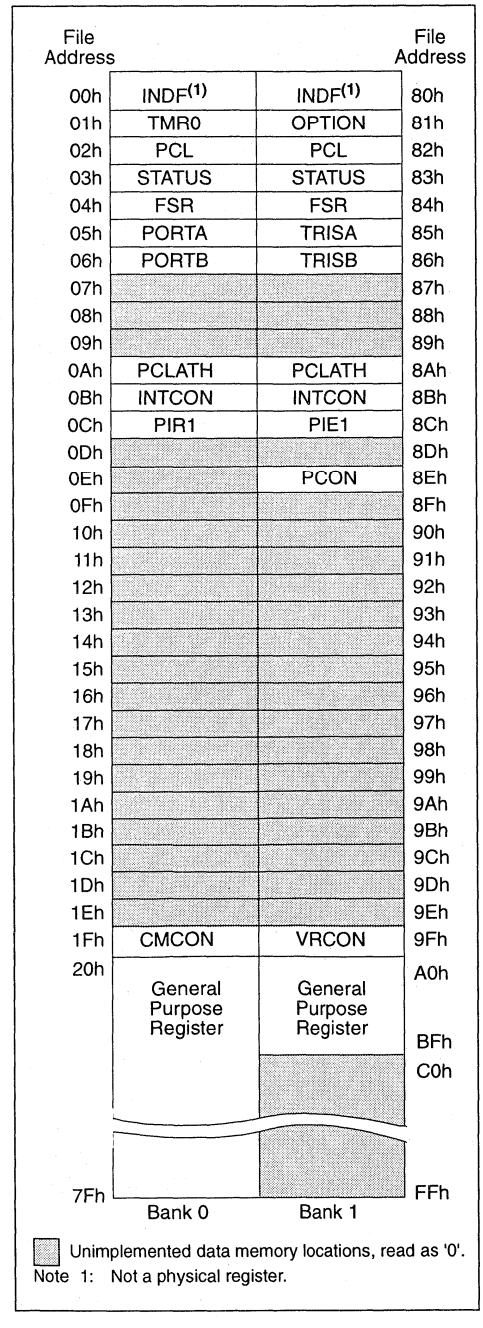


FIGURE 4-5: DATA MEMORY MAP FOR THE PIC16C622



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4.2.2 SPECIAL FUNCTION REGISTERS

The special function registers are registers used by the CPU and Peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM.

The special registers can be classified into two sets (core and peripheral). The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C62X

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR Reset	Value on all other resets(1)
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module's Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP(2)	RP1(2)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	Unimplemented									—	—
08h	Unimplemented									—	—
09h	Unimplemented									—	—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
0Dh-1Eh	Unimplemented									—	—
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h	Unimplemented									—	—
88h	Unimplemented									—	—
89h	Unimplemented									—	—
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----
8Dh	Unimplemented									—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --0x	---- --uq
8Fh-9Eh	Unimplemented									—	—
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) resets include $\overline{MCLR}$ reset, Brown-out Rreset and Watchdog Timer Reset during normal operation.

Note 2: IRP & RPI bits are reserved, always maintain these bits clear.

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4.2.2.1 STATUS REGISTER

The STATUS register, shown in Figure 4-6, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the status register as `000uu1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect any status bit. For other instructions, not affecting any status bits, see the "Instruction Set Summary".

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C62X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 4-6: STATUS REGISTER (ADDRESS 03H OR 83H)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)
The IRP bit is reserved on the PIC16C62X, always maintain this bit clear.

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C62X, always maintain this bit clear.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

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4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT (PSA = 1).

FIGURE 4-7: OPTION REGISTER (ADDRESS 81H)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-8: INTCON REGISTER (ADDRESS 0BH OR 8BH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:** Global Interrupt Enable bit(1)
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

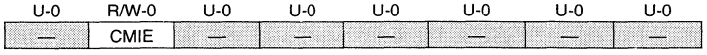
bit 0: **RBIF**: RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

7

4.2.2.4 PIE1 REGISTER

This register contains the individual enable bit for the comparator interrupt.

FIGURE 4-9: PIE1 REGISTER (ADDRESS 8CH)



R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6: **CMIE**: Comparator Interrupt Enable bit
1 = Enables the Comparator interrupt
0 = Disables the Comparator interrupt

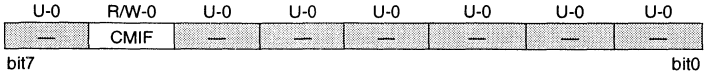
bit 5-0: **Unimplemented**: Read as '0'

4.2.2.5 PIR1 REGISTER

This register contains the individual flag bit for the comparator interrupt.

Note:	Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-10: PIR1 REGISTER (ADDRESS 0CH)



R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6: **CMIF**: Comparator Interrupt Flag bit
1 = Comparator input has changed
0 = Comparator input has not changed

bit 5-0: **Unimplemented**: Read as '0'

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4.2.2.6 PCON REGISTER

The PCON register contains flag bits to differentiate between a Power-on Reset, an external $\overline{MCLR}$ reset, WDT reset or a Brown-out Reset.

Note: $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{BOR}$ is cleared, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (by programming BODEN bit in the Configuration word).

FIGURE 4-11: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1: **$\overline{POR}$**: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0: **$\overline{BOR}$**: Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

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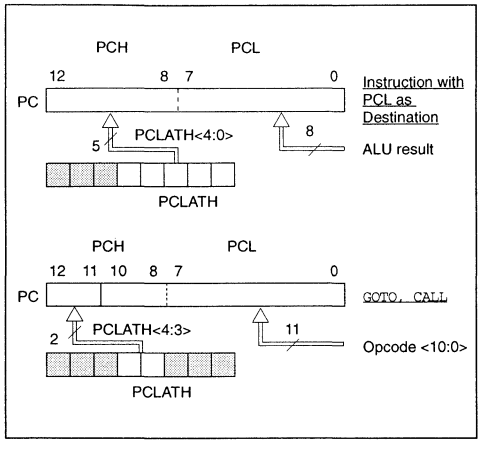
4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-12 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-12: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16C62X family has an 8 level deep x 13-bit wide hardware stack (Figure 4-2 and Figure 4-3). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1:	There are no STATUS bits to indicate stack overflow or stack underflow conditions.
Note 2:	There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.

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4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

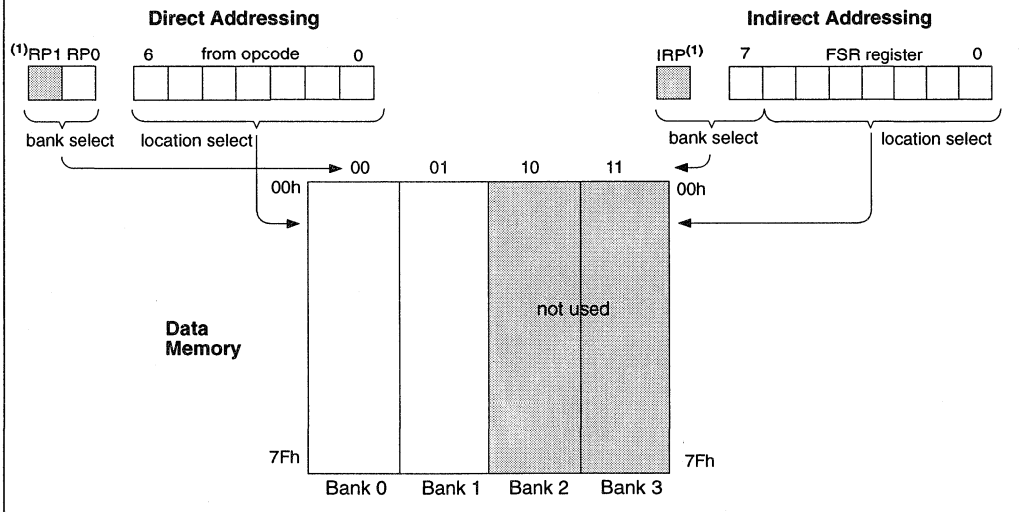
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-13. However, IRP is not used in the PIC16C62X.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;no clear next
                        ;yes continue
CONTINUE:
```

FIGURE 4-13: DIRECT/INDIRECT ADDRESSING PIC16C62X



For memory map detail see Figure 4-4 and Figure 4-5.

Note 1: The RP1 and IRP bits are reserved, always maintain these bits clear.

NOTES:

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5.0 I/O PORTS

The PIC16C62X have two ports, PORTA and PORTB. Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

5.1 PORTA and TRISA Registers

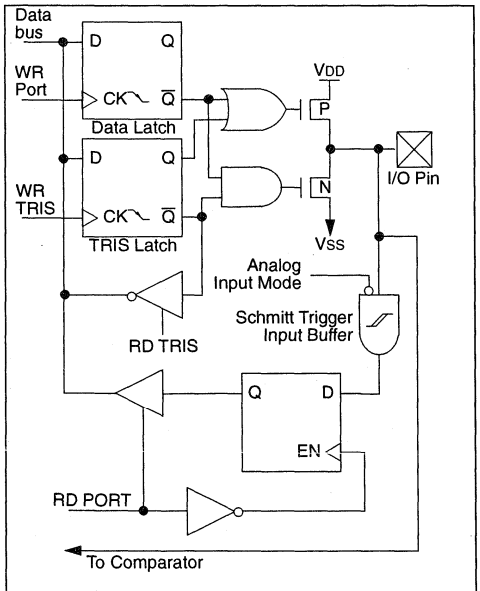
PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. Port RA4 is multiplexed with the T0CKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as input or output.

A '1' in the TRISA register puts the corresponding output driver in a hi- impedance mode. A '0' in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The PORTA pins are multiplexed with comparator and voltage reference functions. The operation of these pins are selected by control bits in the CMCON (comparator control register) register and the VRCON (voltage reference control register) register. When selected as a comparator input, these pins will read as '0's.

FIGURE 5-1: BLOCK DIAGRAM OF RA1:RA0 PINS



Note: I/O pins have protection diodes to VDD and VSS.

Note: On reset, the TRISA register is set to all inputs. The digital inputs are disabled and the comparator inputs are forced to ground to reduce excess current consumption.

TRISA controls the direction of the RA pins, even when they are being used as comparator inputs. The user must make sure to keep the pins configured as inputs when using them as comparator inputs.

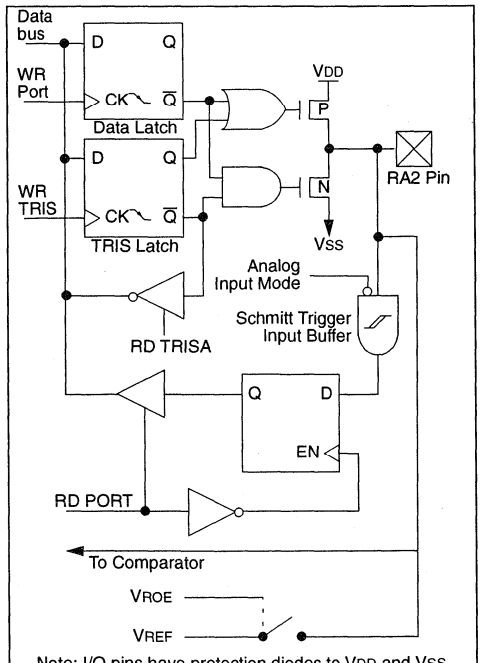
The RA2 pin will also function as the output for the voltage reference. When in this mode, the VREF pin is a very high impedance output. The user must configure TRISA<2> bit as an input and use high impedance loads.

In one of the comparator modes defined by the CMCON register, pins RA3 and RA4 become outputs of the comparators. The TRISA<4:3> bits must be cleared to enable outputs to use this function.

EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF    PORTA       ;Initialize PORTA by setting
                    ;output data latches
MOVLW   0X07        ;Turn comparators off and
MOVWF   CMCON       ;enable pins for I/O
                    ;functions
BSF     STATUS, RP0 ;Select Bank1
MOVLW   0x1F        ;Value used to initialize
                    ;data direction
MOVWF   TRISA       ;Set RA<4:0> as inputs
                    ;TRISA<7:5> are always
                    ;read as '0'.
```

FIGURE 5-2: BLOCK DIAGRAM OF RA2 PIN



Note: I/O pins have protection diodes to VDD and VSS.

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FIGURE 5-3: BLOCK DIAGRAM OF RA3 PIN

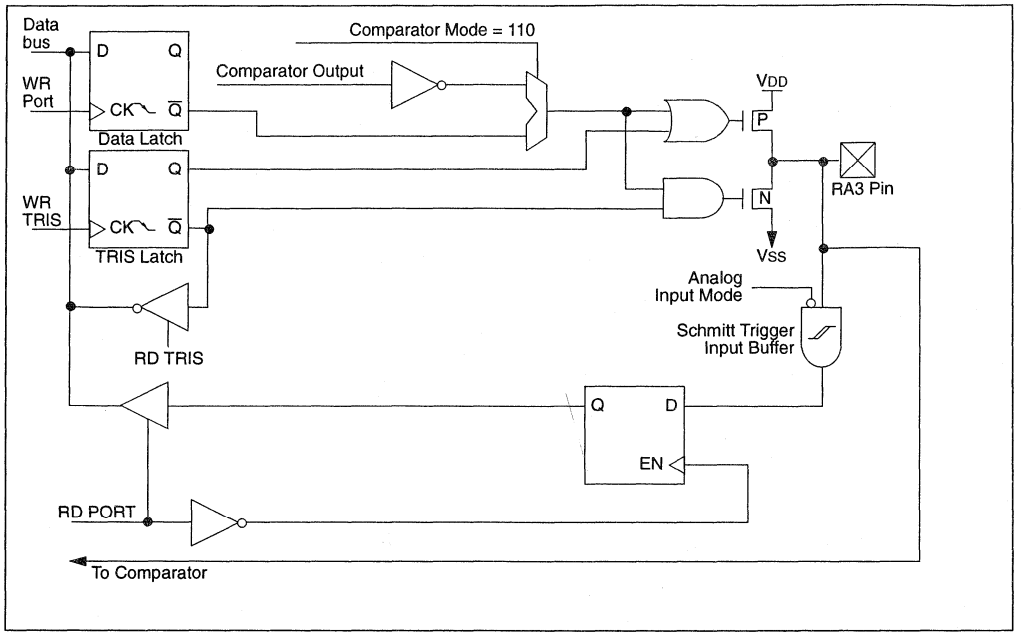

FIGURE 5-4: BLOCK DIAGRAM OF RA4 PIN

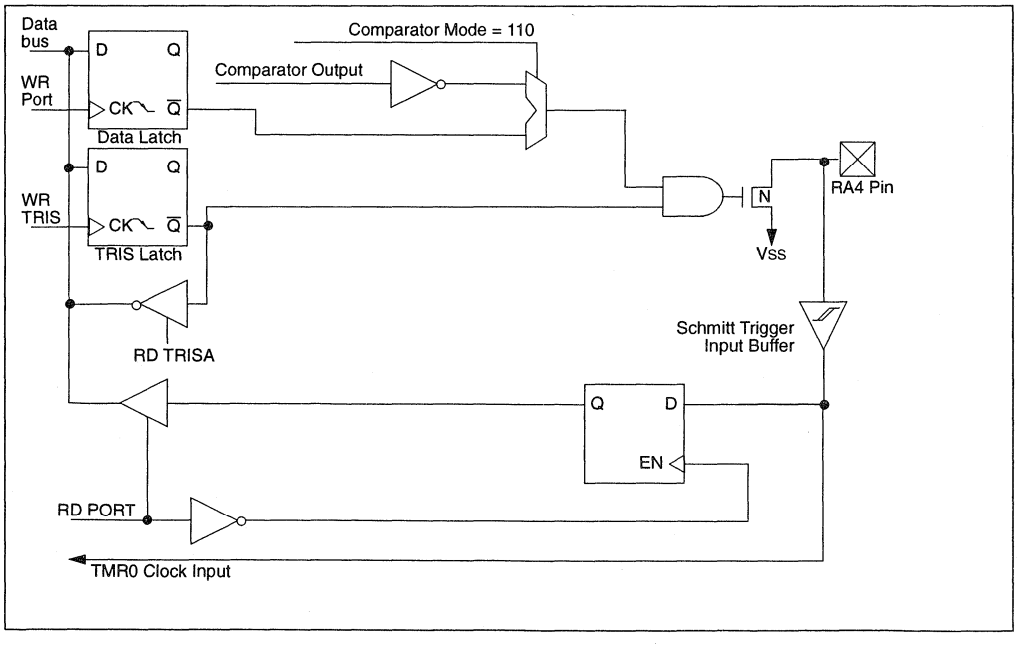

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TABLE 5-1: PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR / BOR	Value on All Other Resets
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0'

Note: Note: Shaded bits are not used by PORTA.

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5.2 PORTB and TRISB Registers

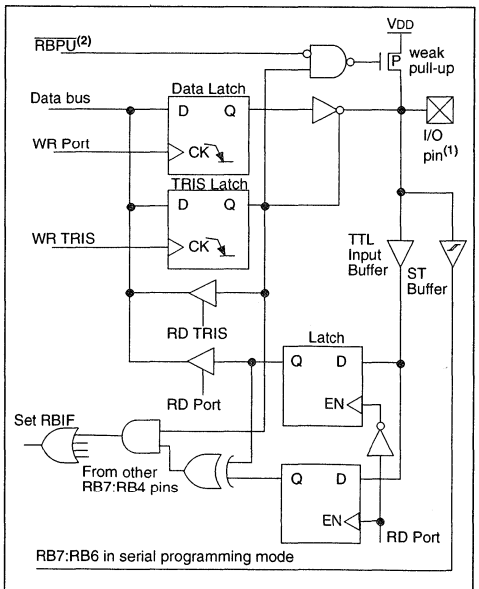
PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a high impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up (≈200 μA typical). A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBPU}}$ (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

FIGURE 5-5: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: I/O pins have diode protection to VDD and VSS.

Note 2: TRISB = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

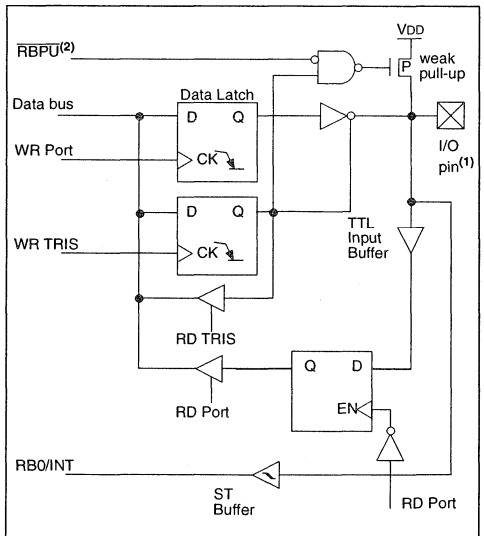
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552 in the Microchip *Embedded Control Handbook*.)

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-6: BLOCK DIAGRAM OF RB3:RB0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.

Note 2: TRISB = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

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TABLE 5-3: PORTB FUNCTIONS

Name	Bit #	Buffer Type	Function
RB0/INT	bit0	TTL/ST(1)	Input/output or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock pin.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data pin.

Legend: ST = Schmitt Trigger, TTL = TTL input
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
Note 2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR / BOR	Value on All Other Resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Note: Shaded bits are not used by PORTB.

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5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read modify write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-2 shows the effect of two sequential read-modify-write instructions (ex., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-2: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

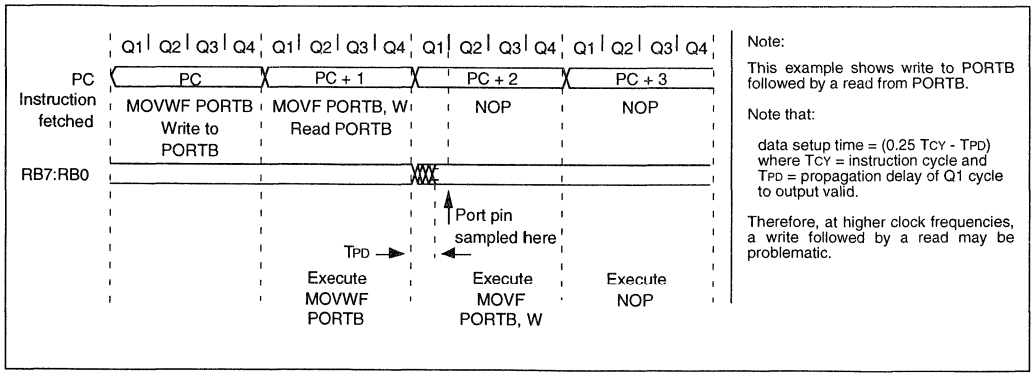
```
; Initial PORT settings:     PORTB<7:4> Inputs
;
;                            PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are not
; connected to other circuitry
;
;                            PORT latch  PORT pins
;                            ----------  ----------

    BCF  PORTB, 7          ; 01pp pppp   11pp pppp
    BCF  PORTB, 6          ; 10pp pppp   11pp pppp
    BSF  STATUS,RP0        ;
    BCF  TRISB, 7          ; 10pp pppp   11pp pppp
    BCF  TRISB, 6          ; 10pp pppp   10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused
; RB7 to be latched as the pin value (High).
```

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-7). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with an NOP or another instruction not accessing this I/O port.

FIGURE 5-7: SUCCESSIVE I/O OPERATION



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6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

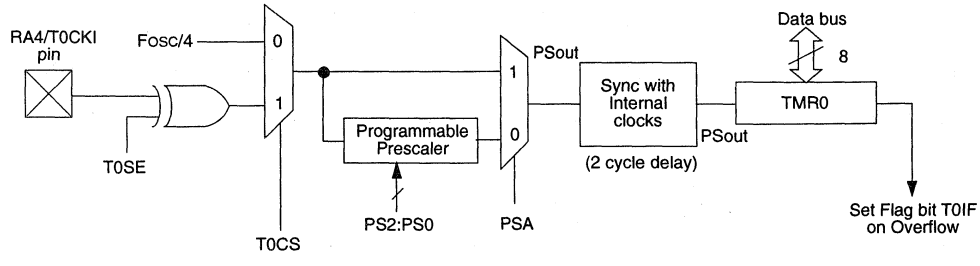
Counter mode is selected by setting the T0CS bit. In this mode Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the WatchdogTimer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

6.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits, T0SE, T0CS, PS2, PS1, PS0 and PSA are located in the OPTION register.
2: The prescaler is shared with Watchdog Timer (Figure 6-6)

FIGURE 6-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER

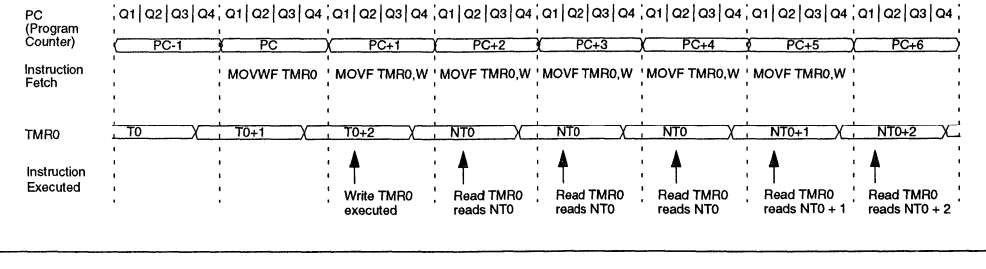


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

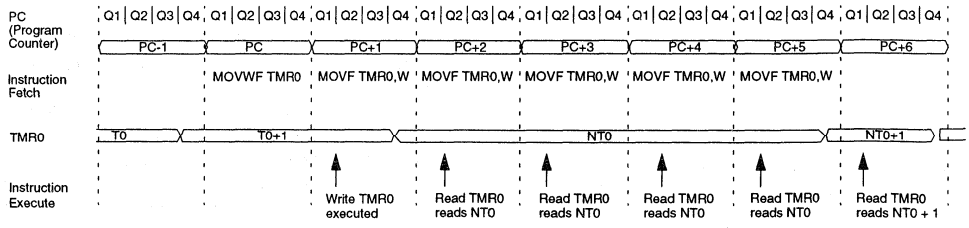
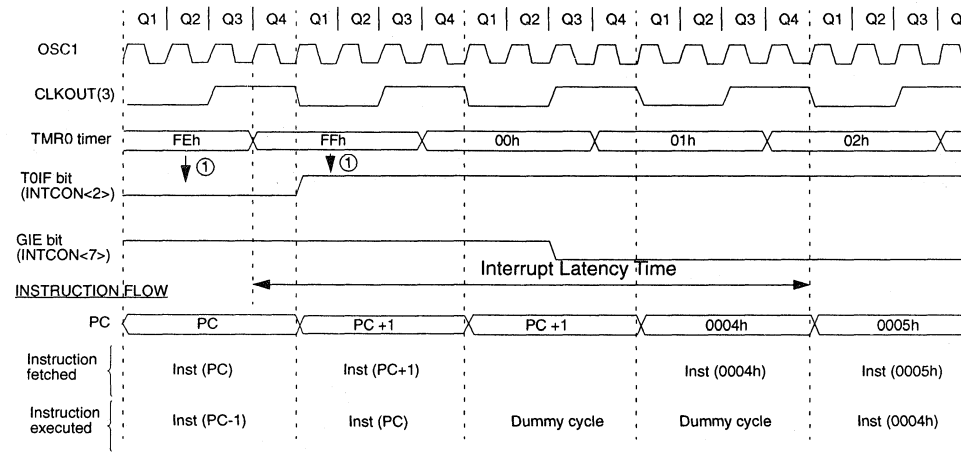


FIGURE 6-4: TIMER0 INTERRUPT TIMING



Note 1: T0IF interrupt flag is sampled here (every Q1).
2: Interrupt latency = 4TCY, where TCY = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.

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6.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

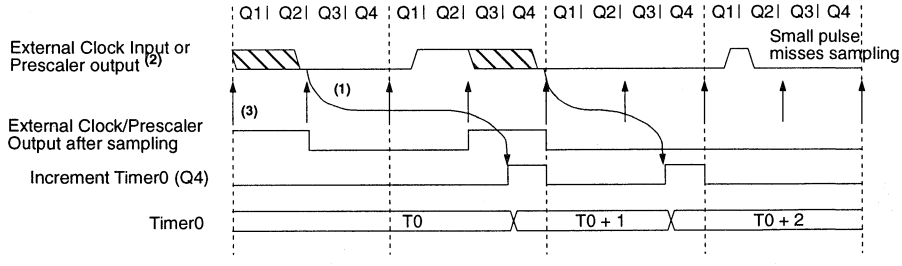
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

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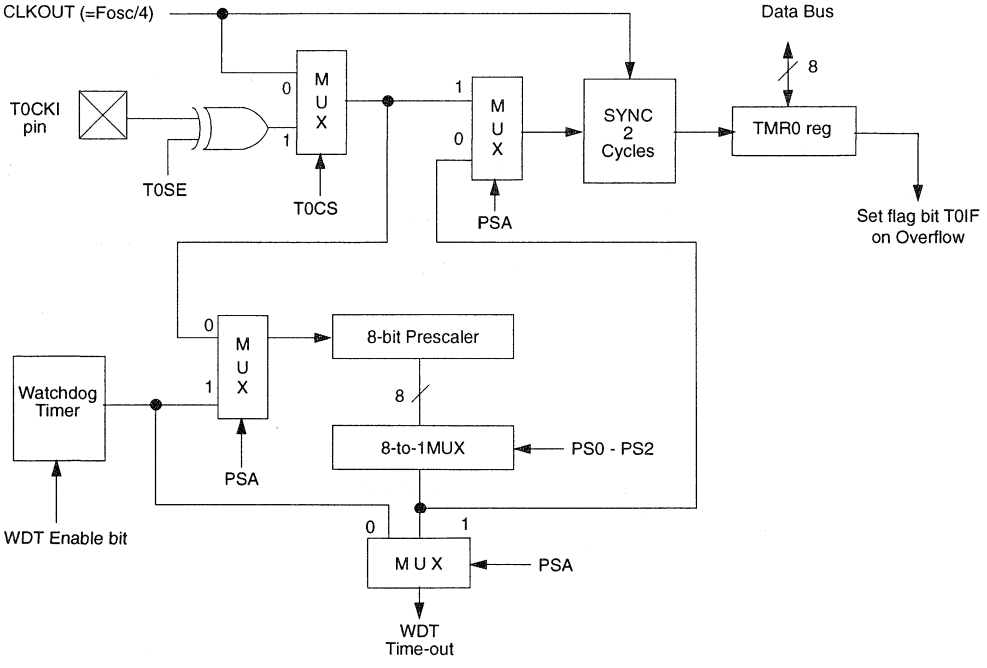
6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0SE, T0CS, PSA, PS0-PS2 are bits in the OPTION register.

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6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS,  RP0 ;Bank 0
CLRF    TMR0         ;Clear TMR0 & Prescaler
BSF     STATUS,  RP0 ;Bank 1
CLRWDT               ;Clears WDT and
                     ;
MOVLW   b'xxxx1xxx'  ;Select new prescaler
MOVWF   OPTION_REG   ;value
BCF     STATUS,  RP0 ;Bank 0
```

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 6-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                ;Clear WDT and
                      ;prescaler
BSF     STATUS, RP0
MOVLW   b'xxxx0xxx'   ;Select TMR0, new
                      ;prescale value and
                      ;clock source
MOVWF   OPTION_REG
BCF     STATUS, RP0
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR / BOR	Value on All Other Resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: — = Unimplemented locations, read as '0'.

Note: Shaded bits are not used by TMR0 module.

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NOTES:

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7.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with the RA0 through RA3 pins. The on-chip Voltage Reference (Section 8.0) can also be an input to the comparators.

The CMCON register, shown in Figure 7-1, controls the comparator input and output multiplexers. A block diagram of the comparator is shown in Figure 7-2.

FIGURE 7-1: CMCON REGISTER (ADDRESS 1Fh)

R-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	-	-	CIS	CM2	CM1	CM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **C2OUT**: Comparator 2 output
1 = C2 VIN+ > C2 VIN–
0 = C2 VIN+ < C2 VIN–

bit 6: **C1OUT**: Comparator 1 output
1 = C1 VIN+ > C1 VIN–
0 = C1 VIN+ < C1 VIN–

bit 5-4: **Unimplemented:** Read as '0'

bit 3: **CIS**: Comparator Input Switch
When CM<2:0>: = 001:
1 = C1 VIN– connects to RA3
0 = C1 VIN– connects to RA0
When CM<2:0> = 010:
1 = C1 VIN– connects to RA3
C2 VIN– connects to RA2
0 = C1 VIN– connects to RA0
C2 VIN– connects to RA1

bit 2-0: **CM<2:0>**: Comparator mode
Figure 7-2.

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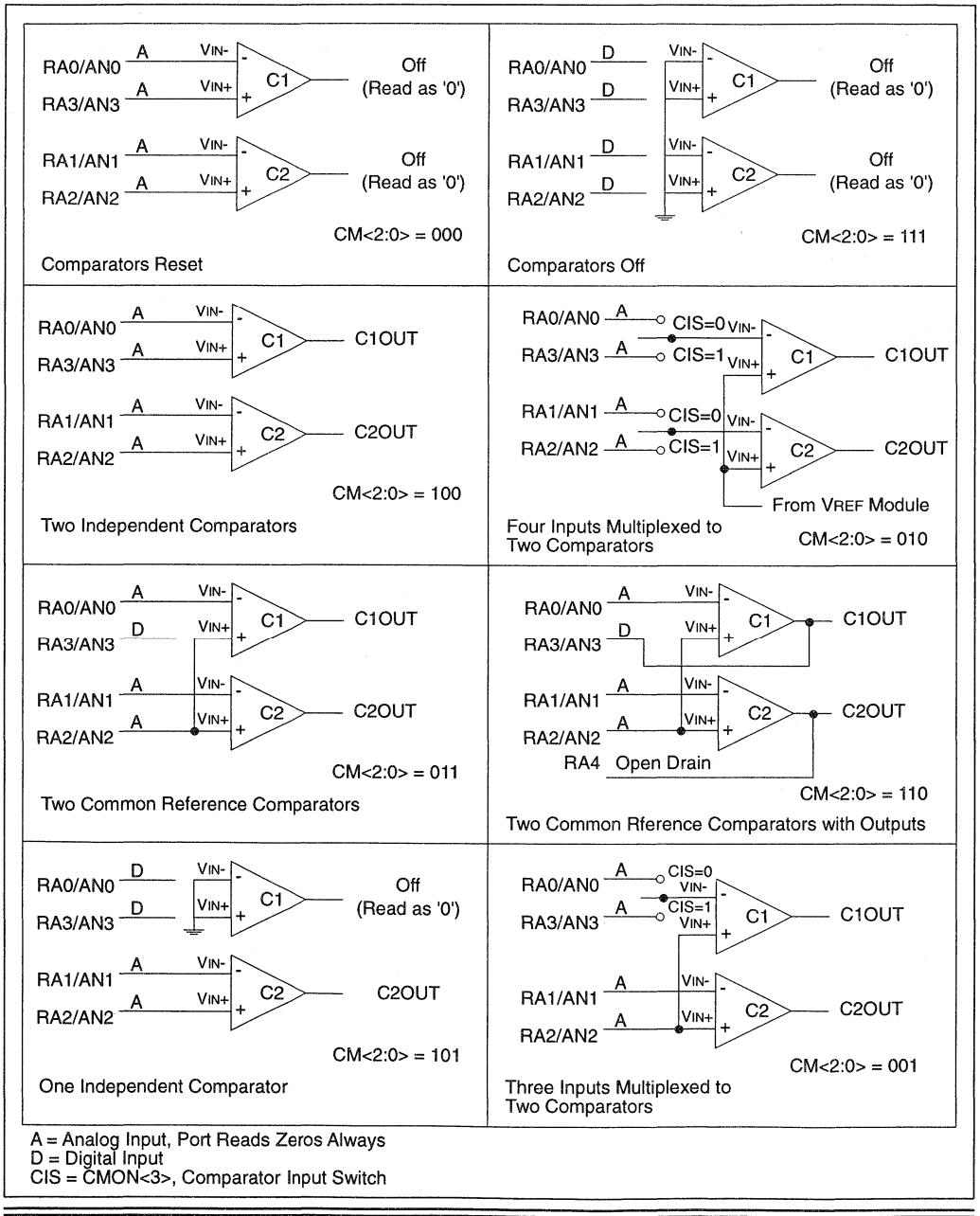
7.1 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON register is used to select the mode. Figure 7-2 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the comparator mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Table 10-2.

Note: Comparator interrupts should be disabled during a comparator mode change otherwise a false interrupt may occur.

FIGURE 7-2: COMPARATOR I/O OPERATING MODES



A = Analog Input, Port Reads Zeros Always
D = Digital Input
CIS = CMON<3>, Comparator Input Switch

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The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

```
FLAG_REG    EQU         0X20
CLRF        FLAG_REG    ;Init flag register
CLRF        PORTA       ;Init PORTA
ANDLW       0xC0        ;Mask comparator bits
IORWF       FLAG_REG,F  ;Store bits in flag register
MOVLW       0x03        ;Init comparator mode
MOVWF       CMCON       ;CM<2:0> = 011
BSF         STATUS,RP0  ;Select Bank1
MOVLW       0x07        ;Initialize data direction
MOVWF       TRISA       ;Set RA<2:0> as inputs
                        ;RA<4:3> as outputs
                        ;TRISA<7:5> always read '0'
BCF         STATUS,RP0  ;Select Bank 0
CALL        DELAY 10    ;10µs delay
MOVF        CMCON,F     ;Read CMCON to end change condition
BCF         PIR1,CMIF   ;Clear pending interrupts
BSF         STATUS,RP0  ;Select Bank 1
BSF         PIE1,CMIE   ;Enable comparator interrupts
BCF         STATUS,RP0  ;Select Bank 0
BSF         INTCON,PEIE ;Enable peripheral interrupts
BSF         INTCON,GIE  ;Global interrupt enable
```

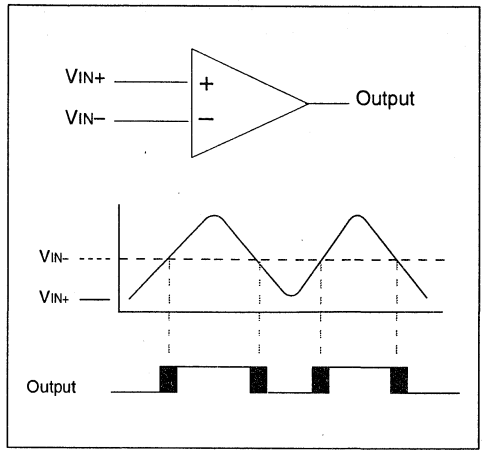
7.2 Comparator Operation

A single comparator is shown in Figure 7-3 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN–, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN–, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-3 represent the uncertainty due to input offsets and response time.

7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN– is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-3).

FIGURE 7-3: SINGLE COMPARATOR



7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD, and can be applied to either pin of the comparator(s).

7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 13, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-2). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

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7.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is guaranteed to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise the maximum delay of the comparators should be used (Table 10-4 and Table 10-5).

7.5 Comparator Outputs

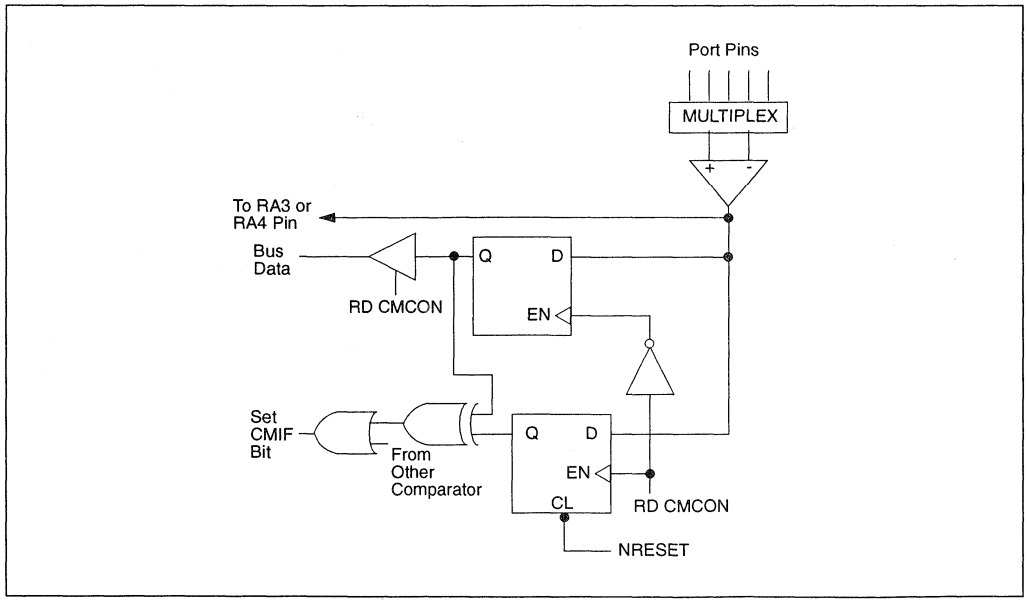
The comparator outputs are read through the CMCON register. These bits are read only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When the CM<2:0> = 110, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 7-4 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/disable for the RA3 and RA4 pins while in this mode.

Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.

2: Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

FIGURE 7-4: COMPARATOR OUTPUT BLOCK DIAGRAM



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7.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that has occurred. The CMIF bit, PIR1<6>, is the comparator interrupt flag. The CMIF bit must be reset by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<6>) interrupt flag may not get set.

The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON. This will end the mismatch condition.

b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

7.7 Comparator Operation During SLEEP

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake up the device from SLEEP mode when enabled. While the comparator is powered-up, higher sleep currents than shown in the power down current specification will occur. Each comparator that is operational will consume additional current as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering sleep. If the device wakes-up from sleep, the contents of the CMCON register are not affected.

7.8 Effects of a RESET

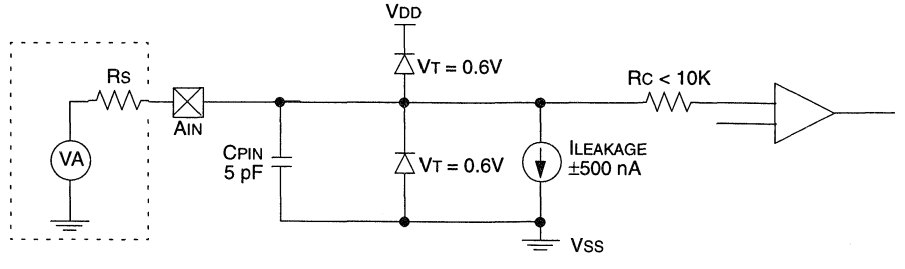
A device reset forces the CMCON register to its reset state. This forces the comparator module to be in the comparator reset mode, CM2:CM0 = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at reset time. The comparators will be powered-down during the reset interval.

7.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 7-5. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

7

FIGURE 7-5: ANALOG INPUT MODEL



Legend		
	CPIN	= Input Capacitance
	VT	= Threshold Voltage
	ILEAKAGE	= Leakage Current At The Pin Due To Various Junctions
	RIC	= Interconnect Resistance
	RS	= Source Impedance
	VA	= Analog Voltage

TABLE 7-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR / BOR	Value on All Other Resets
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

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8.0 VOLTAGE REFERENCE MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Figure 8-1. The block diagram is given in Figure 8-2.

8.1 Configuring the Voltage Reference

The Voltage Reference can output 16 distinct voltage levels for each range.

The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 1: VREF = (VR<3:0>/24) x VDD

if VRR = 0: VREF = (VDD x 1/4) + (VR<3:0>/32) x VDD

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 10-2). Example 8-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

FIGURE 8-1: VRCON REGISTER(ADDRESS 9Fh)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **VREN:** VREF Enable
1 = VREF circuit powered on
0 = VREF circuit powered down, no IDD drain

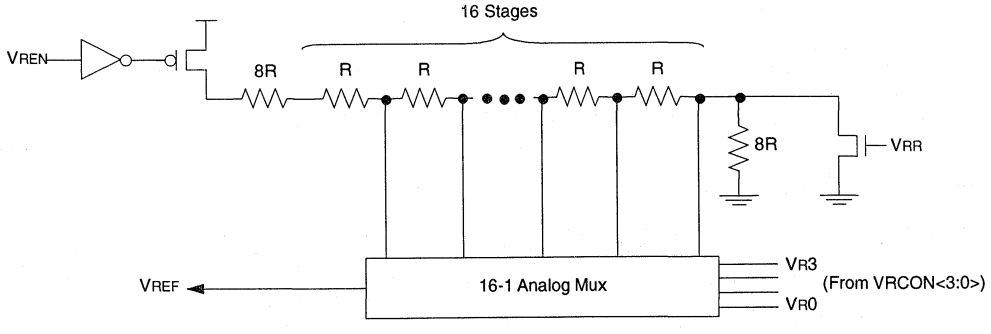
bit 6: **VROE:** VREF Output Enable
1 = VREF is output on RA2 pin
0 = VREF is disconnected from RA2 pin

bit 6: **VRR:** VREF Range selection
1 = Low Range
0 = High Range

bit 4: **Unimplemented:** Read as '0'

bit 3-0: **VR<3:0>**: VREF value selection 0 ≤ VR [3:0] ≤ 15
when VRR = 1: VREF = (VR<3:0>/ 24) * VDD
when VRR = 0: VREF = 1/4 * VDD + (VR<3:0>/ 32) * VDD

FIGURE 8-2: VOLTAGE REFERENCE BLOCK DIAGRAM



Note: R is defined in Table 10-3.

EXAMPLE 8-1: VOLTAGE REFERENCE CONFIGURATION

```
MOVLW   0x02        ; 4 Inputs Muxed
MOVWF   CMCON       ; to 2 comps.
BSF     STATUS,RP0  ; go to Bank 1
MOVLW   0x07        ; RA3-RA0 are
MOVWF   TRISA       ; outputs
MOVLW   0xA6        ; enable VREF
MOVWF   VRCON       ; low range
                    ; set VR<3:0>=6
BCF     STATUS,RP0  ; go to Bank 0
CALL    DELAY10     ; 10µs delay
```

8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-2) keep VREF from approaching VSS or VDD. The Voltage Reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The absolute accuracy of the Voltage Reference can be found in Table 10-3.

8.3 Operation During Sleep

When the device wakes up from sleep through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the Voltage Reference should be disabled.

8.4 Effects of a Reset

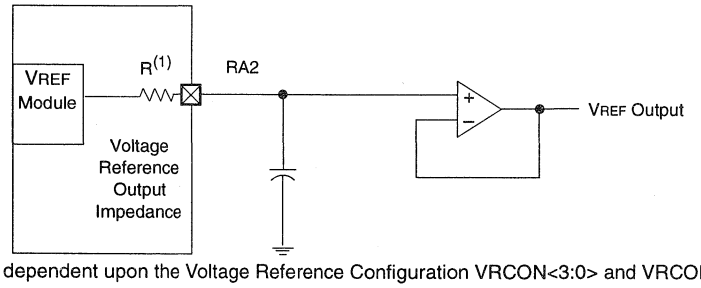
A device reset disables the Voltage Reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

8.5 Connection Considerations

The Voltage Reference Module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the Voltage Reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the Voltage Reference output for external connections to VREF. Figure 8-3 shows an example buffering technique.

FIGURE 8-3: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



Note 1: R is dependent upon the Voltage Reference Configuration VRCON<3:0> and VRCON<5>.

TABLE 8-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR / BOR	Value On All Other Resets
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

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9.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC16C62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

1. OSC selection
2. Reset
   Power-on Reset (POR)
   Power-up Timer (PWRT)
   Oscillator Start-Up Timer (OST)
   Brown-out Reset (BOR)
3. Interrupts
4. Watchdog Timer (WDT)
5. SLEEP
6. Code protection
7. ID Locations
8. In-circuit serial programming

The PIC16C62X has a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Ttimer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs which provides at least a 72 ms reset. With these three functions on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

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9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h – 3FFFh), which can be accessed only during programming.

FIGURE 9-1: CONFIGURATION WORD

CP1	CP0	CP1	CP0	CP1	CP0	—	BODEN	CP1	CP0	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
bit13													bit0

CONFIG Address
REGISTER: 2007h

bit 13-8 **CP<1:0>:** Code protection bits(2)
5-4: 11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 7: **Unimplemented**: Read as '1'

bit 6: **BODEN**: Brown-out Reset Enable bit (1)
1 = BOR enabled
0 = BOR disabled

bit 3: **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit (1)
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRTE}}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.
2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

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9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

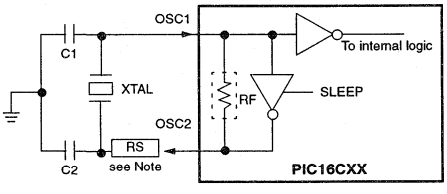
The PIC16CXX can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 9-2). The PIC16CXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 9-3).

FIGURE 9-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 9-1 and Table 9-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 9-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

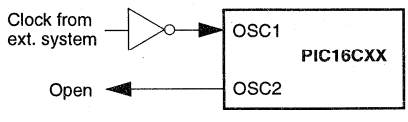


TABLE 9-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS (PRELIMINARY)

Ranges Characterized:		
Mode	**Freq**	**OSC1**
XT	455 kHz 2.0 MHz 4.0 MHz	22 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF
Note: Recommended values of C1 and C2 are identical to the ranges tested table. Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.		

Resonators to be Characterized:		
455 kHz	Panasonic EFO-A455K04B	±0.3%
2.0 MHz	Murata Erie CSA2.00MG	±0.5%
4.0 MHz	Murata Erie CSA4.00MG	±0.5%
8.0 MHz	Murata Erie CSA8.00MT	±0.5%
16.0 MHz	Murata Erie CSA16.00MX	±0.5%
All resonators used did not have built-in capacitors.		

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR (PRELIMINARY)

Mode	Freq	OSC1	OSC2
LP	32 kHz 200 kHz	68 - 100 pF 15 - 30 pF	68 - 100 pF 15 - 30 pF
XT	100 kHz 2 MHz 4 MHz	68 - 150 pF 15 - 30 pF 15 - 30 pF	150 - 200 pF 15 - 30 pF 15 - 30 pF
HS	8 MHz 10 MHz 20 MHz	15 - 30 pF 15 - 30 pF 15 - 30 pF	15 - 30 pF 15 - 30 pF 15 - 30 pF
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.			

Crystals to be Characterized:		
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM
200 kHz	STD XTL 200.000 kHz	± 20 PPM
2.0 MHz	ECS ECS-20-S-2	± 50 PPM
4.0 MHz	ECS ECS-40-S-4	± 50 PPM
10.0 MHz	ECS ECS-100-S-4	± 50 PPM
20.0 MHz	ECS ECS-200-S-4	± 50 PPM

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9.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 9-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 9-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

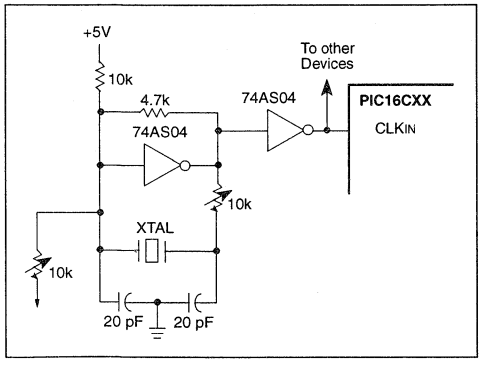
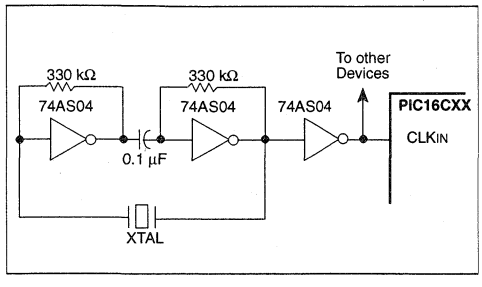


Figure 9-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 9-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



9.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 9-6 shows how the R/C combination is connected to the PIC16CXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kΩ and 100 kΩ.

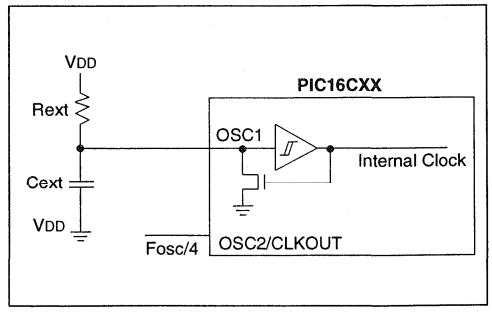
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 11.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 11.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

FIGURE 9-6: RC OSCILLATOR MODE



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9.3 Reset

The PIC16CXX differentiates between various kinds of reset:

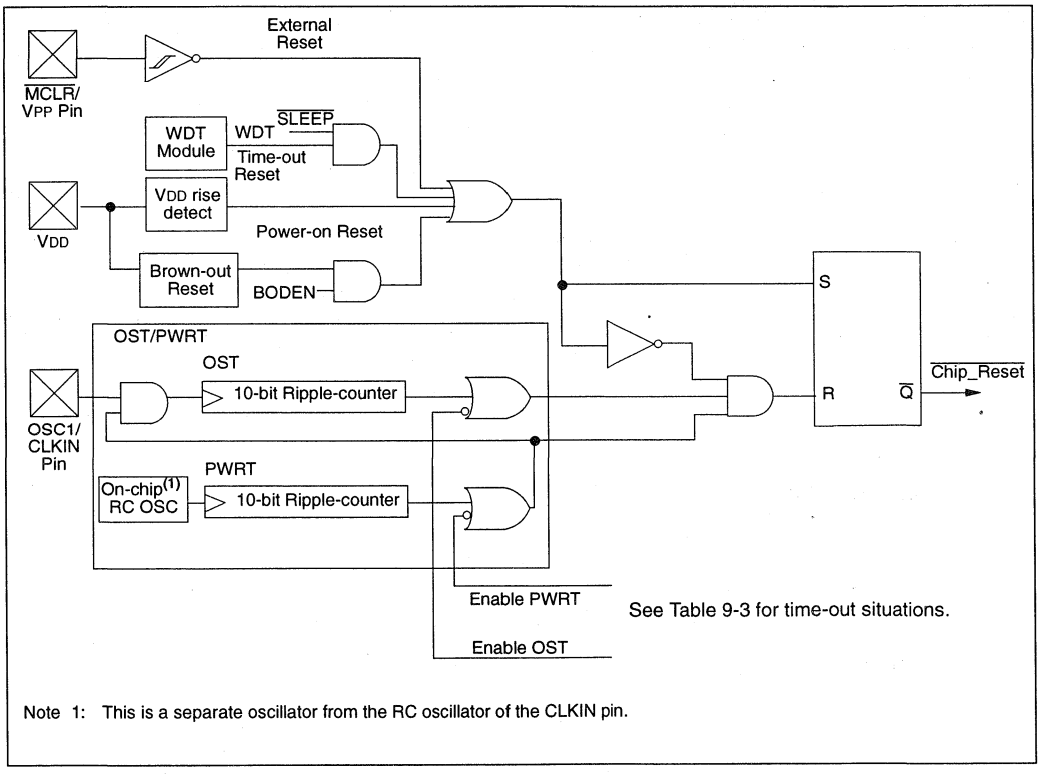
a) Power-on reset (POR)
b) $\overline{MCLR}$ reset during normal operation
c) $\overline{MCLR}$ reset during SLEEP
d) WDT reset (normal operation)
e) WDT wake-up (SLEEP)
f) Brown-out Reset (BOR)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on reset, on $\overline{MCLR}$ or WDT reset and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 9-4. These bits are used in software to determine the nature of the reset. See Table 9-6 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 9-7.

The $\overline{MCLR}$ reset path has a noise filter to detect and ignore small pulses. See Table 10-6 for pulse width specification.

FIGURE 9-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.

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9.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

9.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.6 V – 1.8 V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce internal reset when VDD declines.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607 "Power-up Trouble Shooting".

9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, $\overline{PWRTE}$ can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

The Power-Up Time delay will vary from chip to chip and due to VDD, temperature and process variation. See DC parameters for details.

9.4.3 OSCILLATOR START-UP TIMER (OST)

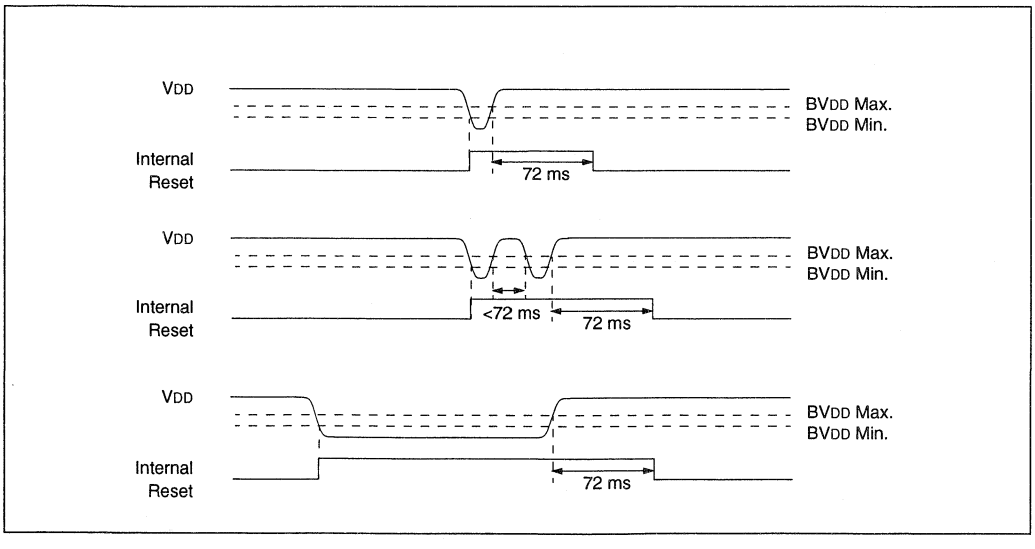
The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on power-on reset or wake-up from SLEEP.

9.4.4 BROWN-OUT RESET (BOR)

The PIC16C62X members have on-chip Brown-out Reset circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (3.8V – 4.2V range) for greater than parameter 35 in Table 10-6, the brown-out situation will reset the chip. A reset is not guaranteed to occur if VDD falls below 4.0V for less than parameter 35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in reset an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-Up Timer will execute a 72 ms reset. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 9-8 shows typical Brown-out situations.

FIGURE 9-8: BROWN-OUT SITUATIONS



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9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and $\overline{PWRTE}$ bit status. For example, in RC mode with $\overline{PWRTE}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 9-9, Figure 9-10 and Figure 9-11 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (see Figure 9-10). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-5 shows the reset conditions for some special registers, while Table 9-6 shows the reset conditions for all the registers.

9.4.6 POWER CONTROL/STATUS REGISTER (PCON)

The power control/status register, PCON (address 8Eh) has two bits.

Bit0 is $\overline{BO}$ (Brown-out). $\overline{BO}$ is unknown on power-on-reset. It must then be set by the user and checked on subsequent resets to see if $\overline{BO}$ = 0 indicating that a brown-out has occurred. The $\overline{BO}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is $\overline{POR}$ (Power-on-reset). It is a '0' on power-on-reset and unaffected otherwise. The user must write a '1' to this bit following a power-on-reset. On a subsequent reset if $\overline{POR}$ is '0', it will indicate that a power-on-reset must have occurred (V_{DD} may have gone too low).

TABLE 9-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset	Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	72 ms + 1024 TOSC	1024 TOSC	72 ms + 1024 TOSC	1024 TOSC
RC	72 ms	—	72 ms	—

TABLE 9-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	
0	x	1	1	Power-on-reset
0	x	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{MCLR}$ reset during normal operation
1	1	1	0	$\overline{MCLR}$ reset during SLEEP

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TABLE 9-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
$\overline{MCLR}$ reset during normal operation	000h	0001 1uuu	---- --uu
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	---- --uu
WDT reset	000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
Interrupt Wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.
Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 9-6: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	• MCLR Reset during normal operation • MCLR Reset during SLEEP • WDT Reset • Brown-out Reset(1)	• Wake up from SLEEP through interrupt • Wake up from SLEEP through WDT time-out
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---x xxxx	---u uuuu	---u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CMCON	1Fh	00-- 0000	00-- 0000	uu-- uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000x	uuuu uuuu(2)
PIR1	0Ch	-0-- ----	-0-- ----	-u-- ----(2)
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	-0-- ----	-0-- ----	-u-- ----
PCON	8Eh	---- --0x	---- --uq(1)	---- --uu
VRCON	9Fh	000- 0000	000- 0000	uuu- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.
Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.
2: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
4: See Table 9-5 for reset value for specific condition.

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FIGURE 9-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): CASE 1

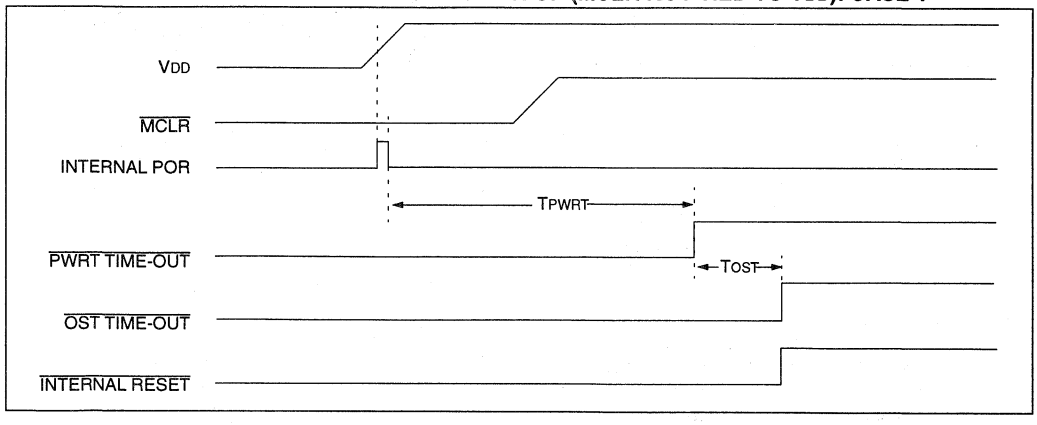

FIGURE 9-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): CASE 2

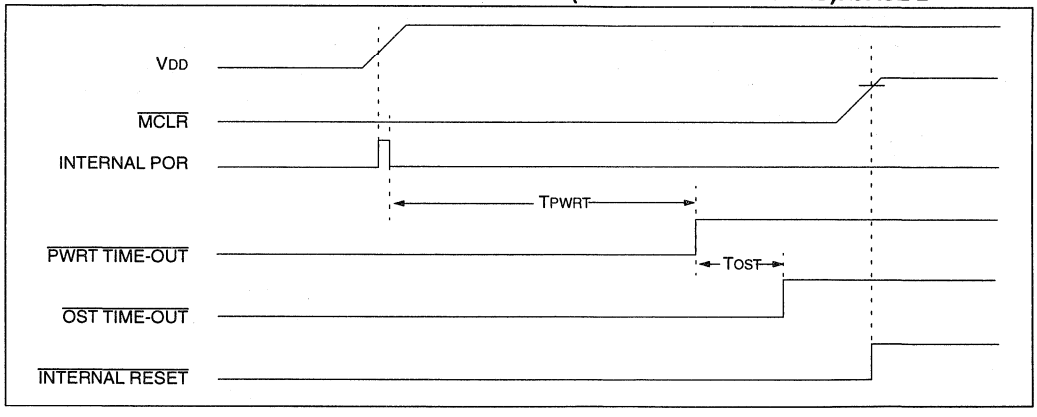

FIGURE 9-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD)

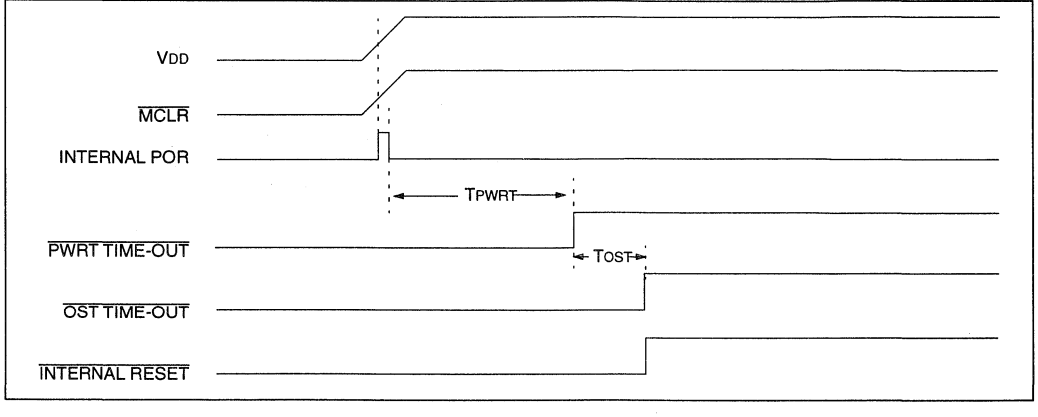

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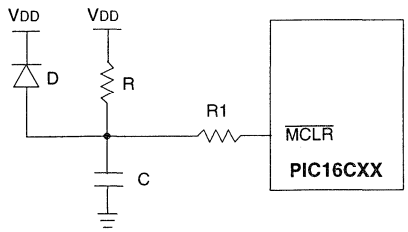
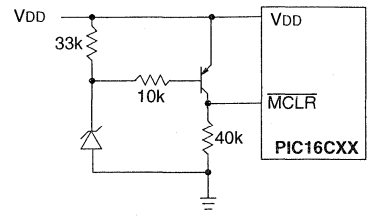
FIGURE 9-12: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



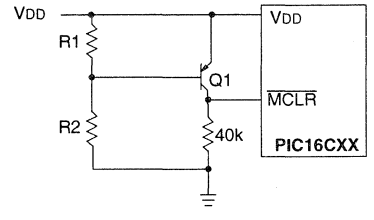
Note 1: External power-on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2: < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
2: Internal Brown-out Reset circuitry should be disabled when using this circuit.

FIGURE 9-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \times \frac{R1}{R1 + R2} = 0.7\ V$$

2: Internal brown-out detection should be disabled when using this circuit.
3: Resistors should be adjusted for the characteristics of the transistor.

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9.5 Interrupts

The PIC16C62X has 4 sources of interrupt:

- External interrupt RB0/INT
- TMR0 overflow interrupt
- PortB change interrupts (pins RB7:RB4)
- Comparator interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits interrupt routine as well as sets the GIE bit, which re-enable RB0/INT interrupts.

The INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

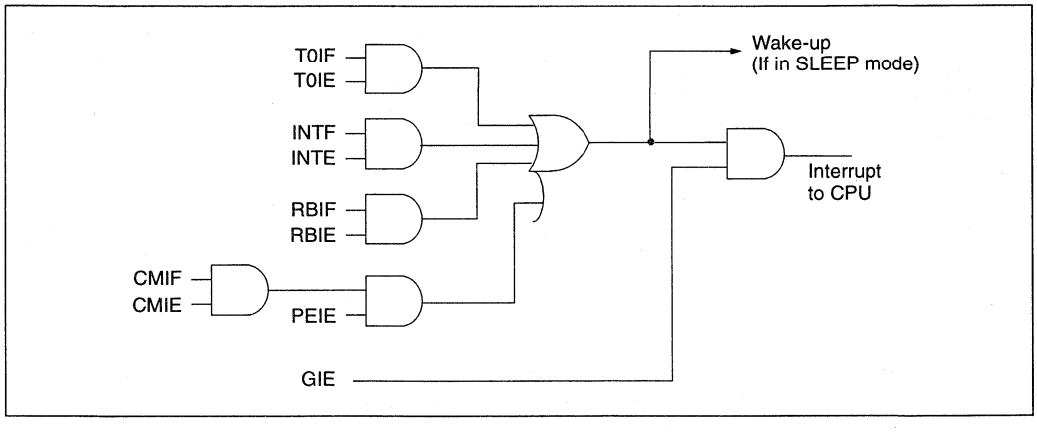
The peripheral interrupt flag is contained in the special register PIR1. The corresponding interrupt enable bit is contained in special registers PIE1.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid RB0/INT recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 9-16). The latency is the same for one or two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note 1:	Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.
2:	en an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The CPU will execute a NOP in the cycle immediately following the instruction which clears the GIE bit. The interrupts which were ignored are still pending to be serviced when the GIE bit is set again.

FIGURE 9-15: INTERRUPT LOGIC



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9.5.1 RB0/INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.8 for details on SLEEP and Figure 9-19 for timing of wake-up from SLEEP through RB0/INT interrupt.

9.5.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 6.0.

9.5.3 PORTB INTERRUPT

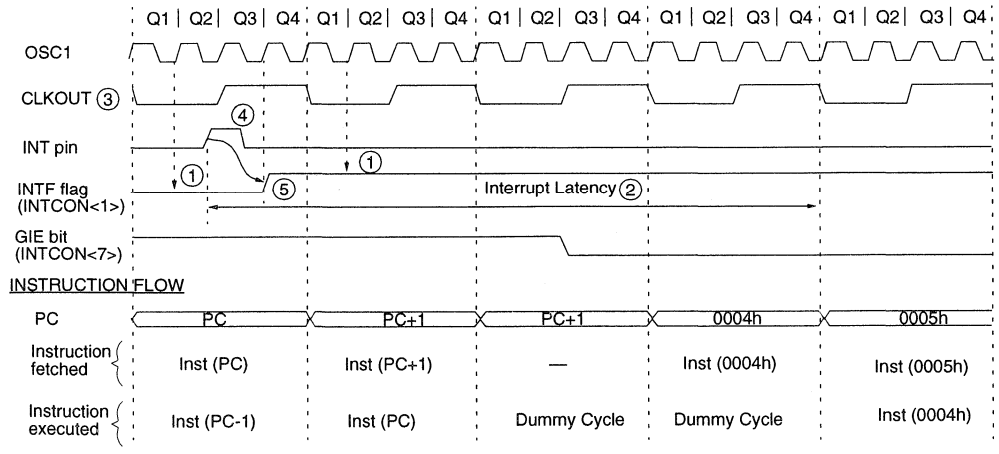
An input change on PORTB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB (Section 5.2).

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

9.5.4 COMPARATOR INTERRUPT

See Section 7.6 for complete description of comparator interrupts.

FIGURE 9-16: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

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9.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt e.g. W register and STATUS register. This will have to be implemented in software.

Example 9-1 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 9-1:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

EXAMPLE 9-1: SAVING THE STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP          ;copy W to temp register,
                        ;could be in either bank
SWAPF   STATUS,W        ;swap status to be saved into W
BCF     STATUS,RP0      ;change to bank 0 regardless
                        ;of current bank
MOVWF   STATUS_TEMP     ;save status to bank 0
                        ;register
    :
    :   (ISR)
    :
SWAPF   STATUS_TEMP,W   ;swap STATUS_TEMP register
                        ;into W, sets bank to original
                        ;state
MOVWF   STATUS          ;move W into STATUS register
SWAPF   W_TEMP,F        ;swap W_TEMP
SWAPF   W_TEMP,W        ;swap W_TEMP into W
```

9.7 Watchdog Timer (WDT)

The watchdog timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

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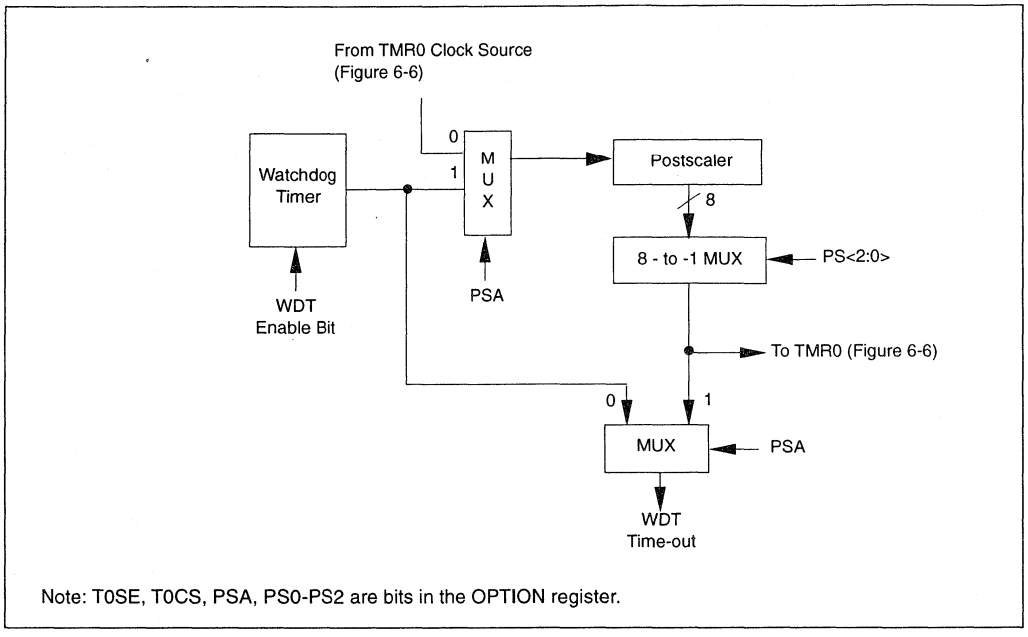
FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM



Note: T0SE, T0CS, PSA, PS0-PS2 are bits in the OPTION register.

FIGURE 9-18: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN(1)	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

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9.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

Note:	It should be noted that a RESET generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.

9.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The first event will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. $\overline{TO}$ bit is cleared if WDT Wake-up occurred.

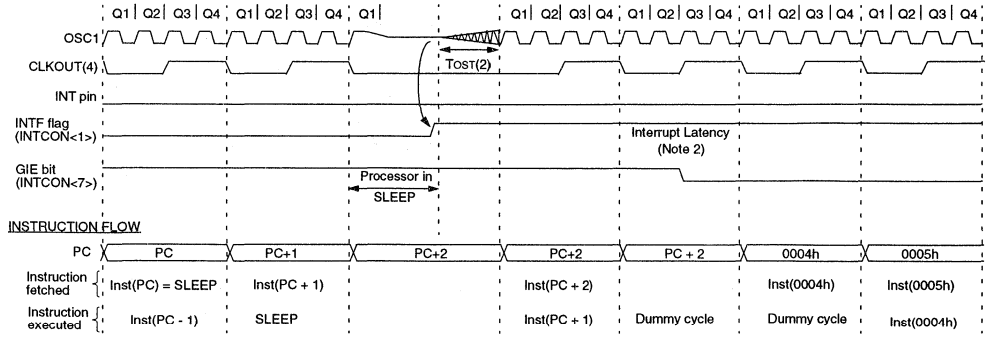
When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

Note:	If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wakeup from sleep. The sleep instruction is completely executed.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

7

FIGURE 9-19: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

9.9 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

9.10 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. Only the least significant 4 bits of the ID locations are used.

9.11 In-Circuit Serial Programming

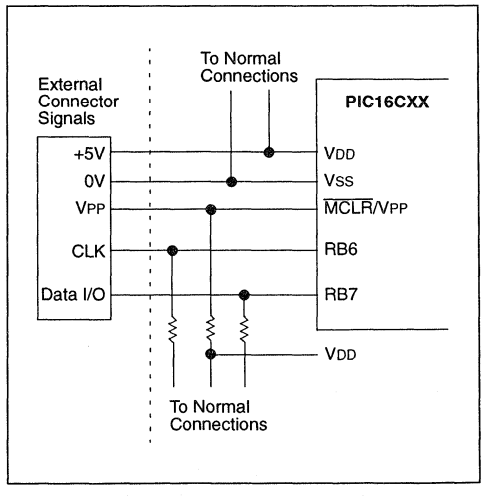
The PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

A typical in-circuit serial programming connection is shown in Figure 9-20.

FIGURE 9-20: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



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10.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias ..... -40° to +125°C

Storage Temperature ..... -65° to +150°C

Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.6V to VDD +0.6V

Voltage on VDD with respect to VSS ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V

Total power Dissipation (Note 1) 1.0W

Maximum Current out of VSS pin ..... 300 mA

Maximum Current into VDD pin ..... 250 mA

Input Clamp Current, IIK (VI <0 or VI> VDD) ..... ±20 mA

Output Clamp Current, IOK (VO <0 or VO>VDD) ..... ±20 mA

Maximum Output Current sunk by any I/O pin ..... 25 mA

Maximum Output Current sourced by any I/O pin ..... 25 mA

Maximum Current sunk by PORTA and PORTB ..... 200 mA

Maximum Current sourced by PORTA and PORTB ..... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 10-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C62X-04	PIC16C62X-20	PIC16LC62X-04	PIC16C62X/JW
RC	VDD: 4.0V to 6.0V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 4.0 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. @3.0V IPD: 0.7 µA typ. @3.0V Freq: 4.0 MHz max.	VDD: 3.0V to 6.0V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz Max.
XT	VDD: 4.0V to 6.0V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 4.0 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. @3.0V IPD: 0.7 µA typ. @3.0V Freq: 4.0 MHz max.	VDD: 3.0V to 6.0V IDD: 3.3 mA max. @5.5V IPD: 20 µA max. @4.0V Freq: 4.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 9.0 mA typ. @5.5V IPD: 1.0 µA typ. @4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. @5.5V IPD: 1.0 µA typ. @4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 35 µA typ. @32 kHz, 3.0V IPD: 1.0 µA typ. @4.0 V Freq: 200 kHz maximum	Do not use in LP mode	VDD: 2.5V to 6.0V IDD: 32 µA max. @32 kHz, 3.0V IPD: 9.0 µA max. @3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 32 µA max. @32 kHz, 3.0V IPD: 9.0 µA Max. @3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that guarantees the specifications required.

10.1 DC CHARACTERISTICS: PIC16C62X-04 (Commercial, Industrial, Automotive) PIC16C62X-20 (Commercial, Industrial, Automotive)

		Standard Operating Conditions (unless otherwise stated) Operating temperature −40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and −40°C ≤ TA ≤ +125°C for automotive					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002	VDR	RAM Data Retention Voltage (Note 1)	–	1.5*	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	–	VSS	–	V	See section on power-on reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	–	–	V/ms	See section on power-on reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.3	V	BODEN configuration bit is cleared
			3.7	4.0	4.4		(Automotive)
D010	IDD	Supply Current (Note 2)	–	1.8	3.3	mA	XT and RC osc configuration FOSC = 4 MHz, VDD = 5.5V, WDT disabled (Note 4)
D010A			–	35	70	µA	LP osc configuration, PIC16C62X-04 only FOSC = 32 kHz, VDD = 4.0V, WDT disabled
D013			–	9.0	20	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V, WDT disabled
	ΔIWDT	WDT Current (Note 5)	–	6.0	20	µA	VDD = 4.0V
					25	µA	(125°C)
D015	ΔIBOR	Brown-out Reset Current (Note 5)	–	350	425	µA	BOR enabled, VDD = 5.0V
	ΔICOMP	Comparator Current for each Comparator (Note 5)	–		100	µA	VDD = 4.0V
	ΔIVREF	VREF Current (Note 5)	–		300	µA	VDD = 4.0V
D020	IPD	Power Down Current (Note 3)	–	1.0	2.5	µA	VDD=4.0V, WDT disabled
					15	µA	(125°C)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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10.1 DC CHARACTERISTICS: PIC16C62X-04 (Commercial, Industrial, Automotive) PIC16C62X-20 (Commercial, Industrial, Automotive) (Cont.)

		Standard Operating Conditions (unless otherwise stated) Operating temperature −40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and −40°C ≤ TA ≤ +125°C for automotive					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	ΔIWDT	WDT Current (Note 5)	–	6.0	20	μA	VDD=4.0V
					25	μA	(125°C)
D023	ΔIBOR	Brown-out Reset Current (Note 5)	–	350	425	μA	BOR enabled, VDD = 5.0V
	ΔICOMP	Comparator Current for each Comparator (Note 5)	–		100	μA	VDD = 4.0V
	ΔIVREF	VREF Current (Note 5)	–		300	μA	VDD = 4.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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10.2 DC CHARACTERISTICS: PIC16LC62X-04 (Commercial, Industrial)

		Standard Operating Conditions (unless otherwise stated) Operating temperature −40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	3.0 2.5	-	6.0 6.0	V	XT and RC osc configuration LP osc configuration
D002	VDR	RAM Data Retention Voltage (Note 1)	–	1.5*	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	–	VSS	–	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	–	–	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.3	V	BODEN configuration bit is cleared
D010	IDD	Supply Current (Note 2)	–	1.4	2.5	mA	XT and RC osc configuration FOSC = 2.0 MHz, VDD = 3.0V, WDT disabled (Note 4)
D010A			–	26	53	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
	ΔIWDT	WDT Current (Note 5)	–	6.0	15	µA	VDD = 3.0V
D015	ΔIBOR	Brown-out Reset Current (Note 5)	–	350	425	µA	$\overline{BOR}$ enabled, VDD = 5.0V
	ΔICOMP	Comparator Current for each Comparator (Note 5)	–		100	µA	VDD = 3.0V
	ΔIVREF	VREF Current (Note 5)	–		300	µA	VDD = 3.0V
D020	IPD	Power Down Current (Note 3)	–	0.7	2	µA	VDD=3.0V, WDT disabled
	ΔIWDT	WDT Current (Note 5)	–	6.0	15	µA	VDD=3.0V
D023	ΔIBOR	Brown-out Reset Current (Note 5)	–	350	425	µA	$\overline{BOR}$ enabled, VDD = 5.0V
	ΔICOMP	Comparator Current for each Comparator (Note 5)	–		100	µA	VDD = 3.0V
	ΔIVREF	VREF Current (Note 5)	–		300	µA	VDD = 3.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD to VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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10.3 DC CHARACTERISTICS: PIC16C62X (Commercial, Industrial, Automotive)
PIC16LC62X (Commercial, Industrial, Automotive)

		Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for automotive Operating voltage VDD range as described in DC spec Table 10-1 and Table 10-2					
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Unit**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	-	0.8V 0.15VDD	V	VDD = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	VSS		0.2VDD	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)	Vss	-	0.2VDD	V	Note1
D033		OSC1 (in XT and HS)	Vss	-	0.3VDD	V	
		OSC1 (in LP)	Vss	-	0.6VDD-1.0	V	
	VIH	**Input High Voltage**					
		I/O ports		-			
D040		with TTL buffer	2.0V	-	VDD	V	
D041		with Schmitt Trigger input	0.8VDD		VDD		
D042		$\overline{MCLR}$ RA4/T0CKI	0.8VDD	-	VDD	V	
D043		OSC1 (XT, HS and LP)	0.7VDD	-	VDD	V	
D043A		OSC1 (in RC mode)	0.9VDD				Note1
D070	IPURB	PORTB weak pull-up current	50	200	400	µA	VDD = 5.0V, VPIN = VSS
		Input Leakage Current					
	IIL	(Notes 2, 3)					
		I/O ports (Except PORTA)			±1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D060		PORTA	-	-	±0.5	µA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance
D061		RA4/T0CKI	-	-	±1.0	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1, $\overline{MCLR}$	-	-	±5.0	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	**Output Low Voltage**					
D080		I/O ports	-	-	0.6	V	IOL=8.5 mA, VDD=4.5V, -40° to +85°C
			-	-	0.6	V	IOL=7.0 mA, VDD=4.5V, +125°C
D083		OSC2/CLKOUT	-	-	0.6	V	IOL=1.6 mA, VDD=4.5V, -40° to +85°C
		(RC only)	-	-	0.6	V	IOL=1.2 mA, VDD=4.5V, +125°C
	VOH	**Output High Voltage** (Note 3)					
D090		I/O ports (Except RA4)	VDD-0.7	-	-	V	IOH=-3.0 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	-	-	V	IOH=-2.5 mA, VDD=4.5V, +125°C
D092		OSC2/CLKOUT	VDD-0.7	-	-	V	IOH=-1.3 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	-	-	V	IOH=-1.0 mA, VDD=4.5V, +125°C
		(RC only)					
*	VOD	**Open-Drain High Voltage**			14*	V	RA4 pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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10.3 DC CHARACTERISTICS: PIC16C62X (Commercial, Industrial, Automotive) PIC16LC62X (Commercial, Industrial, Automotive) (Cont.)

		Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for automotive Operating voltage VDD range as described in DC spec Table 10-1 and Table 10-2					
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Unit**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	Cio	All I/O pins/OSC2 (in RC mode)			50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

TABLE 10-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 2.5V < VDD < 6.0V, -40°C < TA < +125°C, unless otherwise stated. Current consumption is specified in Table 10-1.

Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Input offset voltage			± 5.0	± 10	mV	
Input common mode voltage		0		VDD - 1.5	V	
CMRR		–35*			db	
Response Time(1)			150*	400* 600*	ns ns	PIC16C62X PIC16LC62X
Comparator Mode Change to Output Valid				10*	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from VSS to VDD.

TABLE 10-3: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 2.5V < VDD < 6.0V, -40°C < TA < +125°C, unless otherwise stated. Current consumption is specified in Table 10-1.

Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Resolution		VDD/24		VDD/32	LSB	
Absolute Accuracy				1/4 1/2	LSB LSB	Low Range (VRR=1) High Range (VRR=0)
Unit Resistor Value (R)			2K*		Ω	Figure 8-2
Settling Time(1)				10*	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

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10.4 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

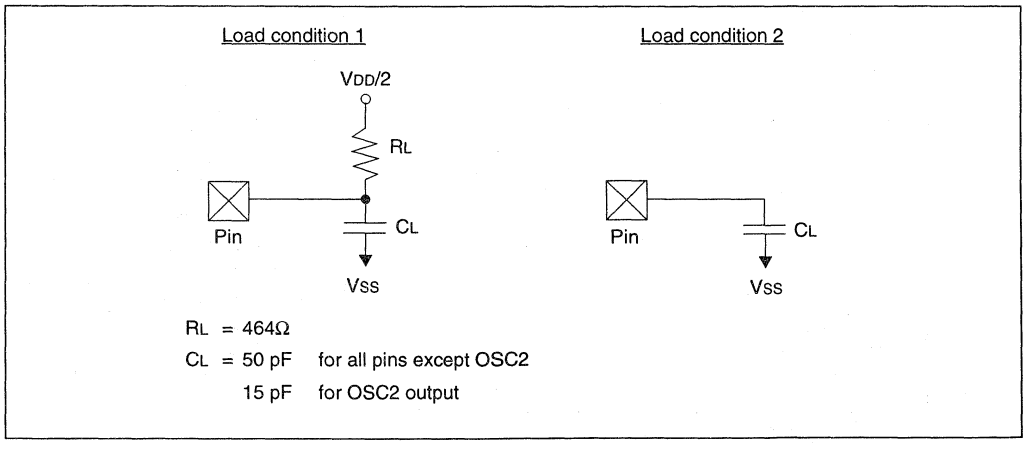
Lowercase subscripts (pp) and their meanings:

pp			
ck	CLKOUT	osc	OSC1
io	I/O port	t0	T0CKI
mc	$\overline{\text{MCLR}}$		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-Impedance

FIGURE 10-1: LOAD CONDITIONS



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10.5 Timing Diagrams and Specifications

FIGURE 10-2: EXTERNAL CLOCK TIMING

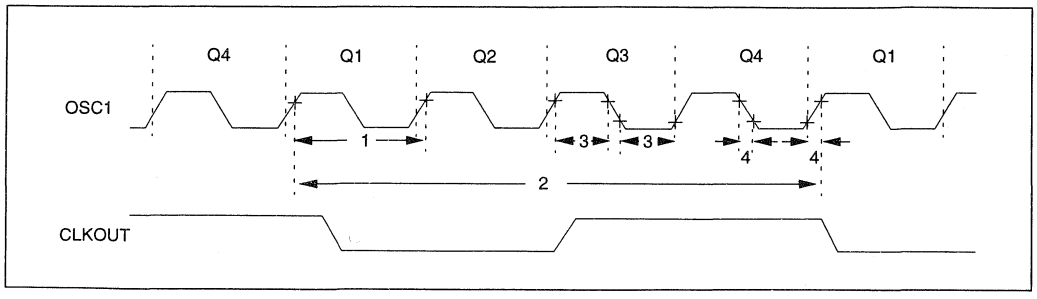

TABLE 10-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode, VDD=5.0V
			DC	—	20	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode, VDD=5.0V
			0.1	—	4	MHz	XT osc mode
			1	—	20	MHz	HS osc mode
			DC	–	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			50	—	—	ns	HS osc mode
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			50	—	1,000	ns	HS osc mode
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	1.0	Fosc/4	DC	µs	TCYS=FOSC/4
3*	TosL, TosH	External Clock in (OSC1) High or Low Time	100*	—	—	ns	XT oscillator, Tosc L/H duty cycle
			2*	—	—	µs	LP oscillator, Tosc L/H duty cycle
			20*	—	—	ns	HS oscillator, Tosc L/H duty cycle
4*	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	25*	—	—	ns	XT oscillator
			50*	—	—	ns	LP oscillator
			15*	—	—	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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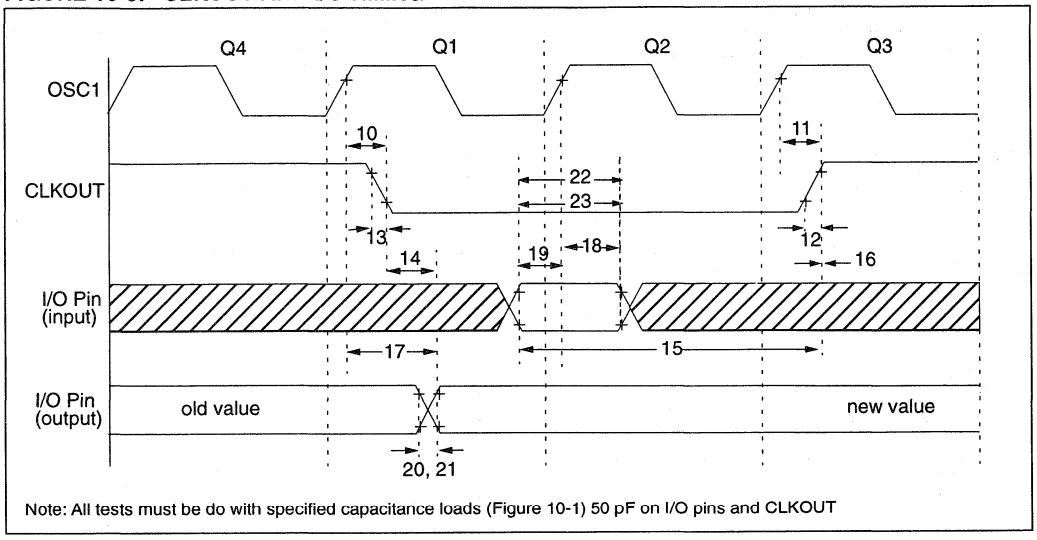
FIGURE 10-3: CLKOUT AND I/O TIMING



Note: All tests must be do with specified capacitance loads (Figure 10-1) 50 pF on I/O pins and CLKOUT

TABLE 10-5: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter #	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓ (1)	— —	75 —	200 400	ns ns	PIC16C62X PIC16LC62X
11*	TosH2ckH	OSC1↑ to CLKOUT↑ (1)	— —	75 —	200 400	ns ns	PIC16C62X PIC16LC62X
12*	TckR	CLKOUT rise time (1)	— —	35 —	100 200	ns ns	PIC16C62X PIC16LC62X
13*	TckF	CLKOUT fall time (1)	— —	35 —	100 200	ns ns	PIC16C62X PIC16LC62X
14*	TckL2ioV	CLKOUT ↓ to Port out valid (1)	—	—	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑ (1)	Tosc +200 ns Tosc +400 ns	— —	— —	ns ns	PIC16C62X PIC16LC62X
16*	TckH2ioI	Port in hold after CLKOUT ↑ (1)	0	—	—	ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	— —	50	150 300	ns ns	PIC16C62X PIC16LC62X
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	— —	— —	ns ns	PIC16C62X PIC16LC62X
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	— —	10 —	40 80	ns ns	PIC16C62X PIC16LC62X
21*	TioF	Port output fall time	— —	10 —	40 80	ns ns	PIC16C62X PIC16LC62X
22*	Tinp	RB0/INT pin high or low time	25 40	— —	— —	ns ns	PIC16C62X PIC16LC62X
23	Trbp	RB<7:4> change interrupt high or low time	TCY	—	—	ns	

* These parameters are characterized but not tested

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC

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FIGURE 10-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

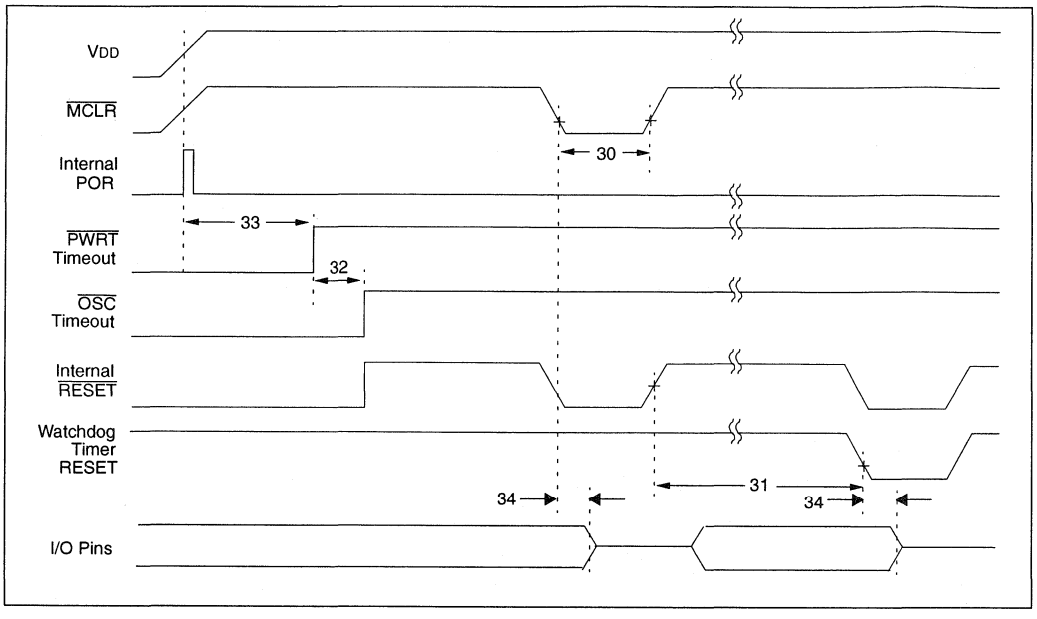

FIGURE 10-5: BROWN-OUT RESET TIMING

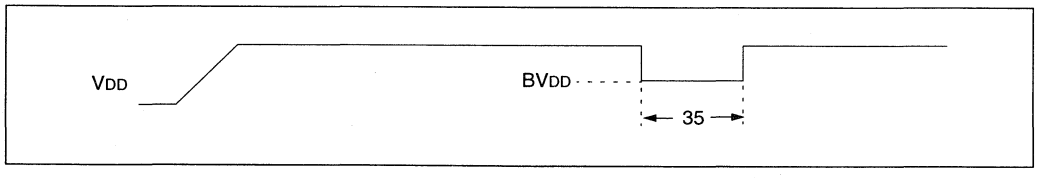

TABLE 10-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2000	—	—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 Tosc	—	—	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	TIOZ	I/O hi-impedance from $\overline{MCLR}$ low		—	2.0	µs	
35	TBOR	Brown-out Reset Pulse Width	100*	—	—	µs	3.8V ≤ VDD ≤ 4.2V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 10-6: TIMER0 CLOCK TIMING

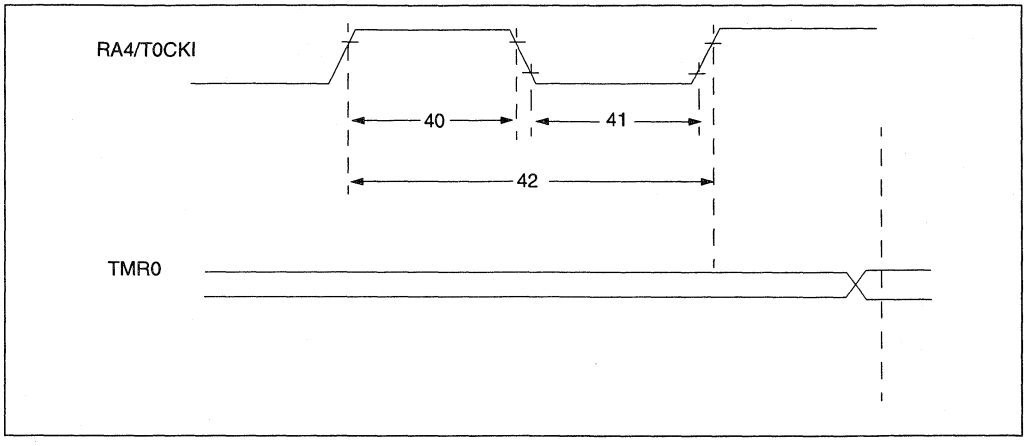


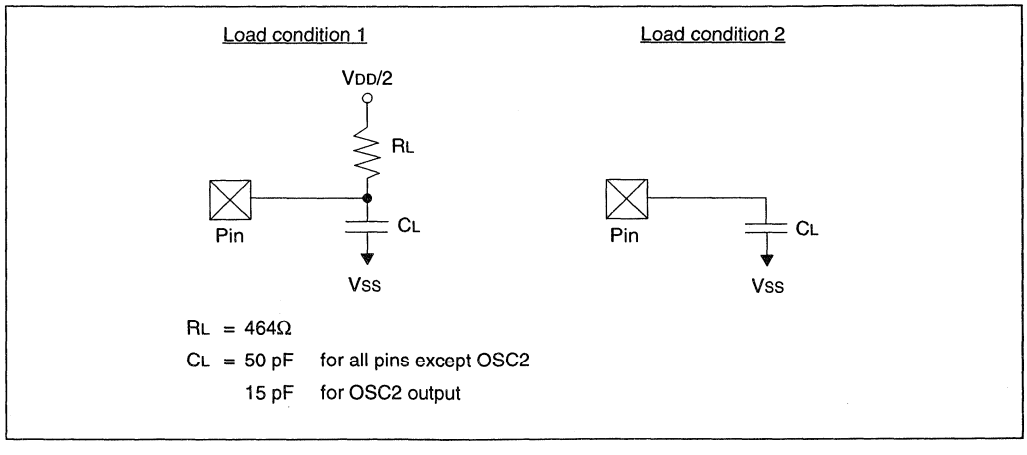
TABLE 10-7: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		TCY + 40* / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 10-7: LOAD CONDITIONS



NOTES:

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11.0 DEVICE CHARACTERIZATION INFORMATION

Not Available at this time.

NOTES:

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APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
3. Data memory paging is slightly redefined. STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
14. FSR is made a full 8-bit register.
15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, /VPP, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-on-Reset ($\overline{POR}$) status bit and a Brown-out Reset status bit ($\overline{BOR}$).
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
18. PORTA inputs are now Schmitt Trigger inputs.
19. Brown-out Reset reset has been added.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

APPENDIX C: WHAT'S NEW

The format of certain sections of this data sheet have been changed to be consistent with other product families.

1. PORTB input buffers have changed to TTL from Schmitt Trigger.

APPENDIX D: WHAT'S CHANGED

1. Table 3-1 was changed to reflect the TTL input buffers on PORTB.
2. Figure 5-5 and Figure 5-6 were updated to reflect the TTL input buffers on PORTB.
3. Figure 9-7 was updated.
4. The orientation of the diode in Figure 9-20 was changed.
5. A device specification for JW devices was added to Table 12-1.
6. Max spec for Brown-out Reset current was changed to 400 μA in Section 12.1 and Section 12.2.
7. Information added to support the 2.5V "LC" devices.

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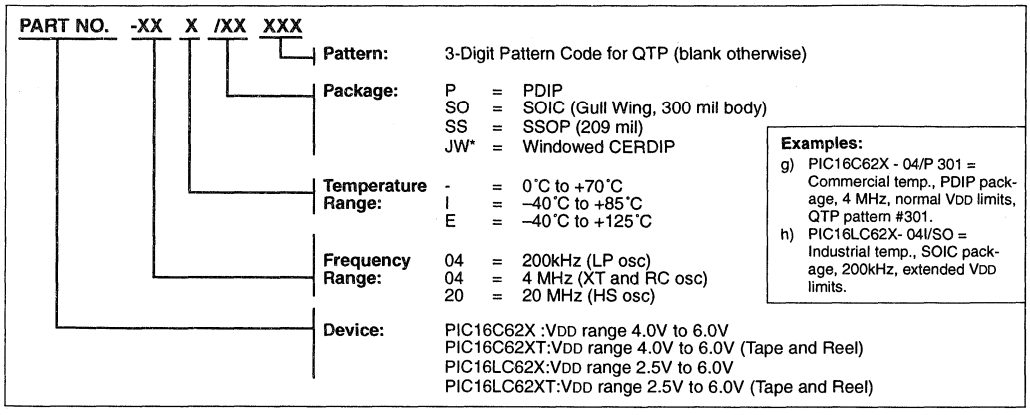
PIC16C62X PRODUCT IDENTIFICATION SYSTEM

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

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Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office.
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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MICROCHIP

SECTION 8
PIC16C6XX MICROCONTROLLER PRODUCT BRIEFS

PIC16C641/642 28-Pin EPROM 8-Bit Microcontroller Product Brief 8-1
PIC16C661/662 40/44-Pin EPROM 8-Bit Microcontroller Product Brief 8-3

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PIC16C641/642

28-Pin EPROM 8-Bit Microcontroller Product Brief

Device	Program Memory	Data Memory	Pins	Analog Comparators	Prog. Vref	PSP	In-circuit Programming
PIC16C641	2K x 14	128 x 8	28	2	Yes	No*	Yes
PIC16C642	4K x 14	176 x 8	28	2	Yes	No*	Yes

High Performance RISC CPU:

- Simple instruction set - 35 total
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle
- ★ Up to 4K x 14 on-chip EPROM program memory
- ★ Program memory hardware parity check
- Up to 176 x 8 general purpose registers (SRAM)
- 8 levels of hardware stack
- Direct, Indirect and Relative addressing modes
- Interrupt capability

Peripheral Features:

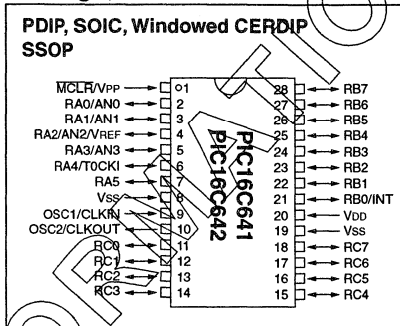
- 22 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- ★ 2 Analog Comparators with input multiplexing
- ★ Programmable reference voltage for comparators

Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- ★ Brown-out Protection
- Watchdog Timer (WDT) with dedicated on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-system programming (via two pins)
- 4 user programmable ID locations

Pin Diagram

PDIP, SOIC, Windowed CERDIP
★ **SSOP**



CMOS Technology:

- ★ Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range: 3.0V to 6.0V
- Commercial, industrial and automotive temperature ranges
- Low power consumption
- < 2.0 mA @ 5.0V, 4.0 MHz
- 15 µA typical @ 3.0V, 32 kHz
- < 1.0 µA typical standby current @ 3.0V

ADVANCE INFORMATION

8

* PIC16C661/662 devices available with Parallel Slave Port (PSP).

NOTES:

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PIC16C661/662

40/44-Pin EPROM 8-Bit Microcontroller Product Brief

Device	Program Memory	Data Memory	Pins	Analog Comparators	Prog. Vref	PSP	In-circuit Programming
PIC16C661	2K x 14	128 x 8	40-44	2	Yes	Yes*	Yes
PIC16C662	4K x 14	176 x 8	40-44	2	Yes	Yes*	Yes

High Performance RISC CPU:

- Simple instruction set - 35 total
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle
- ★ Up to 4K x 14 on-chip EPROM program memory
- ★ Program memory hardware parity check
- Up to 176 x 8 general purpose registers (SRAM)
- 8 levels of hardware stack
- Direct, Indirect and Relative addressing modes
- Interrupt capability

Peripheral Features:

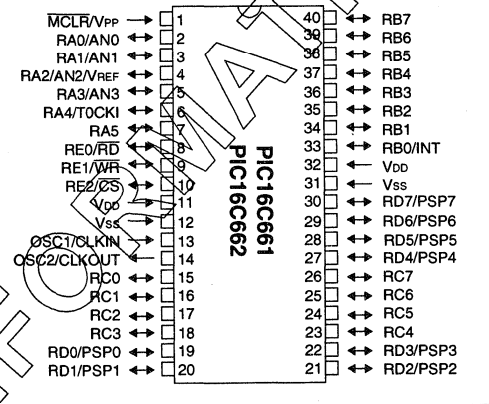
- 33 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- ★ Parallel Slave Port (PSP) 8 bits wide with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls
- ★ 2 Analog Comparators with input multiplexing
- ★ Programmable reference voltage for comparators

Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- ★ Brown-out Protection
- Watchdog Timer (WDT) with dedicated on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-system programming (via two pins)
- 4 user programmable ID locations

Pin Diagram

PDIP, Windowed CERDIP (Also PLCC, MQFP)



CMOS Technology:

- ★ Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range: 3.0V to 6.0V
- Commercial, industrial and automotive temperature ranges
- Low power consumption
- < 2.0 mA @ 5.0V, 4.0 MHz
- 15 µA typical @ 3.0V, 32 kHz
- < 1.0 µA typical standby current @ 3.0V

ADVANCE INFORMATION

8

* PIC16C641/642 devices available without Parallel Slave Port (PSP).

NOTES:

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MICROCHIP

SECTION 9
PIC16C6X MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC16C6X 8-Bit CMOS Microcontrollers 9-1
PIC16CR63/65 8-Bit ROM-Based Microcontroller Product Brief 9-243
PIC16C66/67 EPROM-Based 8-Bit Microcontroller Product Brief 9-245

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MICROCHIP

PIC16C6X

8-Bit CMOS Microcontrollers

Devices included in this data sheet:

- PIC16C61
- PIC16C62
- PIC16C62A
- PIC16CR62
- PIC16C63
- PIC16C64
- PIC16C64A
- PIC16CR64
- PIC16C65
- PIC16C65A

PIC16C6X Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide operating voltage range: 2.5V to 6.0V
- Commercial, Industrial, and Automotive temperature ranges
- Low-power consumption:
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

PIC16C6X Peripheral Features:

- Timer0: 8-bit timer/counter with prescaler
- Timer1: 16-bit timer/counter with prescaler. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with period register, prescaler and postscaler
- Capture/Compare/PWM module(s)
- Capture is 16-bit, max resolution 12.5 ns, Compare is 16-bit, max resolution 200 ns, max. PWM resolution is 10-bit.
- Synchronous Serial Port (SSP) with SPI and I^2C™
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bits wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIC16C6X Features	61	62	62A	R62	63	64	64A	R64	65	65A
Program Memory (EPROM) x 14	1K	2K	2K	—	4K	2K	2K	—	4K	4K
(ROM) x 14	—	—	—	2K	—	—	—	2K	—	—
Data Memory (Bytes) x 8	36	128	128	128	192	128	128	128	192	192
I/O Pins	13	22	22	22	22	33	33	33	33	33
Parallel Slave Port	—	—	—	—	—	Yes	Yes	Yes	Yes	Yes
Capture/Compare/PWM Module	—	1	1	1	2	1	1	1	2	2
Timer Modules	1	3	3	3	3	3	3	3	3	3
Serial Communication	—	SPI/ I^2C	SPI/ I^2C	SPI/ I^2C	SPI/I^2C, USART	SPI/ I^2C	SPI/ I^2C	SPI/ I^2C	SPI/I^2C, USART	SPI/I^2C, USART
In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset	—	—	Yes	Yes	Yes	—	Yes	Yes	—	Yes
Interrupt Sources	3	7	7	7	10	8	8	8	11	11
Sink/Source Current (mA)	25/20	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25	25/25

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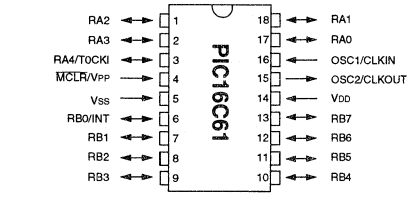
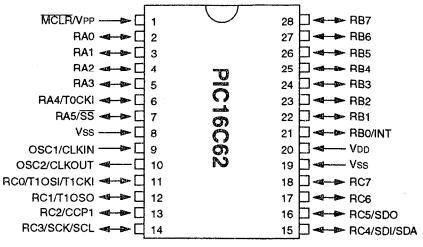
Pin Diagrams

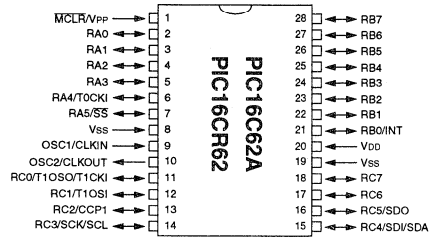
PDIP, SOIC, Windowed CERDIP



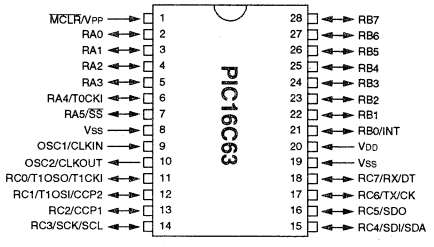
SDIP, SOIC, SSOP, Windowed CERDIP



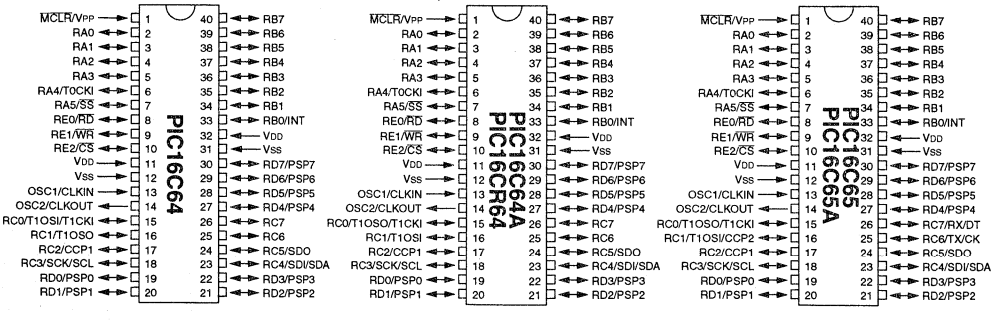
SDIP, SOIC, SSOP, Windowed CERDIP



SDIP, SOIC, Windowed CERDIP



PDIP, Windowed CERDIP



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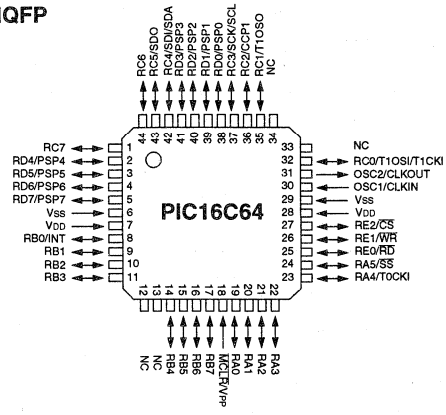
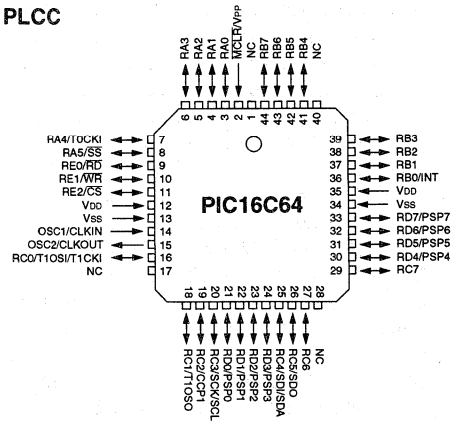
Pin Diagrams (Cont.'d)

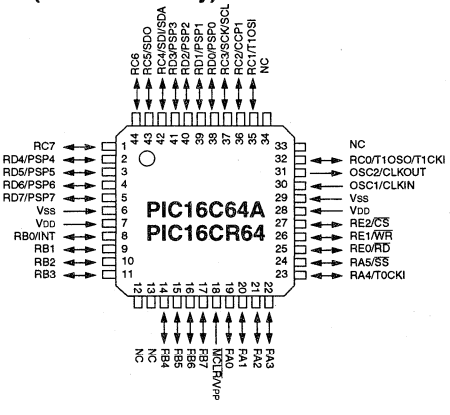
MQFP



PLCC



MQFP, TQFP (PIC16C64A only)



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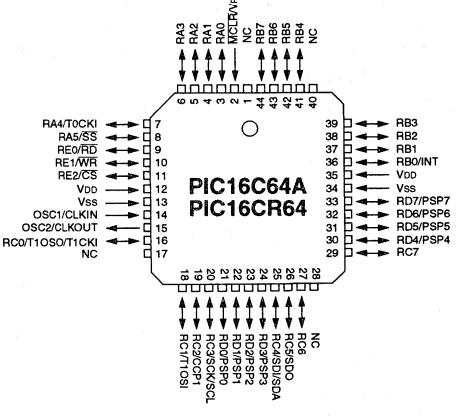
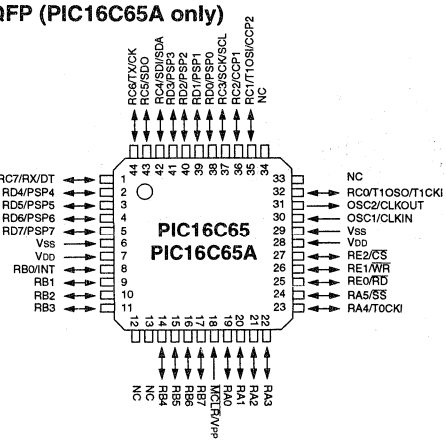


MQFP, TQFP (PIC16C65A only)



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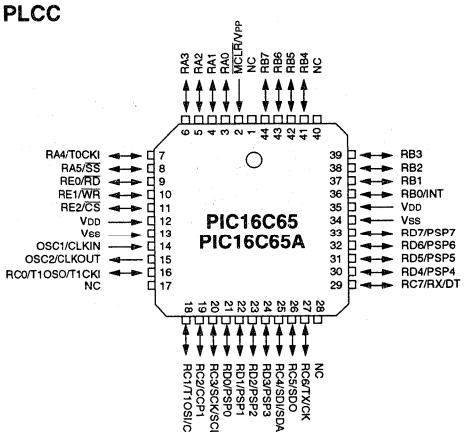

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For register and module descriptions in this data sheet, device legends show which devices apply to those sections. For example, the legend below shows that some features of only the PIC16C62A, PIC16CR62, PIC16C63, PIC16C64A, PIC16CR64, and PIC16C65A are described in this section.

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

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1.0 GENERAL DESCRIPTION

The PIC16CXX is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16CXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C61** device has 36 bytes of RAM and 13 I/O pins. In addition a timer/counter is available.

The **PIC16C62/62A/R62** devices have 128 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI™) or the two-wire Inter-Integrated Circuit (I^2C) bus.

The **PIC16C63** device has 192 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also know as a Serial Communications Interface or SCI.

The **PIC16C64/64A/R64** devices have 128 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. An 8-bit Parallel Slave Port is also provided.

The **PIC16C65/65A** devices have 192 bytes of RAM and 33 I/O pins. In addition, several peripheral features are available, including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also known as a Serial Communications Interface or SCI. An 8-bit Parallel Slave Port is also provided.

The PIC16C6X device family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers a power saving mode. The user can wake the chip from SLEEP through several external and internal interrupts, and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

A UV erasable CERDIP packaged version is ideal for code development, while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C6X family fits perfectly in applications ranging from high-speed automotive and appliance control to low-power remote sensors, keyboards and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use, and I/O flexibility make the PIC16C6X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, serial communication, capture and compare, PWM functions, and co-processor applications).

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to PIC16CXX family of devices (Appendix B).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer, and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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TABLE 1-1: PIC16C6X FAMILY OF DEVICES

	Clock	Memory				Peripherals				Features			
	Maximum Frequency of Operation (MHz)	EPROM	ROM	Data Memory (bytes)	Program Memory (X14 words)	Timer Module(s)	Capture/Compare/PWM Module(s)	Serial Port(s) (SPI/I²C, USART)	Parallel Slave Port	Interrupt Sources	I/O Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Brown-out Reset	Packages
PIC16C62	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I²C	—	7	22	3.0-6.0	Yes	—	28-pin SDIP, SOIC, SSOP
PIC16C62A(1)	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I²C	—	7	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP
PIC16CR62(1)	20	—	2K	128	TMR0, TMR1, TMR2	1	SPI/I²C	—	7	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP
PIC16C63	20	4K	—	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	—	10	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16CR63(1)	20	—	4K	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	—	10	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16C64	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I²C	Yes	8	33	3.0-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP
PIC16C64A(1)	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I²C	Yes	8	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP
PIC16CR64(1)	20	—	2K	128	TMR0, TMR1, TMR2	1	SPI/I²C	Yes	8	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP
PIC16C65	20	4K	—	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	Yes	11	33	3.0-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP
PIC16C65A(1)	20	4K	—	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	Yes	11	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP
PIC16CR65(1)	20	—	4K	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	Yes	11	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.
All PIC16C6X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

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2.0 PIC16C6X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C6X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C6X family of devices, there are four device "types" as indicated in the device number:

1. **C**, as in PIC16**C**64. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**64. These devices have EPROM type memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**64. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**64. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes. Microchip's PICSTART® and PRO MATE™ programmers both support the PIC16C6X. Third party programmers also are available; refer to the *Microchip Third Party Guide* for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP^{SM}) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

ROM devices do not allow serialization information in the program memory space. The user may have this information programmed in the data memory space.

For information on submitting ROM code, please contact your regional sales office.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

For information on submitting ROM code, please contact your regional sales office.

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NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data may be fetched from the same memory using the same bus. Separating program and data busses further allows instructions to be sized differently than 8-bit wide data words. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C61 addresses 1K x 14 of program memory. The PIC16C62/62A/R62/64/64A/R64 address 2K x 14 of program memory, and the PIC16C63/65/65A devices address 4K x 14 of program memory. All program memory is internal.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of "special optimal situations" makes programming with the PIC16CXX simple yet efficient, thus significantly reducing the learning curve.

The PIC16CXX device contains an 8-bit ALU and working register (W). The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending upon the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. Bits C and DC operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

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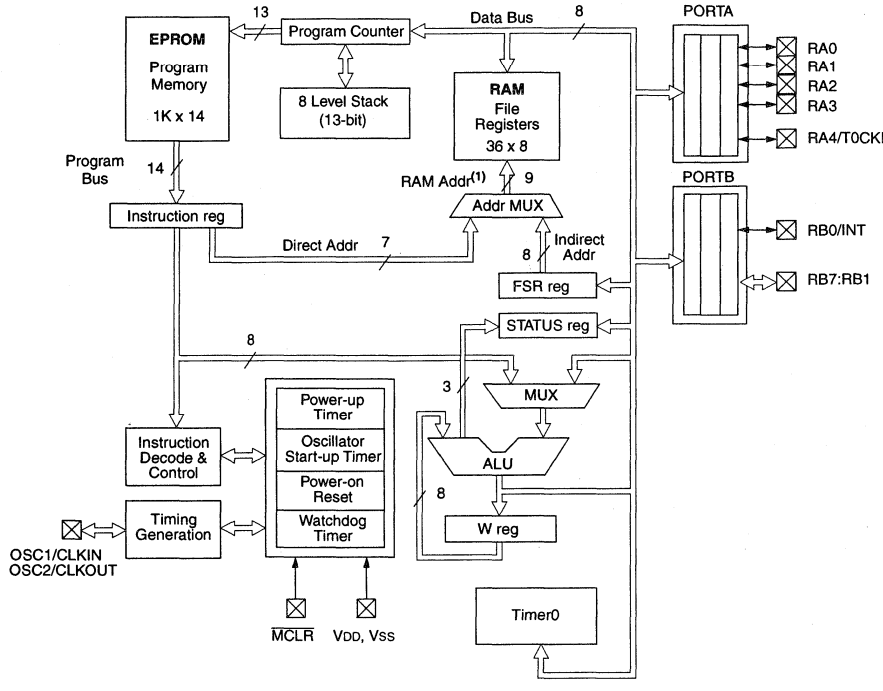
FIGURE 3-1: PIC16C61 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.

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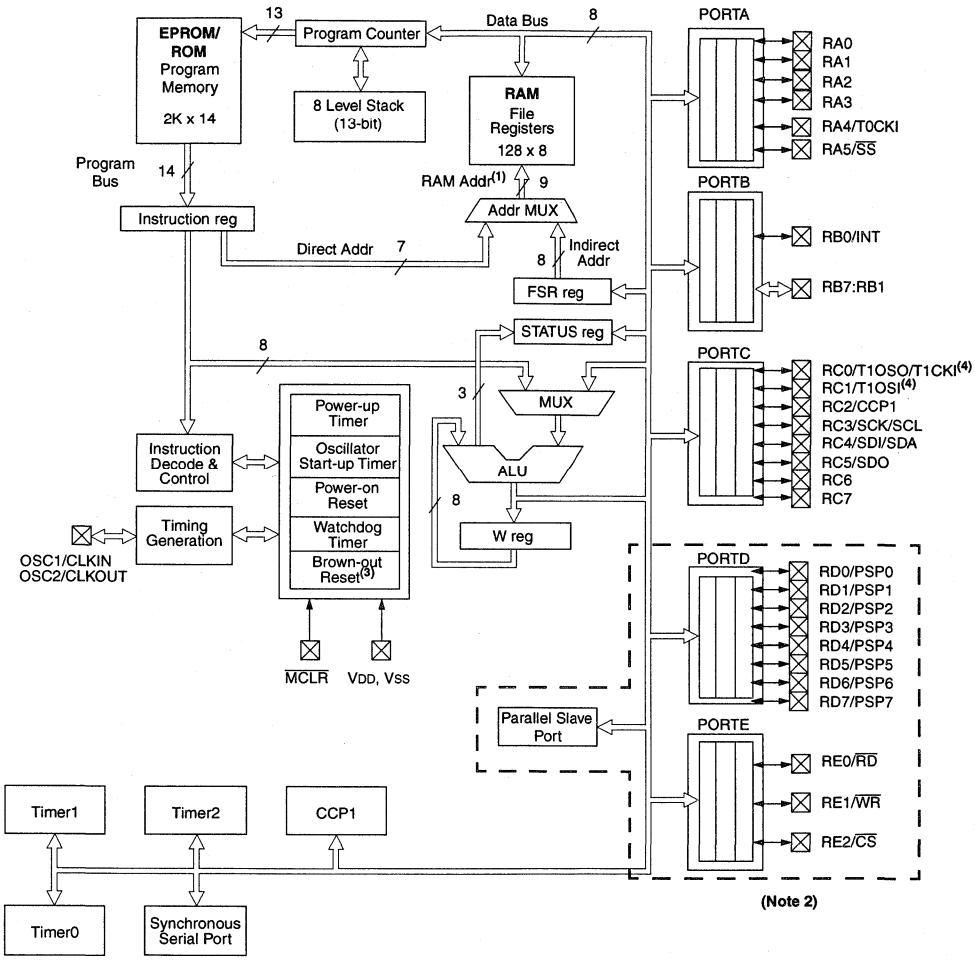
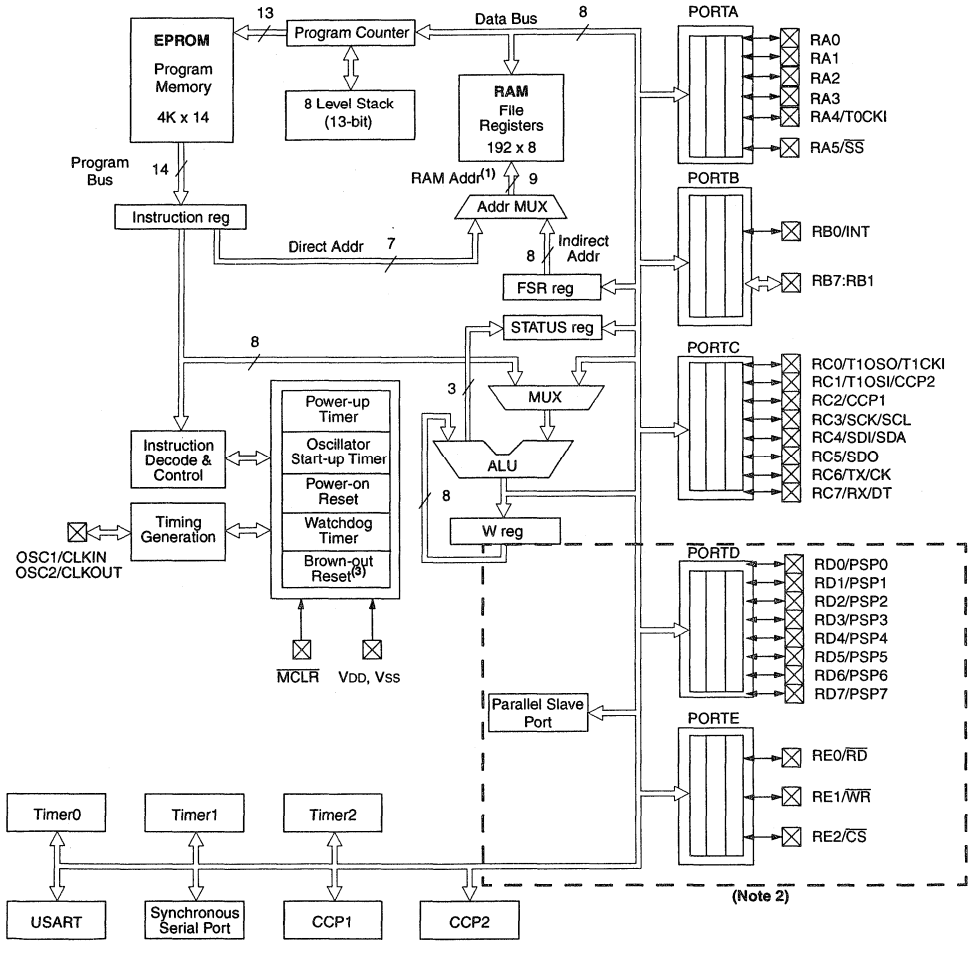
FIGURE 3-2: PIC16C62/62A/R62/64/64A/R64 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.
2: PORTD, PORTE and the Parallel Slave Port are not available on the PIC16C62/62A/R62.
3: Brown-out Reset is not available on the PIC16C62/64.
4: Pin functions T1OSI and T1OSO are swapped on the PIC16C62/64.

9

FIGURE 3-3: PIC16C63/65/65A BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.
2: PORTD, PORTE and the Parallel Slave Port are not available on the PIC16C63.
3: Brown-out Reset is not available on the PIC16C65.

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TABLE 3-1: PIC16C61 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS(1)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	I/P	ST	Master clear reset input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST(2)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST(3)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
2: This buffer is a Schmitt Trigger input when configured as the external interrupt.
3: This buffer is a Schmitt Trigger input when used in serial programming mode.

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TABLE 3-2: PIC16C62/62A/R62/63 PINOUT DESCRIPTION

Pin Name	DIP, SSOP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	9	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	I/P	ST	Master clear reset input/programming voltage input. This pin is an active low reset to the device.
				PORTA is a bi-directional I/O port.
RA0	2	I/O	TTL	
RA1	3	I/O	TTL	
RA2	4	I/O	TTL	
RA3	5	I/O	TTL	
RA4/T0CKI	6	I/O	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/$\overline{SS}$	7	I/O	TTL	Slave select for the synchronous serial port.
				PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	I/O	TTL/ST(4)	RB0/INT can also be selected as an external interrupt pin.
RB1	22	I/O	TTL	
RB2	23	I/O	TTL	
RB3	24	I/O	TTL	
RB4	25	I/O	TTL	Interrupt on change pin.
RB5	26	I/O	TTL	Interrupt on change pin.
RB6	27	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming clock.
RB7	28	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming data.
				PORTC is a bi-directional I/O port.
RC0/T1OSO(1)/T1CKI	11	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output(1)/Timer1 clock input.
RC1/T1OSI(1)/CCP2(2)	12	I/O	ST	RC1/T1OSI can also be selected as a Timer1 oscillator input(1) or Capture2 input/Compare2 output/PWM2 output(2).
RC2/CCP1	13	I/O	ST	RC2/CCP1 can also be selected as a Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	15	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	16	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK(2)	17	I/O	ST	RC6/TX/CK can also be selected as Asynchronous Transmit(2) or USART Synchronous Clock(2).
RC7/RX/DT(2)	18	I/O	ST	RC7/RX/DT can also be selected as the Asynchronous Receive(2) or USART Synchronous Data(2).
VSS	8,19	P	—	Ground reference for logic and I/O pins.
VDD	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C62.
2: The USART and CCP2 are not available on the PIC16C62/62A/R62.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
5: This buffer is a Schmitt Trigger input when used in serial programming mode.

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TABLE 3-3: PIC16C64/64A/R64/65/65A PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	MQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	I/P	ST	Master clear reset input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0	2	3	19	I/O	TTL	
RA1	3	4	20	I/O	TTL	
RA2	4	5	21	I/O	TTL	
RA3	5	6	22	I/O	TTL	
RA4/T0CKI	6	7	23	I/O	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/$\overline{SS}$	7	8	24	I/O	TTL	Slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(4)	RB0/INT can also be selected as an external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST(5)	Interrupt on change pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO(1)/T1CKI	15	16	32	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output(1)/Timer1 clock input.
RC1/T1OSI(1)/CCP2(2)	16	18	35	I/O	ST	RC1/T1OSI/CCP2 can also be selected as a Timer1 oscillator input(1) or Capture2 input/Compare2 output/PWM2 output(2).
RC2/CCP1	17	19	36	I/O	ST	RC2/CCP1 can also be selected as a Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	24	26	43	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK(2)	25	27	44	I/O	ST	RC6/TX/CK can also be selected as Asynchronous Transmit(2) or USART Synchronous Clock(2).
RC7/RX/DT(2)	26	29	1	I/O	ST	RC7/RX/DT can also be selected as the Asynchronous Receive(2) or USART Synchronous Data(2).

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.
2: CCP2 and the USART are not available on the PIC16C64/64A/R64.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
5: This buffer is a Schmitt Trigger input when used in serial programming mode.
6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

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TABLE 3-3: PIC16C64/64A/R64/65/65A PINOUT DESCRIPTION (Cont.'d)

Pin Name	DIP Pin#	PLCC Pin#	MQFP Pin#	Pin Type	Buffer Type	Description
						PORTD can be a bi-directional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(6)	
RD1/PSP1	20	22	39	I/O	ST/TTL(6)	
RD2/PSP2	21	23	40	I/O	ST/TTL(6)	
RD3/PSP3	22	24	41	I/O	ST/TTL(6)	
RD4/PSP4	27	30	2	I/O	ST/TTL(6)	
RD5/PSP5	28	31	3	I/O	ST/TTL(6)	
RD6/PSP6	29	32	4	I/O	ST/TTL(6)	
RD7/PSP7	30	33	5	I/O	ST/TTL(6)	
						PORTE is a bi-directional I/O port.
RE0/$\overline{RD}$	8	9	25	I/O	ST/TTL(6)	RE0/$\overline{RD}$ read control for parallel slave port.
RE1/$\overline{WR}$	9	10	26	I/O	ST/TTL(6)	RE1/$\overline{WR}$ write control for parallel slave port.
RE2/$\overline{CS}$	10	11	27	I/O	ST/TTL(6)	RE2/$\overline{CS}$ select control for parallel slave port.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17, 28,40	12,13, 33,34	—	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: Pin functions T1OSO and T1OSI are reversed on the PIC16C64.
2: CCP2 and the USART are not available on the PIC16C64/64A/R64.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: This buffer is a Schmitt Trigger input when configured as the external interrupt.
5: This buffer is a Schmitt Trigger input when used in serial programming mode.
6: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3, and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clock and instruction execution flow is shown in Figure 3-4.

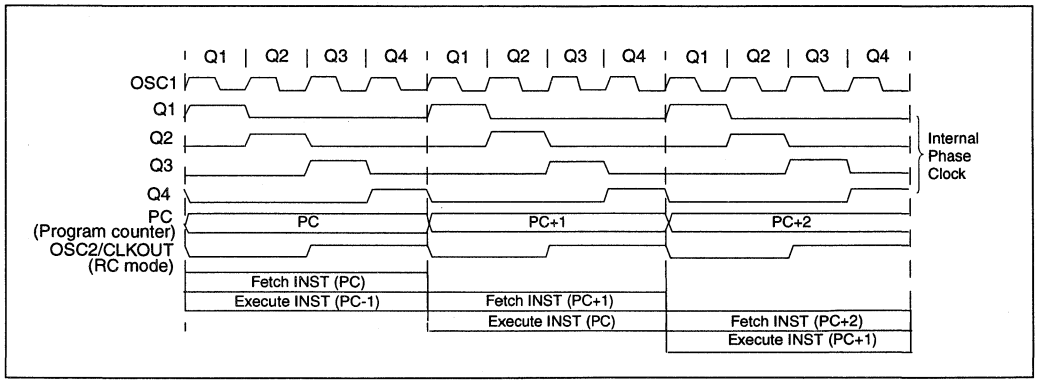
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3, and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-4: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

	Tcy0	Tcy1	Tcy2	Tcy3	Tcy4	Tcy5
1. MOVLW 55h	Fetch 1	Execute 1				
2. MOVWF PORTB		Fetch 2	Execute 2			
3. CALL SUB_1			Fetch 3	Execute 3		
4. BSF PORTA, BIT3 (Forced NOP)				Fetch 4	Flush	
5. Instruction @ address SUB_1					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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NOTES:

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4.0 MEMORY ORGANIZATION

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

4.1 Program Memory Organization

The PIC16C6X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space.

For the PIC16C61, only the first 1K x 14 (0000h-03FFh) is physically implemented. For the PIC16C62/62A/R62/64/64A/R64, only the first 2K x 14 (0000h-07FFh) is physically implemented, and for the PIC16C63/65/65A, only the first 4K x 14 (0000h-0FFFh) is physically implemented. Accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC16C61 PROGRAM MEMORY MAP AND STACK

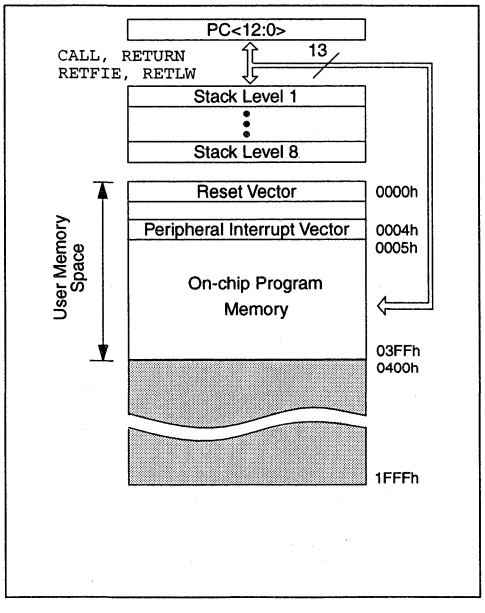


FIGURE 4-2: PIC16C62/62A/R62/64/64A/R64 PROGRAM MEMORY MAP AND STACK

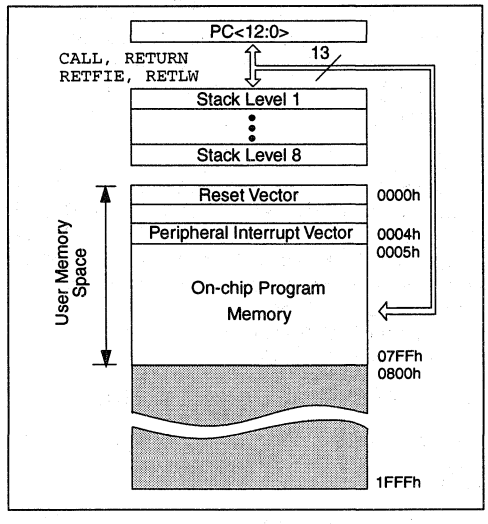
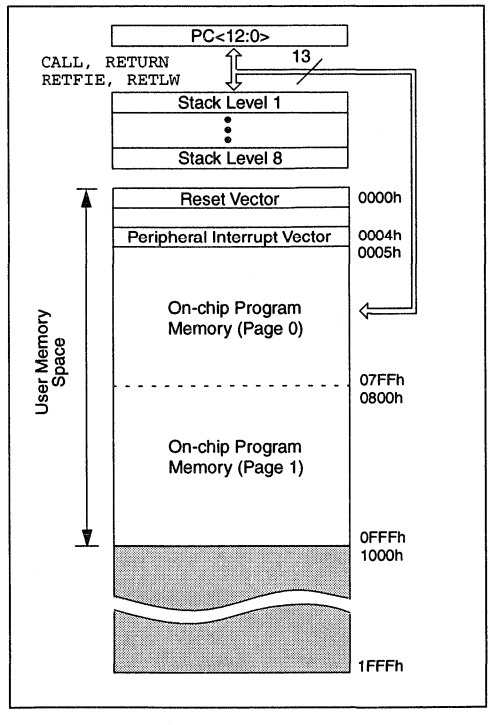


FIGURE 4-3: PIC16C63/65/65A PROGRAM MEMORY MAP AND STACK



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4.2 Data Memory Organization

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The data memory is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bit RP0 is the bank select bit.

RP0 (STATUS<5>) = 1 → Bank 1

RP0 (STATUS<5>) = 0 → Bank 0

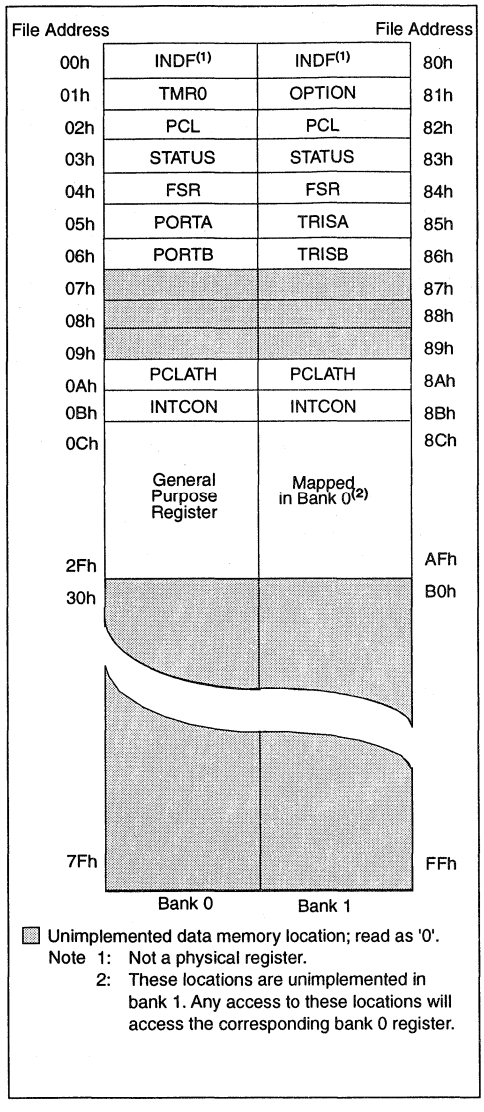
Each Bank extends up to 7Fh (128 bytes). The lower locations of each Bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers implemented as static RAM. Both Bank 0 and Bank 1 contain special function registers. Some "high use" special function registers from Bank 0 are mirrored in Bank 1 for code reduction and quicker access.

4.2.1 GENERAL PURPOSE REGISTERS

These registers are accessed either directly or indirectly through the file select register (FSR) (Section 4.5).

The general purpose register locations 8Ch-AFh of Bank 1 on the PIC16C61 are not physically implemented. These locations are mapped into 0Ch-2Fh of Bank 0.

FIGURE 4-4: PIC16C61 REGISTER FILE MAP



Unimplemented data memory location; read as '0'.

Note 1: Not a physical register.

2: These locations are unimplemented in bank 1. Any access to these locations will access the corresponding bank 0 register.

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FIGURE 4-5: PIC16C62/62A/R62/64/64A/ R64 REGISTER FILE MAP

File Address	Bank 0	Bank 1	File Address
00h	INDF(1)	INDF(1)	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD(2)	TRISD(2)	88h
09h	PORTE(2)	TRISE(2)	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h–1Fh			98h–9Fh
20h–7Fh	General Purpose Register	General Purpose Register	A0h–FFh

Unimplemented data memory location; read as '0'.

Note 1: Not a physical register.
2: PORTD and PORTE are not available on the PIC16C62/62A/R62.

FIGURE 4-6: PIC16C63/65/65A REGISTER FILE MAP

File Address	Bank 0	Bank 1	File Address
00h	INDF(1)	INDF(1)	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD(2)	TRISD(2)	88h
09h	PORTE(2)	TRISE(2)	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	PIR2	PIE2	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H		9Ch
1Dh	CCP2CON		9Dh
1Eh			9Eh
1Fh			9Fh
20h–7Fh	General Purpose Register	General Purpose Register	A0h–FFh

Unimplemented data memory location; read as '0'.

Note 1: Not a physical register
2: PORTD and PORTE are not available on the PIC16C63.

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4.2.2 SPECIAL FUNCTION REGISTERS:

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). The registers associated with the "core" functions are described in this section and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTERS FOR THE PIC16C61

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on all other resets(3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	PORTA Data Latch when written: PORTA pins when read					---x xxxx	---u uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	—	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0-00 000x	0-00 000u
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111
86h	TRISB	PORTB Data Direction Control Register								1111 1111	1111 1111
87h	–	Unimplemented								—	—
88h	–	Unimplemented								—	—
89h	–	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	—	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0-00 000x	0-00 000u

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented locations read as '0'. Shaded locations are unimplemented and read as '0'

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.

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TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--xx xxxx	--uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(6)	(6)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.
2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.
4: The $\overline{BOR}$ bit is reserved on the PIC16C62, always maintain this bit set.
5: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.
6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

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TABLE 4-2: SPECIAL FUNCTION REGISTERS FOR THE PIC16C62/62A/R62 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	(6)	(6)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$(4)	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h-9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.
2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)
3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.
4: The $\overline{BOR}$ bit is reserved on the PIC16C62, always maintain this bit set.
5: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.
6: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C62/62A/R62, always maintain these bits clear.

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TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC16C63

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--xx xxxx	--uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	(5)	(5)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
1Eh-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.

5: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C63, always maintain these bits clear.

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TABLE 4-3: SPECIAL FUNCTION REGISTERS FOR THE PIC16C63 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	(5)	(5)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h(2)	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h(2)	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.

4: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.

5: PIE1<7:6> and PIR1<7:6> are reserved on the PIC16C63, always maintain these bits clear.

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TABLE 4-4: SPECIAL FUNCTION REGISTERS FOR THE PIC16C64/64A/R64

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--xx xxxx	--uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF	(6)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.

4: The $\overline{BOR}$ bit is reserved on the PIC16C64, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.

6: PIE1<6> and PIR1<6> are reserved on the PIC16C64/64A/R64, always maintain these bits clear.

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TABLE 4-4: SPECIAL FUNCTION REGISTERS FOR THE PIC16C64/64A/R64 (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE	(6)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$(4)	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h-9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.

4: The $\overline{BOR}$ bit is reserved on the PIC16C64, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.

6: PIE1<6> and PIR1<6> are reserved on the PIC16C64/64A/R64, always maintain these bits clear.

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TABLE 4-5: SPECIAL FUNCTION REGISTERS FOR THE PIC16C65/65A

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--xx xxxx	--uu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF	(6)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
1Eh-1Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.

4: The $\overline{BOR}$ bit is reserved on the PIC16C65, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.

6: PIE1<6> and PIR1<6> are reserved on the PIC16C65/65A, always maintain these bits clear.

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TABLE 4-5: SPECIAL FUNCTION REGISTERS FOR THE PIC16C65/65A (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets(3)
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE	(6)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$(4)	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented location read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the Program Counter (PC) is not directly accessible. PCLATH is a holding register for the PC whose contents are transferred to the upper byte of the program counter. (PC<12:8>)

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and the Watchdog Timer reset.

4: The $\overline{BOR}$ bit is reserved on the PIC16C65, always maintain this bit set.

5: The IRP and RP1 bits are reserved on the PIC16C6X, always maintain these bits clear.

6: PIE1<6> and PIR1<6> are reserved on the PIC16C65/65A, always maintain these bits clear.

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4.2.2.1 STATUS REGISTER

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A

The STATUS register, shown in Figure 4-7, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

Note 1: Bits IRP and RP1 (STATUS<7:6>) are not used by the PIC16C6X and should be maintained clear. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{borrow}$ and $\overline{digit\ borrow}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 4-7: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset
x = unknown

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)
The IRP bit is not used by the PIC16C6X. The IRP bit is reserved, always maintain this bit clear.

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes.
Only bit RP0 is used by the PIC16C6X. The RP1 bit is reserved, always maintain this bit clear.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF`, `ADDLW`, `SUBLW`, and `SUBWF` instructions) (For $\overline{borrow}$ the polarity is reversed).
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `ADDLW`, `SUBLW`, and `SUBWF` instructions)(For $\overline{borrow}$ the polarity is reversed).
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result
Note: a subtraction is executed by adding the two's complement of the second operand.
For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

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4.2.2.2 OPTION REGISTER

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for TMR0 register, assign the prescaler to the Watchdog Timer by setting the PSA (OPTION<3>) bit.

FIGURE 4-8: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.2.2.3 INTCON REGISTER

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The INTCON Register is a readable and writable register which contains the various enable and flag bits for the TMR0 register overflow, RB port change and external RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-9: INTCON REGISTER FOR PIC16C61 (ADDRESS 0Bh, 8Bh)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	—	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset
x = unknown

bit 7: **GIE:**(1) Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **Unimplemented**: Read as '0'

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4: **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (see Section 5.2 to clear interrupt)
0 = None of the RB7:RB4 pins have changed state

Note 1: If an interrupt occurs while the GIE bit is being cleared, the GIE bit may unintentionally be re-enabled by the `RETFIE` instruction in the user's Interrupt Service Routine. Refer to Section 13.5 for a detailed description.

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FIGURE 4-10: INTCON REGISTER FOR PIC16C62/62A/R62/63/64/64A/R64/65/65A (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R	= Readable bit
W	= Writable bit
U	= Unimplemented bit, read as '0'
- n	= Value at POR reset
x	= unknown

bit 7: **GIE:**(1) Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4: **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (see Section 5.2 to clear the interrupt)
0 = None of the RB7:RB4 pins have changed state

Note 1: For the PIC16C62/64/65, if an interrupt occurs while the GIE bit is being cleared, the GIE bit may unintentionally be re-enabled by the `RETFIE` instruction in the user's Interrupt Service Routine. Refer to Section 13.5 for a detailed description.

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4.2.2.4 PIE1 REGISTER

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

This register contains the individual enable bits for the peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

FIGURE 4-11: PIE1 REGISTER FOR PIC16C62/62A/R62 (ADDRESS 8Ch)

RW-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Reserved**: Always maintain these bits clear.

bit 5-4: **Unimplemented**: Read as '0'

bit 3: **SSPIE**: Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE**: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE**: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: **TMR1IE**: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

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FIGURE 4-12: PIE1 REGISTER FOR PIC16C63 (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Reserved:** Always maintain these bits clear.

bit 5: **RCIE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4: **TXIE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3: **SSPIE:** Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

FIGURE 4-13: PIE1 REGISTER FOR PIC16C64/64A/R64 (ADDRESS 8Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIE:** Parallel Slave Port Read/Write Interrupt Enable bit
1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

bit 6: **Reserved**: Always maintain this bit clear.

bit 5-4: **Unimplemented**: Read as '0'

bit 3: **SSPIE:** Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

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FIGURE 4-14: PIE1 REGISTER FOR PIC16C65/65A (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE	—	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIE:** Parallel Slave Port Read/Write Interrupt Enable bit
1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

bit 6: **Reserved:** Always maintain this bit clear.

bit 5: **RCIE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4: **TXIE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3: **SSPIE:** Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

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4.2.2.5 PIR1 REGISTER

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-15: PIR1 REGISTER FOR PIC16C62/62A/R62 (ADDRESS 0Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Reserved**: Always maintain these bits clear.

bit 5-4: **Unimplemented**: Read as '0'

bit 3: **SSPIF**: Synchronous Serial Port Interrupt Flag bit (must be cleared in software)
1 = The transmission/reception is complete
0 = Waiting to transmit/receive

bit 2: **CCP1IF**: CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflow occurred (must be cleared in software)
0 = No TMR1 register overflow occurred

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FIGURE 4-16: PIR1 REGISTER FOR PIC16C63 (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Reserved:** Always maintain these bits clear.

bit 5: **RCIF:** USART Receive Interrupt Flag bit
1 = The USART receive buffer is full
0 = The USART receive buffer is empty

bit 4: **TXIF:** USART Transmit Interrupt Flag bit
1 = The USART transmit buffer is full
0 = The USART transmit buffer is empty

bit 3: **SSPIF:** Synchronous Serial Port Interrupt Flag bit (must be cleared in software)
1 = The transmission/reception is complete
0 = Waiting to transmit/receive

bit 2: **CCP1IF:** CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflow occurred (must be cleared in software)
0 = No TMR1 register overflow occurred

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FIGURE 4-17: PIR1 REGISTER FOR PIC16C64/64A/R64 (ADDRESS 0Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIF:** Parallel Slave Port Interrupt Flag bit
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write operation has taken place

bit 6: **Reserved:** Always maintain this bit clear.

bit 5-4: **Unimplemented:** Read as '0'

bit 3: **SSPIF:** Synchronous Serial Port Interrupt Flag bit (must be cleared in software)
1 = The transmission/reception is complete
0 = Waiting to transmit/receive

bit 2: **CCP1IF:** CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflow occurred (must be cleared in software)
0 = No TMR1 register occurred

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FIGURE 4-18: PIR1 REGISTER FOR PIC16C65/65A (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF	—	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIF:** Parallel Slave Port Interrupt Flag bit
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write operation has taken place

bit 6: **Reserved:** Always maintain this bit clear.

bit 5: **RCIF:** USART Receive Interrupt Flag bit
1 = The USART receive buffer is full
0 = The USART receive buffer is empty

bit 4: **TXIF:** USART Transmit Interrupt Flag bit
1 = The USART transmit buffer is full
0 = The USART transmit buffer is empty

bit 3: **SSPIF:** Synchronous Serial Port Interrupt Flag bit (must be cleared in software)
1 = The transmission/reception is complete
0 = Waiting to transmit/receive

bit 2: **CCP1IF:** CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflow occurred (must be cleared in software)
0 = No TMR1 register overflow occurred

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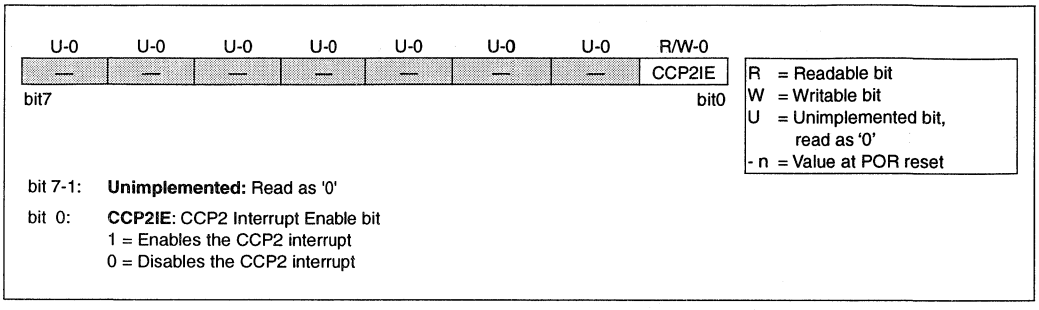
4.2.2.6 PIE2 REGISTER

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

This register contains the CCP2 interrupt enable bit.

FIGURE 4-19: PIE2 REGISTER (ADDRESS 8Dh)



bit 7-1: **Unimplemented:** Read as '0'

bit 0: **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

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4.2.2.7 PIR2 REGISTER

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

This register contains the CCP2 interrupt flag bit.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-20: PIR2 REGISTER (ADDRESS 0Dh)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-1: **Unimplemented:** Read as '0'

bit 0: **CCP2IF**: CCP2 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

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4.2.2.8 PCON REGISTER

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The Power Control register (PCON) contains a flag bit to allow differentiation between a Power-on Reset to an external $\overline{MCLR}$ reset or WDT reset. The PIC16C62A/R62/63/64A/R64/65A contains an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

Note: $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

FIGURE 4-21: PCON REGISTER FOR PIC16C62/64/65 (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-q
—	—	—	—	—	—	$\overline{POR}$	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset
q = value depends on conditions

bit 7-2: **Unimplemented:** Read as '0'

bit 1: $\overline{POR}$: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0: **Reserved**
This bit should be set upon a Power-on Reset by user software and maintained as set. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

FIGURE 4-22: PCON REGISTER FOR PIC16C62A/R62/63/64A/R64/65A (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-q
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset
q = value depends on conditions

bit 7-2: **Unimplemented:** Read as '0'

bit 1: $\overline{POR}$: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0: $\overline{BOR}$: Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

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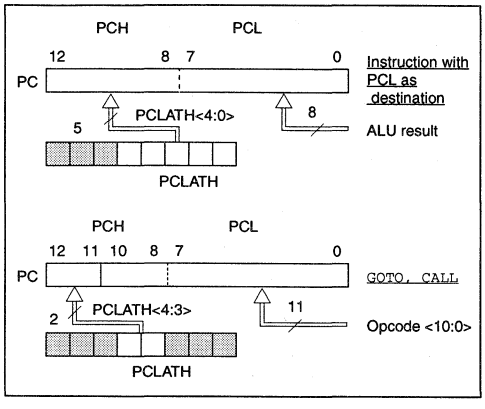
4.3 PCL and PCLATH

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the high byte of the PC is cleared. Figure 4-23 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-23: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16CXX family has an 8 deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or a POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflows or stack underflow conditions.

Note 2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address

4.4 Program Memory Paging

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The PIC16C63/65/65A devices have 4K of program memory, but the CALL and GOTO instructions only have an 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 4K program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (Figure 4-23). When doing a CALL or GOTO instruction, the user must ensure that this page select bit (PCLATH<3>) is programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<3> bit is not required for the return instructions (which POPs the address from the stack).

Note: The PIC16C6X ignores the PCLATH<4> bit, which is used for program memory pages 2 and 3 (1000h - 1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

Devices with 2K or less program memory ignore the PCLATH<3> bit, which is used for program memory page 1 (0800h-0FFFh). The use of PCLATH<3> as a general purpose read/write bit for these devices is not recommended since this may affect upward compatibility with future products.

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Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0x500
BSF     PCLATH,3   ;Select page 1 (800h-FFFh)
CALL    SUB1_P1    ;Call subroutine in
        :          ;page 1 (800h-FFFh)
        :
        :
ORG 0x900
SUB1_P1:           ;called subroutine
        :          ;page 1 (800h-FFFh)
        :
RETURN             ;return to Call subroutine
                   ;in page 0 (000h-7FFh)
```

4.5 Indirect Addressing, INDF and FSR Registers

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

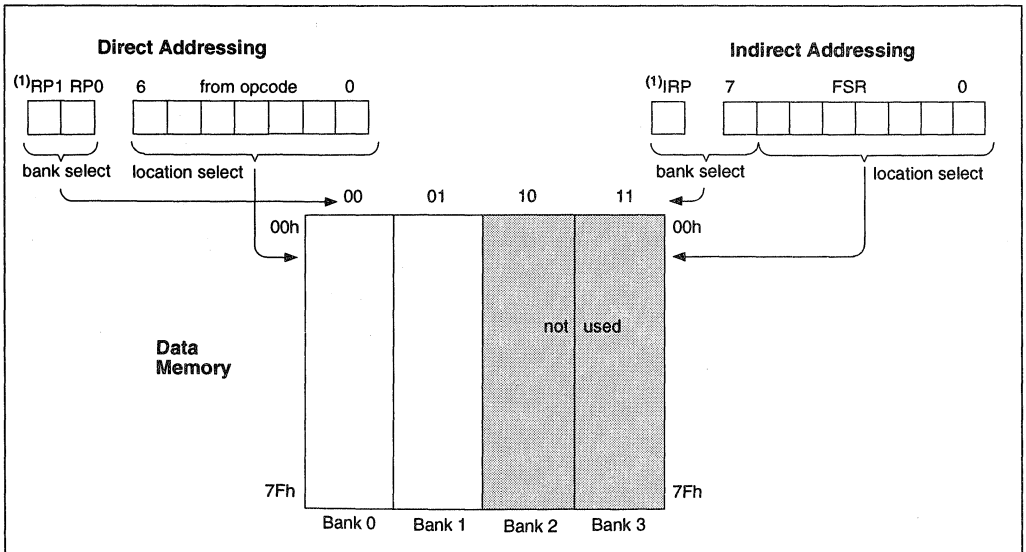
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-24. However, IRP is not used in the PIC16C6X.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

```
        movlw   0x20  ;initialize pointer
        movwf   FSR   ;  to RAM
NEXT    clrf    INDF  ;clear INDF register
        incf    FSR,F ;inc pointer
        btfss   FSR,4 ;all done?
        goto    NEXT  ;NO, clear next
CONTINUE
        :             ;YES, continue
```

FIGURE 4-24: DIRECT/INDIRECT ADDRESSING



For memory map detail see Figure 4-4, Figure 4-5, and Figure 4-6.
Note 1: The IRP and RP1 bits are reserved, always maintain these bits clear.

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5.0 I/O PORTS

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A	

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

5.1 PORTA and TRISA Register

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A	

All devices have a 6-bit wide PORTA, except for the PIC16C61 which has a 5-bit wide PORTA.

Pin RA4/T0CKI is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a bit in the TRISA register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin.

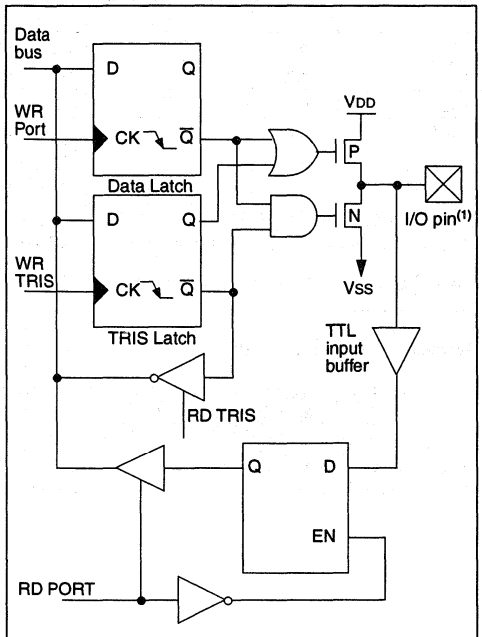
Reading PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefor, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with Timer0 module clock input to become the RA4/T0CKI pin.

EXAMPLE 5-1: INITIALIZING PORTA

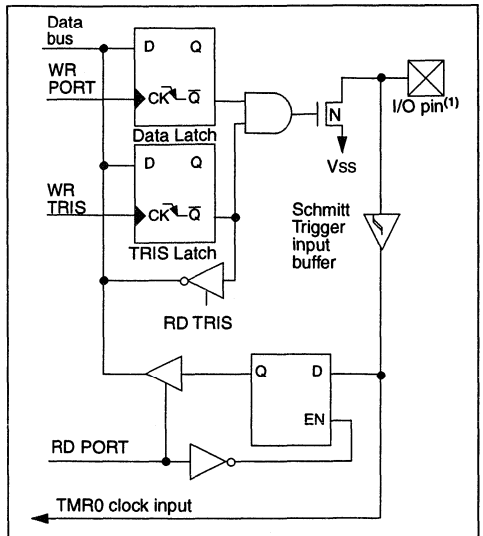
```
CLRF    PORTA       ; Initialize PORTA by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISA       ; Set RA<3:0> as inputs
                    ; RA<5:4> as outputs
                    ; TRISA<7:6> are always
                    ; read as '0'.
```

FIGURE 5-1: BLOCK DIAGRAM OF THE RA3:RA0 PINS AND THE RA5 PIN



Note 1: I/O pins have protection diodes to VDD and VSS.
2: The PIC16C61 does not have an RA5 pin.

FIGURE 5-2: BLOCK DIAGRAM OF THE RA4/T0CKI PIN



Note 1: I/O pin has protection diodes to VSS only.

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TABLE 5-1: PORTA FUNCTIONS

Name	Bit#	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0. Output is open drain type.
RA5/$\overline{SS}$ (1)	bit5	TTL	Input/output or slave select input for synchronous serial port.

Legend: TTL = TTL input, ST = Schmitt Trigger input
Note 1: The PIC16C61 does not have PORTA<5> or TRISA<5>, read as '0'.

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	RA5(1)	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
85h	TRISA	—	—	TRISA5(1)	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.
Note 1: PORTA<5> and TRISA<5> are not implemented on the PIC16C61, read as '0'.

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5.2 PORTB and TRISB Register

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a bit in the TRISB register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISB register puts the contents of the output latch on the selected pin(s).

EXAMPLE 5-2: INITIALIZING PORTB

```
CLRF    PORTB           ; Initialize PORTB by
                        ; clearing output
                        ; data latches
BSF     STATUS, RP0     ; Select Bank 1
MOVLW   0xCF            ; Value used to
                        ; initialize data
                        ; direction
MOVWF   TRISB           ; Set RB<3:0> as inputs
                        ; RB<5:4> as outputs
                        ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBPU}}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are also disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB port change interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.
b) Clear flag bit RBIF.

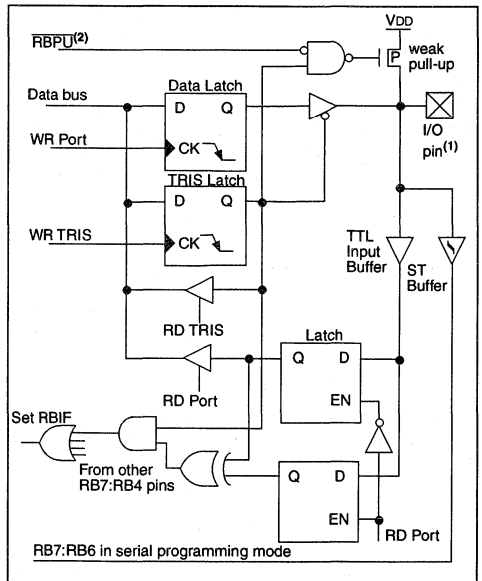
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a keypad and make it possible for wake-up on key-depression. Refer to the Embedded Control Handbook, Application Note, *"Implementing Wake-up on Key Stroke" (AN552).*

Note: For PIC16C61/62/64/65, if a change on the I/O pin should occur when a read operation is being executed (start of the Q2 cycle), then interrupt flag bit RBIF may not get set.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-3: BLOCK DIAGRAM OF THE RB7:RB4 PINS FOR PIC16C61/62/64/65



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

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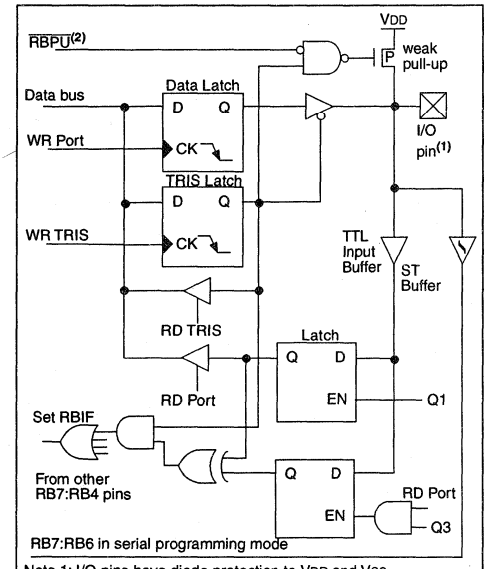
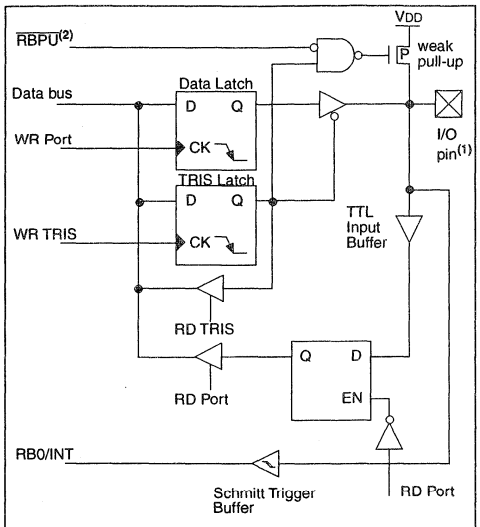
FIGURE 5-4: BLOCK DIAGRAM OF THE RB7:RB4 PINS FOR PIC16C62A/63/64A/65A



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if RBPU = '0' (OPTION<7>).

FIGURE 5-5: BLOCK DIAGRAM OF THE RB3:RB0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if RBPU = '0' (OPTION<7>).

TABLE 5-3: PORTB FUNCTIONS

Name	Bit#	Buffer Type	Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

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5.3 PORTC and TRISC Register

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

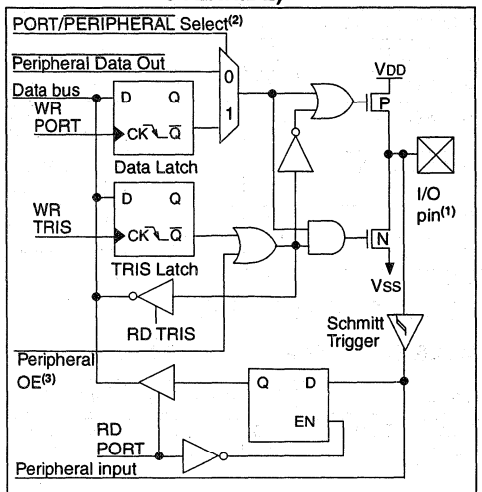
PORTC is an 8-bit bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

EXAMPLE 5-3: INITIALIZING PORTC

```
CLRF    PORTC       ; Initialize PORTC by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISC       ; Set RC<3:0> as inputs
                    ; RC<5:4> as outputs
                    ; RC<7:6> as inputs
```

FIGURE 5-6: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

TABLE 5-5: PORTC FUNCTIONS FOR PIC16C62/64

Name	Bit#	Buffer Type	Function
RC0/T1OSI/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator input or Timer1 clock input
RC1/T1OSO	bit1	ST	Input/output port pin or Timer1 oscillator output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger input

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TABLE 5-6: PORTC FUNCTIONS FOR PIC16C62A/R62/64A/R64

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output or Timer1 clock input
RC1/T1OSI	bit1	ST	Input/output port pin or Timer1 oscillator input
RC2/CCP1	bit2	ST	Input/output port pin or Capture input/Compare output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger input

TABLE 5-7: PORTC FUNCTIONS FOR PIC16C63/65/65A

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output or Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or synchronous serial port data output
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit, or USART Synchronous Clock
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive, or USART Synchronous Data

Legend: ST = Schmitt Trigger input

TABLE 5-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged.

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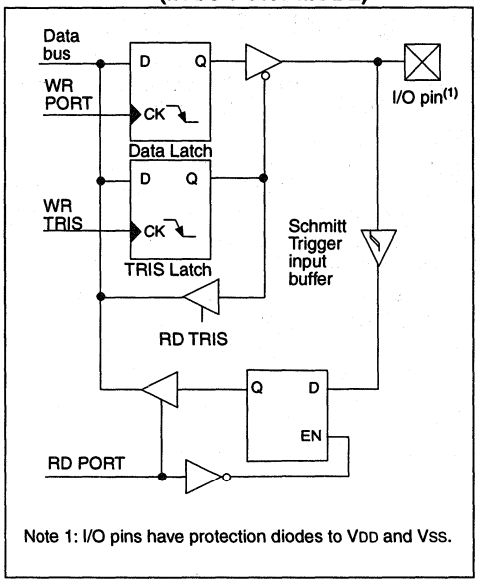
5.4 PORTD and TRISD Register

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 5-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 5-9: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL(1)	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL(1)	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL(1)	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL(1)	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL(1)	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL(1)	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL(1)	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input, TTL = TTL input
Note 1: Buffer is a Schmitt Trigger when in I/O mode, and a TTL buffer when in Parallel Slave Port mode.

TABLE 5-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

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5.5 PORTE and TRISE Register

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

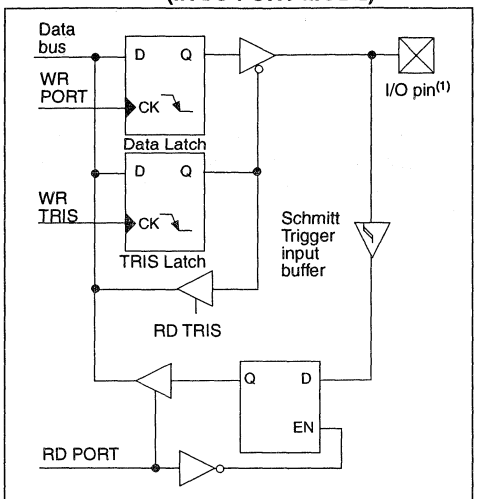
PORTE has three pins, RE2/$\overline{CS}$, RE1/$\overline{WR}$, and RE0/$\overline{RD}$ which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). In this mode the input buffers are TTL.

Figure 5-9 shows the TRISE register, which also controls the parallel slave port operation.

TRISE controls the direction of the RE pins.

FIGURE 5-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-9: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7 : **IBF:** Input Buffer Full Status bit
1 = A word has been received and is waiting to be read by the CPU
0 = No word has been received

bit 6: **OBF:** Output Buffer Full Status bit
1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5: **IBOV:** Input Buffer Overflow Detect bit (in microprocessor mode)
1 = A write occurred when a previously input word has not been read (must be cleared in software)
0 = No overflow occurred

bit 4: **PSPMODE:** Parallel Slave Port Mode Select bit
1 = Parallel slave port mode
0 = General purpose I/O mode

bit 3: **Unimplemented:** Read as '0'

bit 2: **TRISE2:** Direction Control bit for pin RE2/$\overline{CS}$
1 = Input
0 = Output

bit 1: **TRISE1:** Direction Control bit for pin RE1/$\overline{WR}$
1 = Input
0 = Output

bit 0: **TRISE0:** Direction Control bit for pin RE0/$\overline{RD}$
1 = Input
0 = Output

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TABLE 5-11: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/$\overline{RD}$	bit0	ST/TTL(1)	Input/output port pin or Read control input in parallel slave port mode. $\overline{RD}$ 1 = Not a read operation 0 = Read operation. The system reads the PORTD register (if chip selected)
RE1/$\overline{WR}$	bit1	ST/TTL(1)	Input/output port pin or Write control input in parallel slave port mode. $\overline{WR}$ 1 = Not a write operation 0 = Write operation. The system writes to the PORTD register (if chip selected)
RE2/$\overline{CS}$	bit2	ST/TTL(1)	Input/output port pin or Chip select control input in parallel slave port mode. $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input, TTL = TTL input
Note 1: Buffer is a Schmitt Trigger when in I/O mode, and a TTL buffer when in Parallel Slave Port (PSP) mode.

TABLE 5-12: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells not used by PORTE.

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5.6 I/O Programming Considerations

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

5.6.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-4 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 5-4: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

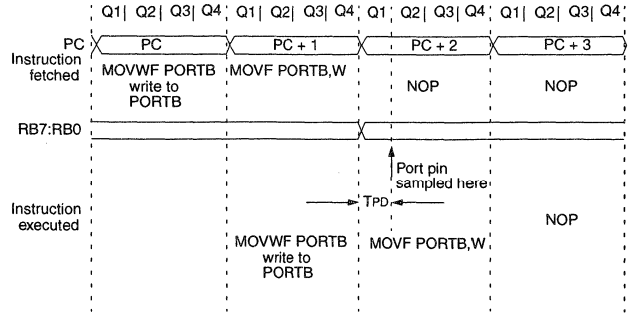
```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                       PORT latch  PORT pins
;                       ----------  ---------
  BCF PORTB, 7      ; 01pp pppp   11pp pppp
  BCF PORTB, 6      ; 10pp pppp   11pp pppp
  BSF STATUS, RP0   ;
  BCF TRISB, 7      ; 10pp pppp   11pp pppp
  BCF TRISB, 6      ; 10pp pppp   10pp pppp
;
;Note that the user may have expected the
;pin values to be 00pp pppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-10). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-10: SUCCESSIVE I/O OPERATION



Note:

This example shows a write to PORTB followed by a read from PORTB.

Note that:

data setup time = (0.25TCY - TPD)

where TCY = instruction cycle
TPD = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

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5.7 Parallel Slave Port

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

PORTD operates as an 8-bit wide parallel slave port, or microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through $\overline{RD}$ control input (RE0/$\overline{RD}$) and $\overline{WR}$ control input pin (RE1/$\overline{WR}$).

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting PSPMODE enables port pin RE0/$\overline{RD}$ to be the $\overline{RD}$ input, RE1/$\overline{WR}$ to be the $\overline{WR}$ input and RE2/$\overline{CS}$ to be the $\overline{CS}$ (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set).

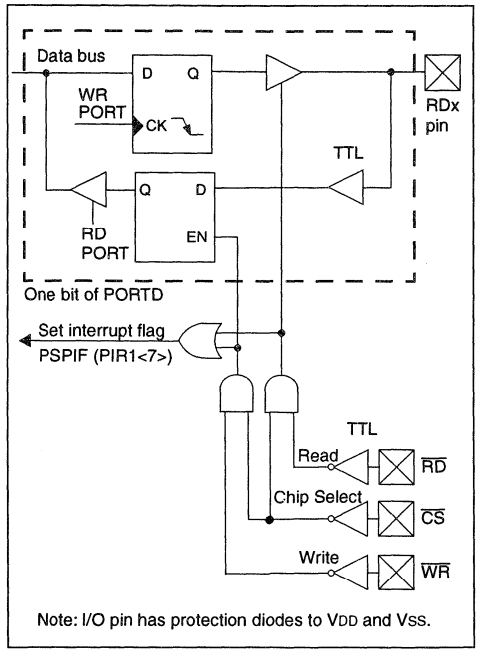
There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored since the microprocessor is controlling the direction of data flow.

Input Buffer Full Status Flag bit IBF (TRISE<7>) is set if a received word is waiting to be read by the CPU. Once the PORTD input latch is read, bit IBF is cleared. IBF is a read only status bit. Output Buffer Full Status Flag bit OBF (TRISE<6>) is set if a word written to PORTD latch is waiting to be read by the external bus. Once the PORTD output latch is read by the microprocessor, bit OBF is cleared. Input Buffer Overflow Status flag bit IBOV (TRISE<5>) is set if a second write to the microprocessor port is attempted when the previous word has not been read by the CPU (the first word is retained in the buffer).

When not in Parallel Slave Port mode, bits IBF (TRISE<7>) and OBF (TRISE<6>) are held clear. However if flag bit IBOV (TRISE<5>) was previously set, it must be cleared in software.

An interrupt is generated and latched into flag bit PSPIF (PIR1<7>) when a read or a write operation is completed. Flag bit PSPIF must be cleared by user software and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

FIGURE 5-11: PORTD AND PORTE AS A PARALLEL SLAVE PORT



Note: I/O pin has protection diodes to VDD and VSS.

TABLE 5-13: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	PSP7	PSP6	PSP5	PSP4	PSP3	PSP2	PSP1	PSP0	xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
0Ch	PIR1	PSPIF	(1)	RCIF(2)	TXIF(2)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE	(1)	RCIE(2)	TXIE(2)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by the PSP.
Note 1: These bits are reserved, always maintain these bits clear.
2: These bits are implemented on the PIC16C63/65/65A only.

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6.0 OVERVIEW OF TIMER MODULES

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

All PIC16C6X devices have three timer modules except for the PIC16C61, which has one timer module. Each module can generate an interrupt to indicate that an event has occurred (i.e., timer overflow). Each of these modules are detailed in the following sections. The timer modules are:

- Timer0 module (Section 7.0)
- Timer1 module (Section 8.0)
- Timer2 module (Section 9.0)

6.1 Timer0 Overview

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The Timer0 module (previously known as RTCC) is a simple 8-bit overflow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. TMR0 can increment at the following rates: 1:1 when the prescaler is assigned to Watchdog Timer, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

6.2 Timer1 Overview

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock (Fosc/4), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

TImer1 also has a prescaler option which allows TMR1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. TMR1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit capture or 16-bit compare and must be synchronized to the device.

6.3 Timer2 Overview

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

Timer2 is an 8-bit timer with a programmable prescaler and a programmable postscaler, as well as an 8-bit Period Register (PR2). Timer2 can be used with the CCP module (in PWM mode) as well as the Baud Rate Generator for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, and 1:16.

The postscaler allows TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP Overview

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The CCP module(s) can operate in one of three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or sixteenth rising edge of the CCPx pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs, an interrupt can be generated and the output pin CCPx can be forced to a given state (High or Low) and Timer1 can be reset. This depends on control bits CCPxM3:CCPxM0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register value as well as to an 8-bit Period Register (PR2). When TMR2 register = PR2 register, the TMR2 register is cleared to 00h, an interrupt may be generated, and the CCPx pin (if an output) will be forced high. When the TMR2 register = Duty Cycle register, the CCPx pin will be forced low.

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7.0 TIMER0 MODULE

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Read and write capability
  - Interrupt on overflow from FFh to 00h
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit T0CS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

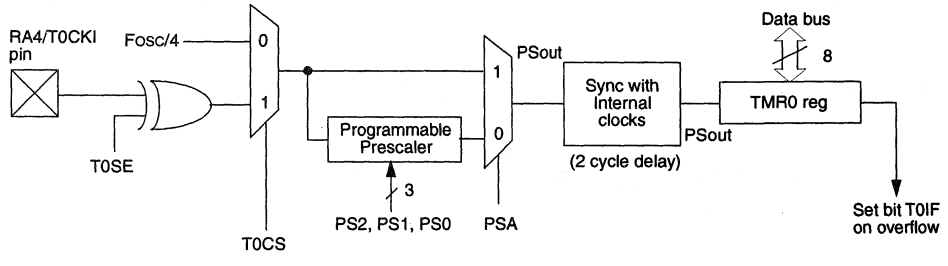
The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 Timer0 Interrupt

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The TMR0 interrupt is generated when the register (TMR0) overflows from FFh to 00h. This overflow sets interrupt flag bit T0IF (INTCON<2>). The interrupt can be masked by clearing enable bit T0IE (INTCON<5>). Flag bit T0IF must be cleared in software by the TImer0 interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. Figure 7-4 displays the Timer0 interrupt timing.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits, T0CS, T0SE, PSA, and PS2, PS1, PS0 are (OPTION<5:0).
2: The prescaler is shared with Watchdog Timer (refer to Figure 7-6 for detailed diagram).

FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER

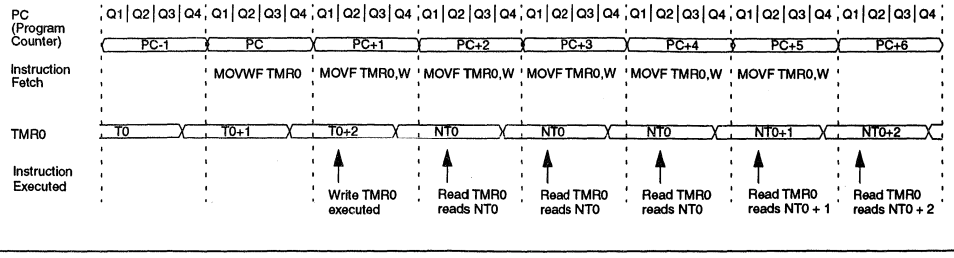


FIGURE 7-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

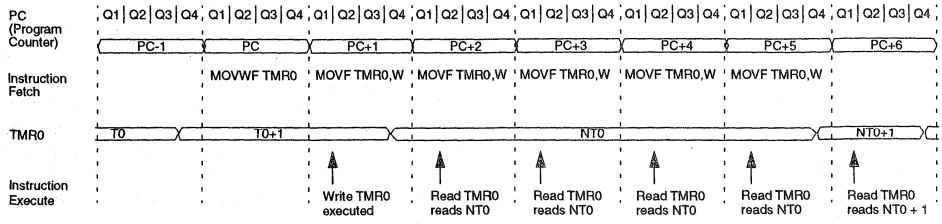
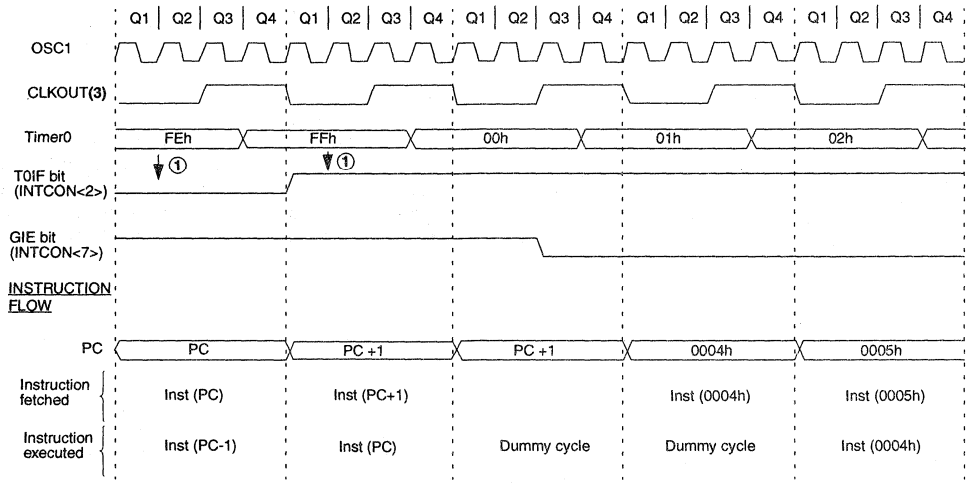


FIGURE 7-4: TIMER0 INTERRUPT TIMING



Note 1: Interrupt flag bit T0IF is sampled here (every Q1).
2: Interrupt latency = 4Tcy where Tcy = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.

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7.2 Using Timer0 with External Clock

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

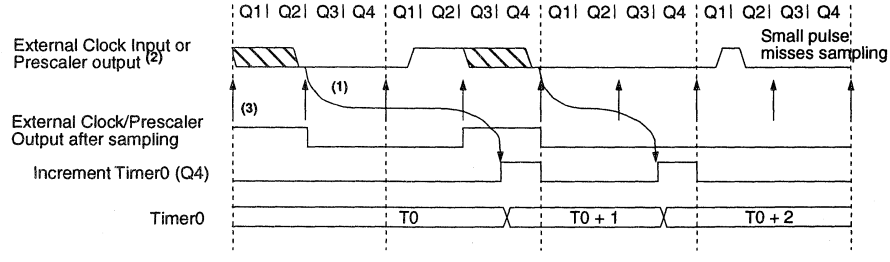
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

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7.3 Prescaler

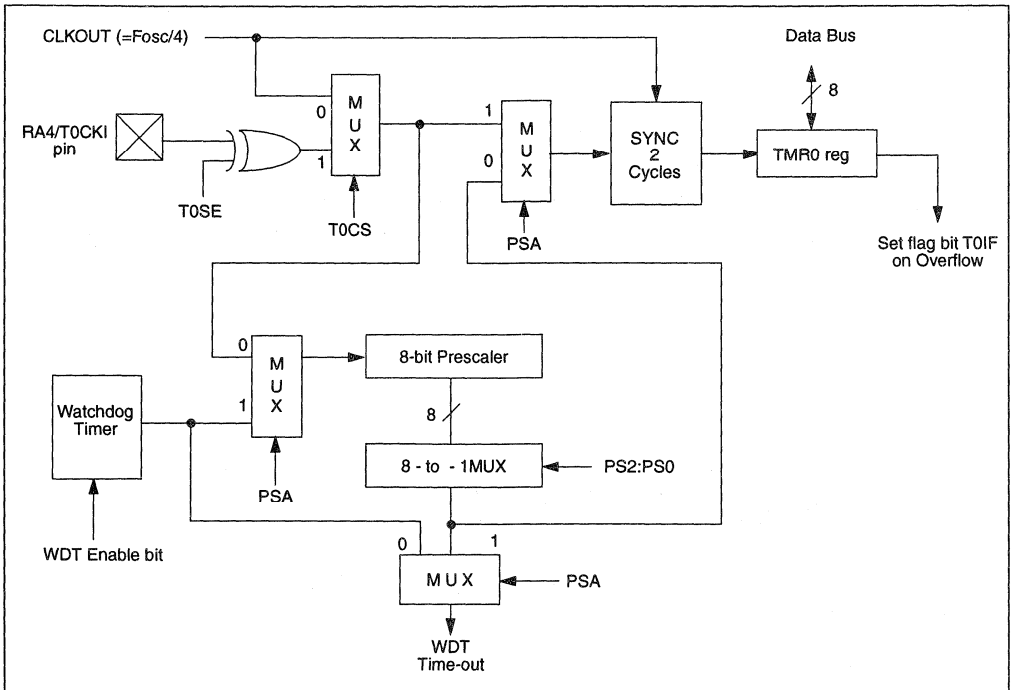
Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. `CLRF 1`, `MOVWF 1`, `BSF 1,x`) will clear the prescaler count. When assigned to Watchdog Timer, a `CLRWDT` instruction will clear the prescaler count along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 7-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are (OPTION<5:0>).

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7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution.

Note: To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This precaution must be followed even if the WDT is disabled.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS, RP0   ;Bank 0
CLRF    TMR0          ;Clear TMR0 & Prescaler
BSF     STATUS, RP0   ;Bank 1
CLRWDT                ;Clears WDT
MOVLW   b'xxxx1xxx'   ;Select new prescale
MOVWF   OPTION_REG    ;value & WDT
BCF     STATUS, RP0   ;Bank 0
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7-2.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                ;Clear WDT and
                      ;prescaler
BSF     STATUS, RP0   ;Bank 1
MOVLW   b'xxxx0xxx'   ;Select TMR0, new
                      ;prescale value and
MOVWF   OPTION_REG    ;clock source
BCF     STATUS, RP0   ;Bank 0
```

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE(1)	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	TRISA5(1)	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.
Note 1: TRISA<5> and bit PEIE are not implemented on the PIC16C61, read as '0'.

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NOTES:

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8.0 TIMER1 MODULE

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

Timer1 is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. Register TMR1 (TMR1H + TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing the TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by clock select bit, TMR1CS (T1CON<1>) (Figure 8-2).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

Timer1 can be turned on or off using the control bit TMR1ON (T1CON<0>).

Timer1 also has an internal "reset input". This reset can be generated by CCP1 or CCP2 (Capture/Compare/PWM) module. See Section 10.0 for details. Figure 8-1 shows the Timer1 control register.

For the PIC16C62A/R62/63/64A/R64/65A, when the Timer1 oscillator is enabled (T1OSCEN is set), the RC1 and RC0 pins become inputs. That is, the TRISC<1:0> value is ignored.

For the PIC16C62/64/65, when the Timer1 oscillator is enabled (T1OSCEN is set), RC1 pin becomes an input, however the RC0 pin will have to be configured as an input by setting the TRISC<0> bit.

The Timer1 module also has a software programmable prescaler.

FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented**: Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off
Note: The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2: **$\overline{\text{T1SYNC}}$**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input

TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit
1 = External clock from T1OSI (on the rising edge) (See pinouts for pin with T1OSI function)
0 = Internal clock (Fosc/4)

bit 0: **TMR1ON**: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

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8.1 Timer1 Operation in Timer Mode

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A

Timer mode is selected by clearing bit TMR1CS (T1CON<1>). In this mode, the input clock to the timer is Fosc/4. The synchronize control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 Timer1 Operation in Synchronized Counter Mode

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A

Counter mode is selected by setting bit TMR1CS. In this mode the timer increments on every rising edge of clock input on T1OSI when enable bit T1OSCEN is set or pin with T1CKI when bit T1OSCEN is cleared.

Note: The T1OSI function is multiplexed to different pins, depending on the device. See the pinout descriptions to see which pin has the T1OSI function.

If $\overline{\text{T1SYNC}}$ is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if an external clock is present, since the synchronization circuit is shut off. The prescaler, however, will continue to increment.

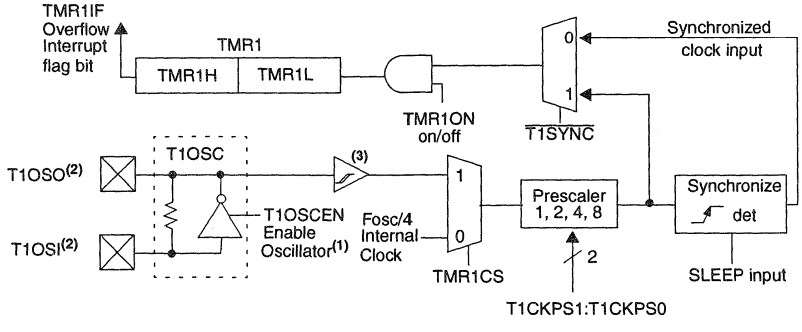
8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

When an external clock input is used for Timer1 in synchronized counter mode, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of TMR1 after synchronization.

When the prescaler is 1:1, the external clock input is the same as the prescaler output. The synchronization of T1CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T1CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to appropriate electrical specification section, parameters 45, 46, and 47.

When a prescaler other than 1:1 is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. In order for the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T1CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T1CKI high and low time is that they do not violate the minimum pulse width requirements of 10 ns). Refer to applicable electrical specification section, parameters 40, 42, 45, 46, and 47.

FIGURE 8-2: TIMER1 BLOCK DIAGRAM



Note 1: When enable bit T1OSCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.
2: See pinouts for pins with T1OSO and T1OSI functions.
3: For the PIC16C62/64/65, the Schmitt Trigger is not implemented in external clock mode.

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8.3 Timer1 Operation in Asynchronous Counter Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and generate an interrupt on overflow which will wake the processor. However, special precautions in software are needed to read-from or write-to the Timer1 register pair, TMR1L and TMR1H (Section 8.3.2).

In asynchronous counter mode, Timer1 cannot be used as a time-base for capture or compare operations.

8.3.1 EXTERNAL CLOCK INPUT TIMING WITH UNSYNCHRONIZED CLOCK

If control bit $\overline{\text{T1SYNC}}$ is set, the timer will increment completely asynchronously. The input clock must meet certain minimum high time and low time requirements, as specified in timing parameters (45 - 47).

8.3.2 READING AND WRITING TMR1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

```
;  All Interrupts are disabled
    MOVF    TMR1H, W        ;Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L, W        ;Read low byte
    MOVWF   TMPL            ;
    MOVF    TMR1H, W        ;Read high byte
    SUBWF   TMPH, W         ;Sub 1st read
                            ;with 2nd read
    BTFSC   STATUS,Z        ;is result = 0
    GOTO    CONTINUE        ;Good 16-bit read
; TMR1L may have rolled over between the read
; of the high and low bytes. Reading the high
; and low bytes now will read a good value.
    MOVF    TMR1H, W        ;Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L, W        ;Read low byte
    MOVWF   TMPL            ;
;   Re-enable Interrupt (if required)
CONTINUE                    ;Continue with
    :                       ;your code
```

8.4 Timer1 Oscillator

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

A crystal oscillator circuit is built in-between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must allow a software time delay to ensure proper oscillator start-up.

TABLE 8-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz(1)	15 pF	15 pF
	100 kHz	15 pF	15 pF
	200 kHz	0 - 15 pF	0 - 15 pF
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.			
Crystals Tested:			
32.768 kHz	Epson C-001R32.768K-A		± 20 PPM
100 kHz	Epson C-2 100.00 KC-P		± 20 PPM
200 kHz	STD XTL 200.000 kHz		± 20 PPM

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8.5 Resetting Timer1 using a CCP Trigger Output

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

CCP2 is implemented on the PIC16C63/65/65A only.

If CCP1 or CCP2 module is configured in Compare mode to generate a "special event trigger" (CCPxM3:CCPxM0 = 1011), this signal will reset Timer1.

Note: The "special event trigger" from the CCP1and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If the Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL registers pair effectively becomes the period register for the Timer1 module.

8.6 Resetting of TMR1 Register Pair (TMR1H + TMR1L)

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The TMR1H and TMR1L registers are not reset on a POR or any other reset except by the CCP1 or CCP2 special event trigger.

T1CON register is reset to 00h on Power-on Reset or a Brown-out Reset. In all other resets, the register is unaffected.

8.7 Timer1 Prescaler

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers

TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: The USART is implemented on the PIC16C63/65/65A only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63, always maintain these bits clear.

3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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9.0 TIMER2 MODULE

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

Timer2 is an 8-bit timer with a prescaler and a postscaler. It is especially suitable as PWM time-base for PWM mode of CCP module(s). TMR2 is a readable and writable register, and is cleared on any device reset.

The input clock (FOSC/4) has a prescale option of 1:1, 1:4 or 1:16 (selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is set during a reset.

The match output of the TMR2 register goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling, inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF (PIR1<1>)).

The Timer2 module can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 9-2 shows the Timer2 control register.

9.1 Timer2 Prescaler and Postscaler

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device reset (POR, BOR, $\overline{MCLR}$ Reset, or WDT Reset).

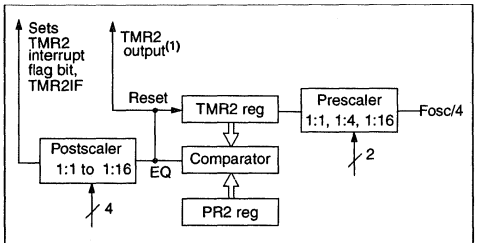
TMR2 register will not clear when T2CON is written, only for a WDT, BOR, POR, and $\overline{MCLR}$ reset.

9.2 Output of TMR2

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

FIGURE 9-1: TIMER2 BLOCK DIAGRAM



Note 1: TMR2 register output can be software selected by the SSP Module as a baud clock.

FIGURE 9-2: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented**: Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits
0000 = 1:1 postscale
0001 = 1:2 postscale
•
•
1111 = 1:16 postscale

bit 2: **TMR2ON**: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0: **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits
00 = 1:1 prescale
01 = 1:4 prescale
1x = 1:16 prescale

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TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer2.

Note 1: The USART is implemented on the PIC16C63/65/65A only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63, always maintain these bits clear.

3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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10.0 CAPTURE/COMPARE/PWM (CCP) MODULE(s)

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A	CCP1
61	62	62A	R62	63	64	64A	R64	65	65A	CCP2

Each CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register, or as a PWM master/slave duty cycle register. Both the CCP1 and CCP2 modules are identical in operation, with the exception of the operation of the special event trigger. Table 10-1 and Table 10-2 show the resources and interactions of the CCP modules(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

CCP2 module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

For use of the CCP modules, refer to the *Embedded Control Handbook*, "Using the CCP Modules" (AN594).

TABLE 10-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

TABLE 10-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base.
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1.
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1.
PWM	PWM	The PWMs will have the same frequency, and update rate (TMR2 interrupt).
PWM	Capture	None
PWM	Compare	None

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FIGURE 10-1: CCP1CON REGISTER (ADDRESS 17h) / CCP2CON REGISTER (ADDRESS 1Dh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX:CCPxY**: PWM Least Significant bits
Capture Mode
Unused
Compare Mode
Unused
PWM Mode
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits
0000 = Capture/Compare/PWM off (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (bit CCPxIF is set)
1001 = Compare mode, clear output on match (bit CCPxIF is set)
1010 = Compare mode, generate software interrupt on match (bit CCPxIF is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set; CCP1 resets TMR1; CCP2 resets TMR1)
11xx = PWM mode

10.1 Capture Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1 (Figure 10-2). An event is defined as:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

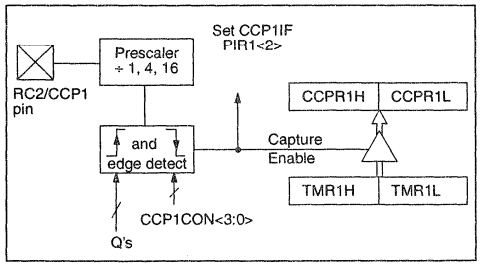
An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

10.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting its corresponding TRIS bit.

Note: If the RC2/CCP1 pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 10-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

10.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep enable bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear flag bit CCP1IF following any such change in operating mode.

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10.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON     ; Turn CCP module off
MOVLW   NEW_CAPT_PS ; Load the W reg with
                    ; the new prescaler
                    ; mode value and CCP ON
MOVWF   CCP1CON     ; Load CCP1CON with
                    ; this value
```

10.2 Compare Mode

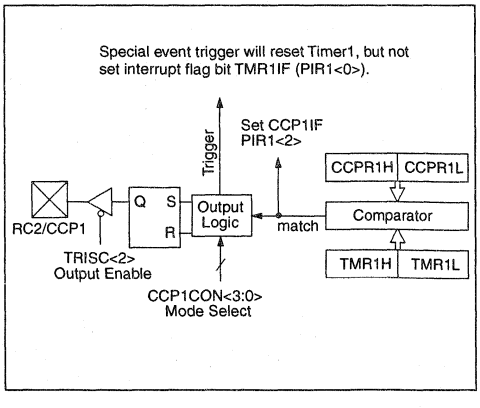
Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven High
- Driven Low
- Remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, a compare interrupt is also generated.

FIGURE 10-3: COMPARE MODE OPERATION BLOCK DIAGRAM



10.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

10.2.1 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

10.2.2 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

10.2.3 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 and CCP2 resets the TMR1 register pair. This allows the CCPR1 and CCPR2 registers to effectively be a 16-bit programmable period register for Timer1.

For compatibility issues, the special event trigger output of CCP2 on PIC16C7X devices also starts an A/D conversion.

Note: The "special event trigger" from the CCP1and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

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10.3 PWM Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

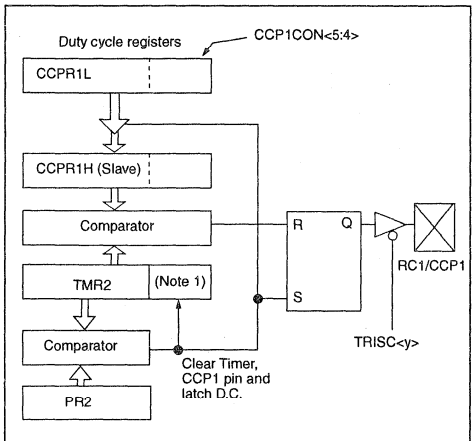
In Pulse Width Modulation (PWM) mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCPx pin is multiplexed with the PORTC data latch, the corresponding TRISC bit must be cleared to make the CCPx pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 10-4 shows a simplified block diagram of the CCP module in PWM mode.

For a step by step procedure on how to set up the CCP module for PWM operation, see Section 10.3.3.

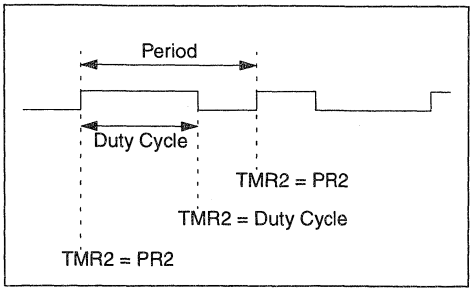
FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base.

A PWM output (Figure 10-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 10-5: PWM OUTPUT



10.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see Section 9.1) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

10.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle:

$$\text{PWM duty cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period (PWM duty cycle = 100%), the CCP1 pin will not be forced to the low level.

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EXAMPLE 10-2: PWM PERIOD AND DUTY CYCLE CALCULATION

Desired PWM frequency is 78.125 kHz,
Fosc = 20 MHz
TMR2 prescale = 1

$$1/78.125\ \text{kHz} = [(\text{PR2}) + 1] \cdot 4 \cdot 1/20\ \text{MHz} \cdot 1$$

$$12.8\ \mu\text{s} = [(\text{PR2}) + 1] \cdot 4 \cdot 50\ \text{ns} \cdot 1$$

$$\text{PR2} = 63$$

Find the maximum resolution of the duty cycle that can be used with a 78.125 kHz frequency and 20 MHz oscillator:

$$1/78.125\ \text{kHz} = 2^{\text{PWM RESOLUTION}} \cdot 1/20\ \text{MHz} \cdot 1$$

$$12.8\ \mu\text{s} = 2^{\text{PWM RESOLUTION}} \cdot 50\ \text{ns} \cdot 1$$

$$256 = 2^{\text{PWM RESOLUTION}}$$

$$\log(256) = (\text{PWM Resolution}) \cdot \log(2)$$

$$8.0 = \text{PWM Resolution}$$

At most, an 8-bit resolution duty cycle can be obtained from a 78.125 kHz frequency and a 20 MHz oscillator, i.e., 0 ≤ CCPR1L:CCP1CON<5:4> ≤ 255. Any value greater than 255 will result in a 100% duty cycle.

In order to achieve higher resolution, the PWM frequency must be decreased. In order to achieve higher PWM frequency, the resolution must be decreased.

Table 10-3 lists example PWM frequencies and resolutions for Fosc = 20 MHz. TMR2 prescaler and PR2 values are also shown.

10.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the appropriate TRISC bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP module for PWM operation.

TABLE 10-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 10-4: REGISTERS ASSOCIATED WITH TIMER1, CAPTURE AND COMPARE

Add	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh(4)	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh(4)	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh(4)	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch(4)	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh(4)	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in these modes.

Note 1: These bits are associated with the USART module, which is implemented on the PIC16C63/65/65A only.
2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63, always maintain these bits clear.
3: These bits are reserved, always maintain these bits clear.
4: These registers are associated with the CCP2 module, which is implemented on the PIC16C63/65/65A only.

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TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh(4)	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh(4)	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's Period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh(4)	CCPR2L	Capture/Compare/PWM2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch(4)	CCPR2H	Capture/Compare/PWM2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh(4)	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.

Note 1: These bits are associated with the USART module, which is implemented on the PIC16C63/65/65A only.

2: Bits PSPIE and PSPIF are reserved on the PIC16C62/62A/R62/63, always maintain these bits clear.

3: These bits are reserved, always maintain these bits clear.

4: These registers are associated with the CCP2 module, which is implemented on the PIC16C63/65/65A only.

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11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

Refer to Application Note AN578, *"Use of the SSP Module in the I^2C Multi-Master Environment."*

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5: **D/$\overline{A}$**: Data/Address bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)
0 = Stop bit was not detected last

bit 3: **S**: Start bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)
0 = Start bit was not detected last

bit 2: **R/$\overline{W}$**: Read/Write bit information (I^2C mode only)
This bit holds the R/W bit information following the last address match. This bit is valid from the address match to the next start bit, stop bit, or $\overline{ACK}$ bit.
1 = Read
0 = Write

bit 1: **UA**: Update Address (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit

Receive (SPI and I^2C modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit (I^2C mode only)
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

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FIGURE 11-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **WCOL**: Write Collision Detect bit
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6: **SSPOV**: Receive Overflow Detect bit

In SPI mode
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR register is lost. Overflow can only occur in slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In master mode the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
0 = No overflow

In I^2C mode
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in transmit mode. SSPOV must be cleared in software in either mode.
0 = No overflow

bit 5: **SSPEN**: Synchronous Serial Port Enable bit

In SPI mode
1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins
0 = Disables serial port and configures these pins as I/O port pins

In I^2C mode
1 = Enables the serial port and configures the SDA and SCL pins as serial port pins
0 = Disables serial port and configures these pins as I/O port pins
In both modes, when enabled, these pins must be properly configured as input or output.

bit 4: **CKP**: Clock Polarity Select bit

In SPI mode
1 = Transmit happens on falling edge, receive on rising edge. Idle state for clock is a high level.
0 = Transmit happens on rising edge, receive on falling edge. Idle state for clock is a low level.

In I^2C mode
SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch) (Used to ensure data setup time)

bit 3-0: **SSPM3:SSPM0**: Synchronous Serial Port Mode Select bits
0000 = SPI master mode, clock = Fosc/4
0001 = SPI master mode, clock = Fosc/16
0010 = SPI master mode, clock = Fosc/64
0011 = SPI master mode, clock = TMR2 output/2
0100 = SPI slave mode, clock = SCK pin. $\overline{SS}$ pin control enabled.
0101 = SPI slave mode, clock = SCK pin. $\overline{SS}$ pin control disabled. $\overline{SS}$ can be used as I/O pin.
0110 = I^2C slave mode, 7-bit address
0111 = I^2C slave mode, 10-bit address
1011 = I^2C start and stop bit interrupts enabled (slave idle)
1110 = I^2C slave mode, 7-bit address with start and stop bit interrupts enabled
1111 = I^2C slave mode, 10-bit address with start and stop bit interrupts enabled

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11.1 SPI Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select ($\overline{SS}$)

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>). These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Output/Input data on the Rising/Falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select Mode (Slave mode only)

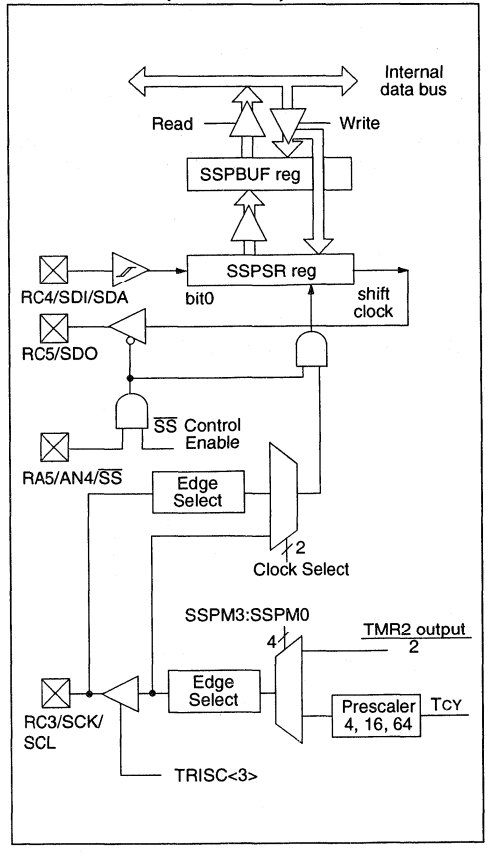
The SSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the Buffer Full bit, BF (SSPSTAT<0>) and flag bit SSPIF are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit, WCOL (SSPCON<7>) will be set. User software must clear bit WCOL so that it can be determined if the following write(s) to the SSPBUF completed successfully. When the application software is expecting to receive valid data, the SSPBUF register should be read before the next byte of data to transfer is written to the SSPBUF register. The Buffer Full bit BF (SSPSTAT<0>) indicates when the SSPBUF register has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF register must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-1 shows the loading of the SSPBUF (SSPSR) register for data transmission. The shaded instruction is only required if the received data is meaningful.

EXAMPLE 11-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
     BSF    STATUS, RP0     ;Specify Bank 1
LOOP BTFSS  SSPSTAT, BF     ;Has data been
                            ;received
                            ;(transmit
                            ;complete)?
     GOTO   LOOP            ;No
     BCF    STATUS, RP0     ;Specify Bank 0
     MOVF   SSPBUF, W       ;W reg = contents
                            ;of SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W reg = contents
                            ; of TXDATA
     MOVWF  SSPBUF          ;New data to xmit
```

The block diagram of the SSP module, when in SPI mode (Figure 11-3), shows that the SSPSR register is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

FIGURE 11-3: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, SSP enable bit SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear enable bit SSPEN, re-initialize SSPCON register, and then set enable bit SSPEN. This configures the SDI, SDO, SCK, and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- $\overline{SS}$ must have TRISA<5> set (if implemented)

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and $\overline{SS}$ could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched interrupt flag bit SSPIF (PIR1<3>) is set.

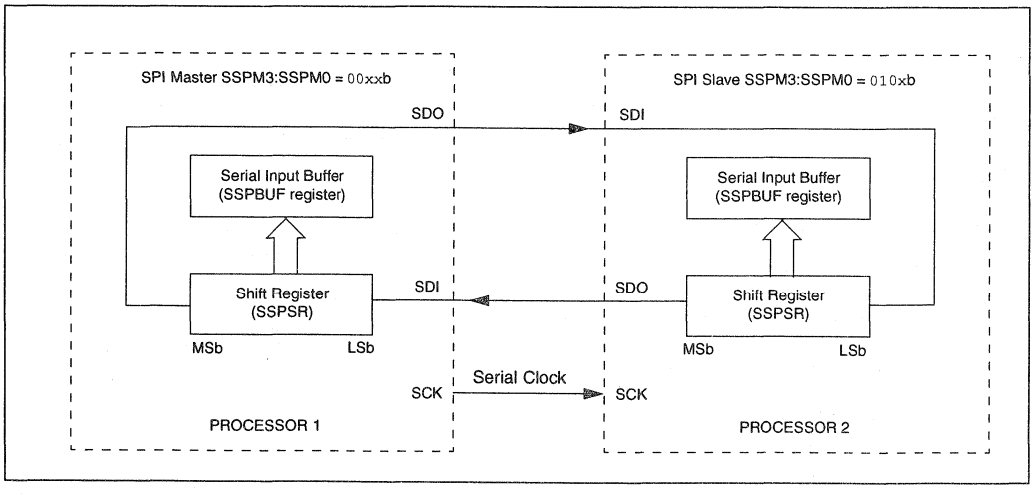
The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-5 and Figure 11-6 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or TCY)
- Fosc/16 (or 4 • TCY)
- Fosc/64 (or 16 • TCY)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

FIGURE 11-4: SPI MASTER/SLAVE CONNECTION



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The $\overline{SS}$ pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set the for synchronous slave mode to be enabled. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. If the SS pin is taken low without resetting SPI mode, the transmission will continue from the point at which it was taken high. External pull-up/ pull-down resistors may be desirable, depending on the application.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-5: SPI MODE TIMING (MASTER MODE OR SLAVE MODE W/O $\overline{SS}$ CONTROL)

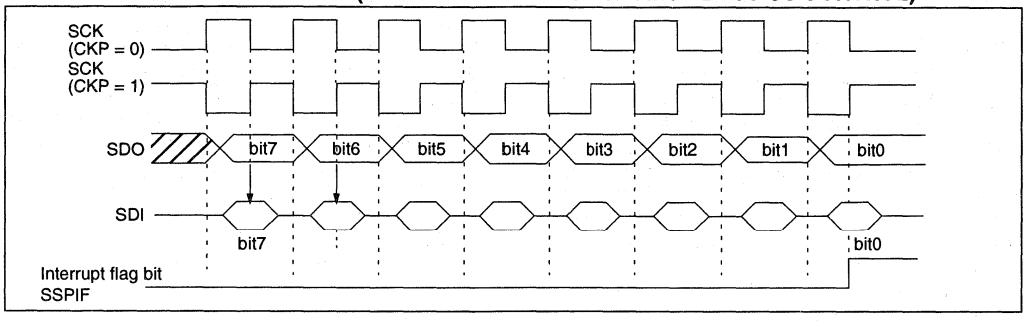

FIGURE 11-6: SPI MODE TIMING (SLAVE MODE WITH $\overline{SS}$ CONTROL)

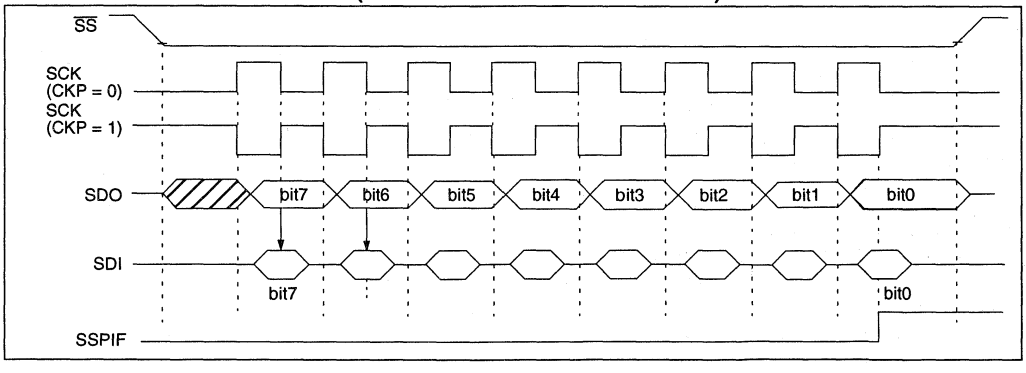

TABLE 11-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by SSP module in SPI mode.

Note 1: These bits are associated with the USART which is implemented on the PIC16C63/65/65A only.
2: PSPIF and PSPIE are reserved on the PIC16C62/62A/R62/63, always maintain these bits clear.
3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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11.2 I²C Overview

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

This section provides an overview of the Inter-Integrated Circuit (I^2C) bus, with Section 11.3 discussing the operation of the SSP module in I^2C mode.

The I^2C bus is a two-wire serial interface developed by the Philips Corporation. The original specification, or standard mode, was for data transfers of up to 100 Kbps. An enhanced specification, or fast mode, supports data transmission up to 400 Kbps. Both standard mode and fast mode devices will inter-operate if attached to the same bus.

The I^2C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master", which initiates transfer on the bus and generates the clock signals to permit that transfer, while the other device(s) acts as the "slave." All portions of the slave protocol are implemented in the SSP module's hardware, except general call support, while portions of the master protocol need to be addressed in the PIC16CXX software. Table 11-2 defines some of the I^2C bus terminology. For additional information on the I^2C interface specification, refer to the Philips Corporation document *"The I^2C bus and how to use it."* #939839340011, which can be obtained from the Philips Corporation.

In the I^2C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to "talk" to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read-from / write-to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of operating in either of these two relations:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level when no device is pulling the line down. The number of devices that may be attached to the I^2C bus is limited only by the maximum bus loading specification of 400 pF.

11.2.1 INITIATING AND TERMINATING DATA TRANSFER

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure 11-7 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted the SDA line can only change state when the SCL line is low.

FIGURE 11-7: START AND STOP CONDITIONS

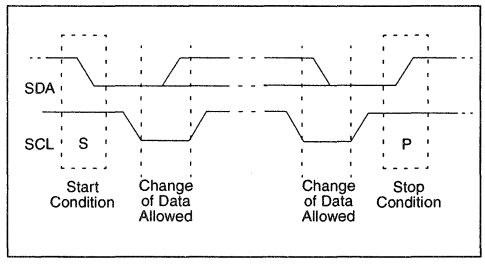

TABLE 11-2: I^2C BUS TERMINOLOGY

Term	Description
Transmitter	The device that sends the data to the bus.
Receiver	The device that receives the data from the bus.
Master	The device which initiates the transfer, generates the clock and terminates the transfer.
Slave	The device addressed by a master.
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensure that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

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11.2.2 ADDRESSING I^2C DEVICES

There are two address formats. The simplest is the 7-bit address format with a R/$\overline{W}$ bit (Figure 11-8). The more complex is the 10-bit address with a R/$\overline{W}$ bit (Figure 11-9). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

FIGURE 11-8: 7-BIT ADDRESS FORMAT

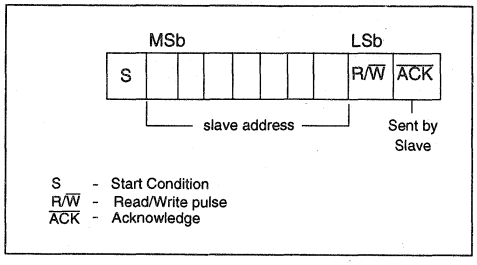
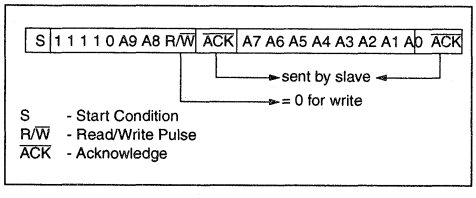


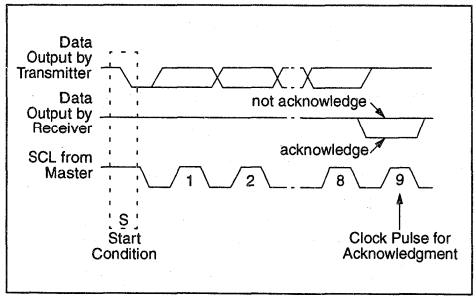
FIGURE 11-9: I^2C 10-BIT ADDRESS FORMAT



11.2.3 TRANSFER ACKNOWLEDGE

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit ($\overline{ACK}$) (Figure 11-10). When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave the SDA line high so that the master can generate the STOP condition (Figure 11-7).

FIGURE 11-10: SLAVE-RECEIVER ACKNOWLEDGE



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level, Figure 11-11. The slave will inherently stretch the clock when it is a transmitter but will not when it is a receiver. The slave will have to clear the SSPCON<4> bit to enable clock stretching when it is a receiver.

FIGURE 11-11: DATA TRANSFER WAIT STATE

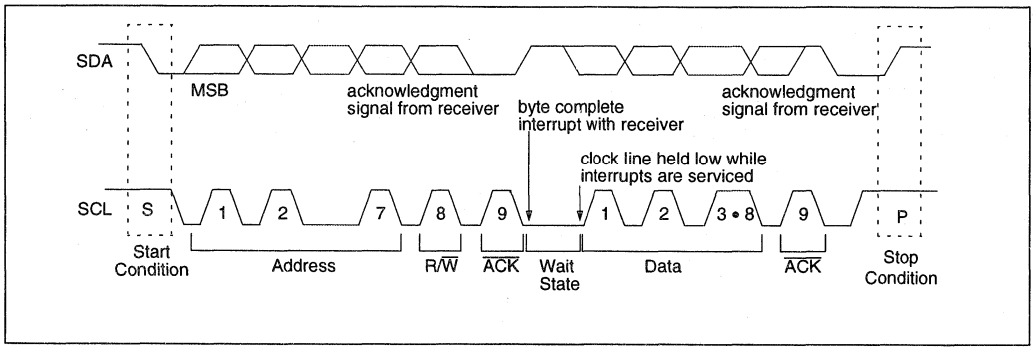


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Figure 11-12 and Figure 11-13 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-14.

FIGURE 11-12: MASTER-TRANSMITTER SEQUENCE

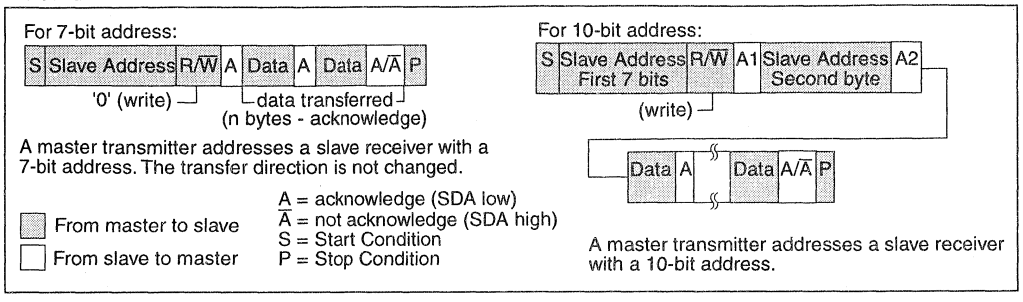


FIGURE 11-13: MASTER-RECEIVER SEQUENCE

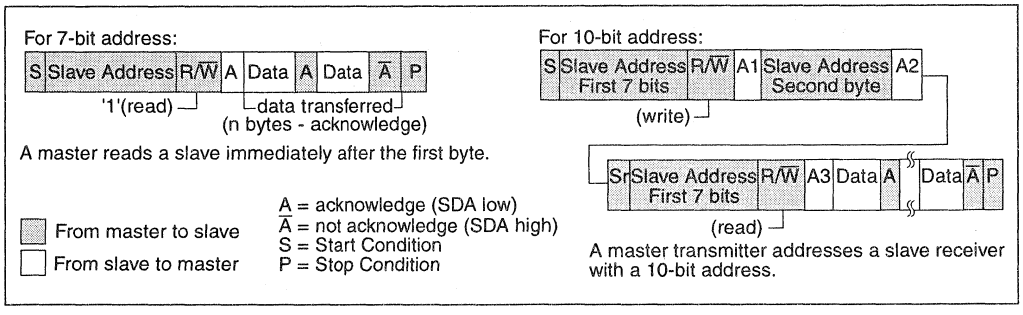
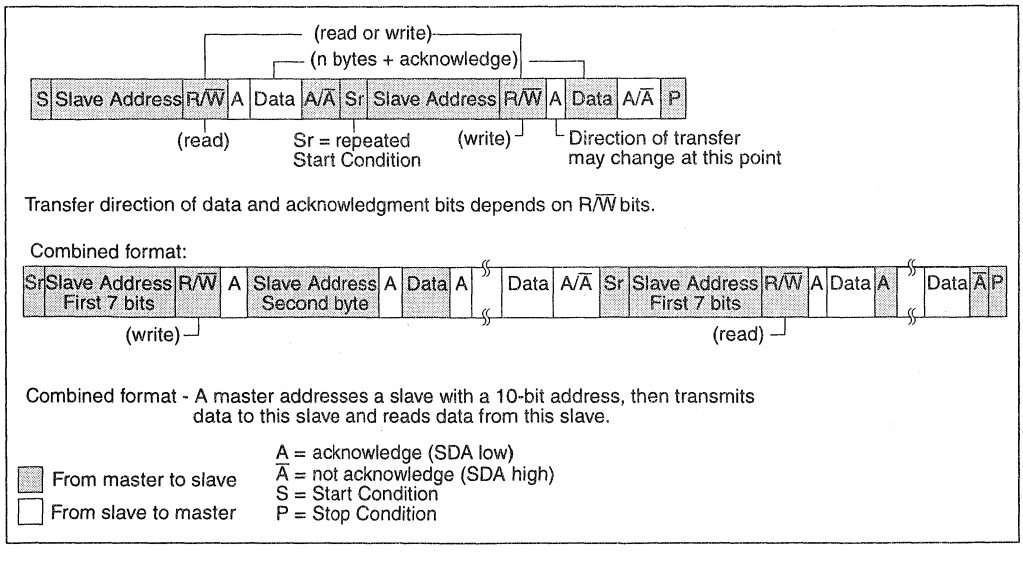


FIGURE 11-14: COMBINED FORMAT



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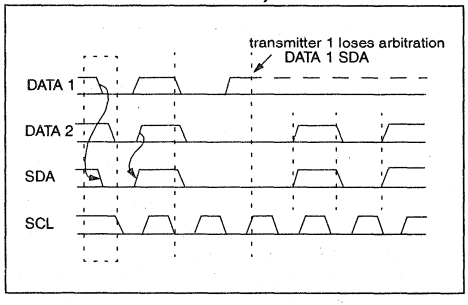
11.2.4 MULTI-MASTER

The I^2C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

11.2.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure 11-15), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

FIGURE 11-15: MULTI-MASTER ARBITRATION (TWO MASTERS)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

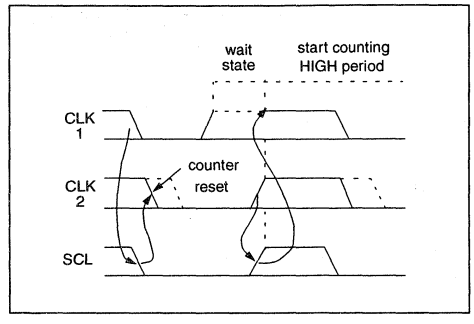
- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

11.2.4.2 CLOCK SYNCHRONIZATION

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period, Figure 11-16.

FIGURE 11-16: CLOCK SYNCHRONIZATION



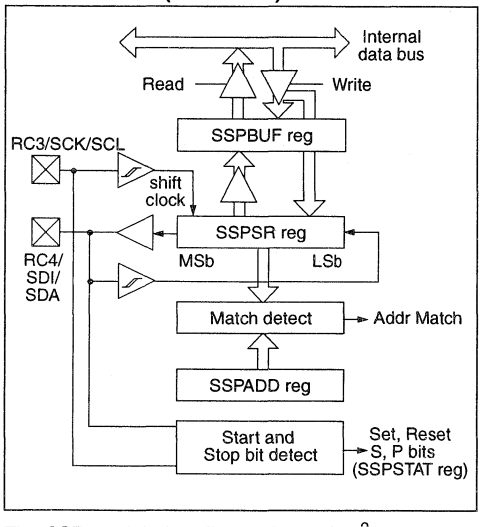
9

11.3 SSP I²C Operation

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The SSP module in I²C mode fully implements all slave functions (except general call support), and provides interrupts on start and stop bits in hardware to facilitate software implementations of the master functions. The SSP module implements the standard and fast mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

FIGURE 11-17: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
- I²C start and stop bit interrupts enabled, slave is idle

Selection of any I²C mode, with enable bit SSPEN set, forces the SCL and SDA pins to be open drains, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written-to or read-from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and overflow detect bit SSPOV (SSPCON<6>) is set, and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

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11.3.1 SLAVE MODE

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge ($\overline{ACK}$) pulse, and then load the SSPBUF register with the received value in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this $\overline{ACK}$ pulse. These are if either (or both):

a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.

b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF register, but interrupt flag bit SSPIF (PIR1<3>) is set. Table 11-3 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register while overflow bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I^2C specification as well as the requirement of the SSP module is shown in timing parameter #100 and parameter #101 (see Electrical Specification section).

11.3.1.1 ADDRESSING

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and bits BF and SSPOV are clear, the following events occur:

a) The SSPSR register value is loaded into the SSPBUF register.

b) The buffer full bit, BF is set.

c) An $\overline{ACK}$ pulse is generated.

d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on falling edge of ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave (Figure 11-9). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/$\overline{W}$ (SSPSTAT<2>) must specify a write, so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for a 10-bit address is as follows with steps 7-9 for slave-transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF and UA are set).
5. Update the SSPADD register with first (high) byte of Address (if match releases SCL line, this will clear bit UA).
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive repeated START condition.
8. Receive first (high) byte of Address (bits SSPIF and BF are set)
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

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TABLE 11-3: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received				
BF	SSPOV	SSPSR → SSPBUF	Generate $\overline{ACK}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if Enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

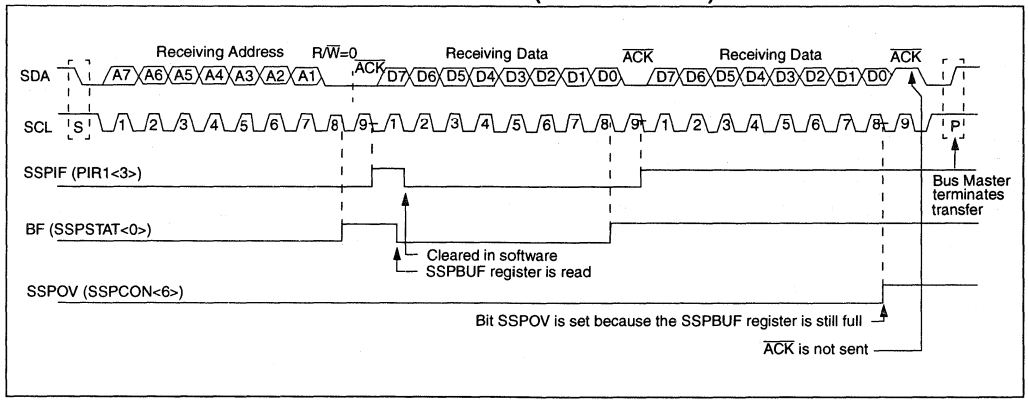
11.3.1.2 RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, bit R/$\overline{W}$ (SSPSTAT<2>) is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists then no acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software, and the SSPSTAT register is used to determine the status of the byte.

FIGURE 11-18: I^2C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



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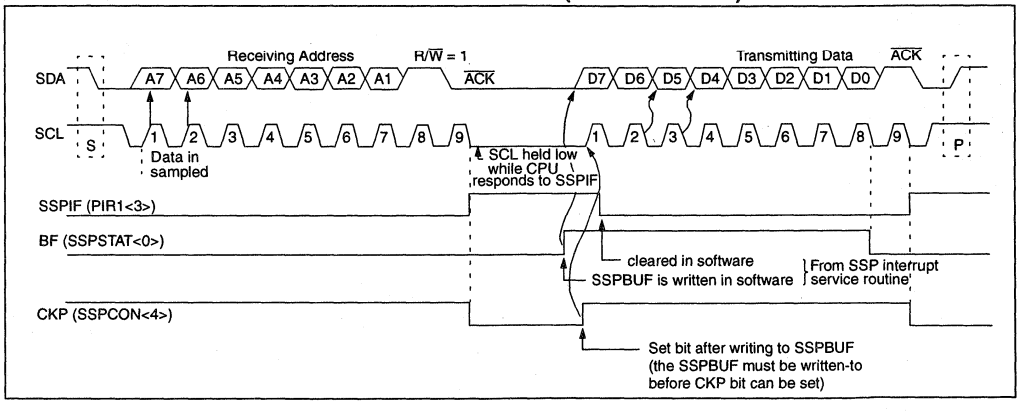
11.3.1.3 TRANSMISSION

When the R/$\overline{W}$ bit of the incoming address byte is set and an address match occurs, bit R/$\overline{W}$ (SSPSTAT<2>) is set. The received address is loaded into the SSPBUF register. The $\overline{ACK}$ pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 11-19).

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. When the $\overline{ACK}$ is latched by the slave, the slave logic is reset and the slave then monitors for another occurrence of the START bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting bit CKP.

FIGURE 11-19: I^2C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



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11.3.2 MASTER MODE

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared by a reset or when the SSP module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is idle with both the S and P bits clear.

In master mode the SCL and SDA lines are manipulated by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause the SSP Interrupt Flag bit SSPIF to be set (SSP Interrupt occurs if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

11.3.3 MULTI-MASTER MODE

In multi-master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle with both bits S and P clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, they are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage communication to the device may be in progress. If addressed, an $\overline{ACK}$ pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

TABLE 11-4: REGISTERS ASSOCIATED WITH I^2C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(2)	(3)	RCIF(1)	TXIF(1)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(2)	(3)	RCIE(1)	TXIE(1)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.
Shaded cells are not used by the SSP module in I^2C mode.

Note 1: These bits are associated with the USART and are implemented on the PIC16C63/65/65A only.
2: PSPIF and PSPIE are reserved on the PIC16C62/62A/R62/63, always maintain these bits clear.
3: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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FIGURE 11-20: OPERATION OF THE I^2C MODULE IN IDLE_MODE, RCV_MODE OR XMIT_MODE

```
IDLE_MODE (7-bit):
if (Addr_match)                 {       Set interrupt;
                                        if (R/W = 1)    {       Send ACK = 0;
                                                                set XMIT_MODE;
                                                        }
                                        else if (R/W = 0) set RCV_MODE;
                                }
RCV_MODE:
if ((SSPBUF=Full) OR (SSPOV = 1))
        {       Set SSPOV;
                Do not acknowledge;
        }
else    {       transfer SSPSR → SSPBUF;
                send ACK = 0;
        }
Receive 8-bits in SSPSR;
Set interrupt;
XMIT_MODE:
While ((SSPBUF = Empty) AND (CKP=0)) Hold SCL Low;
Send byte;
Set interrupt;
if ( ACK Received = 1)          {       End of transmission;
                                        Go back to IDLE_MODE;
                                }
else if ( ACK Received = 0)   Go back to XMIT_MODE;
IDLE_MODE (10-Bit):
If (High_byte_addr_match AND (R/W = 0))
        {       PRIOR_ADDR_MATCH = FALSE;
                Set interrupt;
                if ((SSPBUF = Full) OR ((SSPOV = 1))
                        {       Set SSPOV;
                                Do not acknowledge;
                        }
                else    {       Set UA = 1;
                                Send ACK = 0;
                                While (SSPADD not updated) Hold SCL low;
                                Clear UA = 0;
                                Receive Low_addr_byte;
                                Set interrupt;
                                Set UA = 1;
                                If (Low_byte_addr_match)
                                        {       PRIOR_ADDR_MATCH = TRUE;
                                                Send ACK = 0;
                                                while (SSPADD not updated) Hold SCL low;
                                                Clear UA = 0;
                                                Set RCV_MODE;
                                        }
                        }
        }
else if (High_byte_addr_match AND (R/W = 1)
        {       if (PRIOR_ADDR_MATCH)
                        {       send ACK = 0;
                                set XMIT_MODE;
                        }
                else PRIOR_ADDR_MATCH = FALSE;
        }
```

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NOTES:

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12.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART) MODULE

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also know as a Serial Communications Interface or SCI) The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

Bit SPEN (RCSTA<7>) and bits TRISC<7:6> have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter.

FIGURE 12-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **CSRC**: Clock Source Select bit

Asynchronous mode
Don't care

Synchronous mode
1 = Master mode (Clock generated internally from BRG)
0 = Slave mode (Clock from external source)

bit 6: **TX9**: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5: **TXEN**: Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled
Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4: **SYNC**: USART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3: **Unimplemented:** Read as '0'

bit 2: **BRGH**: High Baud Rate Select bit

Asynchronous mode
1 = High speed

Note: At the time of this printing, the asynchronous high speed mode (BRGH is set) may experience a high rate of receive errors. It is recommended to have the BRGH bit cleared. If you desire a higher baud rate than BRGH=0 can support, refer to the device errata for additional information.

0 = Low speed

Synchronous mode
Unused in this mode

bit 1: **TRMT**: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0: **TX9D**: 9th bit of transmit data. Can be parity bit.

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FIGURE 12-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D
bit7							bit0

R	= Readable bit
W	= Writable bit
U	= Unimplemented bit, read as '0'
- n	= Value at POR reset
x	= unknown

bit 7: **SPEN**: Serial Port Enable bit
(Configures RC7/RX/DT and RC6/TX/CK pins as serial port pins when bits TRISC<7:6> are set)
1 = Serial port enabled
0 = Serial port disabled

bit 6: **RX9**: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5: **SREN**: Single Receive Enable bit

Asynchronous mode
Don't care

Synchronous mode - master
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.

Synchronous mode - slave
Unused in this mode

bit 4: **CREN**: Continuous Receive Enable bit

Asynchronous mode
1 = Enables continuous receive
0 = Disables continuous receive

Synchronous mode
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3: **Unimplemented:** Read as '0'

bit 2: **FERR**: Framing Error bit
1 = Framing error (Can be updated by reading RCREG register and receive next valid byte)
0 = No framing error

bit 1: **OERR**: Overrun Error bit
1 = Overrun error (Can be cleared by clearing bit CREN)
0 = No overrun error

bit 0: **RX9D**: 9th bit of received data (Can be parity bit)

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12.1 USART Baud Rate Generator (BRG)

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 12-1. From this, the error in baud rate can be determined.

Example 12-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz
Desired Baud Rate = 9600
BRGH = 0
SYNC = 0

EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))

9600 = 16000000 /(64 (X + 1))

X = ⌊25.042⌋ = 25

Calculated Baud Rate=16000000 / (64 (25 + 1))

= 9615

$$\text{Error} = \frac{\text{(Calculated Baud Rate - Desired Baud Rate)}}{\text{Desired Baud Rate}}$$

= (9615 - 9600) / 9600

= 0.16%

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the Fosc/(16(X + 1)) equation can reduce the baud rate error in some cases.

Note: At the time of this printing, the asynchronous high speed mode (BRGH is set) may experience a high rate of receive errors. It is recommended to have the BRGH bit cleared. If you desire a higher baud rate than BRGH=0 can support, refer to the device errata for additional information.

Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

TABLE 12-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	N/A

X = value in SPBRG (0 to 255)

TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the BRG.

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TABLE 12-3: BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	FOSC = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-	NA	-	-
9.6	NA	-	-	NA	-	-	9.766	+1.73	255	9.622	+0.23	185
19.2	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129	19.24	+0.23	92
76.8	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32	77.82	+1.32	22
96	96.15	+0.16	51	95.24	-0.79	41	96.15	+0.16	25	94.20	-1.88	18
300	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7	298.3	-0.57	5
500	500	0	9	500	0	7	500	0	4	NA	-	-
HIGH	5000	-	0	4000	-	0	2500	-	0	1789.8	-	0
LOW	19.53	-	255	15.625	-	255	9.766	-	255	6.991	-	255

BAUD RATE (K)	FOSC = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-	0.303	+1.14	26
1.2	NA	-	-	NA	-	-	NA	-	-	1.202	+0.16	207	1.170	-2.48	6
2.4	NA	-	-	NA	-	-	NA	-	-	2.404	+0.16	103	NA	-	-
9.6	9.6	0	131	9.615	+0.16	103	9.622	+0.23	92	9.615	+0.16	25	NA	-	-
19.2	19.2	0	65	19.231	+0.16	51	19.04	-0.83	46	19.24	+0.16	12	NA	-	-
76.8	79.2	+3.13	15	76.923	+0.16	12	74.57	-2.90	11	83.34	+8.51	2	NA	-	-
96	97.48	+1.54	12	1000	+4.17	9	99.43	+3.57	8	NA	-	-	NA	-	-
300	316.8	+5.60	3	NA	-	-	298.3	-0.57	2	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	1267	-	0	100	-	0	894.9	-	0	250	-	0	8.192	-	0
LOW	4.950	-	255	3.906	-	255	3.496	-	255	0.9766	-	255	0.032	-	255

TABLE 12-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD RATE (K)	FOSC = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129	1.203	+0.23	92
2.4	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64	2.380	-0.83	46
9.6	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15	9.322	-2.90	11
19.2	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5
76.8	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1	NA	-	-
96	104.2	+8.51	2	NA	-	-	NA	-	-	NA	-	-
300	312.5	+4.17	0	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	312.5	-	0	250	-	0	156.3	-	0	111.9	-	0
LOW	1.221	-	255	0.977	-	255	0.6104	-	255	0.437	-	255

BAUD RATE (K)	FOSC = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	0.31	+3.13	255	0.3005	-0.17	207	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.2	0	65	1.202	+1.67	51	1.190	-0.83	46	1.202	+0.16	12	NA	-	-
2.4	2.4	0	32	2.404	+1.67	25	2.432	+1.32	22	2.232	-6.99	6	NA	-	-
9.6	9.9	+3.13	7	NA	-	-	9.322	-2.90	5	NA	-	-	NA	-	-
19.2	19.8	+3.13	3	NA	-	-	18.64	-2.90	2	NA	-	-	NA	-	-
76.8	79.2	+3.13	0	NA	-	-	NA	-	-	NA	-	-	NA	-	-
96	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	79.2	-	0	62.500	-	0	55.93	-	0	15.63	-	0	0.512	-	0
LOW	0.3094	-	255	3.906	-	255	0.2185	-	255	0.0610	-	255	0.0020	-	255

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TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD RATE (K)	FOSC = 20 MHz KBAUD	% ERROR	SPBRG value (decimal)	16 MHz KBAUD	% ERROR	SPBRG value (decimal)	10 MHz KBAUD	% ERROR	SPBRG value (decimal)	7.16 MHz KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64	9.520	-0.83	46
19.2	19.230	+0.16	64	19.230	+0.16	51	18.939	-1.36	32	19.454	+1.32	22
38.4	37.878	-1.36	32	38.461	+0.16	25	39.062	+1.7	15	37.286	-2.90	11
57.6	56.818	-1.36	21	58.823	+2.12	16	56.818	-1.36	10	55.930	-2.90	7
115.2	113.636	-1.36	10	111.111	-3.55	8	125	+8.51	4	111.860	-2.90	3
250	250	0	4	250	0	3	NA	-	-	NA	-	-
625	625	0	1	NA	-	-	625	0	0	NA	-	-
1250	1250	0	0	NA	-	-	NA	-	-	NA	-	-

BAUD RATE (K)	FOSC = 5.068 MHz KBAUD	% ERROR	SPBRG value (decimal)	4 MHz KBAUD	% ERROR	SPBRG value (decimal)	3.579 MHz KBAUD	% ERROR	SPBRG value (decimal)	1 MHz KBAUD	% ERROR	SPBRG value (decimal)	32.768 kHz KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.6	0	32	NA	-	-	9.727	+1.32	22	8.928	-6.99	6	NA	-	-
19.2	18.645	-2.94	16	1.202	+0.17	207	18.643	-2.90	11	20.833	+8.51	2	NA	-	-
38.4	39.6	+3.12	7	2.403	+0.13	103	37.286	-2.90	5	31.25	-18.61	1	NA	-	-
57.6	52.8	-8.33	5	9.615	+0.16	25	55.930	-2.90	3	62.5	+8.51	0	NA	-	-
115.2	105.6	-8.33	2	19.231	+0.16	12	111.860	-2.90	1	NA	-	-	NA	-	-
250	NA	-	-	NA	-	-	223.721	-10.51	0	NA	-	-	NA	-	-
625	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1250	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-

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12.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin. If bit BRGH (TXSTA<2>) is clear (i.e., at the low baud rates), the sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 12-3). If bit BRGH is set (i.e., at the high baud rates), the sampling is done on the 3 clock edges preceding the second rising edge after the first falling edge of a x4 clock (Figure 12-4 and Figure 12-5).

FIGURE 12-3: RX PIN SAMPLING SCHEME (BRGH = 0)

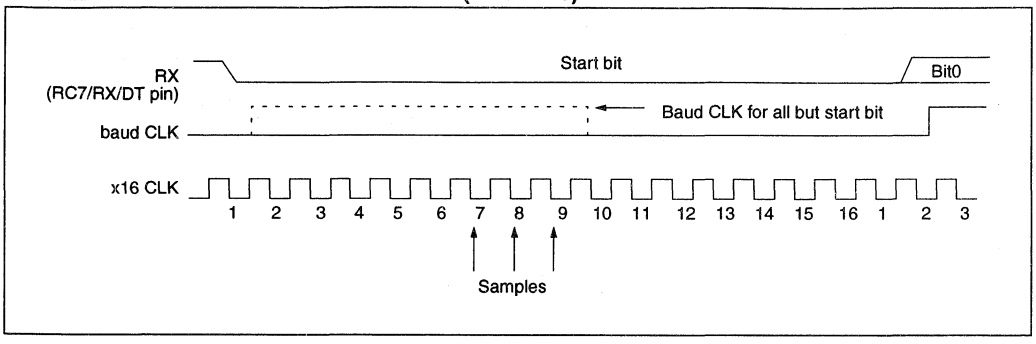


FIGURE 12-4: RX PIN SAMPLING SCHEME (BRGH = 1)

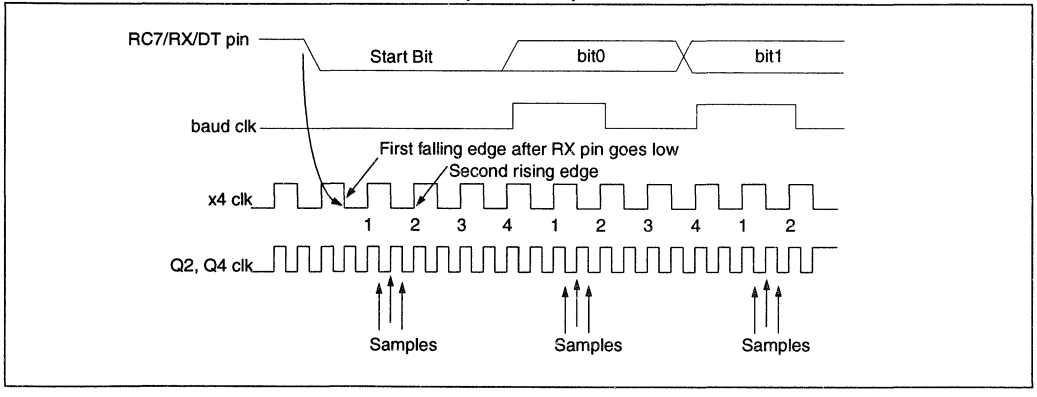
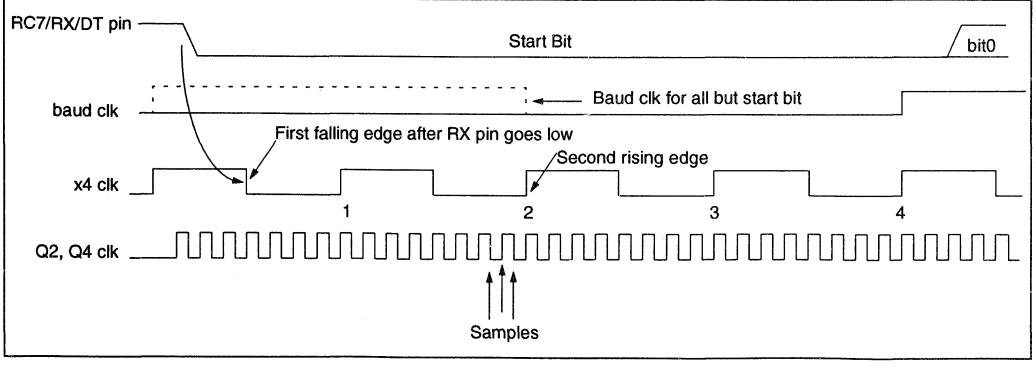


FIGURE 12-5: RX PIN SAMPLING SCHEME (BRGH = 1)



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12.2 USART Asynchronous Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

12.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 12-6. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCY) the TXREG register is empty and flag bit TXIF (PIR1<4>) is set. This interrupt is enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>) shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

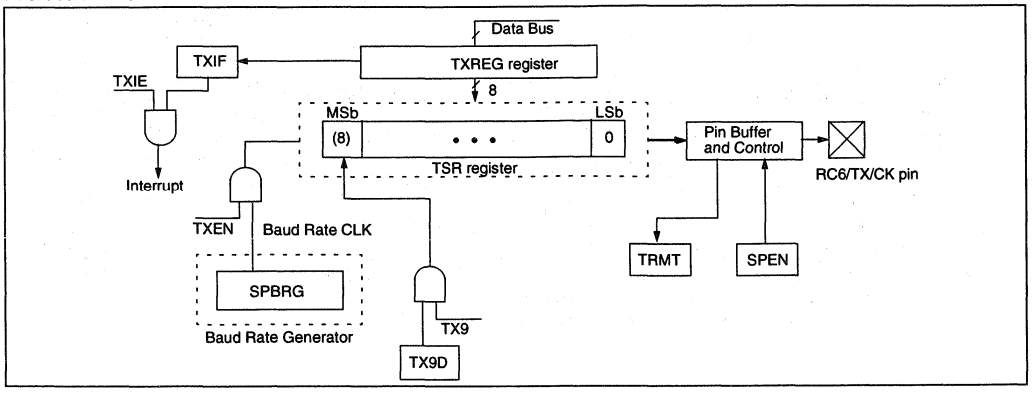
Note 1: The TSR register is not mapped in data memory so it is not available to the user.

Note 2: Flag bit TXIF is set when enable bit TXEN is set.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 12-6). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR register resulting in an empty TXREG register. A back-to-back transfer is thus possible (Figure 12-8). Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. As a result the RC6/TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, transmit bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). In such a case, an incorrect ninth data bit maybe loaded in the TSR register.

FIGURE 12-6: USART TRANSMIT BLOCK DIAGRAM



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Steps to follow when setting up an Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, then set bit BRGH. (Section 12.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).

FIGURE 12-7: ASYNCHRONOUS MASTER TRANSMISSION

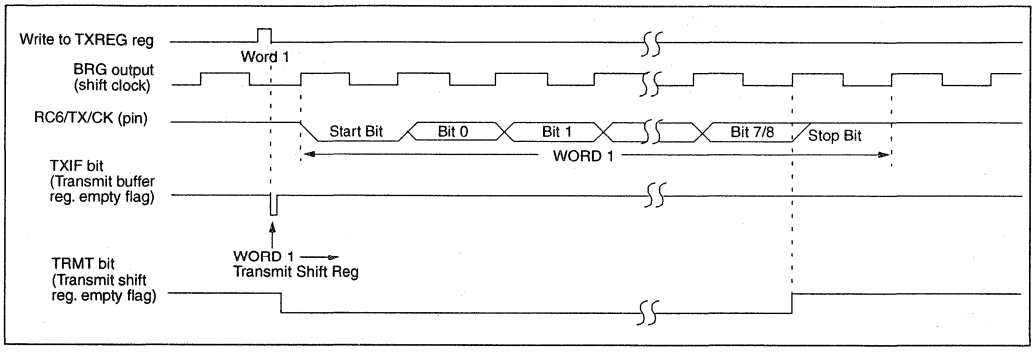
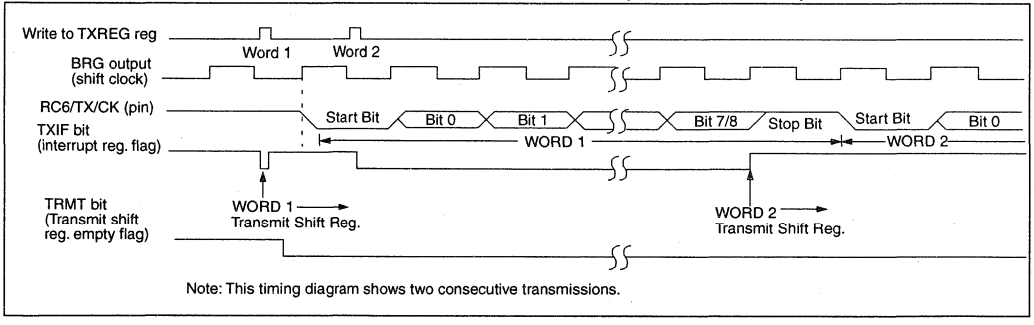


FIGURE 12-8: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 12-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.
Note 1: PSPIF and PSPIE are reserved on the PIC16C63, always maintain these bits clear.
2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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12.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 12-9. The data comes in the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at FOSC.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is double buffered register, i.e., it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG is still full, then the overrun error bit, OERR (RCSTA<1>) will be set. The word in the RSR register will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited, so it is essential to clear overrun bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a stop bit is detected as clear. Error bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG register will load bits RX9D and FERR with new values. Therefore it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old FERR and RX9D information.

FIGURE 12-9: USART RECEIVE BLOCK DIAGRAM

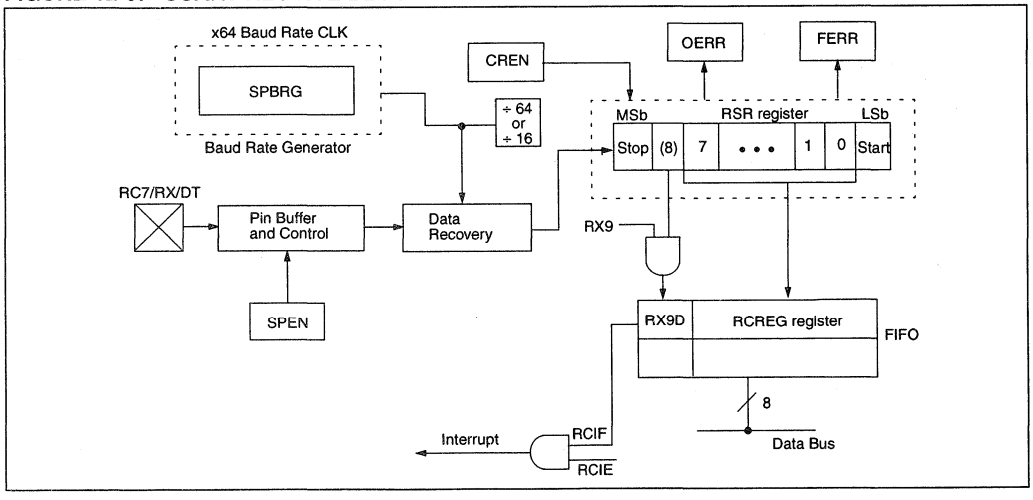
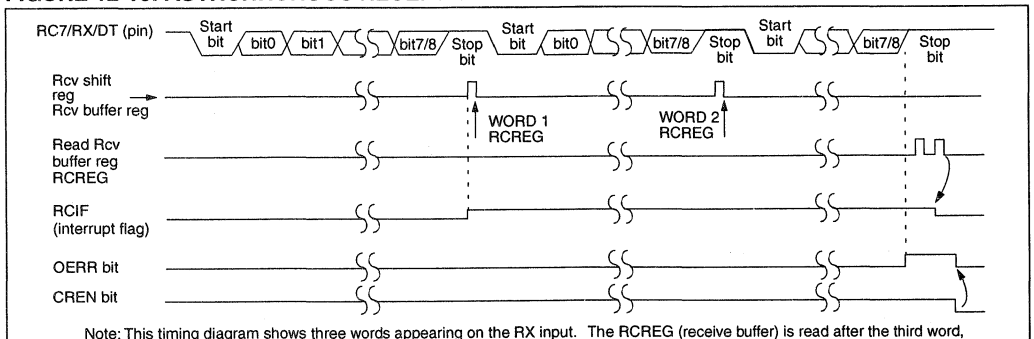


FIGURE 12-10: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing overrun error bit OERR to be set.

Steps to follow when setting up an Asynchronous Reception:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 12.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit RCIE.
4. If 9-bit reception is desired, then set bit RX9.
5. Enable the reception by setting enable bit CREN.
6. Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading the RCREG register.
9. If any error occurred, clear the error by clearing enable bit CREN.

TABLE 12-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.
Note 1: PSPIE and PSPIF are reserved on the PIC16C63, always maintain these bits clear.
2: PIE1<6> and PIR1<6> are reserved, always maintain these bits clear.

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12.3 USART Synchronous Master Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

In Synchronous Master mode the data is transmitted in a half-duplex manner i.e., transmission and reception do not occur at the same time. When transmitting data the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition enable bit SPEN (RCSTA<7>) is set in order to configure the RC6 and RC7 I/O pins to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

12.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 12-6. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR register is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcycle), the TXREG register is empty and interrupt flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the status of enable bit TXIE and cannot be cleared in software. It will clear only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR register is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 12-11). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. This is advantageous when slow baud rates are selected, since the BRG is kept in reset when bits TXEN, CREN, and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR resulting in an empty TXREG register. Back-to-back transfers are possible.

Clearing enable bit TXEN, during a transmission, will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hi-impedance. If, during a transmission, either bit CREN or bit SREN is set the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic however, is not reset although it is disconnected from the pins. In order to reset the transmitter, the user has to clear enable bit TXEN. If enable bit SREN is set (to interrupt an on going transmission and receive a single word), then after the single word is received, enable bit SREN will be cleared, and the serial port will revert back to transmitting since enable bit TXEN is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, enable bit TXEN should be cleared.

In order to select 9-bit transmission, bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR register was empty and the TXREG register was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set bit TX9.
5. Enable the transmission by setting enable bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.

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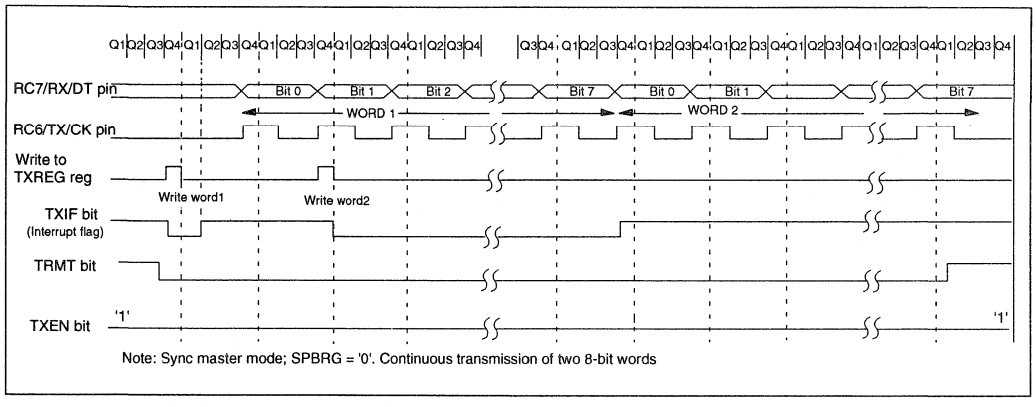
TABLE 12-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

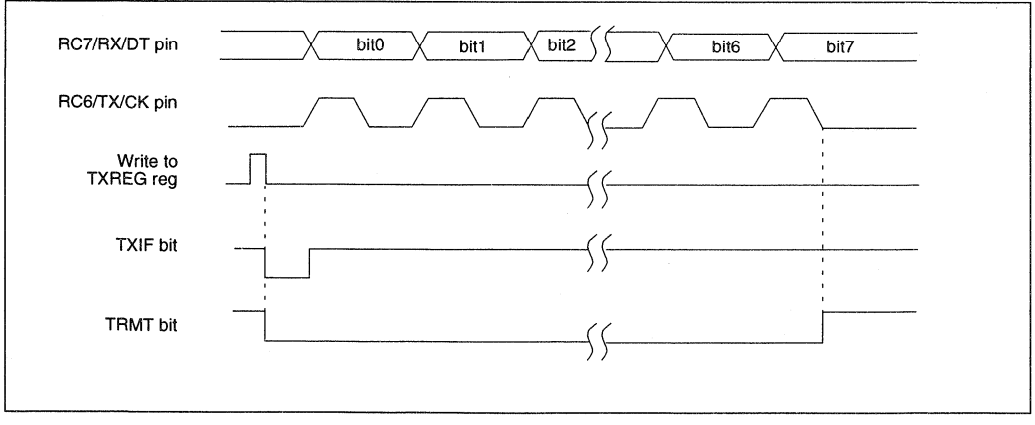
Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Master Transmission.
Note 1: PSPIE and PSPIF are reserved on the PIC16C63, always maintain these bits clear.
2: PIE1<6> and PIR1<6> are reserved, always maintain these bits clear.

FIGURE 12-11: SYNCHRONOUS TRANSMISSION



Note: Sync master mode; SPBRG = '0'. Continuous transmission of two 8-bit words

FIGURE 12-12: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



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12.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous Mode is selected, reception is enabled by setting either enable bit SREN (RCSTA<5>) bit or enable bit CREN (RCSTA<4>). Data is sampled on the DT pin on the falling edge of the clock. If enable bit SREN is set, then only a single word is received. If enable bit CREN is set, the reception is continuous until bit CREN is cleared. If both the bits are set then bit CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to the RCREG register (if it is empty). When the transfer is complete, interrupt bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is reset by the hardware. In this case, it is reset when the RCREG register has been read and is empty. The RCREG is a double buffered register, i.e., it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR register. On the clocking of the last bit of the third byte, if the RCREG register is still full, then overrun error bit, OERR (RCSTA<1>) is set. The word in the RSR register will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun error bit OERR has to be cleared in software (by clearing bit CREN). If bit OERR is set, transfers from the RSR to the RCREG are inhibited, so it is essential to clear bit OERR if it is set. The 9th receive bit is buffered the same way as the receive data. Reading the RCREG register will load bit RX9D with a new value. Therefore it is essential for the user to read the RCSTA register before reading the RCREG register in order not to lose the old RX9D bit information.

Steps to follow when setting up Synchronous Master Reception:

1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. Ensure bits CREN and SREN are clear.
4. If interrupts are desired, then set enable bit RCIE.
5. If 9-bit reception is desired, then set bit RX9.
6. If a single reception is required, set enable bit SREN. For continuous reception set enable bit CREN.
7. Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
8. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
9. Read the 8-bit received data by reading the RCREG register.
10. If any error occurred, clear the error by clearing enable bit CREN.

TABLE 12-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Master Reception.
Note 1: PSPIF and PSPIE are reserved on the PIC16C63, always maintain these bits clear.
2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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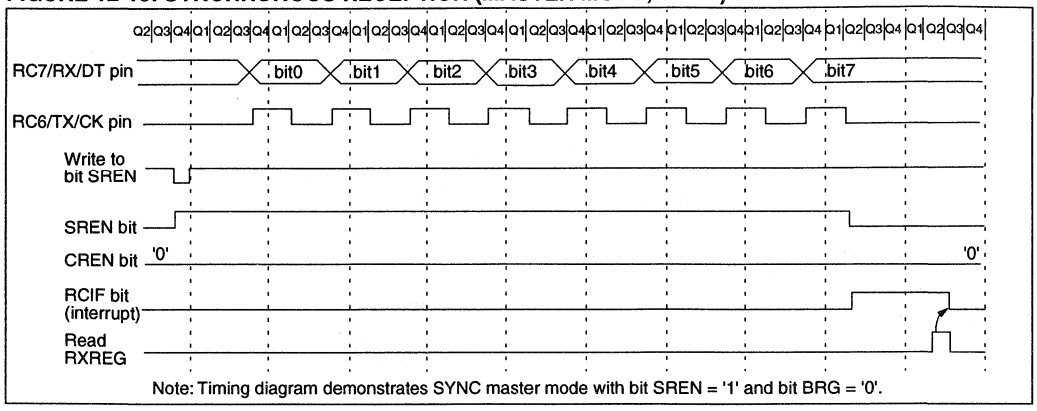
FIGURE 12-13: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates SYNC master mode with bit SREN = '1' and bit BRG = '0'.

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12.4 USART Synchronous Slave Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

Synchronous Slave Mode differs from Master Mode in the fact that the shift clock is supplied externally at the CK pin (instead of being supplied internally in master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

12.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

a) The first word will immediately transfer to the TSR register and transmit.
b) The second word will remain in TXREG register.
c) Flag bit TXIF will not be set.
d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
e) If enable bit TXIE is set, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up Synchronous Slave Transmission:

1. Enable the synchronous slave serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
2. Clear bits CREN and SREN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set bit TX9.
5. Enable the transmission by setting bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.

12.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, enable bit SREN is a don't care in slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

1. Enable the synchronous master serial port by setting bits SYNC and SPEN, and clearing bit CSRC.
2. If interrupts are desired, then set enable bit RCIE.
3. If 9-bit reception is desired, then set bit RX9.
4. To enable reception, set enable bit CREN.
5. Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
6. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREG register.
8. If any error occurred, clear the error by clearing enable bit CREN.

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TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Slave Transmission.
Note 1: PSPIF and PSPIE are reserved on the PIC16C63, always maintain these bits clear.
2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

TABLE 12-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	(2)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	(2)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Synchronous Slave Reception.
Note 1: PSPIF and PSPIE are reserved on the PIC16C63, always maintain these bits clear.
2: PIR1<6> and PIE1<6> are reserved, always maintain these bits clear.

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13.0 SPECIAL FEATURES OF THE CPU

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP mode
- Code protection
- ID locations
- In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external reset, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

13.1 Configuration Bits

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 13-1: CONFIGURATION WORD FOR PIC16C61

—	—	—	—	—	—	—	—	—	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-5: **Unimplemented**: Read as '1'

bit 4: **CP0**: Code protection bit
1 = Code protection off
0 = All memory is code protected, but 00h - 3Fh is writable

bit 3: **PWRTE**: Power-up Timer Enable bit
1 = Power-up Timer enabled
0 = Power-up Timer disabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

9

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FIGURE 13-2: CONFIGURATION WORD FOR PIC16C62/64/65

—	—	—	—	—	—	—	—	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-6: **Unimplemented:** Read as '1'

bit 5-4: **CP1:CP0:** Code Protection bits
11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 3: **PWRTE:** Power-up Timer Enable bit
1 = Power-up Timer enabled
0 = Power-up Timer disabled

bit 2: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

FIGURE 13-3: CONFIGURATION WORD FOR PIC16C62A/R62/63/64A/R64/65A

CP1	CP0	CP1	CP0	CP1	CP0	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-8: **CP1:CP0:** Code Protection bits(2)
bit 5:4 11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 7: **Unimplemented:** Read as '1'

bit 6: **BODEN:** Brown-out Reset Enable bit (1)
1 = Brown-out Reset enabled
0 = Brown-out Reset disabled

bit 3: **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit (1)
1 = Power-up Timer disabled
0 = Power-up Timer enabled

bit 2: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRTE}}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.
2: All of the CP1:CP0 pairs have to be given the same value to implement the code protection scheme listed.

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13.2 Oscillator Configurations

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

13.2.1 OSCILLATOR TYPES

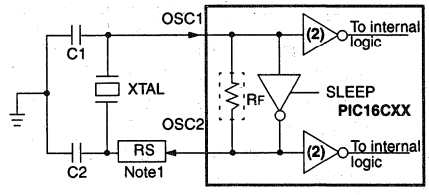
The PIC16CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

13.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In LP, XT, or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 13-4). The PIC16CXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in LP, XT, or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 13-5).

FIGURE 13-4: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



See Table 13-1, Table 13-2, Table 13-3 and Table 13-4 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.

2: For the PIC16C61 the buffer is on the OSC2 pin, all other devices have the buffer on the OSC1 pin.

FIGURE 13-5: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

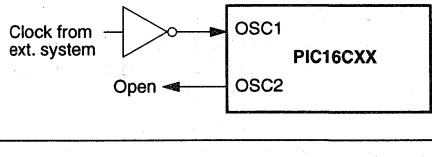


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TABLE 13-1: CERAMIC RESONATORS PIC16C61

Ranges Tested:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	47 - 100 pF 15 - 68 pF 15 - 68 pF	47 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	15 - 68 pF 10 - 47 pF	15 - 68 pF 10 - 47 pF
Note: Recommended values of C1 and C2 are identical to the ranges tested table. Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.			
Resonators Used:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%	
All resonators used did not have built-in capacitors.			

TABLE 13-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C61

Mode	Freq	OSC1	OSC2
LP	32 kHz 200 kHz	33 - 68 pF 15 - 47 pF	33 - 68 pF 15 - 47 pF
XT	100 kHz 500 kHz 1 MHz 2 MHz 4 MHz	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF
HS	8 MHz 20 MHz	15 - 47 pF 15 - 47 pF	15 - 47 pF 15 - 47 pF
Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.			

TABLE 13-3: CERAMIC RESONATORS PIC16C62/62A/R62/63/64/64A/ R64/65/65A

Ranges Tested:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF
Note: Recommended values of C1 and C2 are identical to the ranges tested table. Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.			
Resonators Used:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%	
All resonators used did not have built-in capacitors.			

TABLE 13-4: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C62/62A/R62/63/64/ 64A/R64/65/65A

Mode	Freq	OSC1	OSC2
LP	32 kHz(1) 200 kHz	15 - 47 pF 15 - 33 pF	15 - 47 pF 15 - 33 pF
XT	100 kHz 500 kHz 1 MHz 2 MHz 4 MHz	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF
HS	8 MHz 20 MHz	15 - 47 pF 15 - 47 pF	15 - 47 pF 15 - 47 pF
Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components. Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.			

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13.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 13-6 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 13-6: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

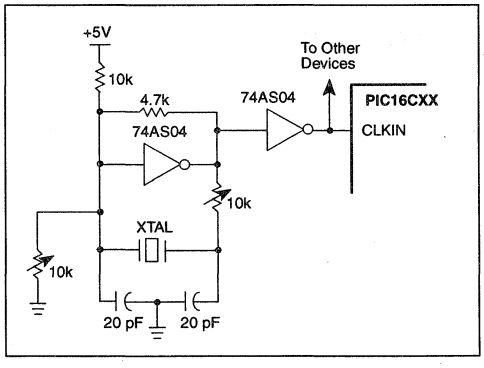
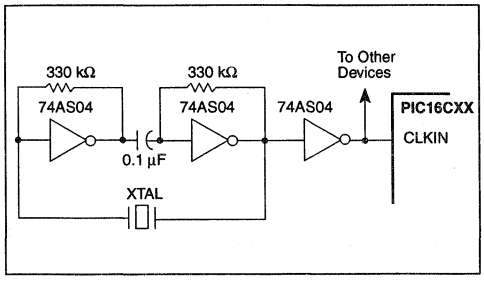


Figure 13-7 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 13-7: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



13.2.4 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 13-8 shows how the RC combination is connected to the PIC16CXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable or stop completely. For very high Rext values (e.g. 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

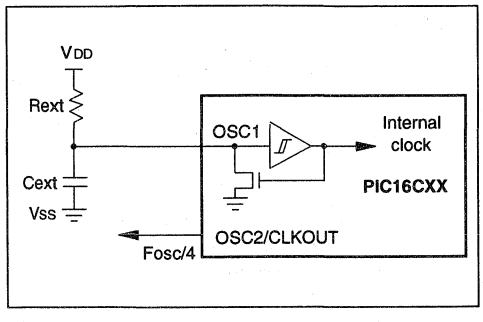
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See characterization data for desired device for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characterization data for desired device for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-4 for waveform).

FIGURE 13-8: RC OSCILLATOR MODE



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13.3 Reset

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The PIC16CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{MCLR}$ reset during normal operation
- $\overline{MCLR}$ reset during SLEEP
- WDT Reset (normal operation)
- Brown-out Reset (BOR) - PIC16C62A/R62/63/64A/R64/65A

Some registers are not affected in any reset condition, their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on $\overline{MCLR}$ or WDT Reset, on $\overline{MCLR}$ reset during SLEEP, and on Brown-out Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation.

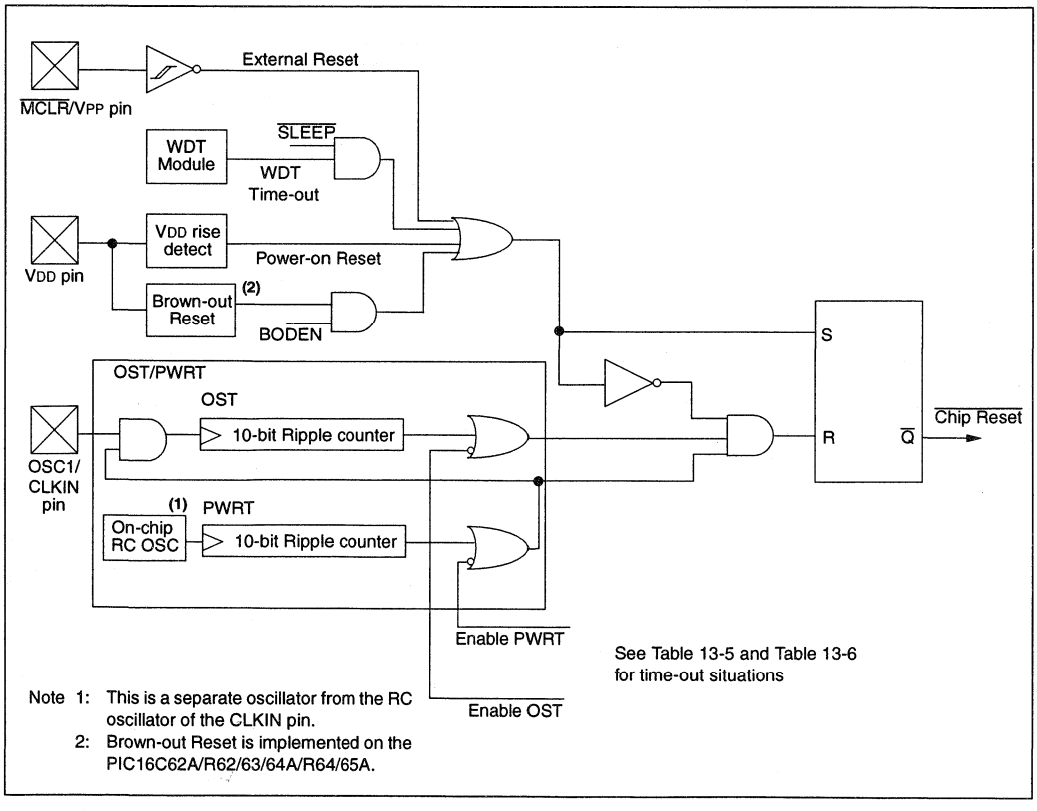
The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 13-7, Table 13-8, and Table 13-9. These bits are used in software to determine the nature of the reset. See Table 13-12 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 13-9.

On the PIC16C62A/R62/63/64A/R64/65A, the $\overline{MCLR}$ reset path has a noise filter to detect and ignore small pulses. See parameter #34 for pulse width specifications.

It should be noted that a WDT Reset does not drive the $\overline{MCLR}$ pin low.

FIGURE 13-9: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.
2: Brown-out Reset is implemented on the PIC16C62A/R62/63/64A/R64/65A.

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13.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

13.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the MCLR/VPP pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*."

13.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

13.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures the crystal oscillator or resonator has started and stabilized.

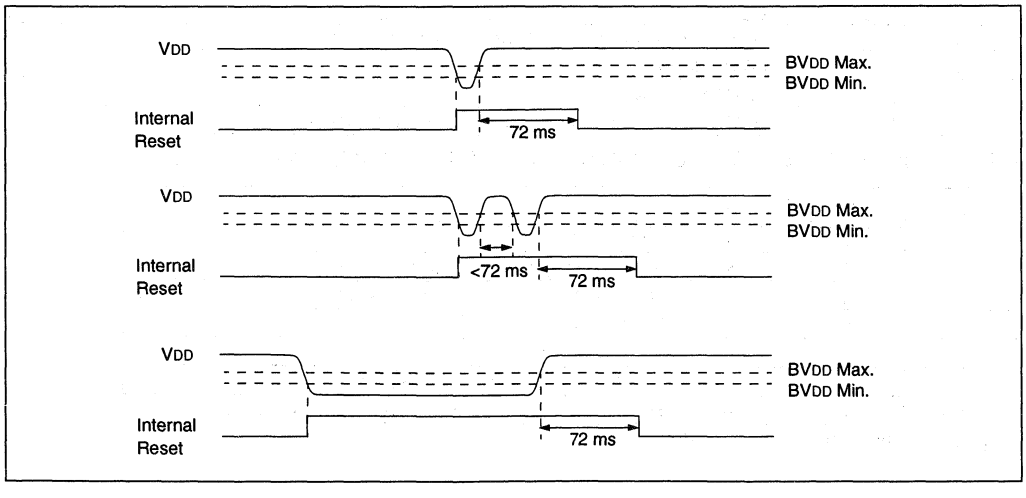
The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

13.4.4 BROWN-OUT RESET (BOR)

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (parameter D005 in Electrical Specification section) for greater than parameter #34 (see Electrical Specification section), the brown-out situation will reset the chip. A reset may not occur if VDD falls below 4.0V for less than parameter #34. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 13-10 shows typical brown-out situations.

FIGURE 13-10: BROWN-OUT SITUATIONS



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13.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First a PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode, with the PWRT disabled, there will be no time-out at all. Figure 13-11, Figure 13-12, and Figure 13-13 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if the $\overline{MCLR}$/VPP pin is kept low long enough, the time-outs will expire. Then bringing the $\overline{MCLR}$/VPP pin high will begin execution immediately (Figure 13-14). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 13-10 and Table 13-11 show the reset conditions for some special function registers, while Table 13-12 shows the reset conditions for all the registers.

13.4.6 POWER CONTROL/STATUS REGISTER (PCON)

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The Power Control/Status Register, PCON has up to 2 bits, depending upon the device. Bit0 is not implemented on the PIC16C62/64/65.

Bit0 is $\overline{BOR}$ (Brown-out Reset Status bit). $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{BOR}$ cleared, indicating that a brown-out has occurred. The $\overline{BOR}$ status bit is a "Don't Care" and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is $\overline{POR}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 13-5: TIME-OUT IN VARIOUS SITUATIONS, PIC16C61/62/64/65

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024 TOSC
RC	72 ms	—	—

TABLE 13-6: TIME-OUT IN VARIOUS SITUATIONS, PIC16C62A/R62/63/64A/R64/65A

Oscillator Configuration	Power-up		Brown-out	Wake up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024 TOSC
RC	72 ms	—	72 ms	—

TABLE 13-7: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C61

$\overline{TO}$	$\overline{PD}$	
1	1	Power-on Reset or $\overline{MCLR}$ reset during normal operation
0	1	WDT Reset
0	0	WDT Wake-up
1	0	$\overline{MCLR}$ reset during SLEEP or interrupt wake-up from SLEEP

TABLE 13-8: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C62/64/65

$\overline{POR}$	$\overline{TO}$	$\overline{PD}$	
0	1	1	Power-on Reset
0	0	x	Illegal, $\overline{TO}$ is set on a Power-on Reset
0	x	0	Illegal, $\overline{PD}$ is set on a Power-on Reset
1	0	1	WDT Reset
1	0	0	WDT Wake-up
1	u	u	$\overline{MCLR}$ reset during normal operation
1	1	0	$\overline{MCLR}$ reset during SLEEP or interrupt wake-up from SLEEP

Legend: x = unknown, u = unchanged

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TABLE 13-9: STATUS BITS AND THEIR SIGNIFICANCE FOR PIC16C62A/R62/63/64A/R64/65A

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{TO}$ is set on a Power-on Reset
0	x	x	0	Illegal, $\overline{PD}$ is set on a Power-on Reset
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{MCLR}$ reset during normal operation
1	1	1	0	$\overline{MCLR}$ reset during SLEEP or interrupt wake-up from SLEEP

Legend: x = unknown, u = unchanged

TABLE 13-10: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C61/62/64/65

	Program Counter	STATUS	PCON(2)
Power-on Reset	000h	0001 1xxx	---- --0-
$\overline{MCLR}$ reset during normal operation	000h	000u uuuu	---- --u-
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	---- --u-
WDT Reset	000h	0000 1uuu	---- --u-
WDT Wake-up	PC + 1	uuu0 0uuu	---- --u-
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.
2: The PCON register is not implemented on the PIC16C61.

TABLE 13-11: RESET CONDITION FOR SPECIAL REGISTERS ON PIC16C62A/R62/63/64A/R64/65A

	Program Counter	STATUS	PCON
Power-on Reset	000h	0001 1xxx	---- --0x
$\overline{MCLR}$ reset during normal operation	000h	000u uuuu	---- --uu
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

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TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices										Power-on Reset Brown-out Reset	MCLR Reset during: – normal operation – SLEEP WDT Reset	Wake-up via interrupt or WDT Wake-up
W	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	61	62	62A	R62	63	64	64A	R64	65	65A	N/A	N/A	N/A
TMR0	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	61	62	62A	R62	63	64	64A	R64	65	65A	0000h	0000h	PC + 1(2)
STATUS	61	62	62A	R62	63	64	64A	R64	65	65A	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	61	62	62A	R62	63	64	64A	R64	65	65A	---x xxxx	---u uuuu	---u uuuu
	61	62	62A	R62	63	64	64A	R64	65	65A	--xx xxxx	--uu uuuu	--uu uuuu
PORTB	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	61	62	62A	R62	63	64	64A	R64	65	65A	---- -xxx	---- -uuu	---- -uuu
PCLATH	61	62	62A	R62	63	64	64A	R64	65	65A	---0 0000	---0 0000	---u uuuu
INTCON	61	62	62A	R62	63	64	64A	R64	65	65A	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	61	62	62A	R62	63	64	64A	R64	65	65A	00-- 0000	00-- 0000	uu-- uuuu(1)
	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu(1)
PIR2	61	62	62A	R62	63	64	64A	R64	65	65A	---- ---0	---- ---0	---- ---u(2)
TMR1L	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	61	62	62A	R62	63	64	64A	R64	65	65A	--00 0000	--uu uuuu	--uu uuuu
TMR2	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu
T2CON	61	62	62A	R62	63	64	64A	R64	65	65A	-000 0000	-000 0000	-uuu uuuu
SSPBUF	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu
CCPR1L	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	61	62	62A	R62	63	64	64A	R64	65	65A	--00 0000	--00 0000	--uu uuuu
RCSTA	61	62	62A	R62	63	64	64A	R64	65	65A	0000 -00x	0000 -00x	uuuu -uuu
TXREG	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu
RCREG	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu
CCPR2L	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2H	61	62	62A	R62	63	64	64A	R64	65	65A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu
OPTION	61	62	62A	R62	63	64	64A	R64	65	65A	1111 1111	1111 1111	uuuu uuuu
TRISA	61	62	62A	R62	63	64	64A	R64	65	65A	---1 1111	---1 1111	---u uuuu
	61	62	62A	R62	63	64	64A	R64	65	65A	--11 1111	--11 1111	--uu uuuu
TRISB	61	62	62A	R62	63	64	64A	R64	65	65A	1111 1111	1111 1111	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

3: See Table 13-10 and Table 13-11 for reset value for specific conditions.

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TABLE 13-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Register	Applicable Devices										Power-on Reset Brown-out Reset	MCLR Reset during: – normal operation – SLEEP WDT Reset	Wake-up via interrupt or WDT Wake-up
TRISC	61	62	62A	R62	63	64	64A	R64	65	65A	1111 1111	1111 1111	uuuu uuuu
TRISD	61	62	62A	R62	63	64	64A	R64	65	65A	1111 1111	1111 1111	uuuu uuuu
TRISE	61	62	62A	R62	63	64	64A	R64	65	65A	0000 -111	0000 -111	uuuu -uuu
PIE1	61	62	62A	R62	63	64	64A	R64	65	65A	00-- 0000	00-- 0000	uu-- uuuu
	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu
PIE2	61	62	62A	R62	63	64	64A	R64	65	65A	---- ---0	---- ---0	---- ---u
PCON	61	62	62A	R62	63	64	64A	R64	65	65A	---- --0u	---- --uu	---- --uu
	61	62	62A	R62	63	64	64A	R64	65	65A	---- --0-	---- --u-	---- --u-
PR2	61	62	62A	R62	63	64	64A	R64	65	65A	1111 1111	1111 1111	1111 1111
SSPADD	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	61	62	62A	R62	63	64	64A	R64	65	65A	--00 0000	--00 0000	--uu uuuu
TXSTA	61	62	62A	R62	63	64	64A	R64	65	65A	0000 -010	0000 -010	uuuu -uuu
SPBRG	61	62	62A	R62	63	64	64A	R64	65	65A	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

3: See Table 13-10 and Table 13-11 for reset value for specific conditions.

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FIGURE 13-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 1

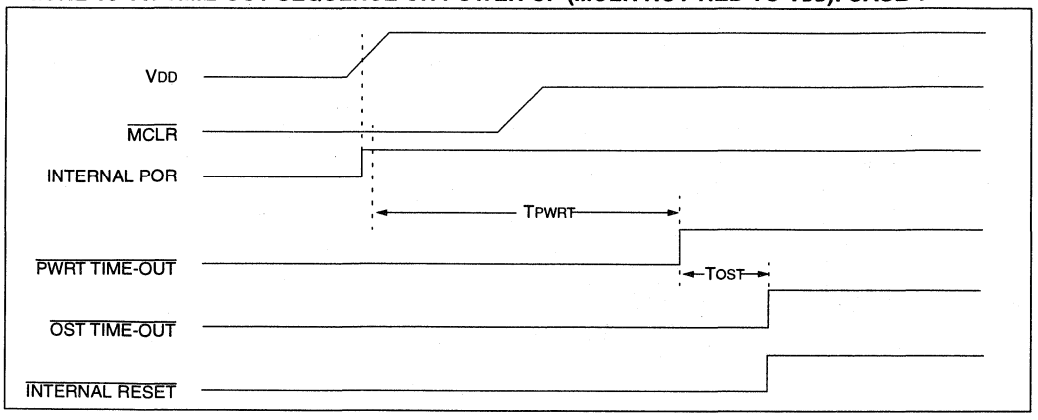

FIGURE 13-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 2

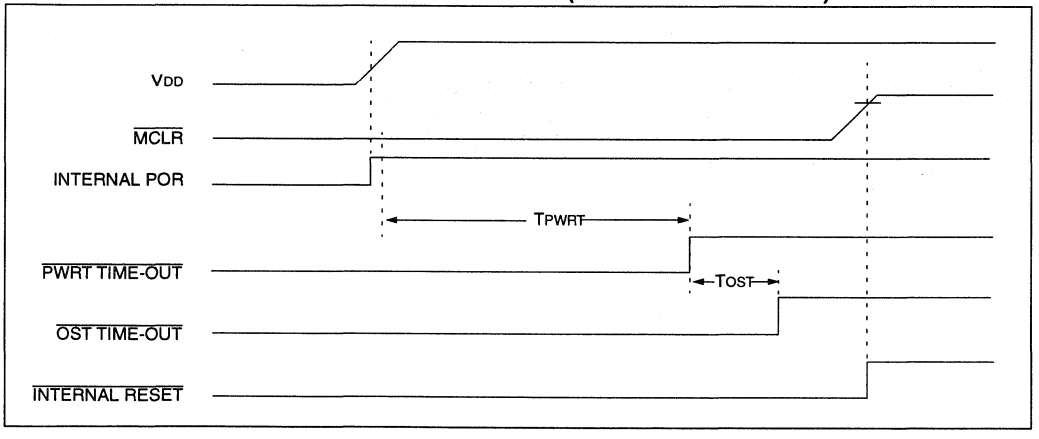

FIGURE 13-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD})

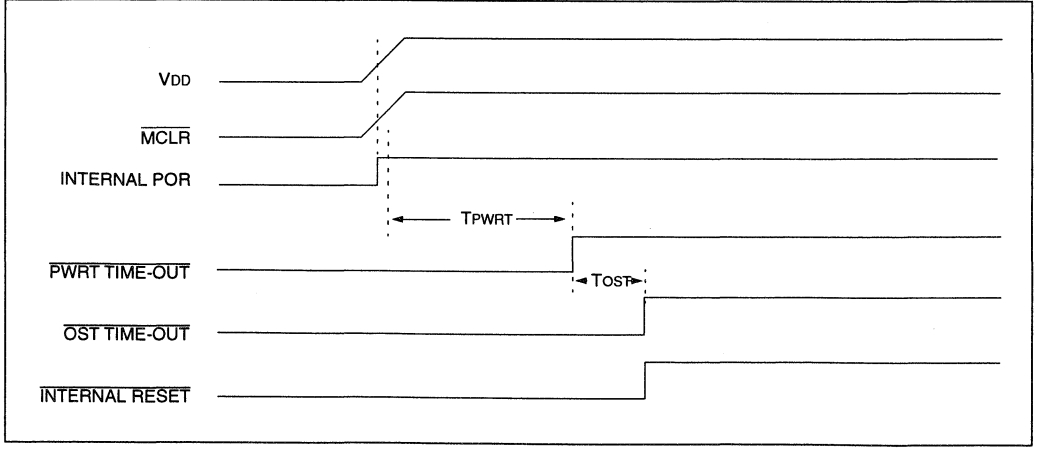

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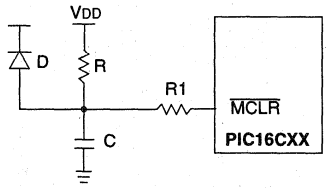
FIGURE 13-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

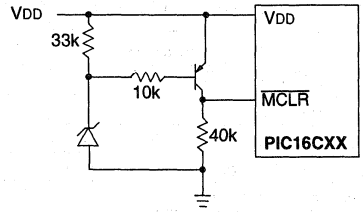


Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the devices electrical specifications.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrostatic Overstress (EOS).

FIGURE 13-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

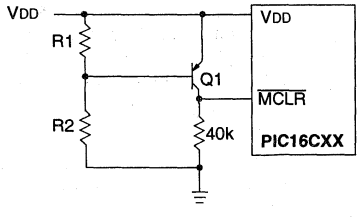


Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

2: Internal brown-out detection on the PIC16C62A/R62/63/64A/R64/65A should be disabled when using this circuit.

3: Resistors should be adjusted for the characteristics of the transistors.

FIGURE 13-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Internal brown-out detection on the PIC16C62A/R62/63/64A/R64/65A should be disabled when using this circuit.

3: Resistors should be adjusted for the characteristics of the transistors.

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13.5 Interrupts

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The PIC16C6X family has up to 11 sources of interrupt:

Interrupt Sources		Applicable Devices								
External interrupt RB0/INT	61	62	62A	R62	63	64	64A	R64	65	65A
TMR0 overflow interrupt	61	62	62A	R62	63	64	64A	R64	65	65A
PORTB change interrupt (pins RB7:RB4)	61	62	62A	R62	63	64	64A	R64	65	65A
TMR1 overflow interrupt	61	62	62A	R62	63	64	64A	R64	65	65A
TMR2 matches period interrupt	61	62	62A	R62	63	64	64A	R64	65	65A
CCP1 interrupt	61	62	62A	R62	63	64	64A	R64	65	65A
CCP2 interrupt	61	62	62A	R62	63	64	64A	R64	65	65A
USART Receive	61	62	62A	R62	63	64	64A	R64	65	65A
USART Transmit	61	62	62A	R62	63	64	64A	R64	65	65A
Synchronous serial port interrupt	61	62	62A	R62	63	64	64A	R64	65	65A
Parallel slave port read/write interrupt	61	62	62A	R62	63	64	64A	R64	65	65A

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or global enable bit, GIE.

Global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register. GIE is cleared on reset.

The "return from interrupt" instruction, `RETFIE`, exits the interrupt routine as well as sets the GIE bit, which re-enable interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flag bits are contained in the INTCON register.

The peripheral interrupt flag bits are contained in special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2 and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, bit GIE is cleared to disable any further interrupts, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the RB0/INT pin or RB port change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 13-20). The latency is the same for one or two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note: For the PIC16C61/62/64/65

If an interrupt occurs while the Global Interrupt Enable bit, GIE is being cleared, bit GIE may unintentionally be re-enabled by the user's Interrupt Service Routine (the `RETFIE` instruction). The events that would cause this to occur are:

1. An instruction clears the GIE bit while an interrupt is acknowledged
2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the `RETFIE` instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.
4. Perform the following to ensure that interrupts are globally disabled.

```
LOOP BCF INTCON,GIE     ;Disable Global
                        ;Interrupt bit
     BTFSC INTCON,GIE   ;Global Interrupt
                        ;Disabled?
     GOTO  LOOP         ;NO, try again
     :                  ;Yes, continue
                        ;with program flow
```


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FIGURE 13-17: INTERRUPT LOGIC FOR PIC16C61

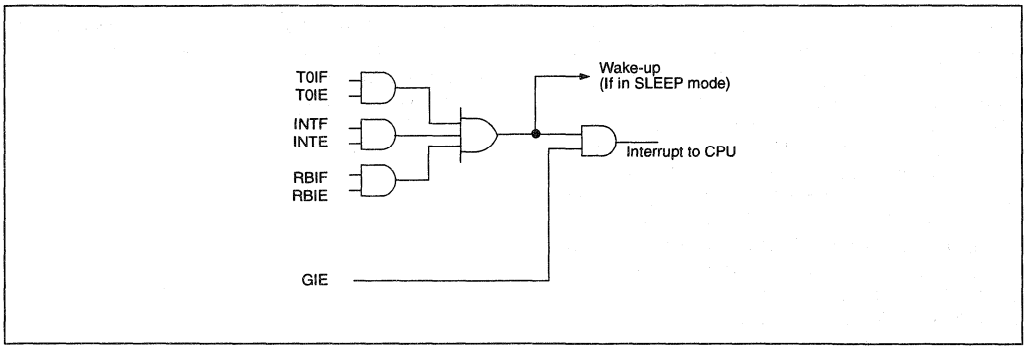


FIGURE 13-18: INTERRUPT LOGIC FOR PIC16C62/62A/R62/63

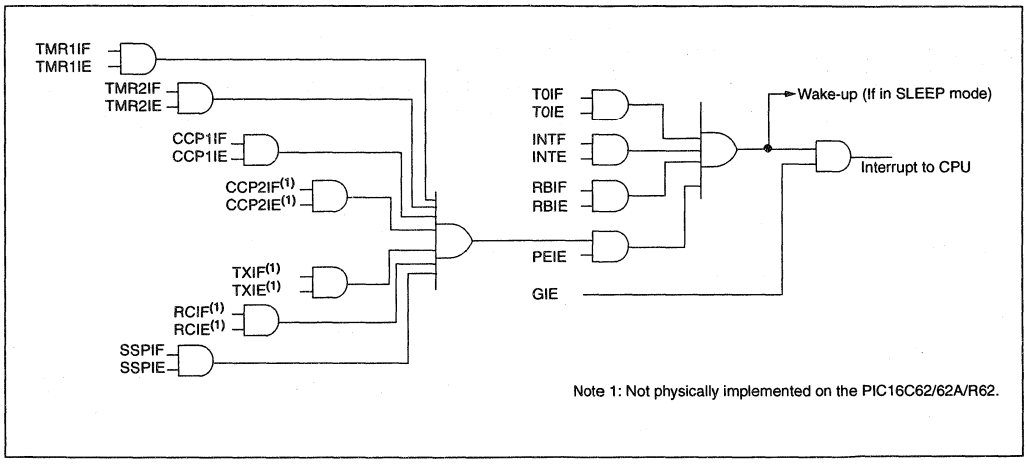
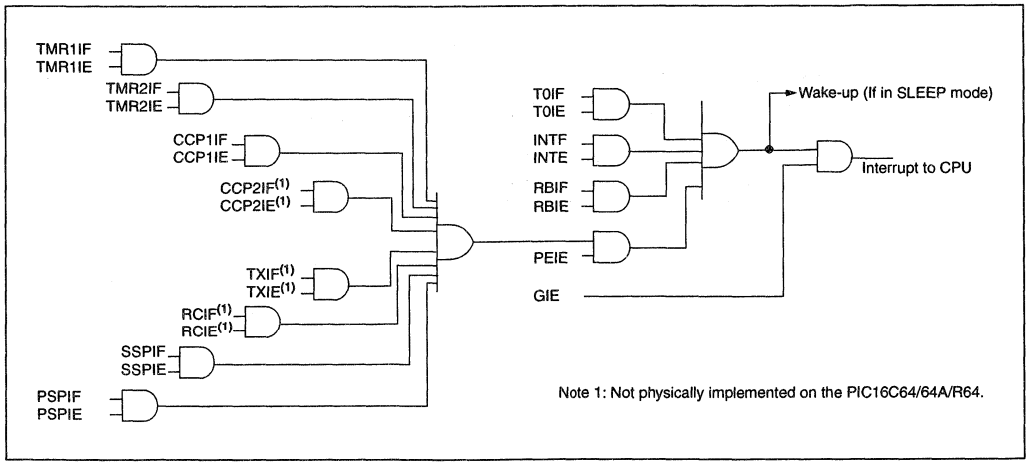


FIGURE 13-19: INTERRUPT LOGIC FOR PIC16C64/64A/R64/65/65A



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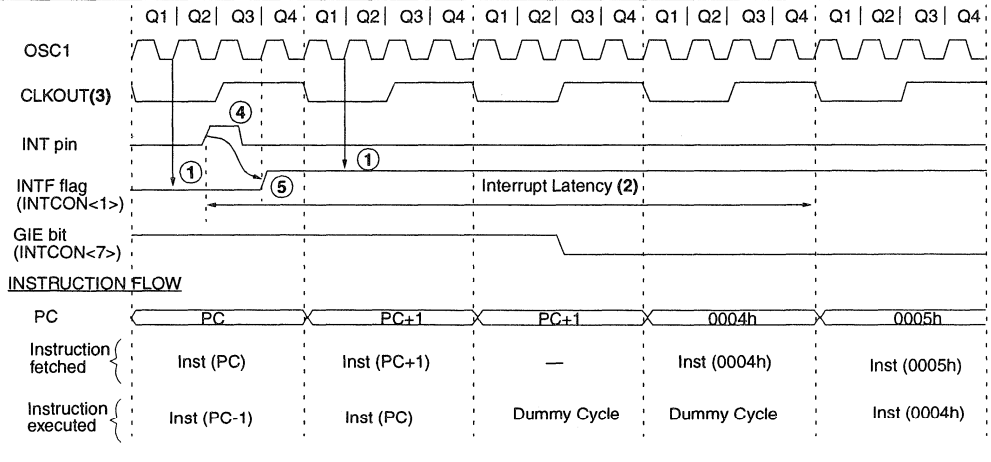
13.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if edge select bit INTEDG (OPTION<6>) is set, or falling, if bit INTEDG is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP, if enable bit INTE was set prior to going into SLEEP. The status of global enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 13.8 for details on SLEEP mode.

13.5.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 7.0).

FIGURE 13-20: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4Tcy where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width spec of INT pulse, refer to AC specs.
5: INTF can to be set anytime during the Q4-Q1 cycles.

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13.5.3 PORTB INTERRUPT ON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>) (Section 5.2).

Note: For the PIC16C61/62/64/65 if a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then flag bit RBIF may not get set.

13.6 Context Saving During Interrupts

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 13-1 and Example 13-2 store and restore the STATUS and W registers. For all PIC16C6X devices with greater than 1K of program memory (all devices except PIC16C61), the register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1).

The examples:

a) Stores the W register.
b) Stores the STATUS register in bank 0.
c) Executes ISR code.
d) Restores STATUS register (and bank select bit).
e) Restores W register.

EXAMPLE 13-1: SAVING STATUS AND W REGISTERS IN RAM (PIC16C61)

```
MOVWF    W_TEMP           ;Copy W to TEMP register, could be bank one or zero
SWAPF    STATUS,W         ;Swap status to be saved into W
MOVWF    STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF    STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                          ;(sets bank to original state)
MOVWF    STATUS           ;Move W into STATUS register
SWAPF    W_TEMP,F         ;Swap W_TEMP
SWAPF    W_TEMP,W         ;Swap W_TEMP into W
```

EXAMPLE 13-2: SAVING STATUS AND W REGISTERS IN RAM (PIC16C62/62A/R62/63/64/64A/R64/65/65A)

```
MOVWF    W_TEMP           ;Copy W to TEMP register, could be bank one or zero
SWAPF    STATUS,W         ;Swap status to be saved into W
BCF      STATUS,RP0       ;Change to bank zero, regardless of current bank
MOVWF    STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF    STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                          ;(sets bank to original state)
MOVWF    STATUS           ;Move W into STATUS register
SWAPF    W_TEMP,F         ;Swap W_TEMP
SWAPF    W_TEMP,W         ;Swap W_TEMP into W
```


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13.7 Watchdog Timer (WDT)

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device reset. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (WDT Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 13.1).

13.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

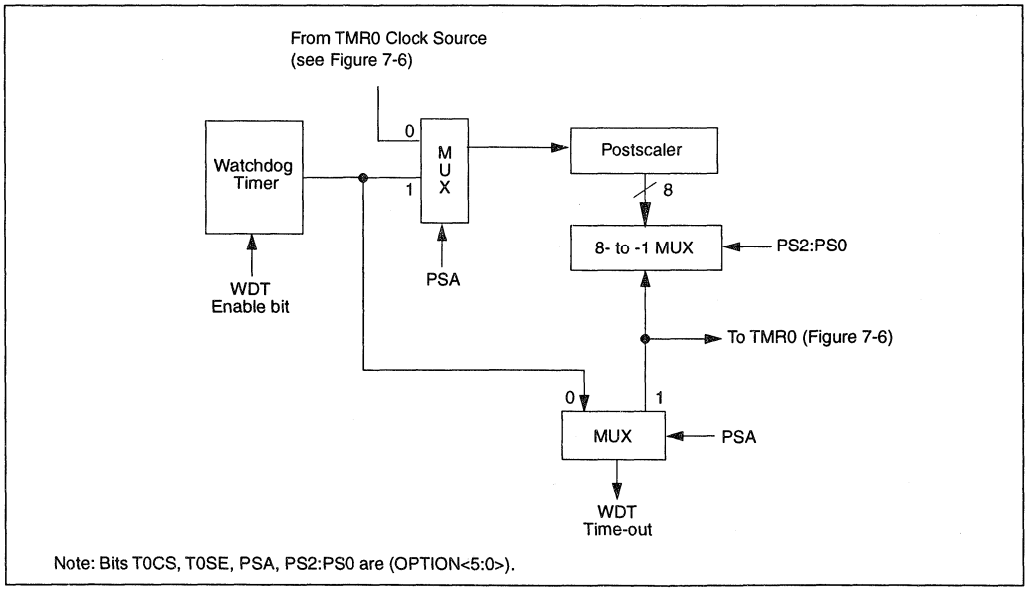
The $\overline{TO}$ bit in the STATUS register will be cleared upon a WDT time-out.

13.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When the prescaler is assigned to the WDT, always execute a CLRWDT instruction before changing the prescale value, otherwise a WDT reset may occur.

FIGURE 13-21: WATCHDOG TIMER BLOCK DIAGRAM



Note: Bits T0CS, T0SE, PSA, PS2:PS0 are (OPTION<5:0>).

FIGURE 13-22: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN(1)	CP1	CP0	PWRTE(1)	WDTE	FOSC1	FOSC0
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 13-1, Figure 13-2, and Figure 13-3 for details of these bits for the specific device.

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13.8 Power-down Mode (SLEEP)

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, status bit $\overline{PD}$ (STATUS<3>) is cleared, status bit $\overline{TO}$ (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or VSS, ensure no external circuitry is drawing current from the I/O pin, and disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC).

13.8.1 WAKE-UP FROM SLEEP

The device can wake from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$/VPP pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or some peripheral interrupts.

External $\overline{MCLR}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. SSP (Start/Stop) bit detect interrupt.
3. SSP transmit or receive in slave mode (SPI/I^2C).
4. CCP capture mode interrupt.
5. Parallel Slave Port read or write.
6. USART TX or RX (synchronous slave mode).

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

13.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep . The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

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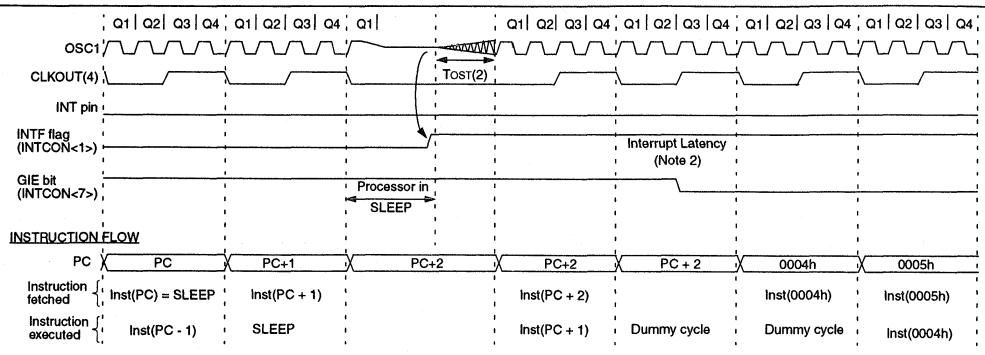
FIGURE 13-23: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.

2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.

3: GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these osc modes, but shown here for timing reference.

13.9 Program Verification/Code Protection

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A	

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

13.10 ID Locations

Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A	

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

For ROM devices, these values are submitted along with the ROM code.

13.11 In-Circuit Serial Programming

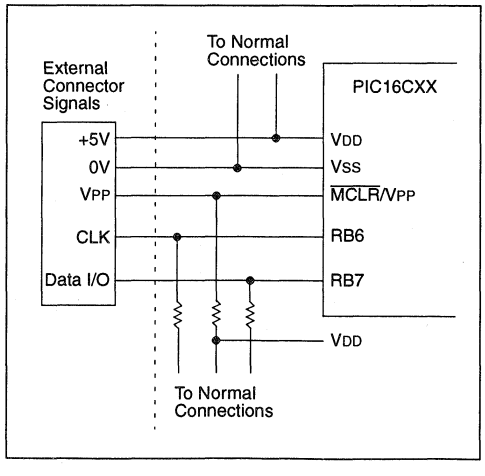
Applicable Devices										
61	62	62A	R62	63	64	64A	R64	65	65A	

The PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding pins RB6 and RB7 low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device in program/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

FIGURE 13-24: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



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Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A |

14.0 ELECTRICAL CHARACTERISTICS FOR PIC16C61

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V

Total power dissipation (Note 1) ..... 800 mW

Maximum current out of VSS pin ..... 150 mA

Maximum current into VDD pin ..... 100 mA

Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 20 mA

Maximum current sunk by PORTA ..... 80 mA

Maximum current sourced by PORTA ..... 50 mA

Maximum current sunk by PORTB ..... 150 mA

Maximum current sourced by PORTB ..... 100 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 14-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C61-04	PIC16C61-20	PIC16LC61-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.0 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 15 µA typ. at 32 kHz, 4.0V IPD: 0.6 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 9 µA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 9 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

14.1 DC Characteristics: PIC16C61-04 (Commercial, Industrial, Automotive) PIC16C61-20 (Commercial, Industrial, Automotive)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration (PIC16C61-20) FOSC = 20 MHz, VDD = 5.5V
D020	Power-down Current (Note 3)	IPD	-	7	28	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.0	14	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.0	16	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			-	1.0	20	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

14.2 DC Characteristics: PIC16LC61-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	3.0	-	6.0	V	XT, RC, and LP osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	1.4	2.5	mA	FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	15	32	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP osc configuration
D020	Power-down Current (Note 3)	IPD	-	5	20	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.6	9	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.6	12	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

14.3 DC Characteristics: PIC16C61-04 (Commercial, Industrial, Automotive)
PIC16C61-20 (Commercial, Industrial, Automotive)
PIC16LC61-04 (Commercial, Industrial, Automotive)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 14.1 and Section 14.2.

Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		Vss	-	0.8V	V	
D031	with Schmitt Trigger buffer		Vss	-	0.2VDD	V	
D032	$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		0.36VDD	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.45VDD	-	VDD		For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.85VDD	-	VDD	V	For entire VDD range
D042	$\overline{MCLR}$, RA4/T0CKI		0.85VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	† 400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 14.1 and Section 14.2.

Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

14.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

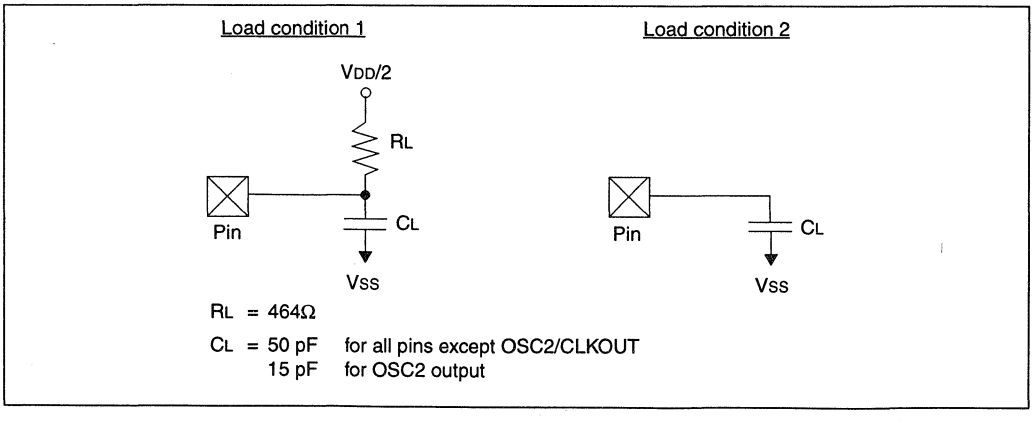
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 14-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

14.5 Timing Diagrams and Specifications

FIGURE 14-2: EXTERNAL CLOCK TIMING

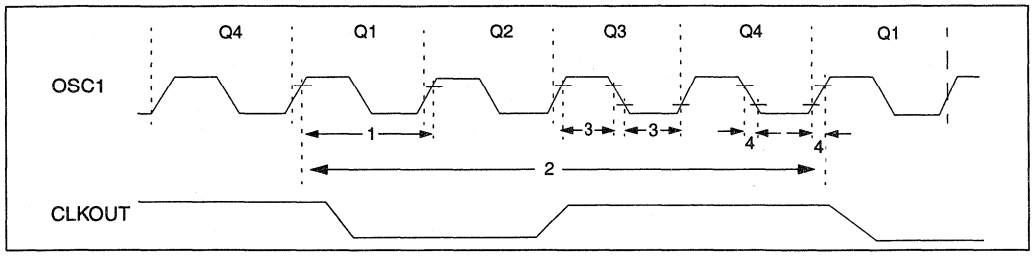

TABLE 14-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C61-04,
			DC	—	20	MHz	HS osc mode (PIC16C61-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			1	—	4	MHz	HS osc mode (PIC16C61-04,
			1	—	20	MHz	HS osc mode (PIC16C61-20)
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C61-04,
			50	—	—	ns	HS osc mode (PIC16C61-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	1,000	ns	HS osc mode (PIC16C61-04,
			50	—	1,000	ns	HS osc mode (PIC16C61-20)
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	1.0	TCY	DC	µs	Tcy = 4/Fosc
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	50	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			10	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	25	—	—	ns	XT oscillator
			50	—	—	ns	LP oscillator
			15	—	—	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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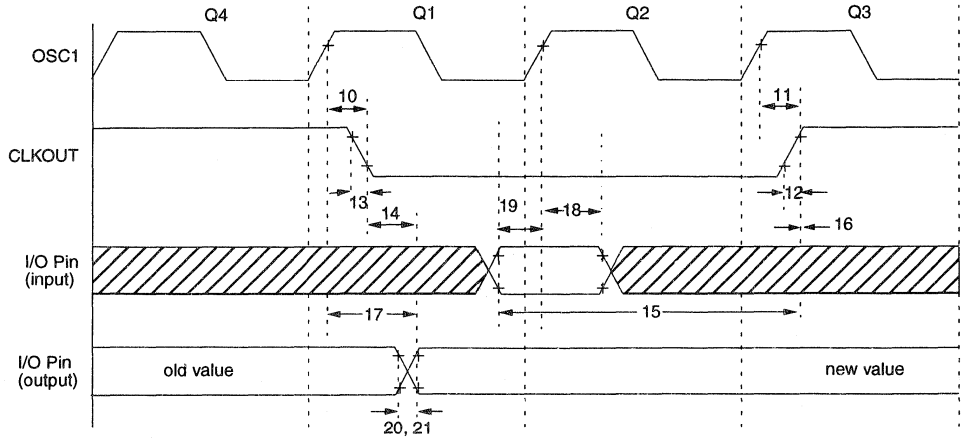
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 14-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 14-1 for load conditions.

TABLE 14-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time		—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	—	80 - 100	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		TBD	—	—	ns	
20*	TioR	Port output rise time	PIC16C61	—	10	25	ns	
			PIC16LC61	—	—	60	ns	
21*	TioF	Port output fall time	PIC16C61	—	10	25	ns	
			PIC16LC61	—	—	60	ns	
22††*	Tinp	RB0/INT pin high or low time		20	—	—	ns	
23††*	Trbp	RB7:RB4 change int high or low time		20	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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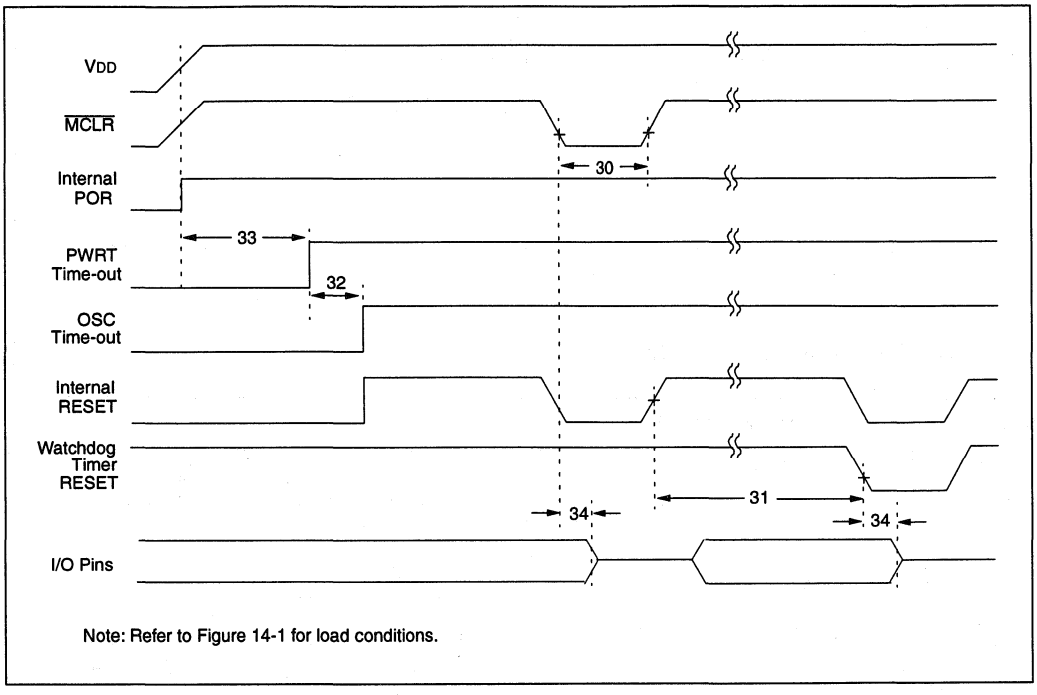
Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 14-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 14-1 for load conditions.

TABLE 14-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	$\overline{MCLR}$ Pulse Width (low)	200	—	—	ns	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—		TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34*	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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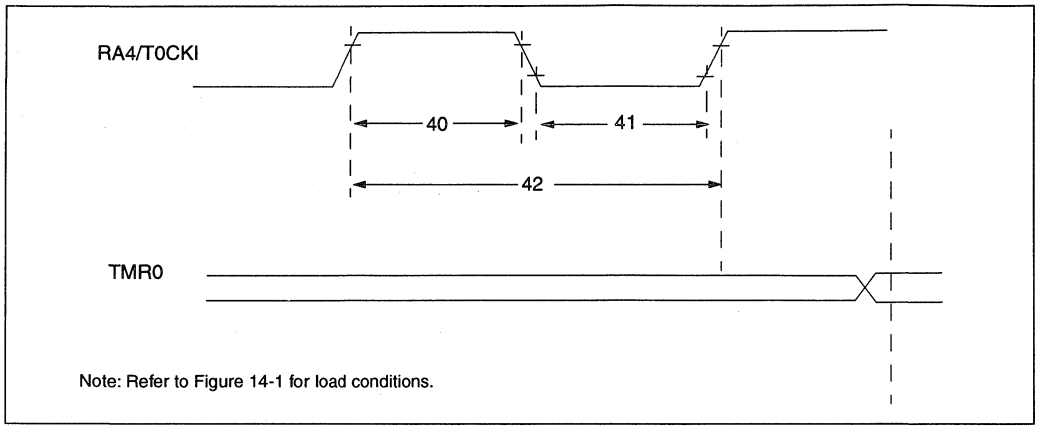
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 14-5: TIMER0 CLOCK TIMINGS



Note: Refer to Figure 14-1 for load conditions.

TABLE 14-5: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		Greater of: 20 µs or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

15.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C61

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 15-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

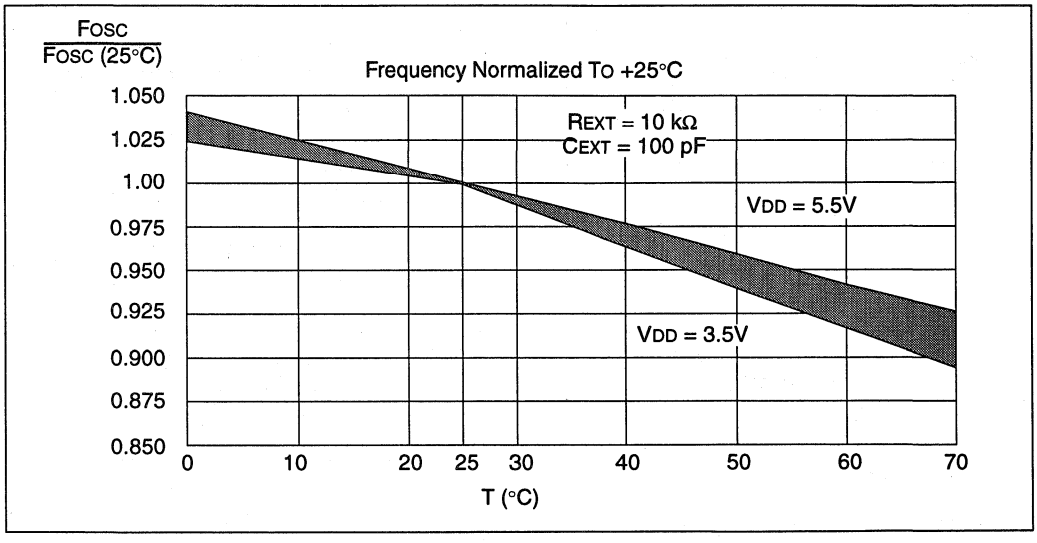

TABLE 15-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20 pF	4.7k	4.52 MHz	± 17.35%
	10k	2.47 MHz	± 10.10%
	100k	290.86 kHz	± 11.90%
100 pF	3.3k	1.92 MHz	± 9.43%
	4.7k	1.48 MHz	± 9.83%
	10k	788.77 kHz	± 10.92%
	100k	88.11 kHz	± 16.03%
300 pF	3.3k	726.89 kHz	± 10.97%
	4.7k	573.95 kHz	± 10.14%
	10k	307.31 kHz	± 10.43%
	100k	33.82 kHz	± 11.24%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

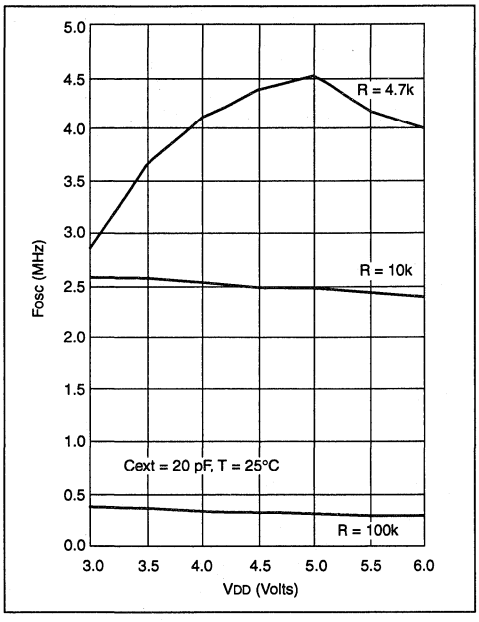


FIGURE 15-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

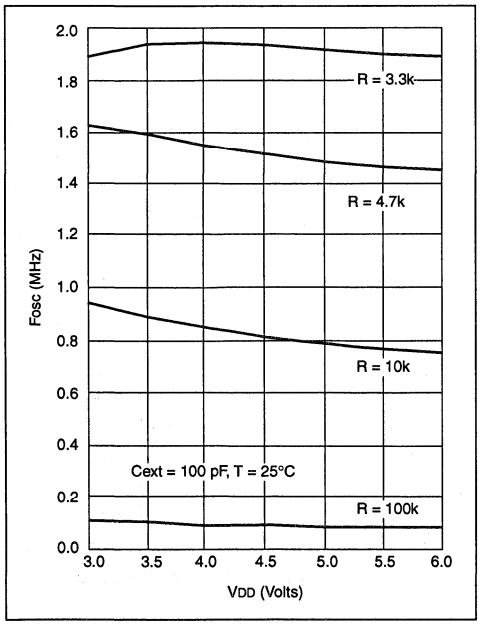


FIGURE 15-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

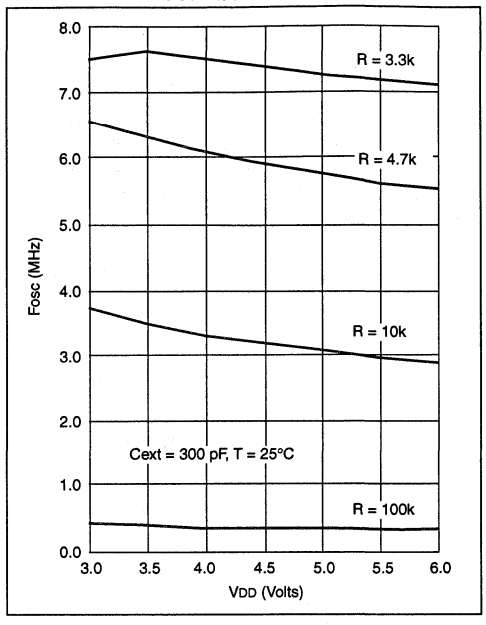
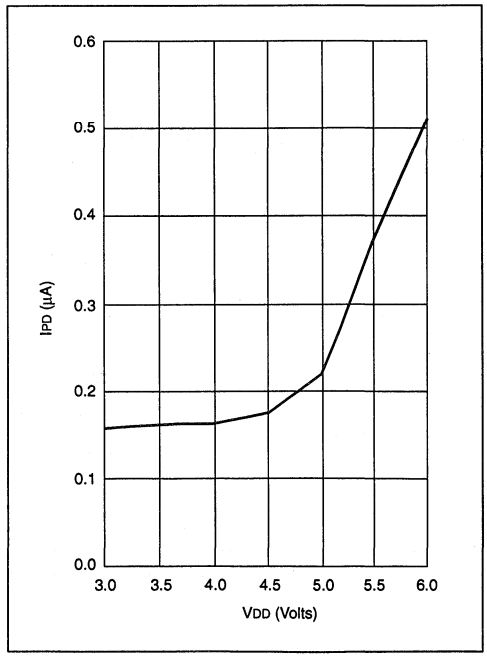


FIGURE 15-5: TYPICAL IPD vs. VDD WATCHDOG TIMER DISABLED 25°C



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-6: TYPICAL IPD VS. VDD WATCHDOG TIMER ENABLED 25°C

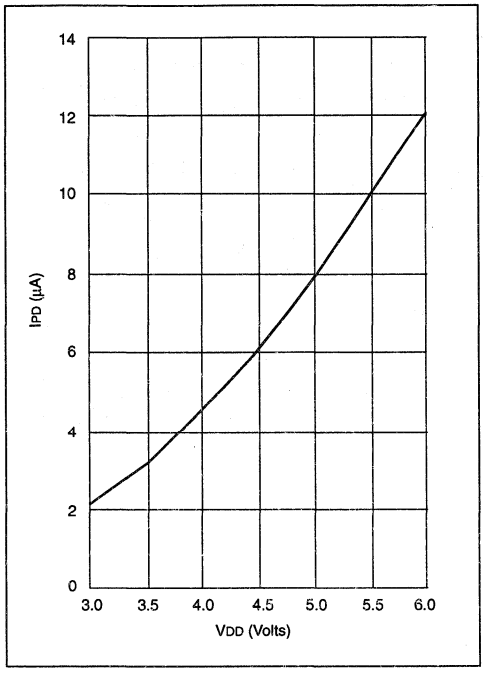
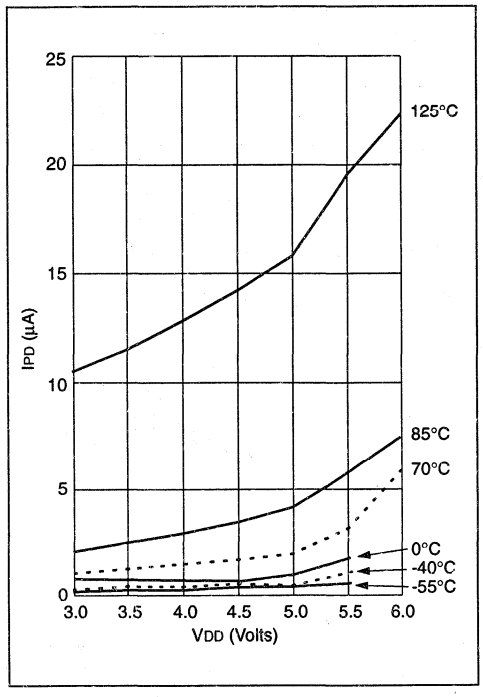


FIGURE 15-7: MAXIMUM IPD VS. VDD WATCHDOG DISABLED



Data based on matrix samples. See first page of this section for details.

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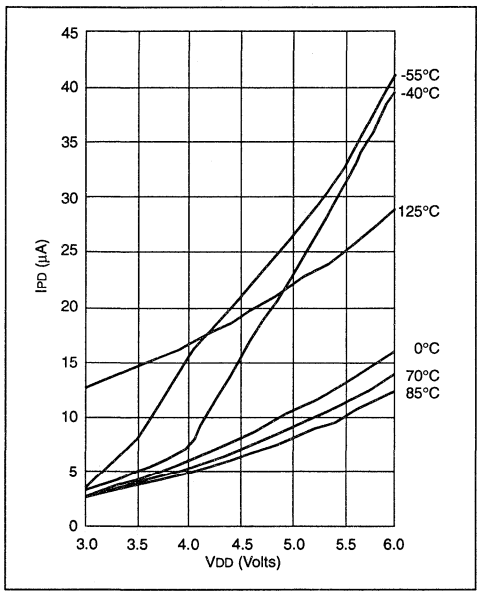
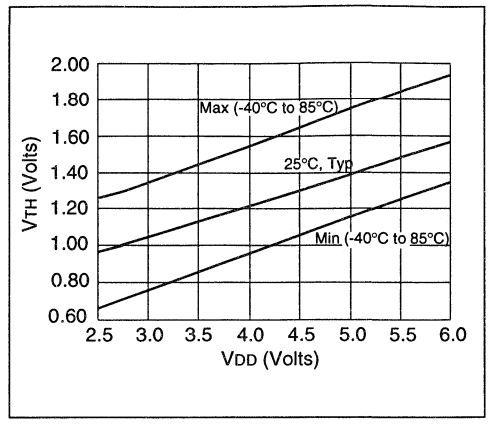
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-8: MAXIMUM IPD VS. VDD WATCHDOG ENABLED*



*IPD, with Watchdog Timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the Watchdog Timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 15-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS VS. VDD



Data based on matrix samples. See first page of this section for details.

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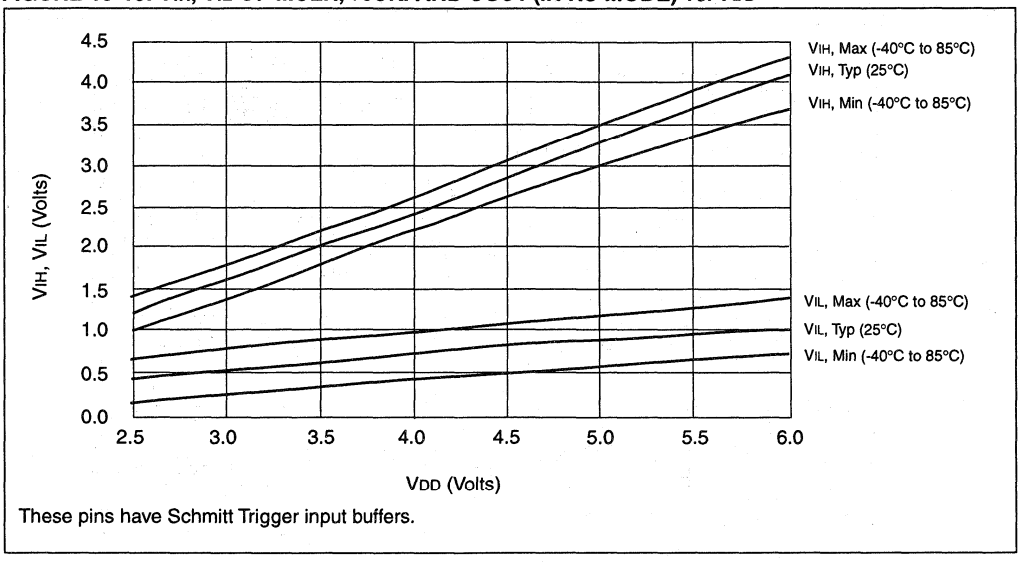
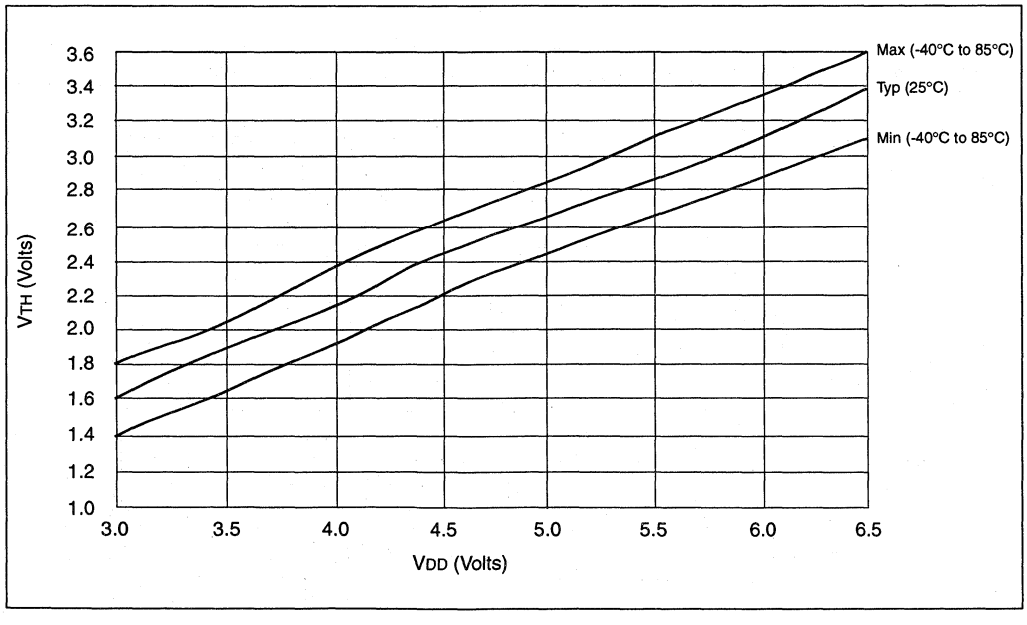
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-10: VIH, VIL OF $\overline{MCLR}$, T0CKI AND OSC1 (IN RC MODE) VS. VDD



These pins have Schmitt Trigger input buffers.

FIGURE 15-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) VS. VDD



Data based on matrix samples. See first page of this section for details.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-12: TYPICAL IDD vs. FREQUENCY (EXTERNAL CLOCK, 25°C)

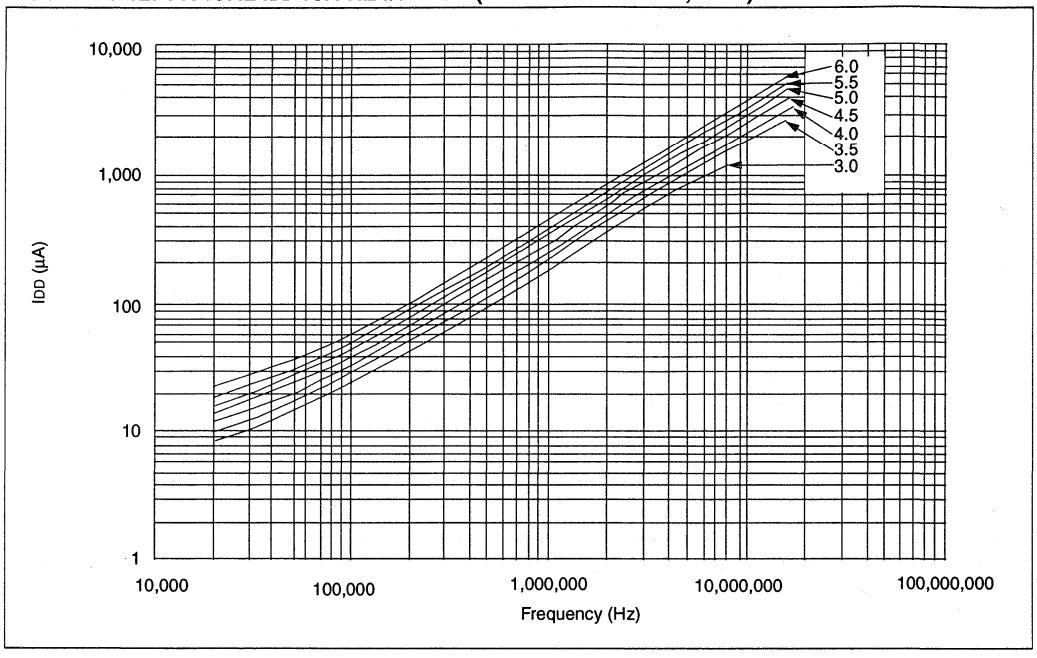
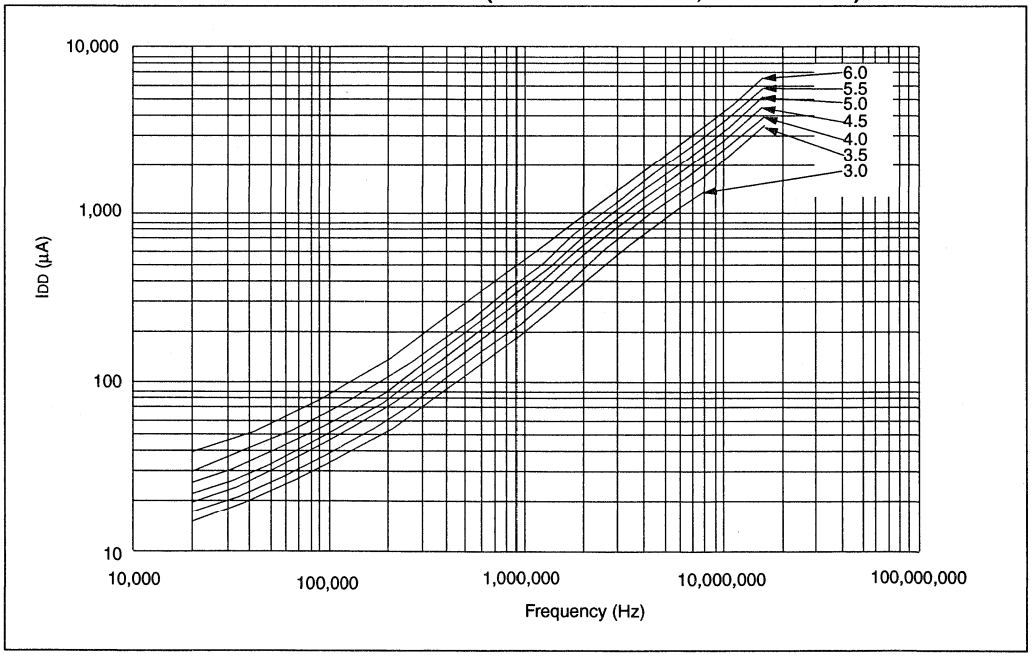


FIGURE 15-13: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK, -40° TO +85°C)



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-14: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, -55° TO +125°C)

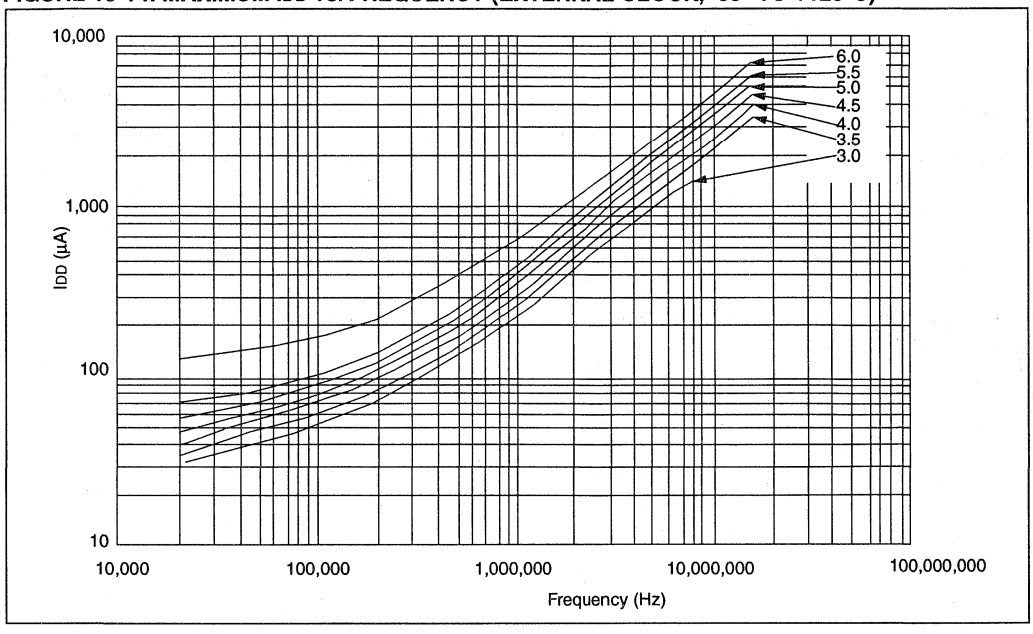


FIGURE 15-15: WDT TIMER TIME-OUT PERIOD VS. VDD

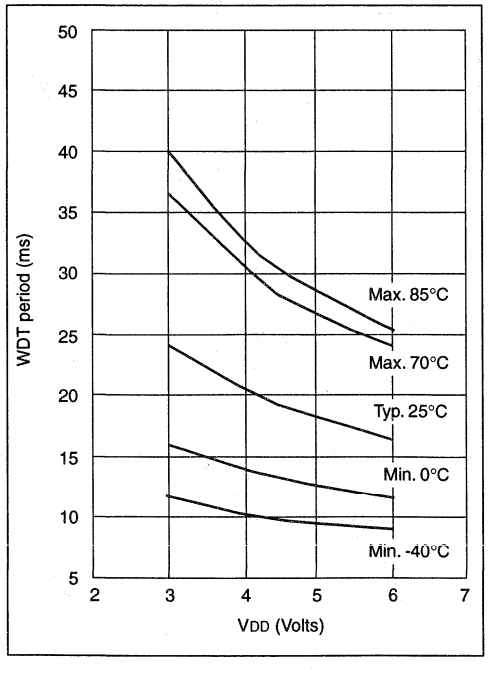
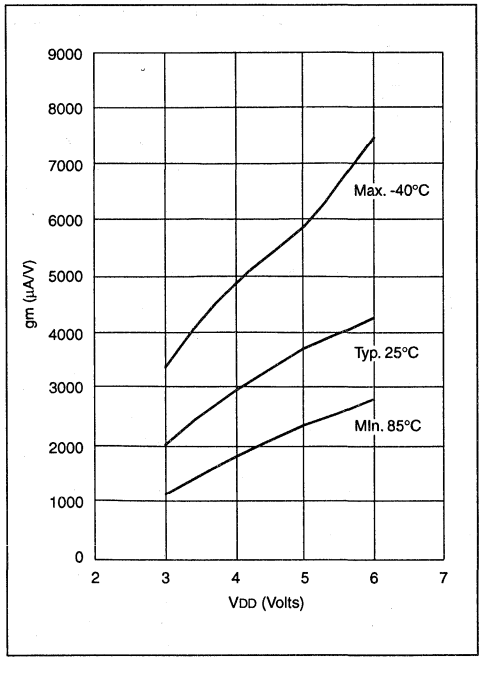


FIGURE 15-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR VS. VDD



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

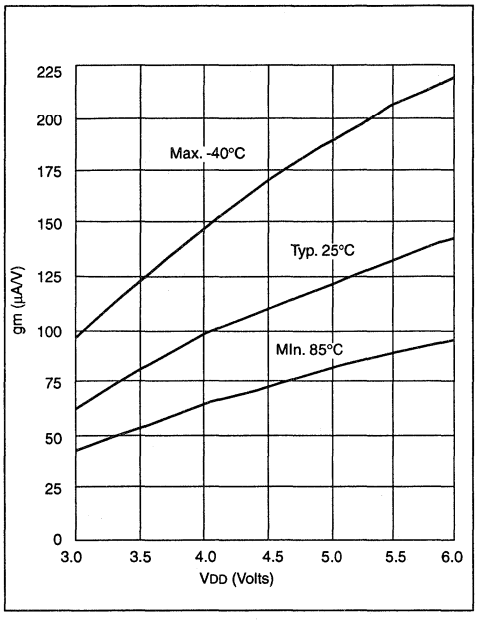


FIGURE 15-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

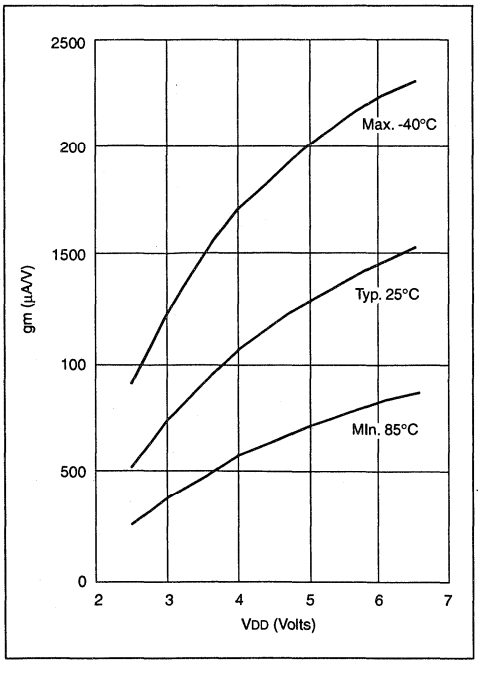


FIGURE 15-19: IOH vs. VOH, VDD = 3V

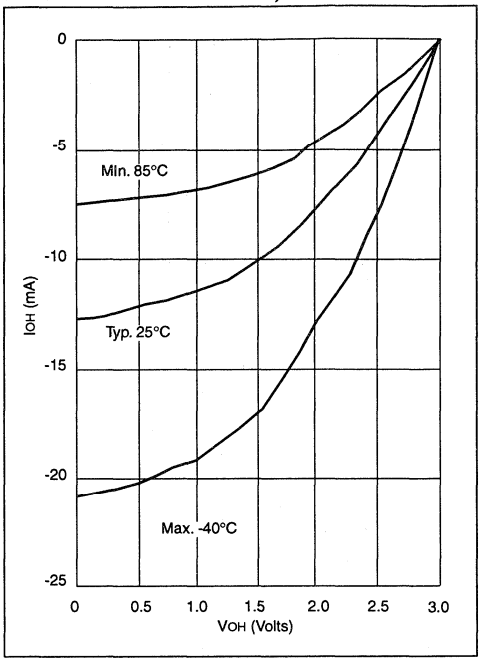
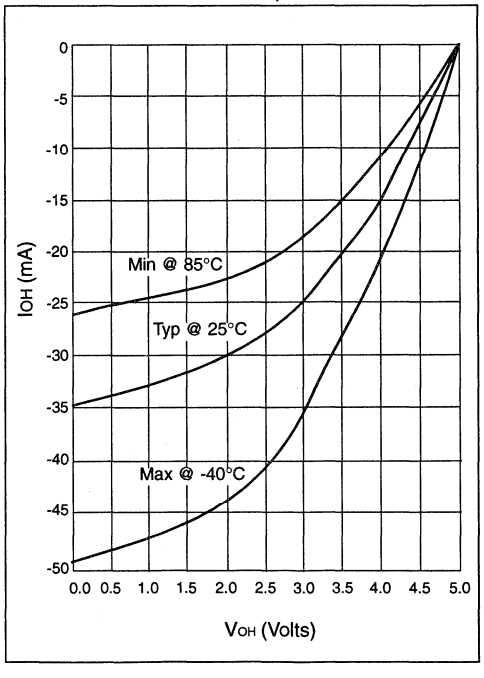


FIGURE 15-20: IOH vs. VOH, VDD = 5V



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 15-21: IOL VS. VOL, VDD = 3V

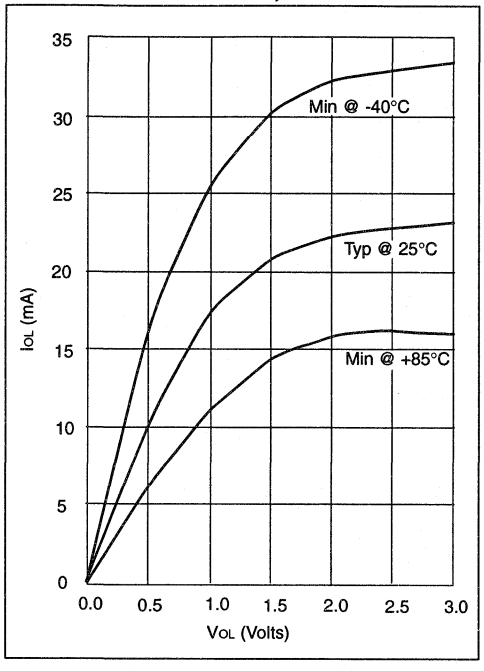

FIGURE 15-22: IOL VS. VOL, VDD = 5V

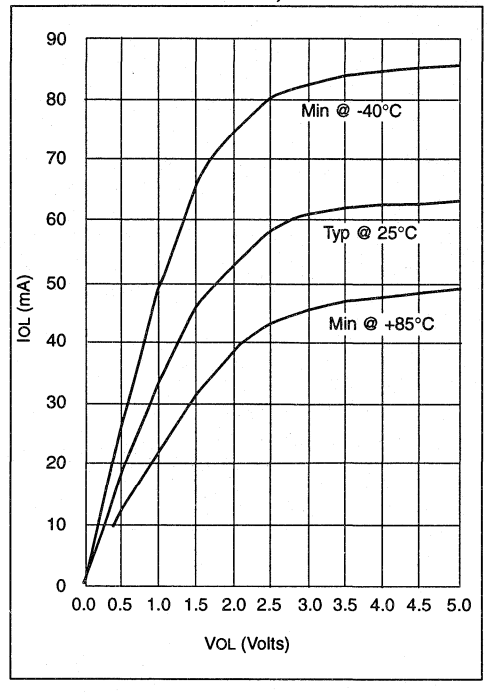

TABLE 15-2: INPUT CAPACITANCE*

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1/CLKIN	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

*All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

Data based on matrix samples. See first page of this section for details.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

NOTES:

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

16.0 ELECTRICAL CHARACTERISTICS FOR PIC16C62/64

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V
Total power dissipation (Note 1) 1.0W
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin ..... 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA, PORTB, and PORTE* (combined) ..... 200 mA
Maximum current sourced by PORTA, PORTB, and PORTE* (combined) ..... 200 mA
Maximum current sunk by PORTC and PORTD* (combined) ..... 200 mA
Maximum current sourced by PORTC and PORTD* (combined) ..... 200 mA

* PORTD and PORTE not available on the PIC16C62.

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 16-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C62-04 PIC16C64-04	PIC16C62-10 PIC16C64-10	PIC16C62-20 PIC16C64-20	PIC16LC62-04 PIC16LC64-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 µA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq:4 MHz max.	VDD: 3.0V to 6.0V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 µA max. at 4V Freq:4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 µA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq:4 MHz max.	VDD: 3.0V to 6.0V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3.0V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 21 µA max. at 4V Freq:4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq:200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq:200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq:200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

16.1 DC Characteristics: PIC16C62-04, PIC16C64-04 (Commercial, Industrial) PIC16C62-10, PIC16C64-10 (Commercial, Industrial) PIC16C62-20, PIC16C64-20 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2, 5)	IDD	-	2.7	5.0	mA	XT, RC, osc configuration (PIC16C62/64-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration (PIC16C62/64-20) FOSC = 20 MHz, VDD = 5.5V
D020	Power-down Current (Note 3, 5)	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.5	21	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.5	24	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

16.2 DC Characteristics: PIC16LC62-04, PIC16LC64-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	3.0	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2, 5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-down Current (Note 3, 5)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	13.5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	18	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

9

Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

16.3 DC Characteristics: PIC16C62-04, PIC16C64-04 (Commercial, Industrial) PIC16C62-10, PIC16C64-10 (Commercial, Industrial) PIC16C62-20, PIC16C64-20 (Commercial, Industrial) PIC16LC62-04, PIC16LC64-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 16.1 and Section 16.2				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI,OSC1 (in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH					
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD		For entire VDD range
D042	MCLR, RA4/T0CKI, RC7:RC4, RD7:RD4, RB0/INT		0.8VDD	-	VDD	V	
D042A	RE2:RE0, OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	200	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 16.1 and Section 16.2				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	
D102	SCL, SDA in I^2C mode	CB	-	-	400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

16.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

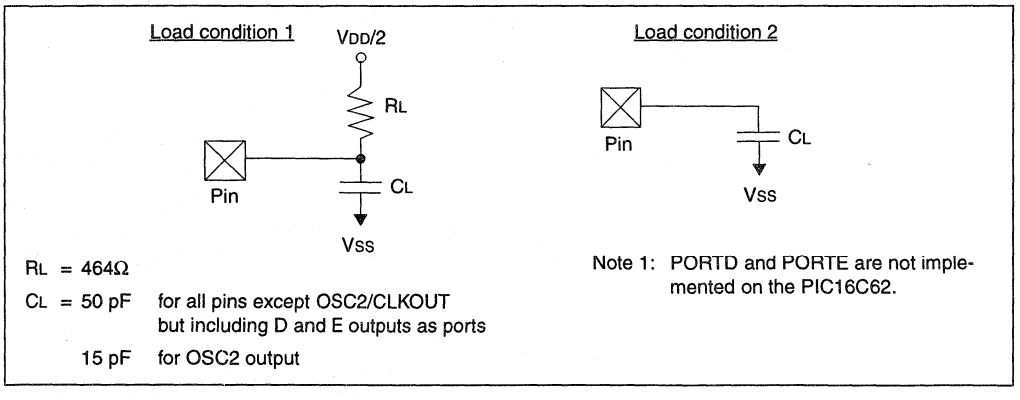
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 16-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



RL = 464Ω

CL = 50 pF for all pins except OSC2/CLKOUT but including D and E outputs as ports

15 pF for OSC2 output

Note 1: PORTD and PORTE are not implemented on the PIC16C62.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

16.5 Timing Diagrams and Specifications

FIGURE 16-2: EXTERNAL CLOCK TIMING

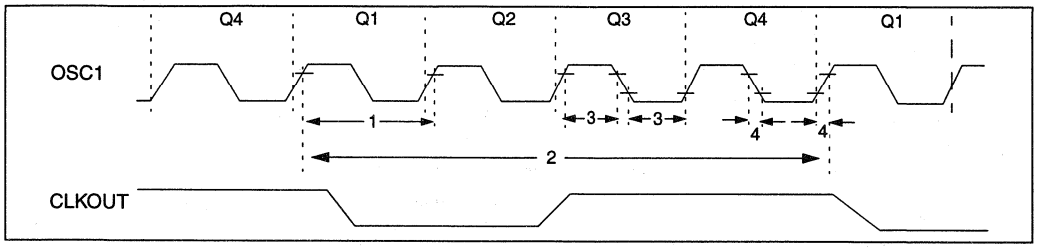

TABLE 16-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C62/64-04,
			DC	—	20	MHz	HS osc mode (PIC16C62/64-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C62/64-04,
			4	—	10	MHz	HS osc mode (PIC16C62/64-10)
			4	—	20	MHz	HS osc mode (PIC16C62/64-20)
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C62/64-04,
			100	—	—	ns	HS osc mode (PIC16C62/64-10)
			50	—	—	ns	HS osc mode (PIC16C62/64-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C62/64-04,
			100	—	250	ns	HS osc mode (PIC16C62/64-10)
			50	—	1,000	ns	HS osc mode (PIC16C62/64-20)
			5	—	—	µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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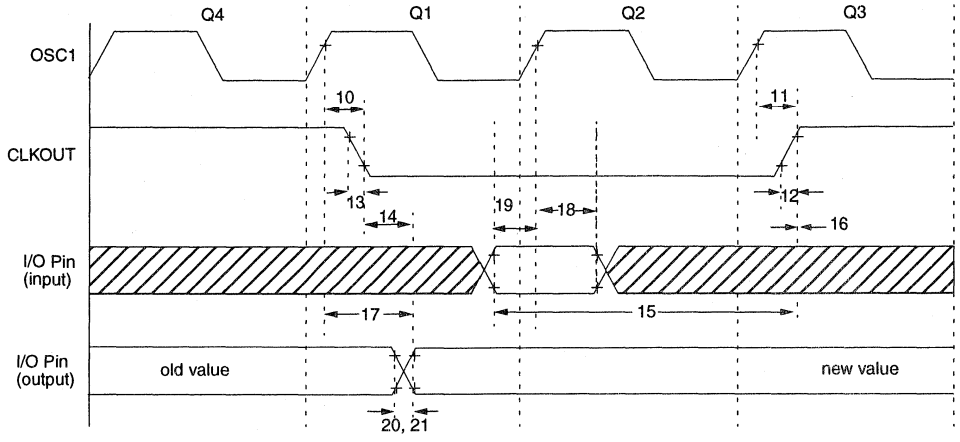
Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 16-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 16-1 for load conditions.

TABLE 16-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameters	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		TOSC + 200	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C62/64	100	—	—	ns	
			PIC16LC62/64	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C62/64	—	10	40	ns	
			PIC16LC62/64	—	—	80	ns	
21*	TioF	Port output fall time	PIC16C62/64	—	10	40	ns	
			PIC16LC62/64	—	—	80	ns	
22††*	Tinp	INT pin high or low time		Tcy	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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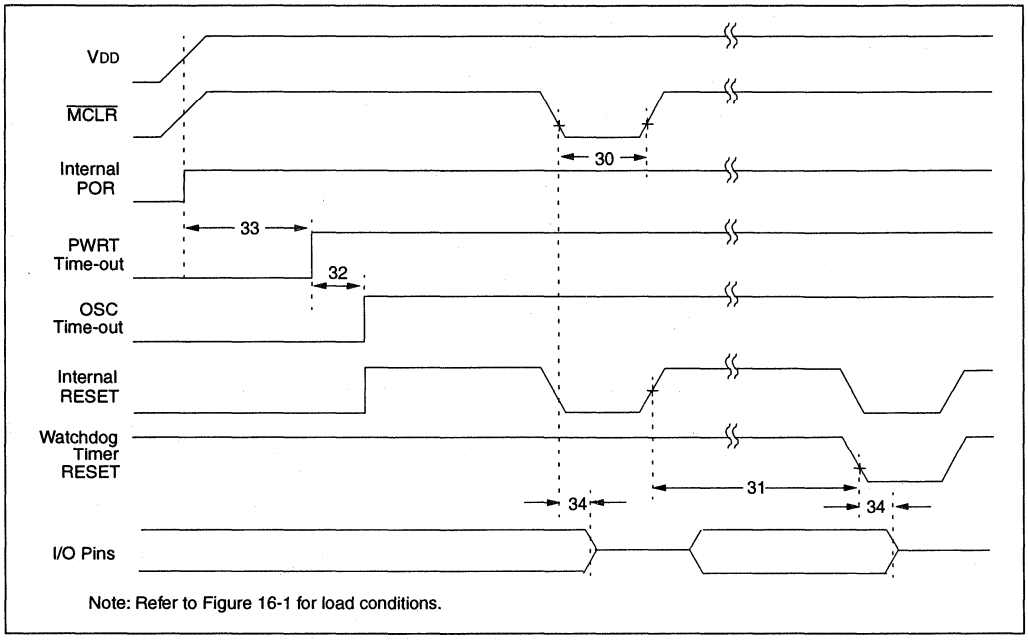
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 16-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 16-1 for load conditions.

TABLE 16-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	$\overline{MCLR}$ Pulse Width (low)	100	—	—	ns	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34*	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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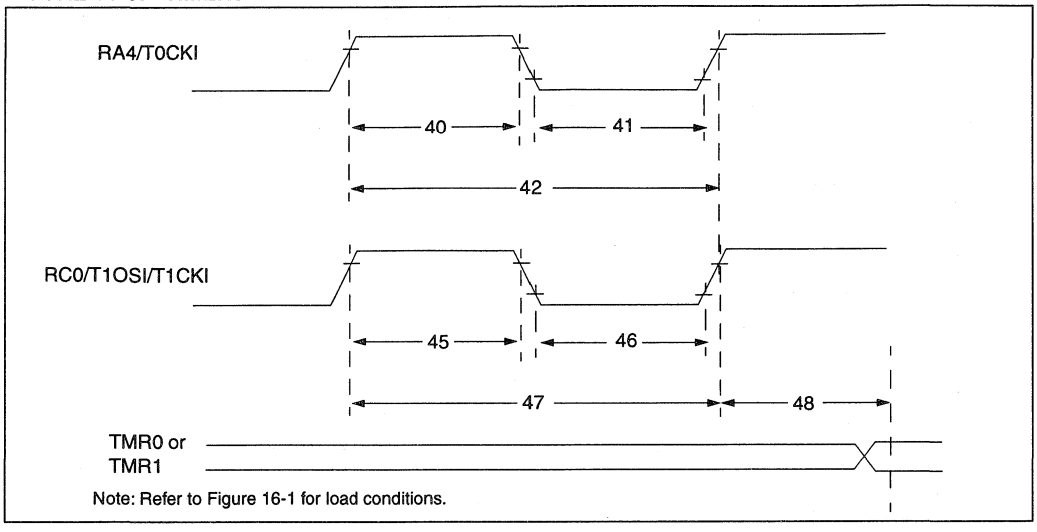
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 16-5: TIMER0 AND TIMER1 CLOCK TIMINGS



Note: Refer to Figure 16-1 for load conditions.

TABLE 16-5: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		Greater of: 20 µs or TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler	0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler PIC16C62/64	15	—	—	ns	
			Synchronous, With Prescaler PIC16LC62/64	25	—	—	ns	
			Asynchronous	2TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler	0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler PIC16C62/64	15	—	—	ns	
			Synchronous, With Prescaler PIC16LC62/64	25	—	—	ns	
			Asynchronous	2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous	Greater of: 20 µs or TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	Greater of: 20 µs or 4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)		DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment		2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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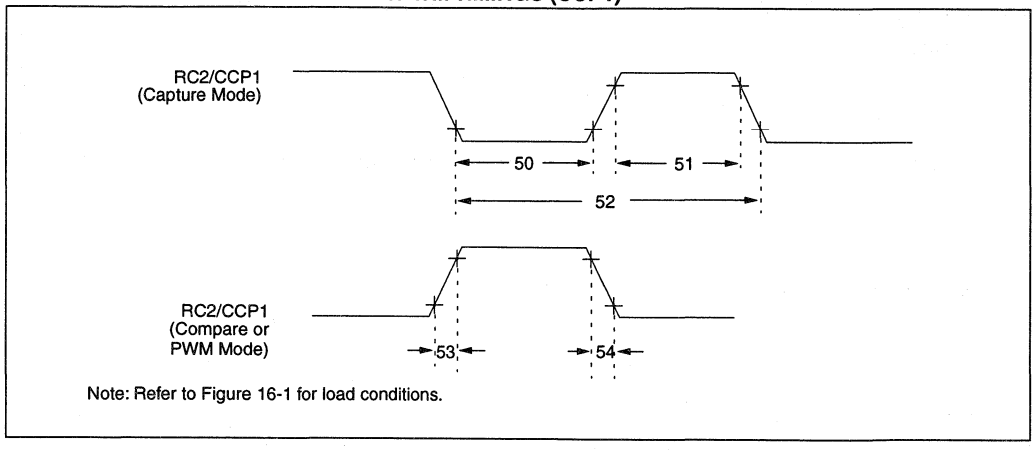
FIGURE 16-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1)



Note: Refer to Figure 16-1 for load conditions.

TABLE 16-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C62/64	10	—	—	ns	
				PIC16LC62/64	20	—	—	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C62/64	10	—	—	ns	
				PIC16LC62/64	20	—	—	ns	
52*	TccP	CCP1 input period			3TCY + 40 / N	—	—	ns	N = prescale value (1,4 or 16)
53	TccR	CCP1 output rise time		PIC16C62/64	—	10	25	ns	
				PIC16LC62/64	—	25	45	ns	
54	TccF	CCP1 output fall time		PIC16C62/64	—	10	25	ns	
				PIC16LC62/64	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

9

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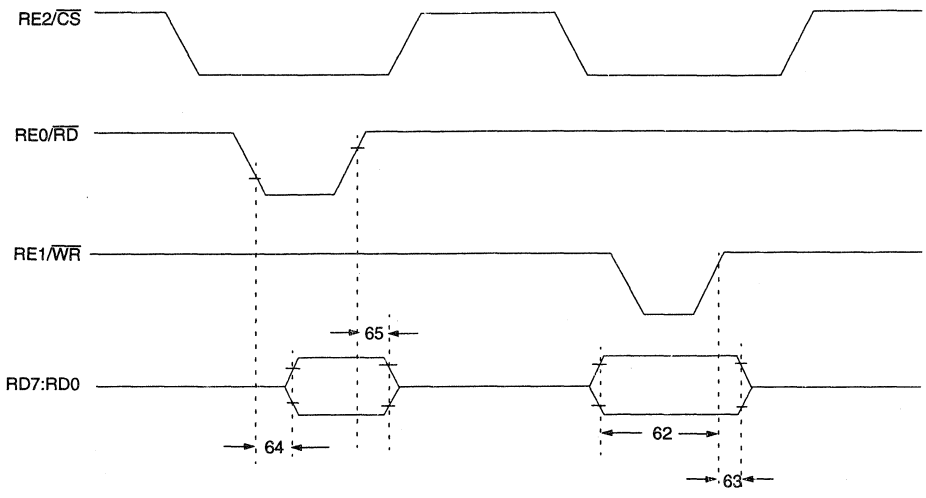
Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 16-7: PARALLEL SLAVE PORT TIMING (PIC16C64)



Note: Refer to Figure 16-1 for load conditions

TABLE 16-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C64)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20	—	—	ns	
63*	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	PIC16C64	20	—	—	ns	
			PIC16LC64	35	—	—	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		—	—	80	ns	
65	TrdH2dtI	RD↑ or CS↑ to data–out invalid		10	—	30	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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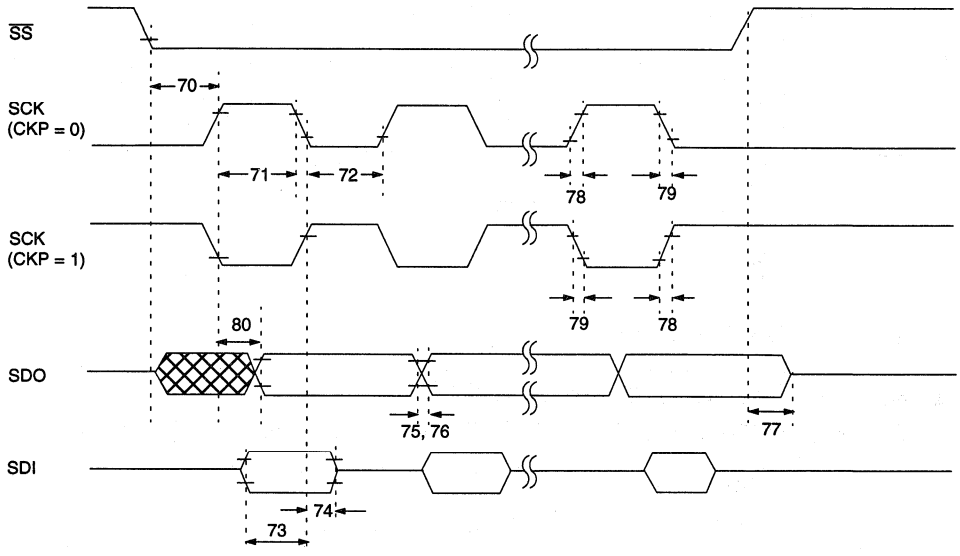
FIGURE 16-8: SPI MODE TIMING



Note: Refer to Figure 16-1 for load conditions

TABLE 16-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input	TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75	TdoR	SDO data output rise time	—	10	25	ns	
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	$\overline{SS}$↓ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	—	10	25	ns	
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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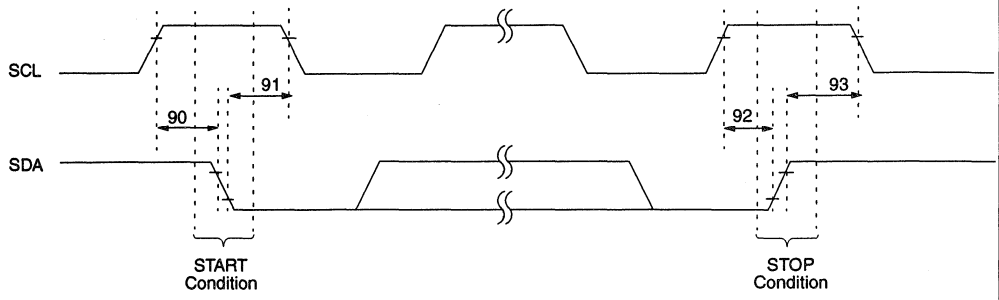
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 16-9: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 16-1 for load conditions

TABLE 16-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	—	—		
91	THD:STA	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

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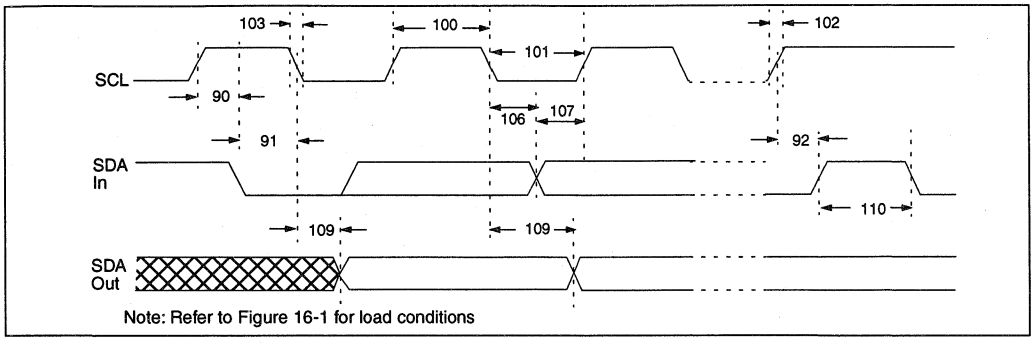
FIGURE 16-10: I²C BUS DATA TIMING



Note: Refer to Figure 16-1 for load conditions

TABLE 16-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C64 must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16C64 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C64 must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16C64 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max. + tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

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NOTES:

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Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

17.0 ELECTRICAL CHARACTERISTICS FOR PIC16C62A/R62/64A/R64

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V
Total power dissipation (Note 1) 1.0W
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin ..... 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) ..... 200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) ..... 200 mA
Maximum current sunk by PORTC and PORTD (combined) ..... 200 mA
Maximum current sourced by PORTC and PORTD (combined) ..... 200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 17-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C62A-04 PIC16CR62-04 PIC16C64A-04 PIC16CR64-04	PIC16C62A-10 PIC16CR62-10 PIC16C64A-10 PIC16CR64-10	PIC16C62A-20 PIC16CR62-20 PIC16C64A-20 PIC16CR64-20	PIC16LC62A-04 PIC16LCR62-04 PIC16LC64A-04 PIC16LCR64-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.0 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3.0V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

17.1 DC Characteristics: PIC16C62A-04,PIC16C64A-04 (Commercial, Industrial, Automotive) PIC16CR62-04,PIC16CR64-04 (Commercial, Industrial, Automotive) PIC16C62A-10,PIC16C64A-10 (Commercial, Industrial, Automotive) PIC16CR62-10,PIC16CR64-10 (Commercial, Industrial, Automotive) PIC16C62A-20,PIC16C64A-20 (Commercial, Industrial, Automotive) PIC16CR62-20,PIC16CR64-20 (Commercial, Industrial, Automotive)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
			3.7	4.0	4.4	V	Automotive Range Only
D010	Supply Current (Note 2, 5)	IDD	-	2.7	5	mA	XT, RC, osc configuration (PIC16C62A/R62/64A/R64-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	10	20	mA	HS osc configuration (PIC16C62A/R62/64A/R64-20) FOSC = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	Δ IBOR	-	350	425	µA	BOR enabled, VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D020	Power-down Current	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021	(Note 3, 5)		-	1.5	16	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.5	19	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			-	2.5	19	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	Δ IBOR	-	350	425	µA	BOR enabled, VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

17.2 DC Characteristics: PIC16LC62A-04,PIC16LCR62-04 (Commercial, Industrial) PIC16LC64A-04, PIC16LCR64-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
D010	Supply Current (Note 2, 5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled, VDD = 5.0V
D020	Power-down Current (Note 3, 5)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled, VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

17.3 DC Characteristics: PIC16C62A-04,PIC16C64A-04 (Commercial, Industrial, Automotive) PIC16CR62-04,PIC16CR64-04 (Commercial, Industrial, Automotive) PIC16C62A-10,PIC16C64A-10 (Commercial, Industrial, Automotive) PIC16CR62-10,PIC16CR64-10 (Commercial, Industrial, Automotive) PIC16C62A-20,PIC16C64A-20 (Commercial, Industrial, Automotive) PIC16CR62-20,PIC16CR64-20 (Commercial, Industrial, Automotive) PIC16LC62A-04,PIC16LC64A-04 (Commercial, Industrial) PIC16LCR62-04,PIC16LCR64-04 (Commercial, Industrial)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 17.1 and Section 17.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		Vss	-	0.5V	V	
D031	with Schmitt Trigger buffer		Vss	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI,OSC1 (in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR, RA4/T0CKI, RC7:RC4, RD7:RD4, RB0/INT,RE2:RE0		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 17.1 and Section 17.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO			50	pF	
D102	SCL, SDA in I^2C mode	Cb			400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

17.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

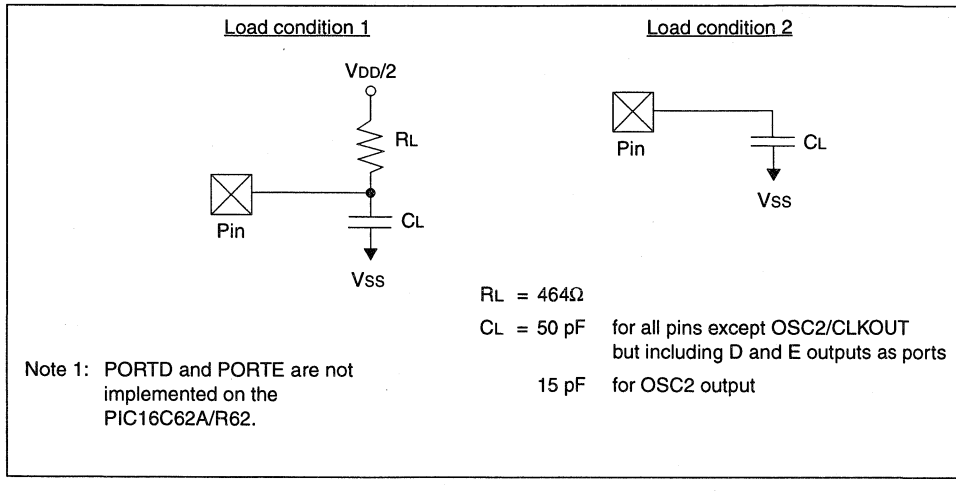
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 17-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



Note 1: PORTD and PORTE are not implemented on the PIC16C62A/R62.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

17.5 Timing Diagrams and Specifications

FIGURE 17-2: EXTERNAL CLOCK TIMING

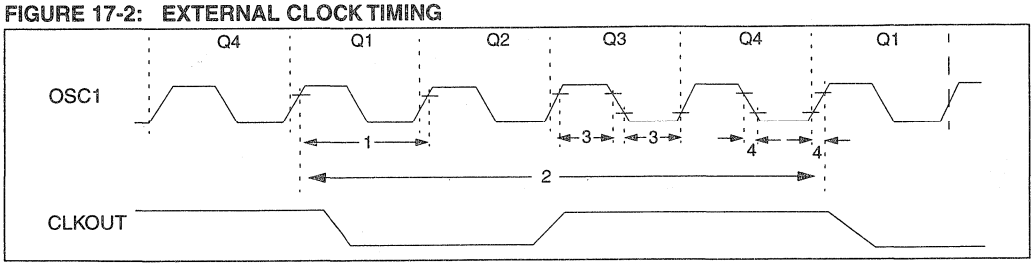


TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C64A/CR64-04, PIC16LC64A/LCR64-04)
			DC	—	20	MHz	HS osc mode (PIC16C64A/CR64-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C64A/CR64-04, PIC16LC64A/LCR64-04)
			4	—	10	MHz	HS osc mode (PIC16C64A/CR64-10)
			4	—	20	MHz	HS osc mode (PIC16C64A/CR64-20)
			5	—	200	kHz	LP osc mode

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C64A/CR64-04, PIC16LC64A/LCR64-04)
			100	—	—	ns	HS osc mode (PIC16C64A/CR64-10)
			50	—	—	ns	HS osc mode (PIC16C64A/CR64-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C64A/CR64-04, PIC16LC64A/LCR64-04)
			100	—	250	ns	HS osc mode (PIC16C64A/CR64-10)
			50	—	250	ns	HS osc mode (PIC16C64A/CR64-20)
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	TCY = 4/FOSC
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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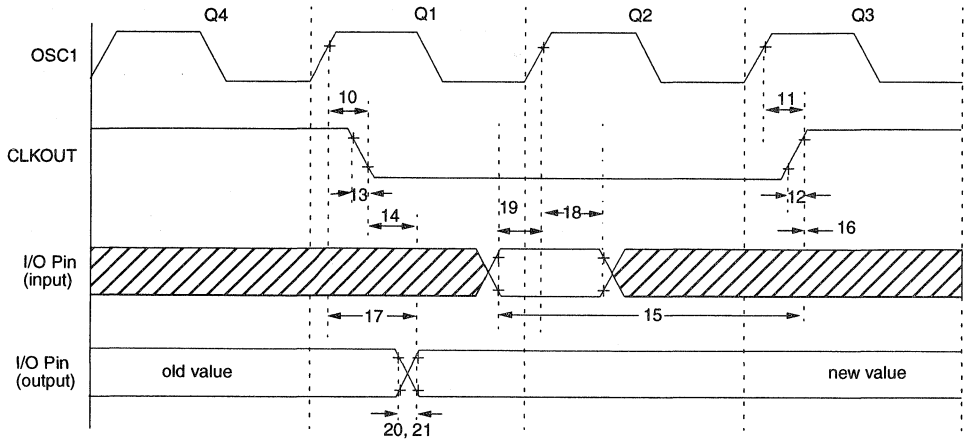
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 17-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 17-1 for load conditions.

TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameters	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		Tosc + 200	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C62A/ R62/64A/R64	100	—	—	ns	
			PIC16LC62A/ R62/64A/R64	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C62A/ R62/64A/R64	—	10	40	ns	
			PIC16LC62A/ R62/64A/R64	—	—	80	ns	
21*	TioF	Port output fall time	PIC16C62A/ R62/64A/R64	—	10	40	ns	
			PIC16LC62A/ R62/64A/R64	—	—	80	ns	
22††*	Tinp	RB0/INT pin high or low time		Tcy	—	—	ns	
23††*	Trbp	RB7:RB4 change int high or low time		Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

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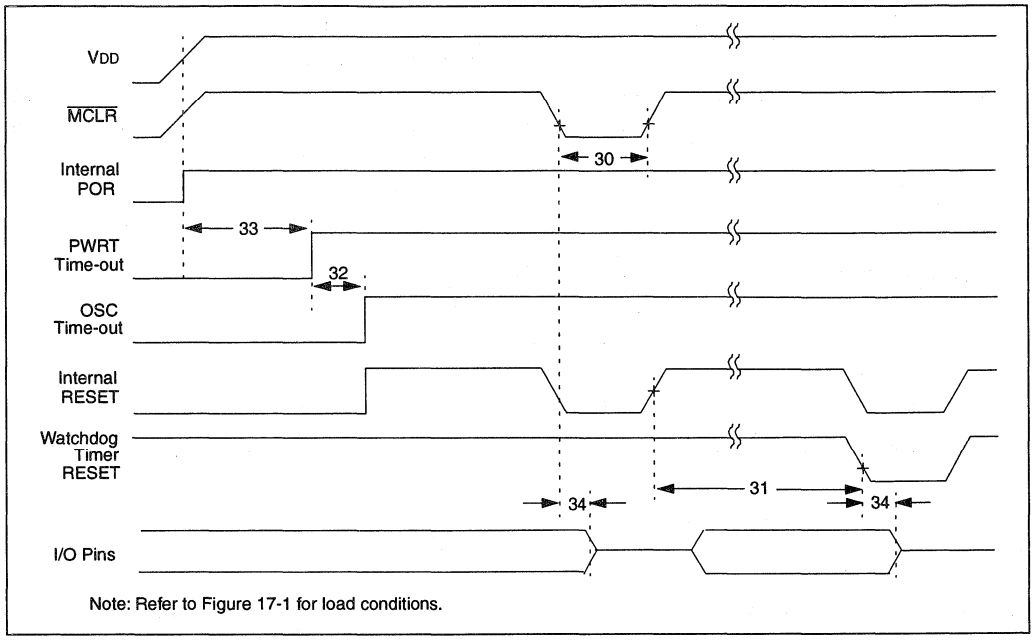
FIGURE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 17-1 for load conditions.

FIGURE 17-5: BROWN-OUT RESET TIMING

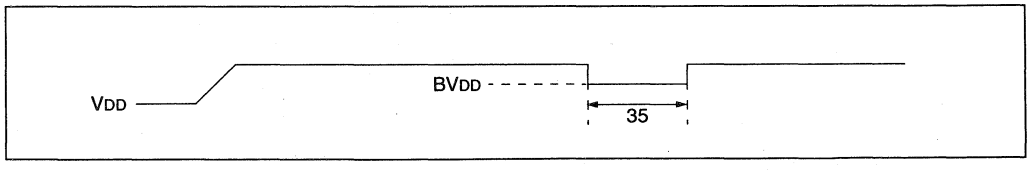


TABLE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from MCLR Low or WDT Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	µs	VDD ≤ BVDD (param. D005)

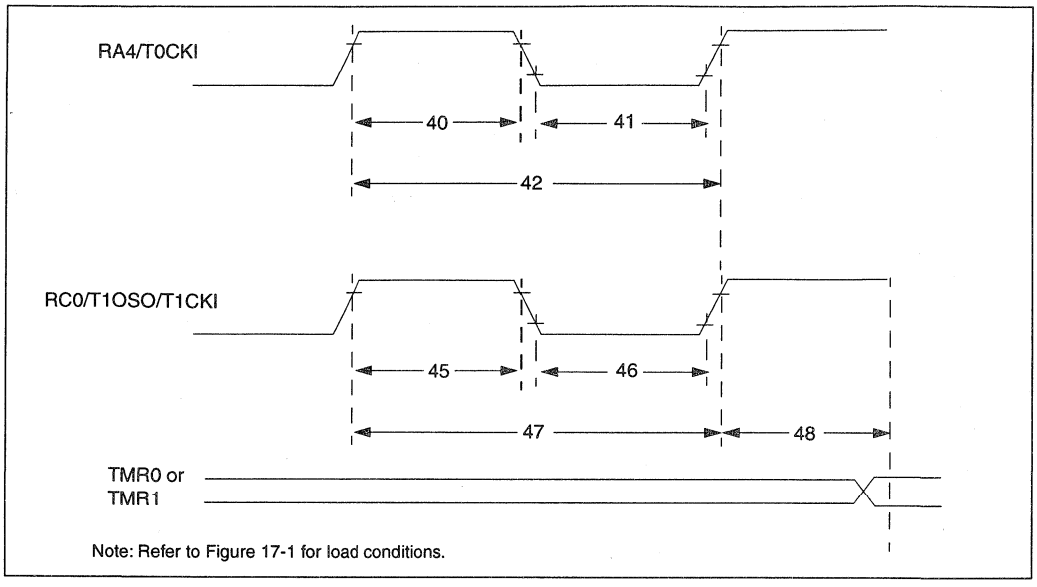
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

9

Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 17-6: TIMER0 AND TIMER1 CLOCK TIMINGS



Note: Refer to Figure 17-1 for load conditions.

TABLE 17-5: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period			TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler	PIC16C62A/R62/64A/R64	15	—	—	ns	
				PIC16LC62A/R62/64A/R64	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler	PIC16C62A/R62/64A/R64	15	—	—	ns	
				PIC16LC62A/R62/64A/R64	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous		TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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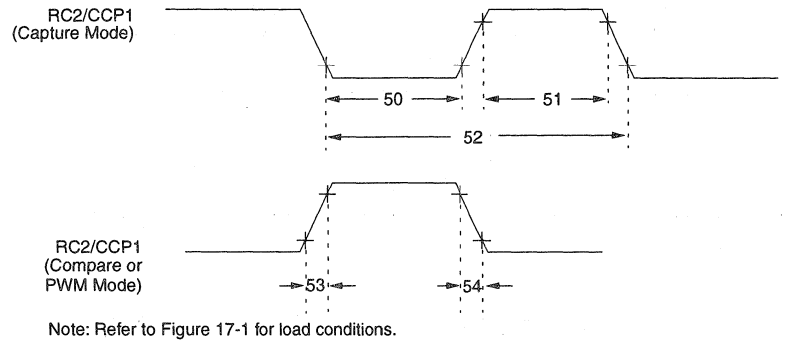
FIGURE 17-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1)



Note: Refer to Figure 17-1 for load conditions.

TABLE 17-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C62A/R62/64A/R64	10	—	—	ns	
				PIC16LC62A/R62/64A/R64	20	—	—	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C62A/R62/64A/R64	10	—	—	ns	
				PIC16LC62A/R62/64A/R64	20	—	—	ns	
52*	TccP	CCP1 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 output rise time		PIC16C62A/R62/64A/R64	—	10	25	ns	
				PIC16LC62A/R62/64A/R64	—	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16C62A/R62/64A/R64	—	10	25	ns	
				PIC16LC62A/R62/64A/R64	—	25	45	ns	

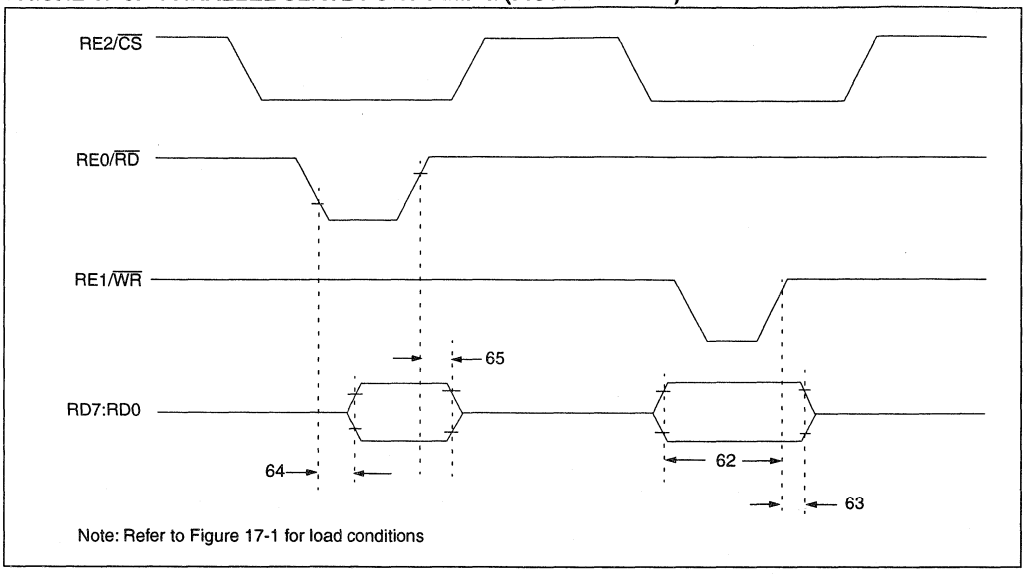
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 17-8: PARALLEL SLAVE PORT TIMING (PIC16C64A/R64)



Note: Refer to Figure 17-1 for load conditions

TABLE 17-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C64A/R64)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20	—	—	ns	
				25	—	—	ns	Automotive Range Only
63*	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	PIC16C64A/R64	20	—	—	ns	
			PIC16LC64A/R64	35	—	—	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		—	—	80	ns	
				—	—	90	ns	Automotive Range Only
65*	TrdH2dtI	RD↑ or CS↑ to data–out invalid		10	—	30	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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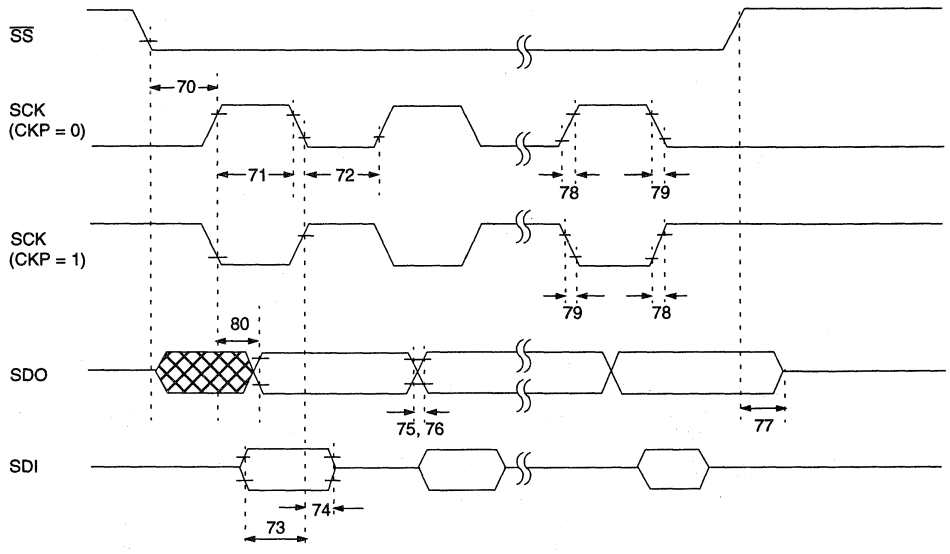
Applicable Devices 61 62 62A R62 63 64 64A R64 65 65A

FIGURE 17-9: SPI MODE TIMING



Note: Refer to Figure 17-1 for load conditions

TABLE 17-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	TCY	—	—	ns	
71*	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72*	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75*	TdoR	SDO data output rise time	—	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
77*	TssH2doZ	SS↓ to SDO output hi-impedance	10	—	50	ns	
78*	TscR	SCK output rise time (master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (master mode)	—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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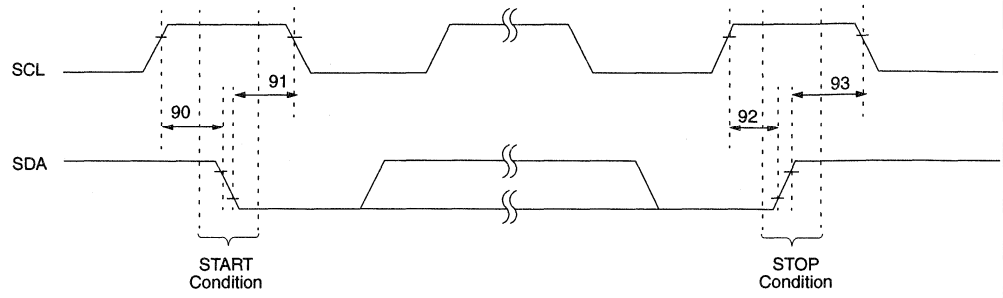
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 17-10: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 17-1 for load conditions

TABLE 17-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93*	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

*Characterized but not tested.

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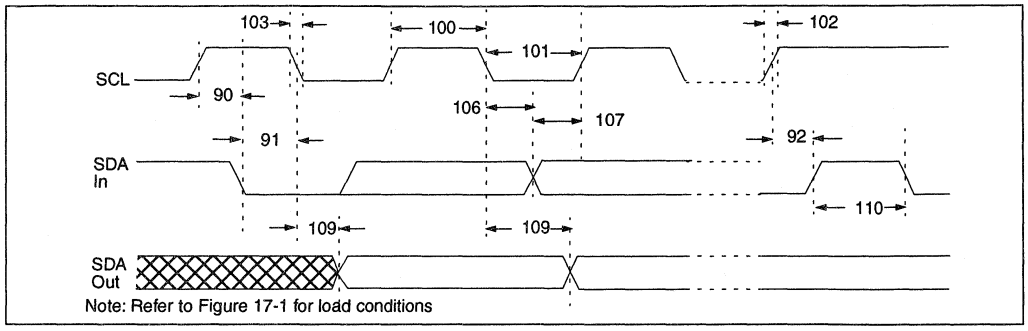
FIGURE 17-11: I^2C BUS DATA TIMING



Note: Refer to Figure 17-1 for load conditions

TABLE 17-10: I^2C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C64A/R64 must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16C64A/R64 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C64A/R64 must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16C64A/R64 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91*	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

* Characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

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NOTES:

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Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

18.0 ELECTRICAL CHARACTERISTICS FOR PIC16C65

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V
Total power dissipation (Note 1) 1.0W
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin ..... 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) ..... 200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) ..... 200 mA
Maximum current sunk by PORTC and PORTD (combined) ..... 200 mA
Maximum current sourced by PORTC and PORTD (combined) ..... 200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 18-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C65-04	PIC16C65-10	PIC16C65-20	PIC16LC65-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3V IPD: 800 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3V IPD: 800 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V IPD 1.0 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

18.1 DC Characteristics: PIC16C65-04 (Commercial, Industrial) PIC16C65-10 (Commercial, Industrial) PIC16C65-20 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2, 5)	IDD	-	2.7	5	mA	XT, RC osc configuration (PIC16C65-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration (PIC16C65-20) FOSC = 20 MHz, VDD = 5.5V
D020	Power-down Current (Note 3, 5)	IPD	-	10.5	800	µA	VDD = 4.0V, WDT enabled,-40°C to +85°C
D021			-	1.5	800	µA	VDD = 4.0V, WDT disabled,-0°C to +70°C
D021A			-	1.5	800	µA	VDD = 4.0V, WDT disabled,-40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

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Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

18.2 DC Characteristics: PIC16LC65-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	3.0	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2, 5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	105	µA	LP osc configuration FOSC = 32 kHz, VDD = 4.0V, WDT disabled
D020	Power-down Current	IPD	-	7.5	800	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021	(Note 3, 5)		-	0.9	800	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	800	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

18.3 DC Characteristics: PIC16C65-04 (Commercial, Industrial) PIC16C65-10 (Commercial, Industrial) PIC16C65-20 (Commercial, Industrial) PIC16LC65-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 18.1 and Section 18.2				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI,OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD		For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD		For entire VDD range
D042	MCLR, RA4/T0CKI, RC7:RC4, RD7:RD4, RB0/INT, RE2:RE0		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7 VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	VSS ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	VSS ≤ VPIN ≤ VDD, XT, HS, and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 18.1 and Section 18.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	
D102	SCL, SDA in I^2C mode	CB	-	-	400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

18.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

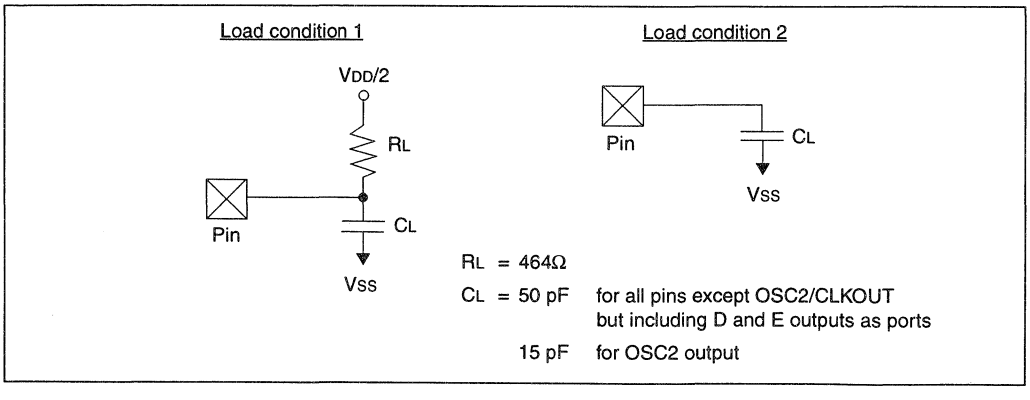
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 18-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



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Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

18.5 Timing Diagrams and Specifications

FIGURE 18-2: EXTERNAL CLOCK TIMING

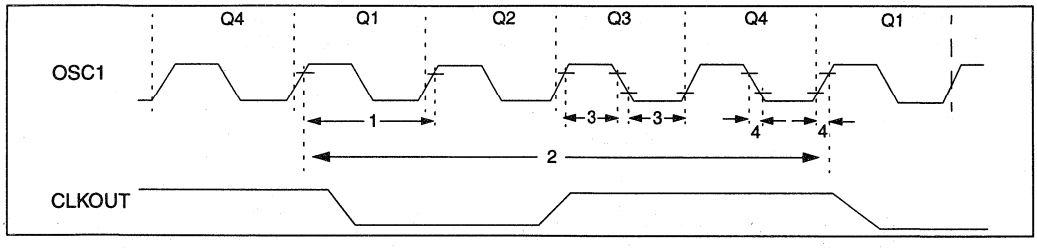

TABLE 18-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C65-04, PIC16LC65-04)
			DC	—	20	MHz	HS osc mode (PIC16C65-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C65-04, PIC16LC65-04)
			4	—	10	MHz	HS osc mode (PIC16C65-10)
			4	—	20	MHz	HS osc mode (PIC16C65-20)
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C65-04, PIC16LC65-04)
			100	—	—	ns	HS osc mode (PIC16C65-10)
			50	—	—	ns	HS osc mode (PIC16C65-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C65-04, PIC16LC65-04)
			100	—	250	ns	HS osc mode (PIC16C65-10)
			50	—	250	ns	HS osc mode (PIC16C65-20)
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	TCY = 4/FOSC
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	50	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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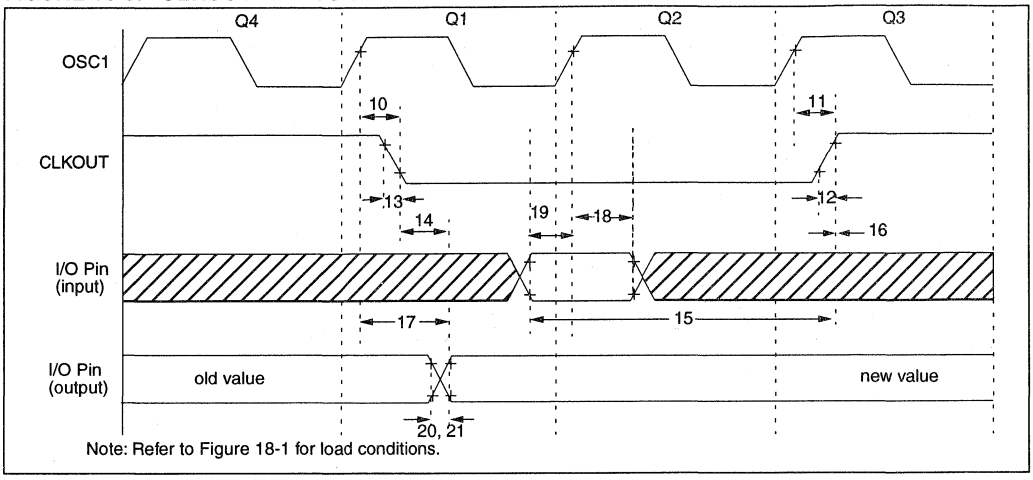
Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 18-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 18-1 for load conditions.

TABLE 18-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C65	100	—	—	ns	
			PIC16LC65	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C65	—	10	25	ns	
			PIC16LC65	—	—	60	ns	
21*	TioF	Port output fall time	PIC16C65	—	10	25	ns	
			PIC16LC65	—	—	60	ns	
22††*	Tinp	RB0/INT pin high or low time		Tcy	—	—	ns	
23††*	Trbp	RB7:RB4 change int high or low time		Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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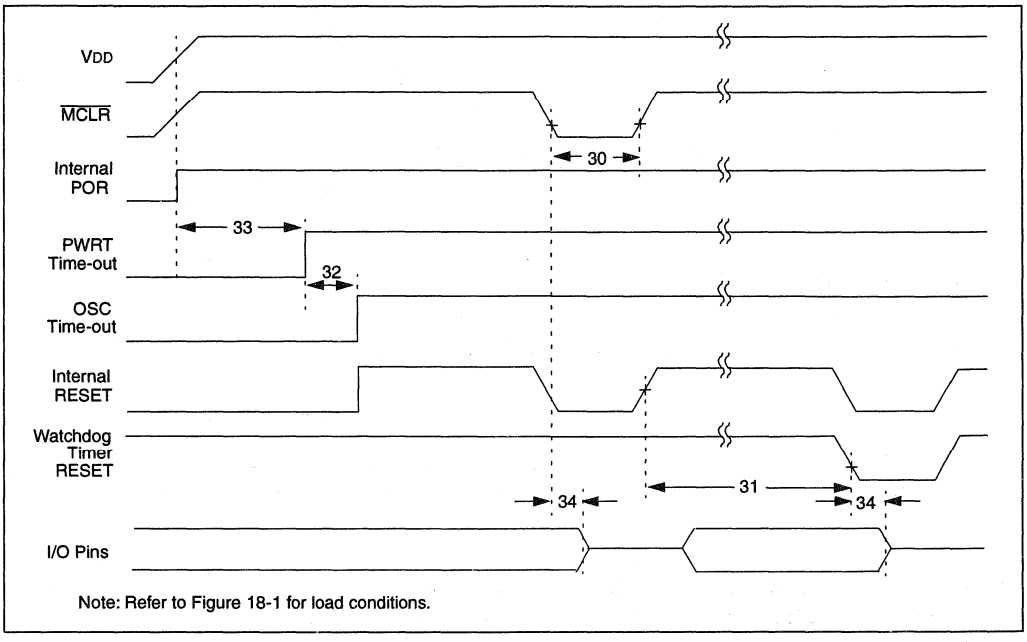
Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 18-1 for load conditions.

TABLE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30*	TmcL	$\overline{MCLR}$ Pulse Width (low)	100	—	—	ns	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period or WDT reset	28	72	132	ms	VDD = 5V, -40°C to +85°C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low	—	—	100	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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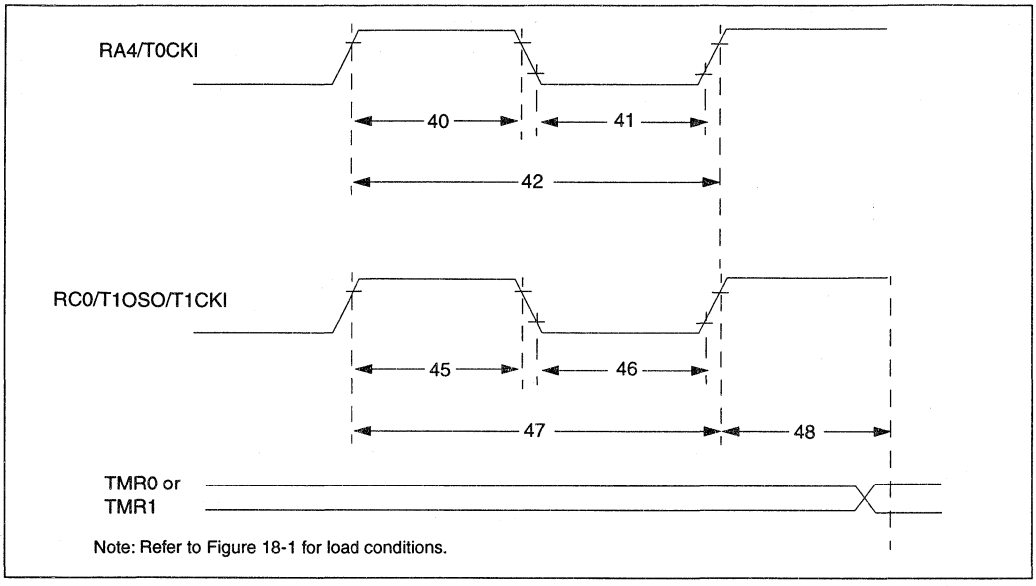
Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 18-5: TIMER0 AND TIMER1 CLOCK TIMINGS



Note: Refer to Figure 18-1 for load conditions.

TABLE 18-5: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period			Greater of: 20 µs or TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler	PIC16C65	15	—	—	ns	
				PIC16LC65	25	—	—	ns	
			Asynchronous		2 TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler	PIC16C65	15	—	—	ns	
				PIC16LC65	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous		Greater of: 20 µs or TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		Greater of: 20 µs or 4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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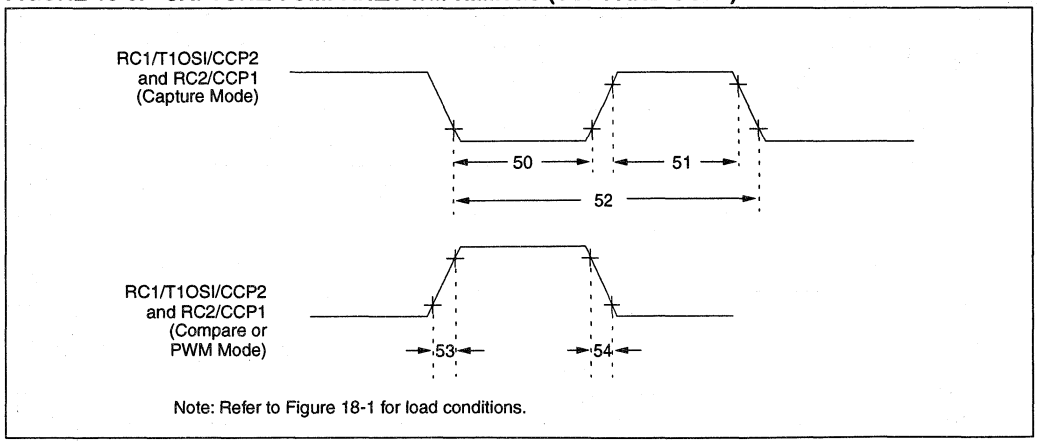
FIGURE 18-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 18-1 for load conditions.

TABLE 18-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C65	10	—	—	ns	
				PIC16LC65	20	—	—	ns	
51*	TccH	CCP1 and CCP2 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C65	10	—	—	ns	
				PIC16LC65	20	—	—	ns	
52*	TccP	CCP1 and CCP2 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4, or 16)
53	TccR	CCP1 and CCP2 output rise time		PIC16C65	—	10	25	ns	
				PIC16LC65	—	25	45	ns	
54	TccF	CCP1 and CCP2 output fall time		PIC16C65	—	10	25	ns	
				PIC16LC65	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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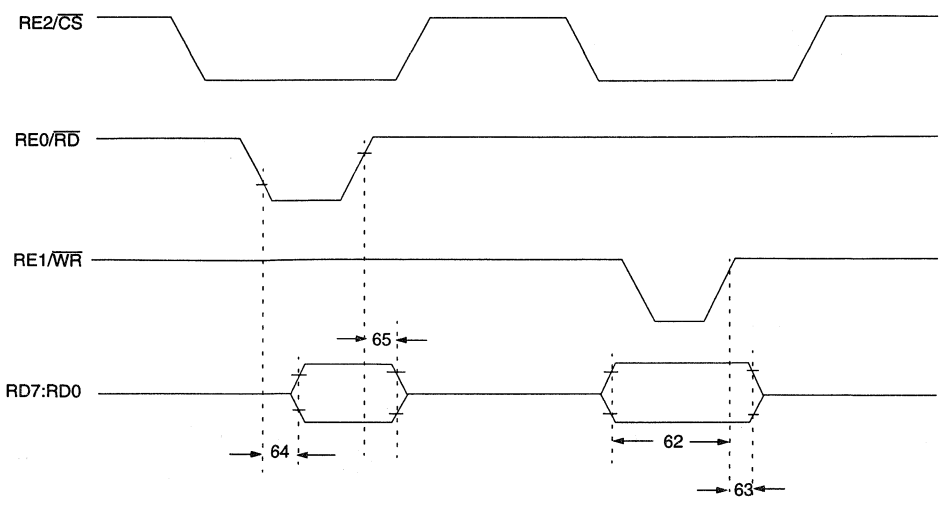
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 18-7: PARALLEL SLAVE PORT TIMING



Note: Refer to Figure 18-1 for load conditions

TABLE 18-7: PARALLEL SLAVE PORT REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time)		20	—	—	ns	
63*	TwrH2dtI	$\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ to data–in invalid (hold time)	PIC16C65	20	—	—	ns	
			PIC16LC65	35	—	—	ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data–out valid		—	—	80	ns	
65	TrdH2dtI	$\overline{RD}\uparrow$ or $\overline{CS}\uparrow$ to data–out invalid		10	—	30	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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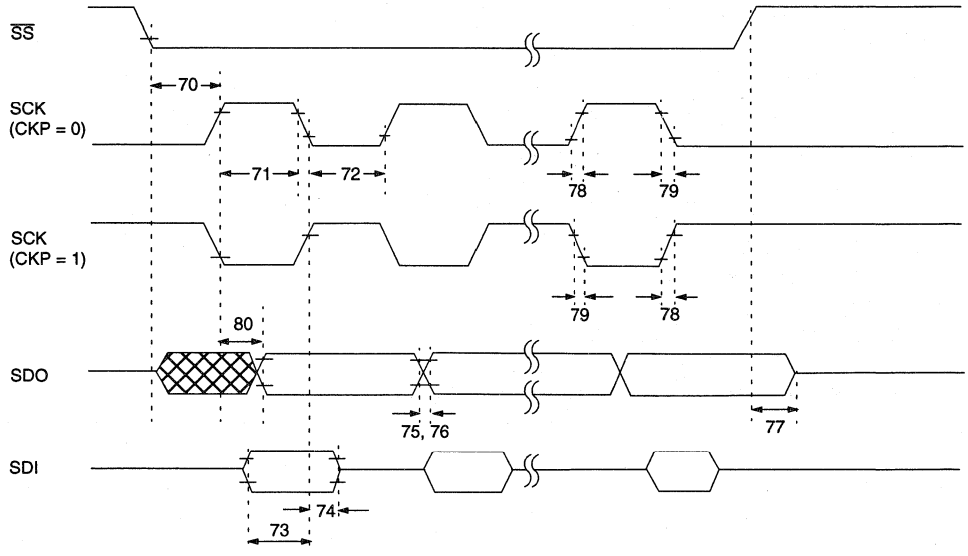
FIGURE 18-8: SPI MODE TIMING



Note: Refer to Figure 18-1 for load conditions

TABLE 18-8: SPI MODE REQUIREMENTS

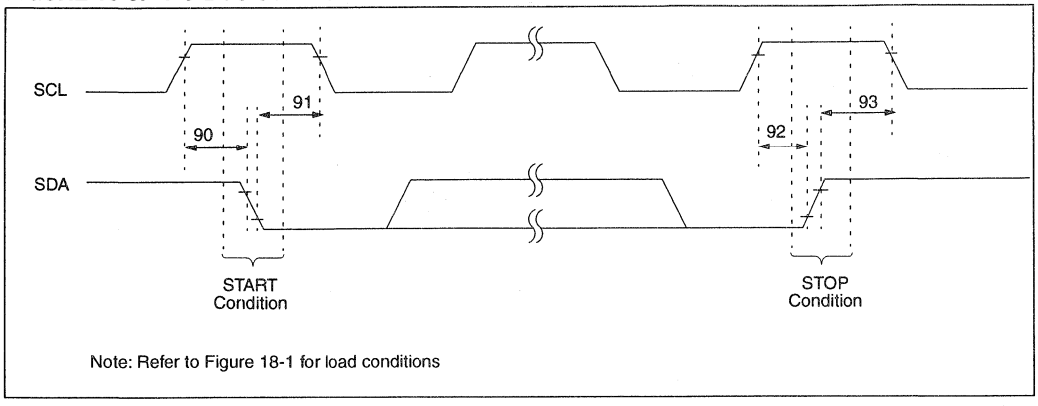
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input	TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75	TdoR	SDO data output rise time	—	10	25	ns	
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	$\overline{SS}$↓ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	—	10	25	ns	
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 18-9: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 18-1 for load conditions

TABLE 18-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

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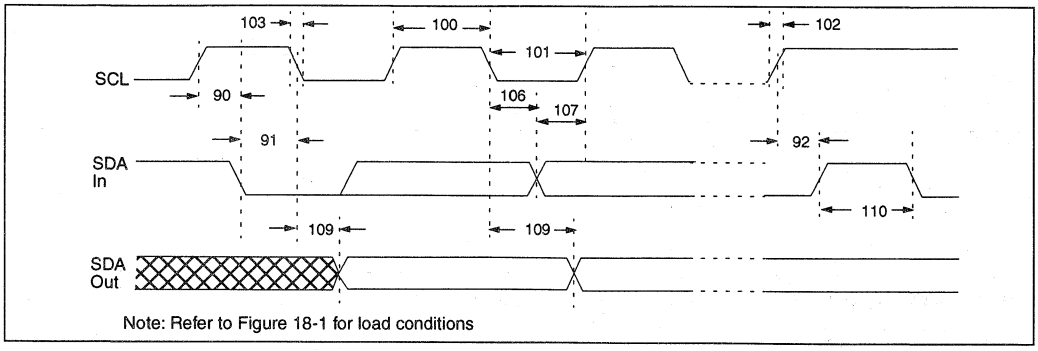
Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 18-10: I²C BUS DATA TIMING



Note: Refer to Figure 18-1 for load conditions

TABLE 18-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C65 must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16C65 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C65 must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16C65 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

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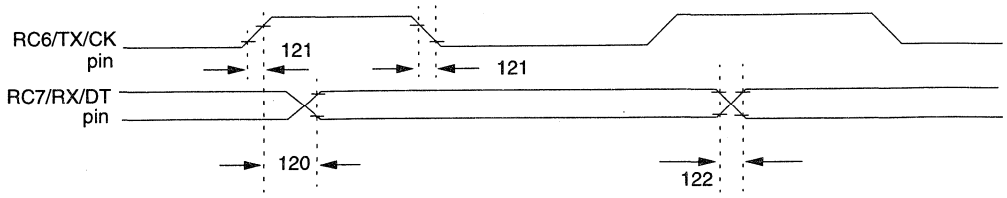
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 18-11: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



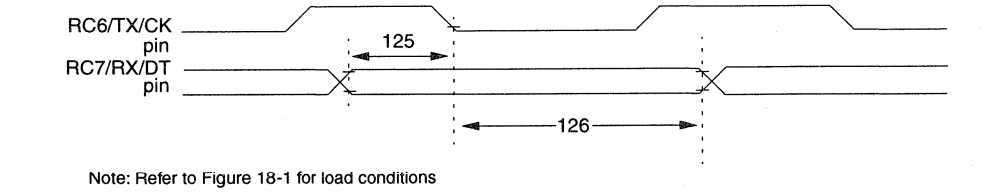
Note: Refer to Figure 18-1 for load conditions

TABLE 18-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	tckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16C65	—	—	80	ns	
			PIC16LC65	—	—	100	ns	
121	tckrf	Clock out rise time and fall time (Master Mode)	PIC16C65	—	—	45	ns	
			PIC16LC65	—	—	50	ns	
122	tdtrf	Data out rise time and fall time	PIC16C65	—	—	45	ns	
			PIC16LC65	—	—	50	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-12: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 18-1 for load conditions

TABLE 18-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	tdtV2ckl	SYNC RCV (MASTER & SLAVE) Data hold before CK ↓ (DT hold time)	15	—	—	ns	
126	tckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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19.0 ELECTRICAL CHARACTERISTICS FOR PIC16C63/65A

Absolute Maximum Ratings (†)

Ambient temperature under bias ..... -55 to + 125°C
Storage temperature ..... -65°C to + 150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V
Total power dissipation (Note 1) 1.0W
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin ..... 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (Note 3) (combined) ..... 200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (Note 3) (combined) ..... 200 mA
Maximum current sunk by PORTC and PORTD (Note 3) (combined) ..... 200 mA
Maximum current sourced by PORTC and PORTD (Note 3) (combined) ..... 200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - $\sum$ IOH} + $\sum$ {(VDD-VOH) x IOH} + $\sum$(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$/VPP pin rather than pulling this pin directly to VSS.

Note 3: PORTD and PORTE not available on the PIC16C63.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C63-04 PIC16C65A-04	PIC16C63-10 PIC16C65A-10	PIC16C63-20 PIC16C65A-20	PIC16LC63-04 PIC16LC65A-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

19.1 DC Characteristics: PIC16C63-04,PIC16C65A-04 (Commercial,Industrial,Automotive) PIC16C63-10,PIC16C65A-10 (Commercial,Industrial,Automotive) PIC16C63-20,PIC16C65A-20 (Commercial,Industrial,Automotive)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
			3.7	4.0	4.4	V	Automotive Range Only
D010	Supply Current (Note 2, 5)	IDD	-	2.7	5	mA	XT, RC, osc configuration (PIC16C63/65A-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	10	20	mA	HS osc configuration (PIC16C63/65A-20) FOSC = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled, VDD = 5.0V
D020	Power-down Current (Note 3, 5)	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled,-40°C to +85°C
D021			-	1.5	16	µA	VDD = 4.0V, WDT disabled,-0°C to +70°C
D021A			-	1.5	19	µA	VDD = 4.0V, WDT disabled,-40°C to +85°C
D021B			-	2.5	19	µA	VDD = 4.0V, WDT disabled,-40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled, VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

19.2 DC Characteristics: PIC16LC63-04,PIC16LC65A-04 (Commercial,Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2, 5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled, VDD = 5.0V
D020	Power-down Current (Note 3, 5)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled, VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

19.3 DC Characteristics: PIC16C63-04,PIC16C65A-04 (Commercial,Industrial,Automotive) PIC16C63-10,PIC16C65A-10 (Commercial,Industrial,Automotive) PIC16C63-20,PIC16C65A-20 (Commercial,Industrial,Automotive) PIC16LC63-04,PIC16LC65A-04 (Commercial,Industrial)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI, OSC1 (in RC mode)		Vss	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR RA4/T0CKI, RC7:RC4, RD7:RD4, RB0/INT, RE2:RE0		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	
D102	SCL, SDA in I^2C mode	Cb	-	-	400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C6X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

19.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

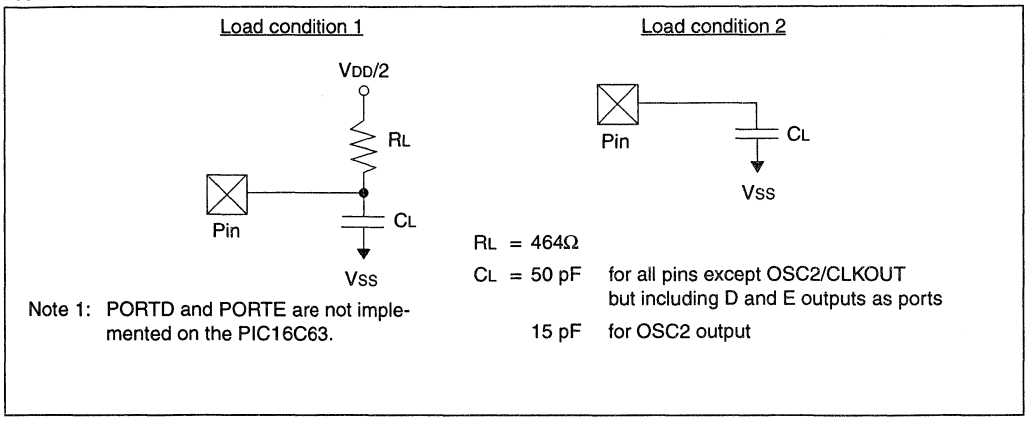
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 19-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



Note 1: PORTD and PORTE are not implemented on the PIC16C63.

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19.5 Timing Diagrams and Specifications

FIGURE 19-2: EXTERNAL CLOCK TIMING

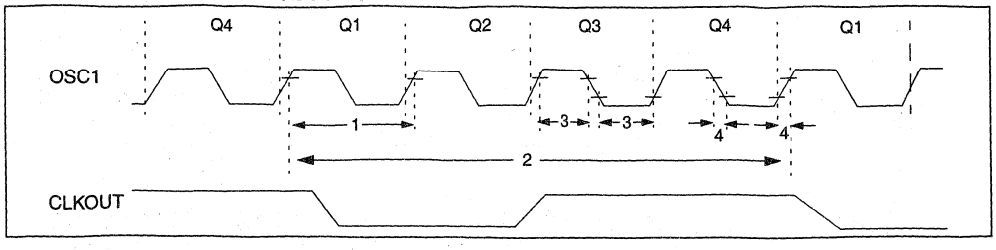

TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C63/65A-04)
			DC	—	20	MHz	HS osc mode (PIC16C63/65A-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C63/65A-04)
			4	—	10	MHz	HS osc mode (PIC16C63/65A-10)
			4	—	20	MHz	HS osc mode (PIC16C63/65A-20)
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C63/65A-04)
			100	—	—	ns	HS osc mode (PIC16C63/65A-10)
			50	—	—	ns	HS osc mode (PIC16C63/65A-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C63/65A-04)
			100	—	250	ns	HS osc mode (PIC16C63/65A-10)
			50	—	250	ns	HS osc mode (PIC16C63/65A-20)
			5	—	—	µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	Tcy = 4/Fosc
3*	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4*	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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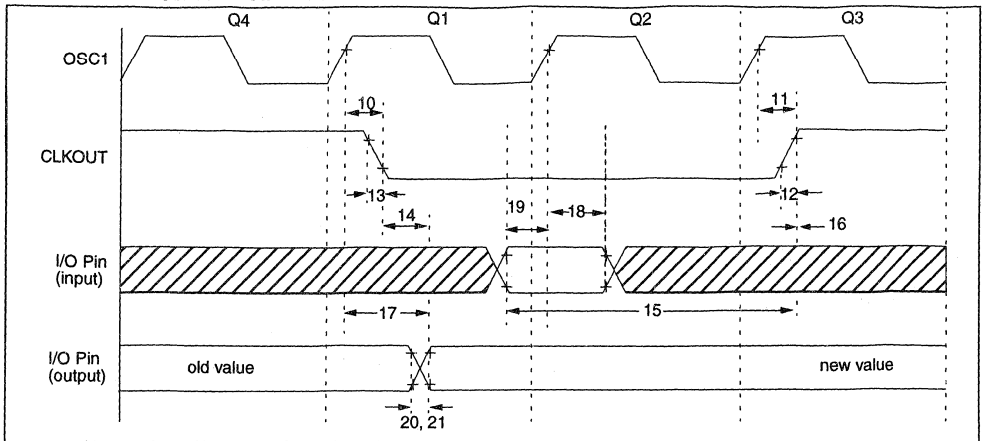
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 19-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 19-1 for load conditions.

TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		Tosc + 200	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C63/65A	100	—	—	ns	
			PIC16LC63/65A	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C63/65A	—	10	40	ns	
			PIC16LC63/65A	—	—	80	ns	
21*	TioF	Port output fall time	PIC16C63/65A	—	10	40	ns	
			PIC16LC63/65A	—	—	80	ns	
22††*	Tinp	INT pin high or low time		Tcy	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edge.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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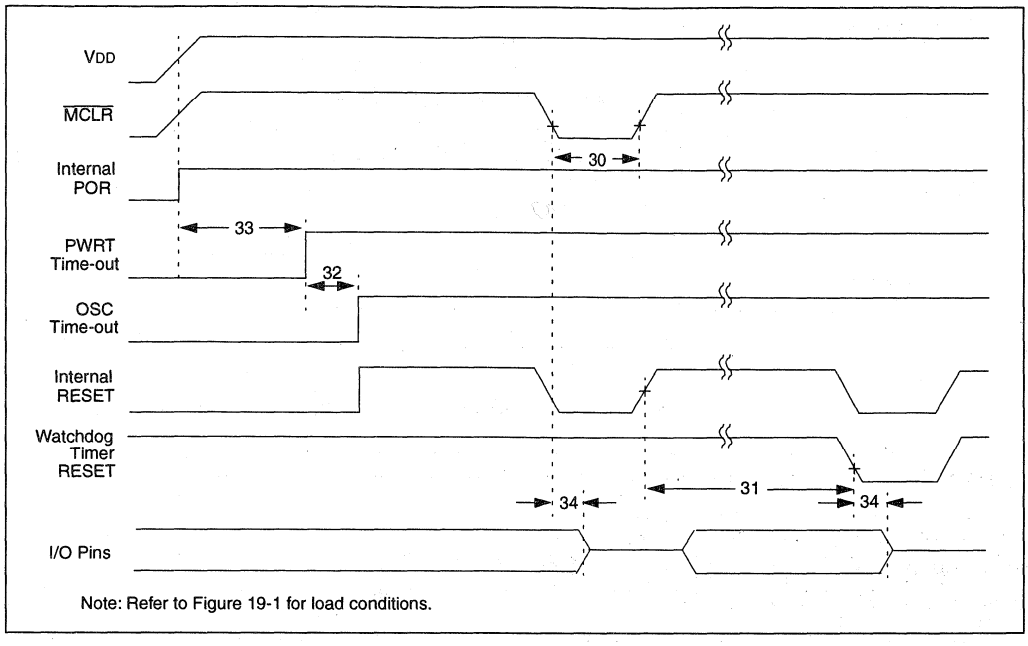
Applicable Devices | 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 19-1 for load conditions.

FIGURE 19-5: BROWN-OUT RESET TIMING

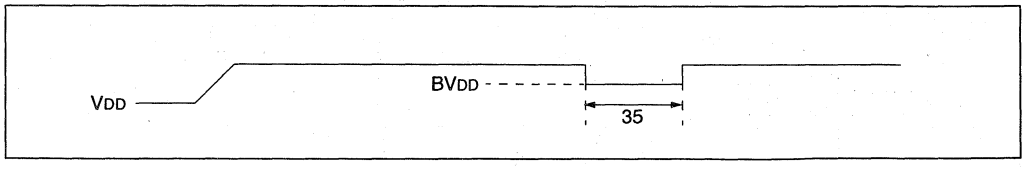


TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or WDT reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	µs	VDD ≤ BVDD (D005)

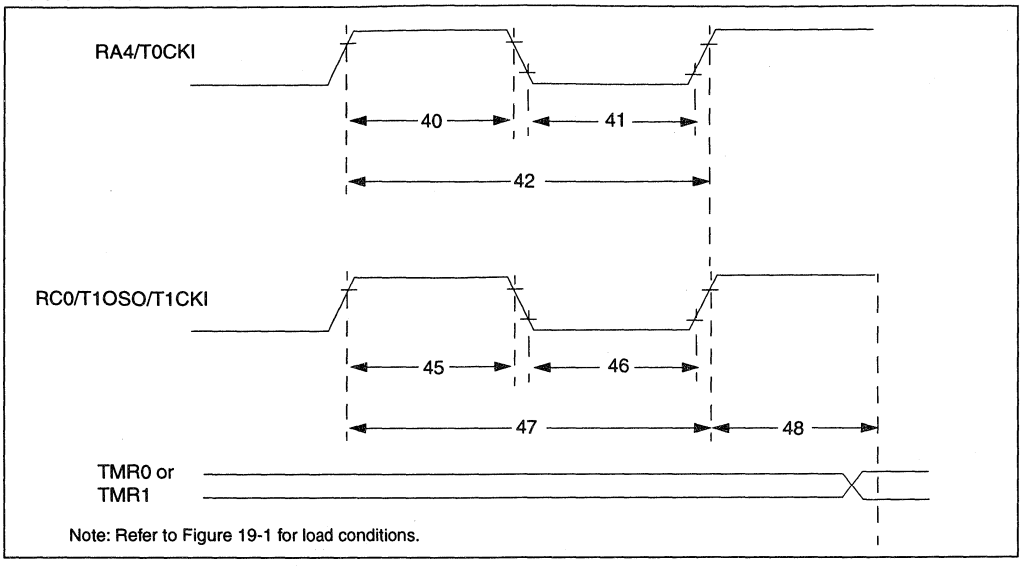
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

9

Applicable Devices 61 | 62 | 62A | R62 | 63 | 64 | 64A | R64 | 65 | 65A

FIGURE 19-6: TIMER0 AND TIMER1 CLOCK TIMINGS



Note: Refer to Figure 19-1 for load conditions.

TABLE 19-5: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period			TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler	PIC16C63/65A	15	—	—	ns	
				PIC16LC63/65A	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, With Prescaler	PIC16C63/65A	15	—	—	ns	
				PIC16LC63/65A	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous		TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)			DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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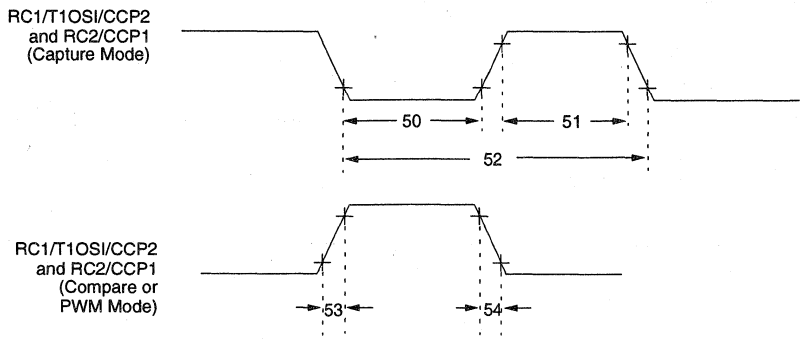
FIGURE 19-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 19-1 for load conditions.

TABLE 19-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C63/65A	10	—	—	ns	
				PIC16LC63/65A	20	—	—	ns	
51*	TccH	CCP1 and CCP2 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C63/65A	10	—	—	ns	
				PIC16LC63/65A	20	—	—	ns	
52*	TccP	CCP1 and CCP2 input period			3TCY + 40 / N	—	—	ns	N = prescale value (1,4, or 16)
53*	TccR	CCP1 and CCP2 output rise time		PIC16C63/65A	—	10	25	ns	
				PIC16LC63/65A	—	25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time		PIC16C63/65A	—	10	25	ns	
				PIC16LC63/65A	—	25	45	ns	

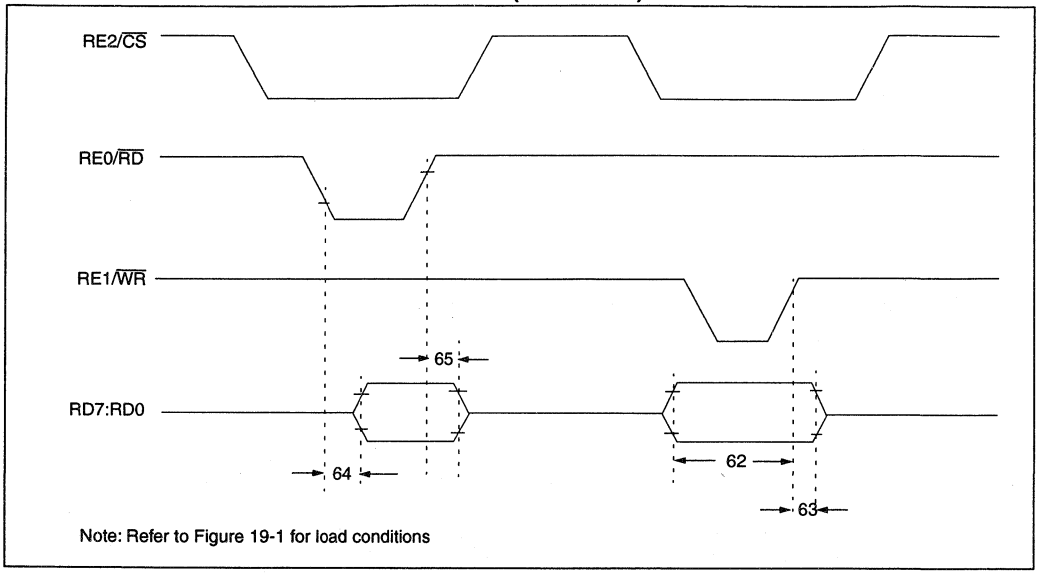
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 19-8: PARALLEL SLAVE PORT TIMING (PIC16C65A)



Note: Refer to Figure 19-1 for load conditions

TABLE 19-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C65A)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62*	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20	—	—	ns	
				25	—	—	ns	Automotive Range Only
63*	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	PIC16C65A	20	—	—	ns	
			PIC16LC65A	35	—	—	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		—	—	80	ns	
				—	—	90	ns	Automotive Range Only
65*	TrdH2dtI	RD↑ or CS↑ to data–out invalid		10	—	30	ns	

* Characterized but not tested

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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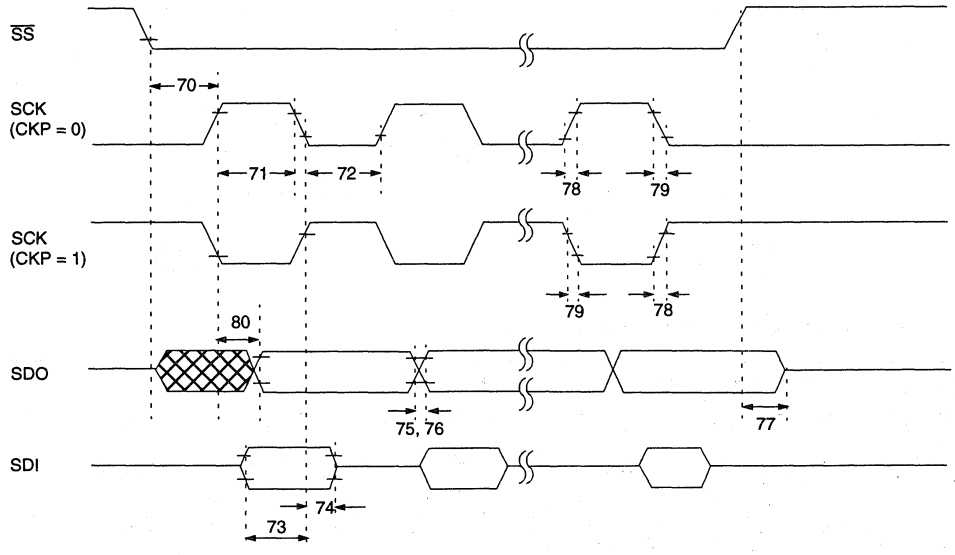
FIGURE 19-9: SPI MODE TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input	TCY	—	—	ns	
71*	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72*	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75*	TdoR	SDO data output rise time	—	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
77*	TssH2doZ	$\overline{SS}\downarrow$ to SDO output hi-impedance	10	—	50	ns	
78*	TscR	SCK output rise time (master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (master mode)	—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

* Characterized but not tested

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

9

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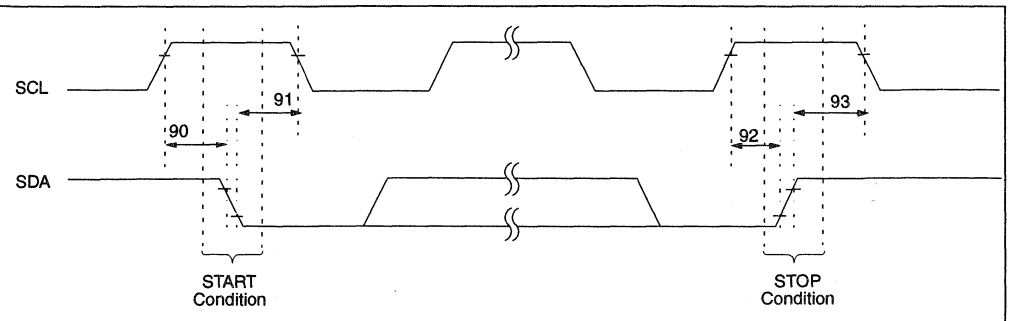
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 19-10: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91*	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92*	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

*Characterized but not tested

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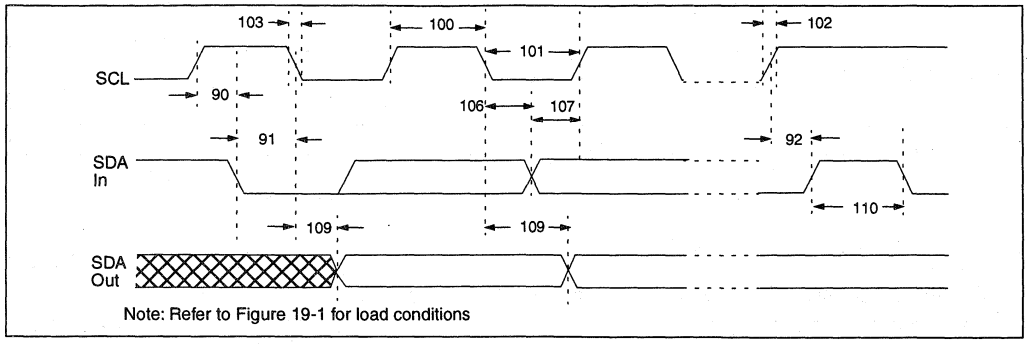
FIGURE 19-11: I^2C BUS DATA TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-10: I^2C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C65A must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16C65A must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C65A must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16C65A must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91*	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	At 125°C tested to 20 ns min.
			400 kHz mode	0	0.9	µs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

* Characterized but not tested

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

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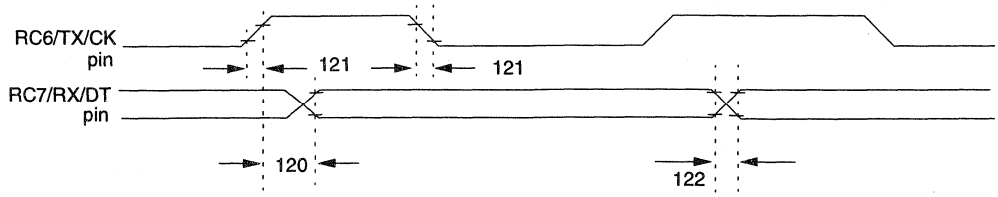
Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 19-12: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



Note: Refer to Figure 19-1 for load conditions

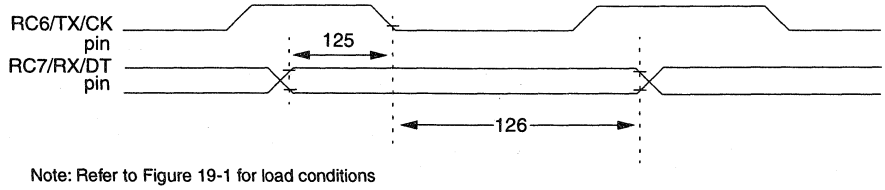
TABLE 19-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120*	tckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16C63/65A	—	—	80	ns	
			PIC16LC63/65A	—	—	100	ns	
121*	tckrf	Clock out rise time and fall time (Master Mode)	PIC16C63/65A	—	—	45	ns	
			PIC16LC63/65A	—	—	50	ns	
122*	tdtrf	Data out rise time and fall time	PIC16C63/65A	—	—	45	ns	
			PIC16LC63/65A	—	—	50	ns	

* Characterized but not tested

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-13: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125*	tdtV2ckl	SYNC RCV (MASTER & SLAVE) Data hold before CK ↓ (DT hold time)	15	—	—	ns	
126*	tckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

* Characterized but not tested

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

20.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR: PIC16C62, PIC16C62A, PIC16CR62, PIC16C63, PIC16C64, PIC16C64A, PIC16CR64, PIC16C65A

he graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25°C, while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 20-1: TYPICAL IPD vs. VDD (WDT DISABLED, RC MODE)

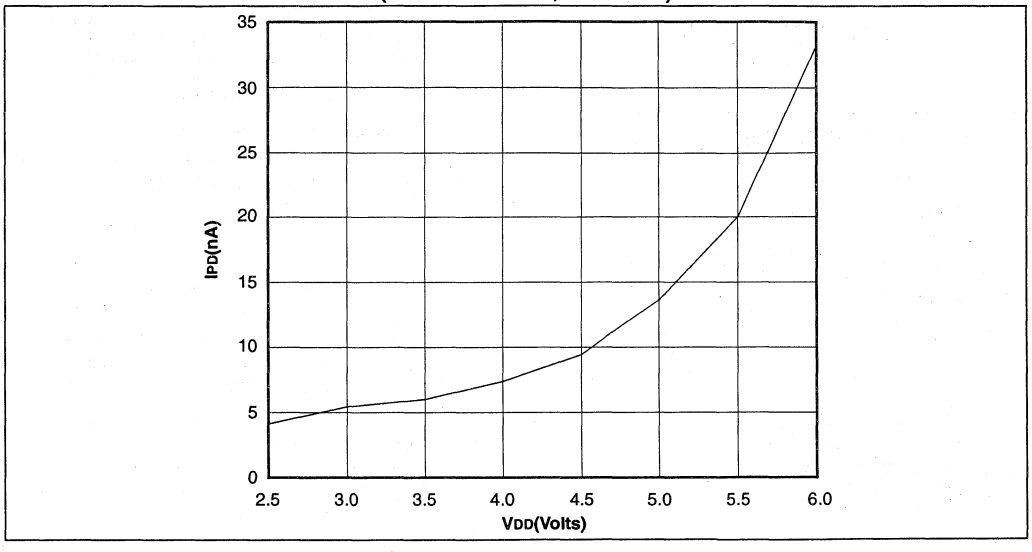
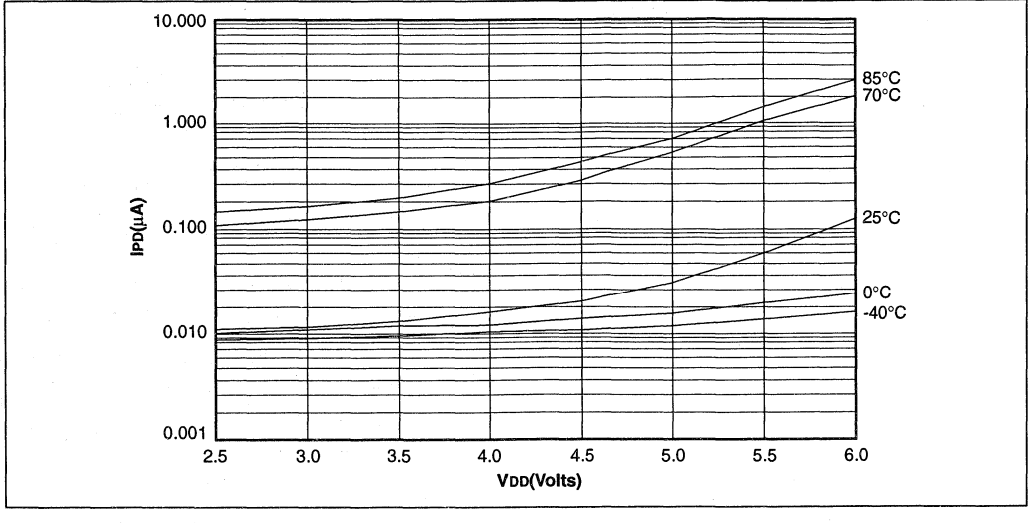


FIGURE 20-2: MAXIMUM IPD vs. VDD (WDT DISABLED, RC MODE)



9

FIGURE 20-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

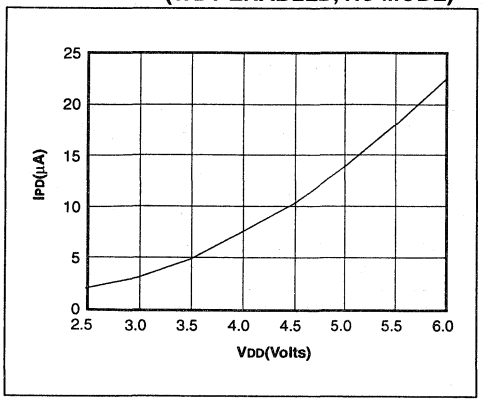


FIGURE 20-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

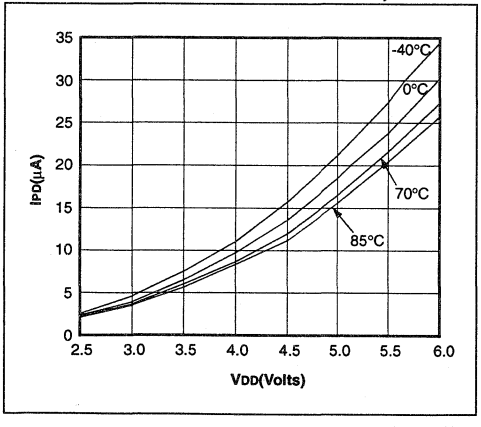
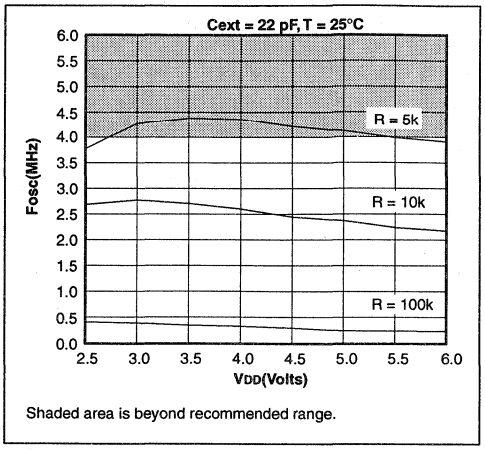


FIGURE 20-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Shaded area is beyond recommended range.

FIGURE 20-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

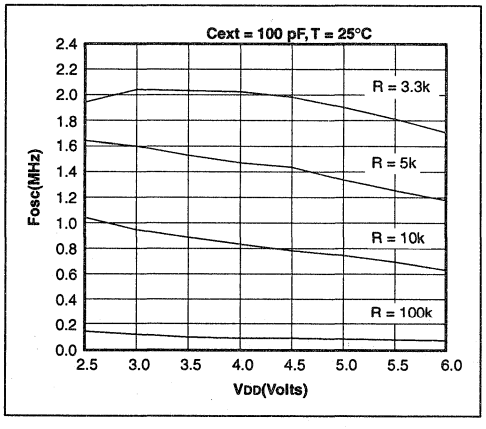
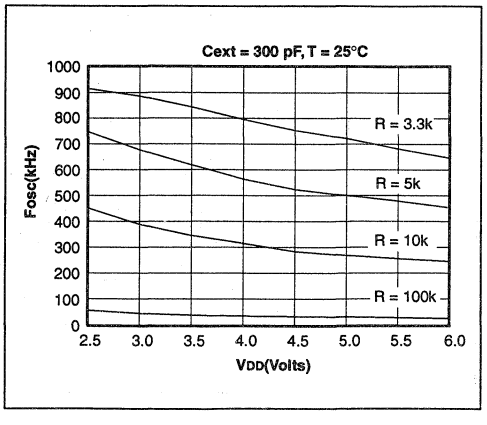


FIGURE 20-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Data based on matrix samples. See first page of this section for details.

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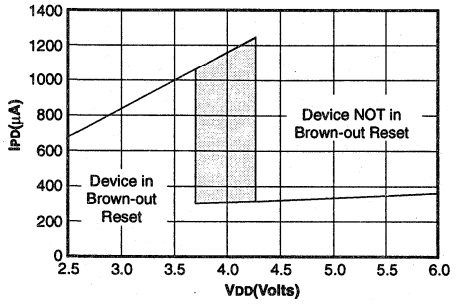
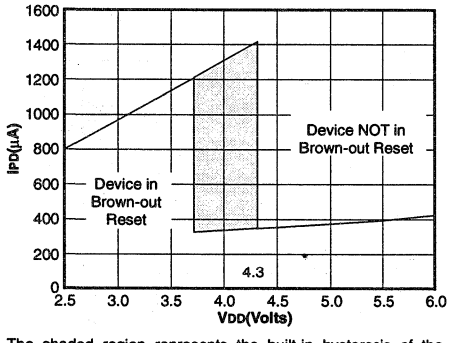
FIGURE 20-8: TYPICAL IPD vs. VDD BROWN-OUT DETECT ENABLED (RC MODE)



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

FIGURE 20-9: MAXIMUM IPD vs. VDD BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

FIGURE 20-10: TYPICAL IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

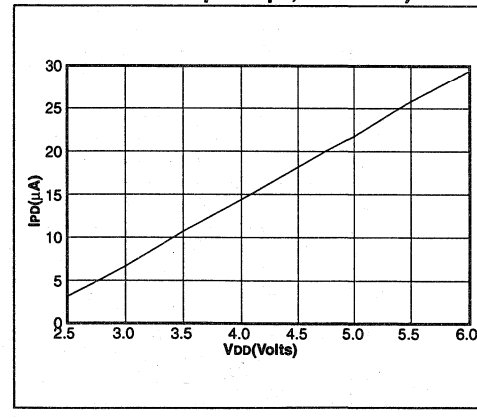
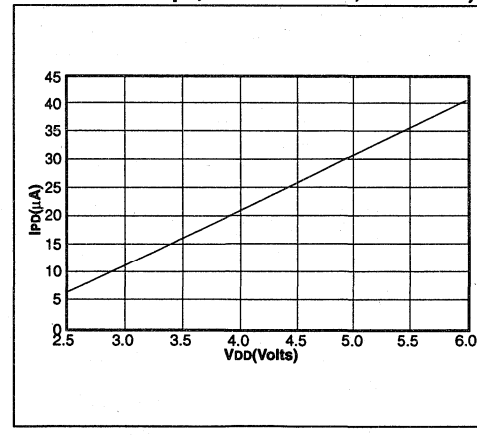


FIGURE 20-11: MAXIMUM IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)



Data based on matrix samples. See first page of this section for details.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 20-12: TYPICAL IDD vs. FREQUENCY (RC MODE @ 22 pF, 25°C)

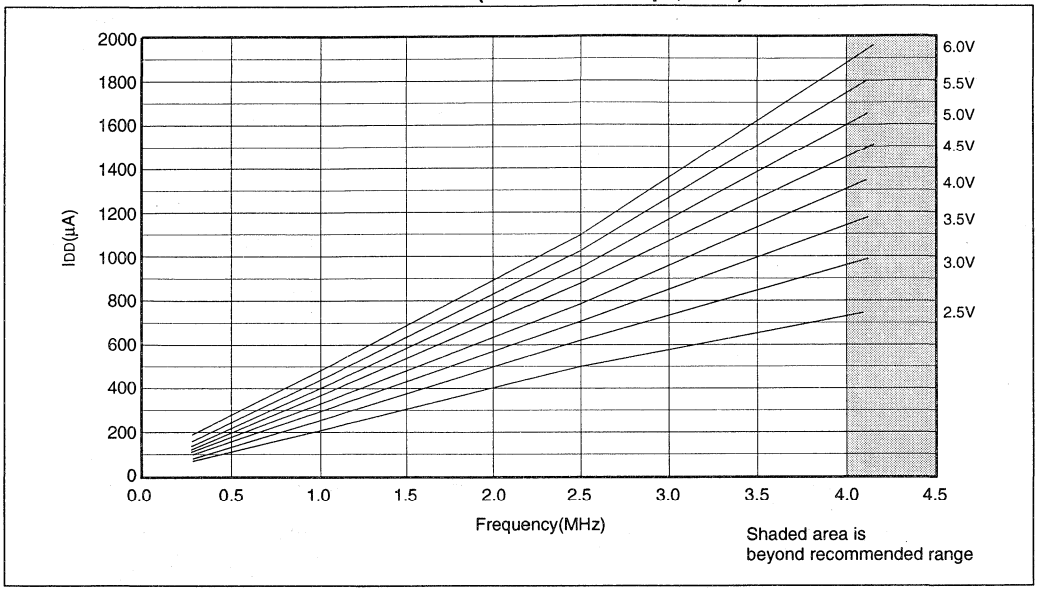
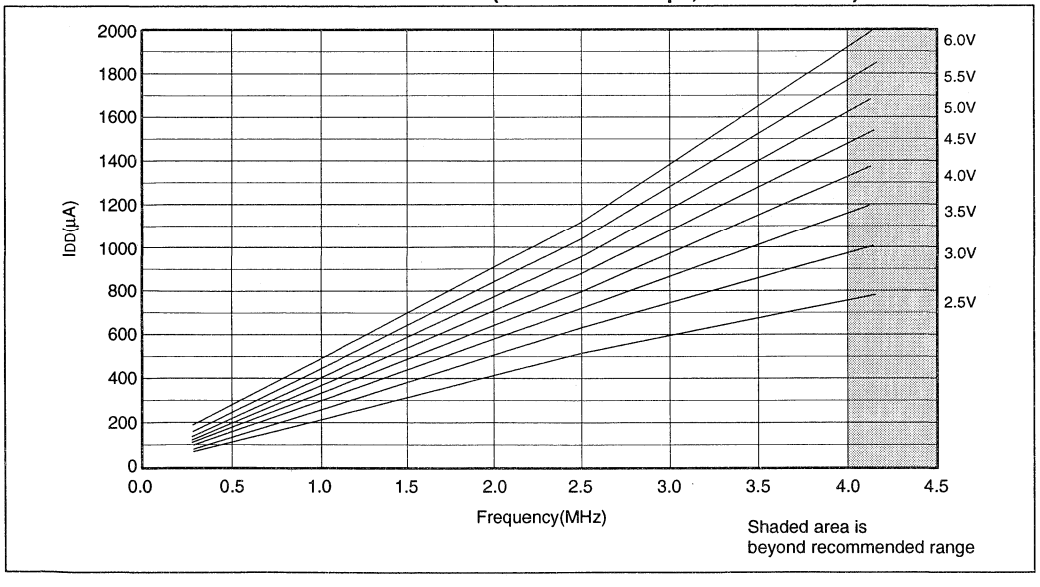


FIGURE 20-13: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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FIGURE 20-14: TYPICAL IDD vs. FREQUENCY (RC MODE @ 100 pF, 25°C)

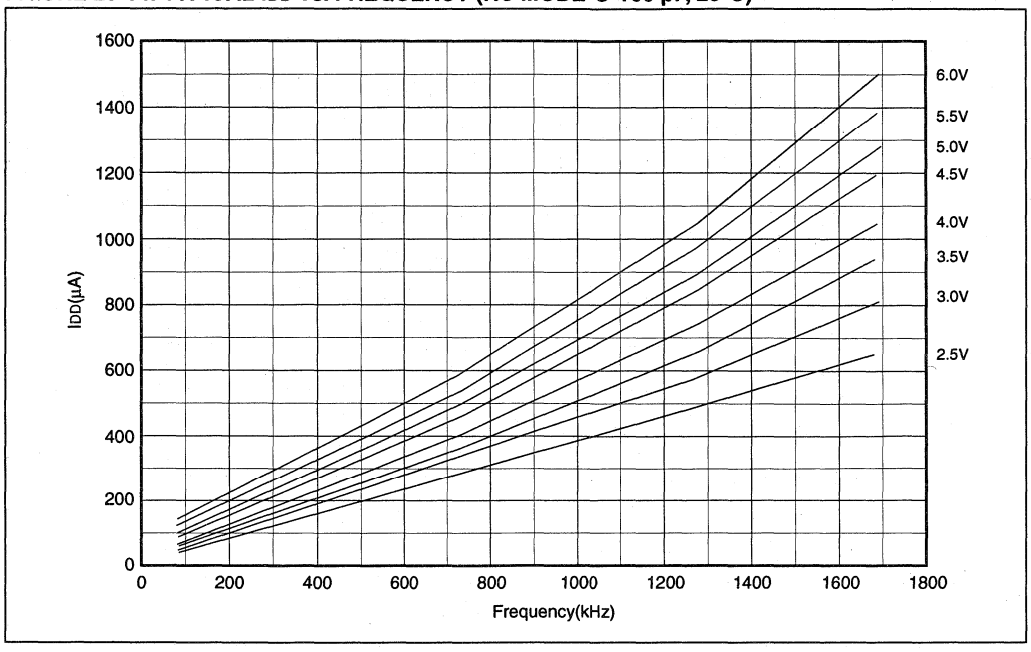
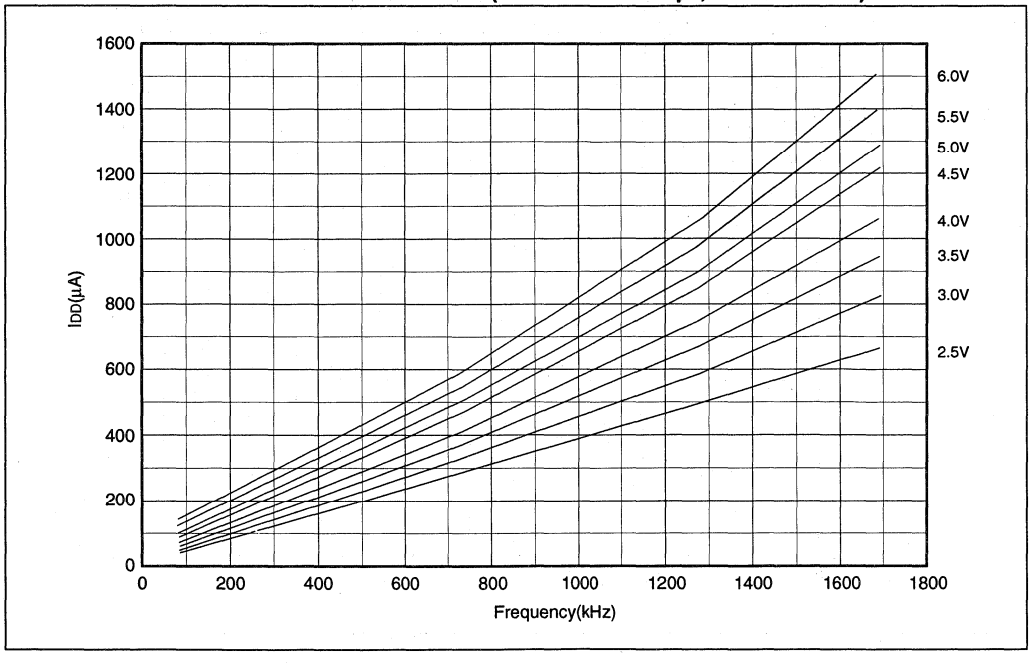


FIGURE 20-15: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

9

Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 20-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

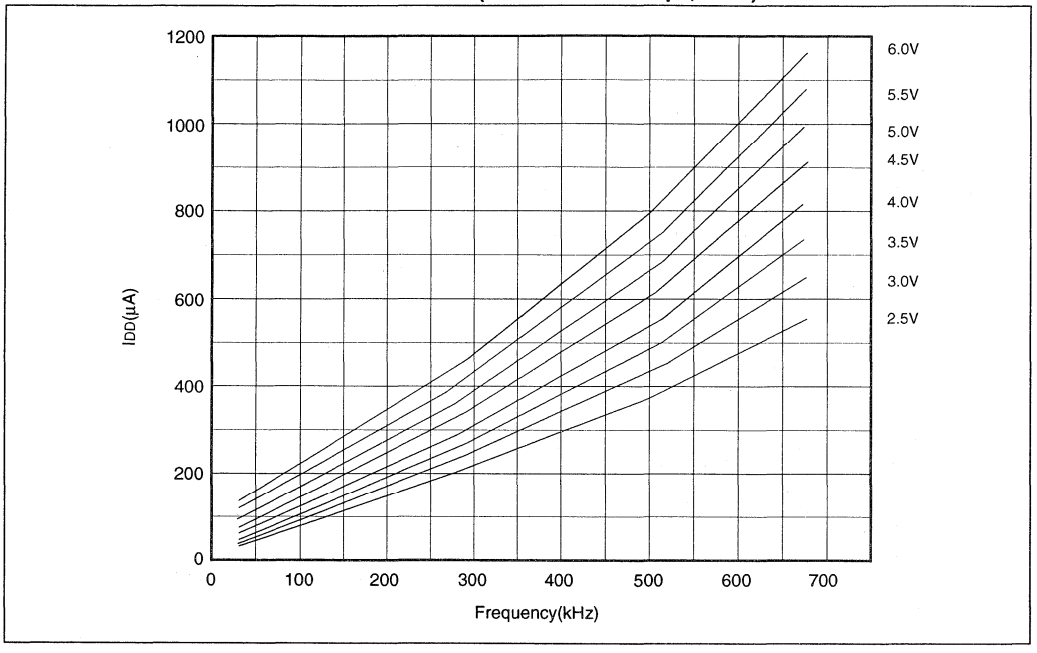
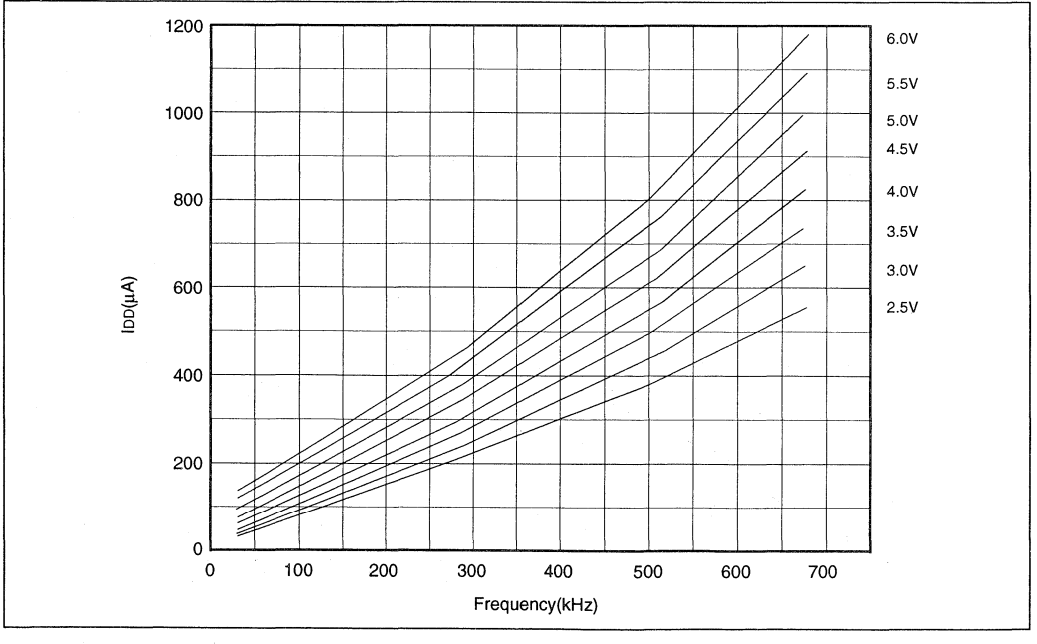


FIGURE 20-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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FIGURE 20-18: TYPICAL IDD vs. CAPACITANCE @ 500 kHz (RC MODE)

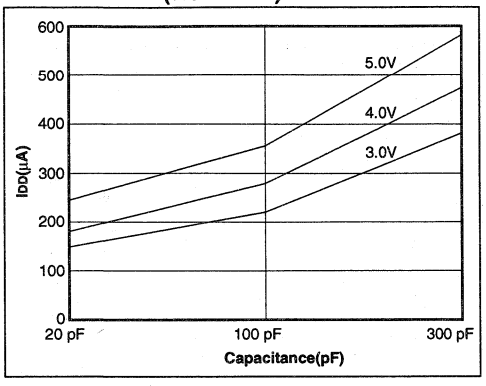


TABLE 20-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
22 pF	5k	4.12 MHz	± 1.4%
	10k	2.35 MHz	± 1.4%
	100k	268 kHz	± 1.1%
100 pF	3.3k	1.80 MHz	± 1.0%
	5k	1.27 MHz	± 1.0%
	10k	688 kHz	± 1.2%
	100k	77.2 kHz	± 1.0%
300 pF	3.3k	707 kHz	± 1.4%
	5k	501 kHz	± 1.2%
	10k	269 kHz	± 1.6%
	100k	28.3 kHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

FIGURE 20-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs. VDD

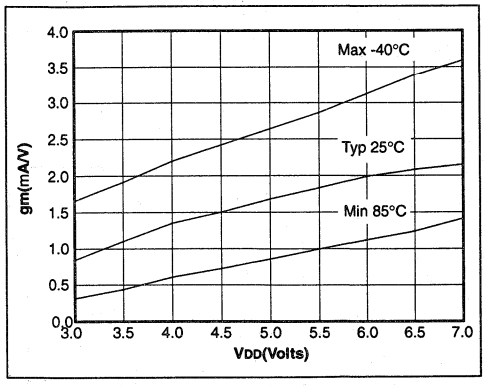


FIGURE 20-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs. VDD

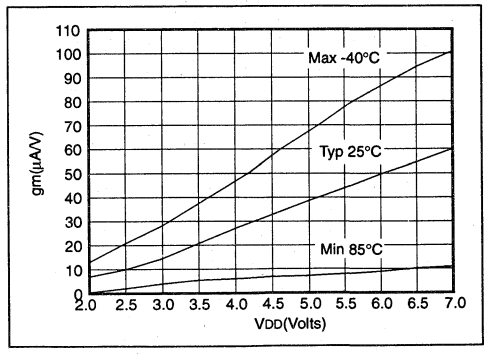
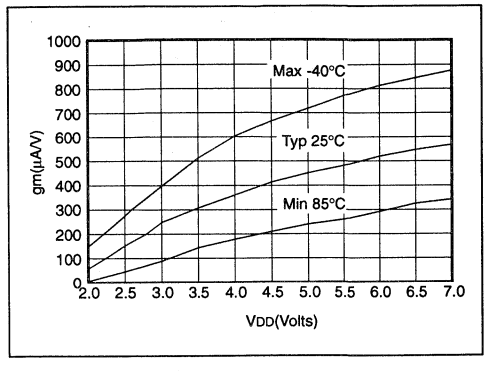


FIGURE 20-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs. VDD



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 20-22: TYPICAL XTAL STARTUP TIME vs. VDD (LP MODE, 25°C)

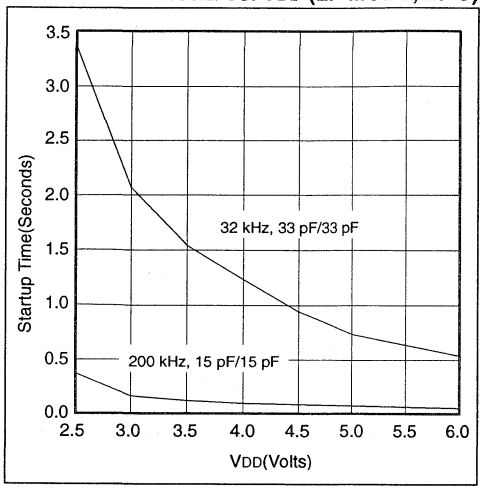

FIGURE 20-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)

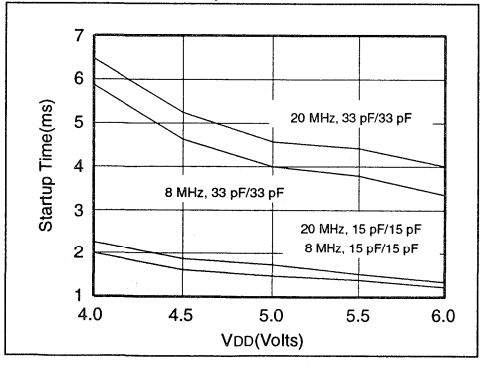

FIGURE 20-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)

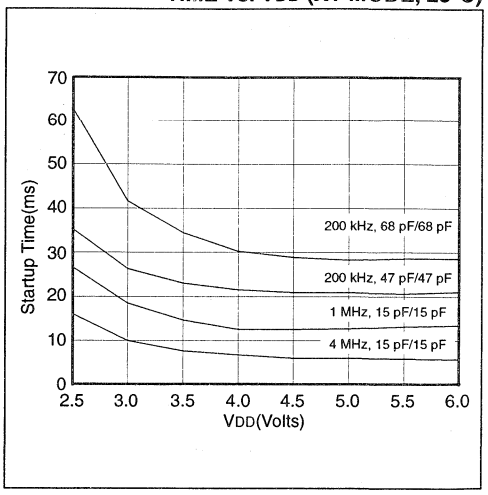

TABLE 20-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

Crystals Used		
32 kHz	Epson C-001R32.768K-A	± 20 PPM
200 kHz	STD XTL 200.000KHz	± 20 PPM
1 MHz	ECS ECS-10-13-1	± 50 PPM
4 MHz	ECS ECS-40-20-1	± 50 PPM
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM

Data based on matrix samples. See first page of this section for details.

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FIGURE 20-25: TYPICAL IDD vs. FREQUENCY (LP MODE, 25°C)

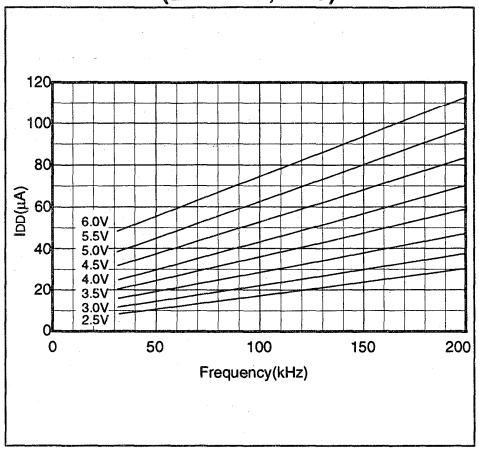


FIGURE 20-26: MAXIMUM IDD vs. FREQUENCY (LP MODE, 85°C TO -40°C)

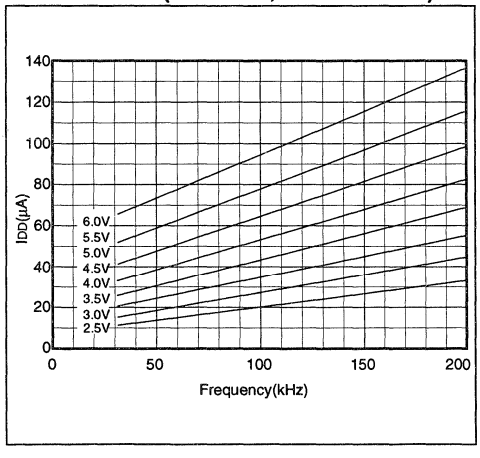


FIGURE 20-27: TYPICAL IDD vs. FREQUENCY (XT MODE, 25°C)

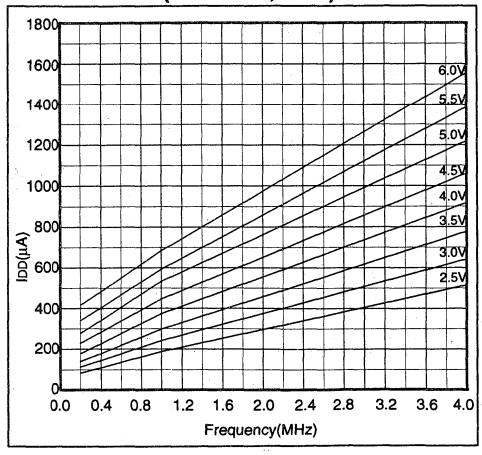
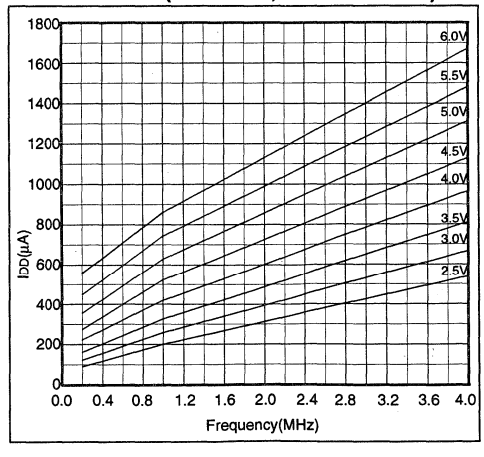


FIGURE 20-28: MAXIMUM IDD vs. FREQUENCY (XT MODE, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	61	62	62A	R62	63	64	64A	R64	65	65A

FIGURE 20-29: TYPICAL IDD vs. FREQUENCY (HS MODE, 25°C)

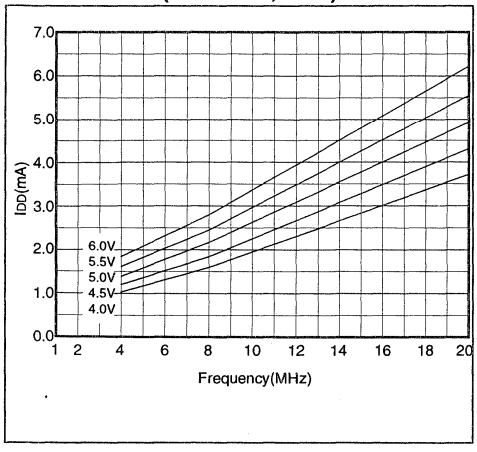
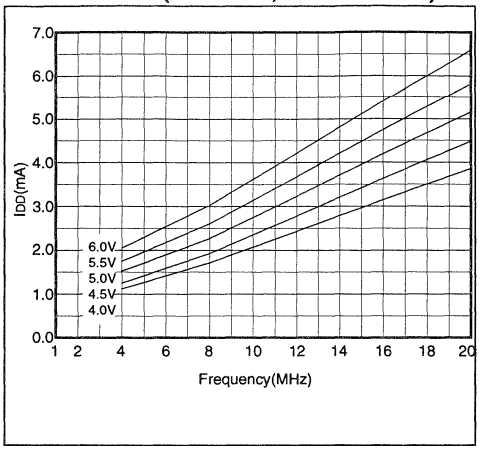


FIGURE 20-30: MAXIMUM IDD vs. FREQUENCY (HS MODE, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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APPENDIX A: MODIFICATIONS

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (192 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
3. Data memory paging is redefined slightly. STATUS register is modified.
4. Four new instructions have been added: `RETURN`, `RETFIE`, `ADDLW`, and `SUBLW`. Two instructions `TRIS` and `OPTION` are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake-up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. Timer0 pin is also a port pin (RA4/T0CKI) now.
14. FSR is made a full 8-bit register.
15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
16. Power Control register (PCON) is added with a Power-on Reset status bit ($\overline{\text{POR}}$).(Not on the PIC16C61).
17. Brown-out Reset has been added to the following devices:
    PIC16C62A/R62/63/64A/R64/65A.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for `CALL`, `GOTO`.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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APPENDIX C: WHAT'S NEW

Added characterization data for all previously uncharacterized PIC16C6X devices.

APPENDIX D: WHAT'S CHANGED

Minor changes, spelling and grammatical changes.

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PIC16C6X Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NO. -XX X /XX XXX

Pattern:	3-Digit Pattern Code for QTP (blank otherwise)		
Package:	L	=	PLCC
	P	=	PDIP
	SO	=	SOIC (Gull Wing, 300 mil body)
	PQ	=	MQFP (Metric PQFP)
	TQ	=	TQFP
	JW*	=	Windowed CERDIP
	SS	=	Shrink SOIC (Gull Wing, 300 mil body)
Temperature Range:	-	=	0°C to +70°C (T for tape/reel)
	I	=	−40°C to +85°C (S for tape/reel)
	E	=	−40°C to +125°C
Frequency Range:	04	=	200 KHz (PIC16C6X-04)
	04	=	4 MHz
	10	=	10 MHz
	20	=	20 MHz
Device:	PIC16C6X	:VDD range 4.0V to 6.0V	
	PIC16C6XT	:VDD range 4.0V to 6.0V (Tape and Reel)	
	PIC16LC6X	:VDD range 2.5V to 6.0V	
	PIC16LC6XT	:VDD range 2.5V to 6.0V (Tape and Reel)	
	PIC16CR6X	:VDD range 4.0V to 6.0V	
	PIC16CR6XT	:VDD range 4.0V to 6.0V (Tape and Reel)	
	PIC16LCR6X	:VDD range 2.5V to 6.0V	
	PIC16LCR6XT	:VDD range 2.5V to 6.0V	

Examples:

a)PIC16C61 - 04/P 301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern #301
b)PIC16LC64 - 04I/PQ = Industrial temp., MQFP package, 4 MHz, extended VDD limits
c)PIC16C65 - 10E/P = Automotive temp., PDIP package, 10 MHz, normal VDD limits

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office.
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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PIC16CR63/65

8-Bit ROM-Based Microcontroller Product Brief

Device	Program Memory	Data Memory	Pins	CCP	SSP	USART	PSP
PIC16CR63	4K x 14	192 x 8	28	2	Yes	Yes	No
PIC16CR65	4K x 14	192 x 8	40-44	2	Yes	Yes	Yes

High Performance RISC CPU:

- Simple instruction set - 35 total
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle
- ★ 4K x 14 on-chip ROM program memory
- 192 x 8 general purpose registers (SRAM)
- Eight levels of hardware stack
- Interrupt capability

Peripheral Features:

- High current sink/source
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler
- TMR1: 16-bit timer/counter (time-base for capture/compare). TMR1 can be incremented during sleep via external crystal/clock (for real-time clock)
- TMR2: 8-bit timer/counter with 8-bit period register (time-base for PWM), prescaler and postscaler
- ★ Two CCP pins that can be configured as capture input, PWM output, or compare output
  - Capture is 16-bit, max resolution 12.5 ns
  - Compare is 16-bit, max resolution 200 ns
  - PWM resolution is 1- to 10-bit. Maximum PWM frequency @: 8-bit resolution = 80 kHz, 10-bit resolution = 20 kHz
- Synchronous Serial Port (SSP) with two modes of operation:
  - 3-wire SPI™ (Supports all 4 SPI modes)
  - I^2C™ slave mode
- ★ USART (supports high and low speed) SCI
- Parallel Slave Port (PSP), 8-bits wide with external RD, WR, and CS controls (PIC16CR65 only)

Special Microcontroller Features:

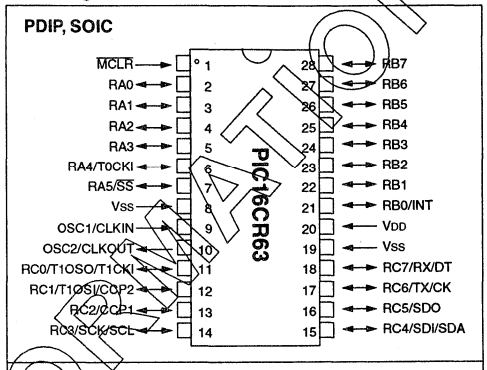
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Brown-out Reset circuitry

CMOS Technology:

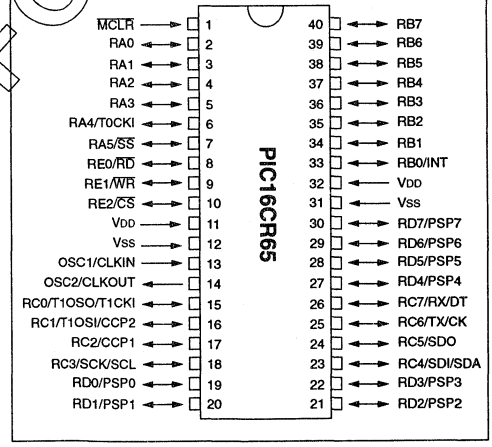
- Low-power, high-speed CMOS ROM technology
- Fully static design
- Wide operating voltage range (2.5V to 5.5V)

Pin Diagrams

PDIP, SOIC



PDIP (Also PLCC, TQFP, MQFP)



- Commercial, industrial and automotive temperature ranges
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - < 1.0 µA typical standby current @ 3.0V

ADVANCE INFORMATION

I^2C is a trademark of Philips Corporation. SPI is a trademark of Motorola Corporation.

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NOTES:

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PIC16C66/67

EPROM-Based 8-Bit Microcontroller Product Brief

Device	Program Memory	Data Memory	Pins	8-Bit A/D	CCP	SSP	USART	PSP
PIC16C66	8K x 14	368 x 8	28	–*	2	Yes	Yes	No
PIC16C67	8K x 14	368 x 8	40-44	–*	2	Yes	Yes	Yes

High Performance RISC CPU:

- Simple instruction set - 35 total
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle
- ★ 8K x 14 on-chip EPROM program memory
- ★ 368 x 8 general purpose registers (SRAM)
- Eight levels of hardware stack
- Interrupt capability

Peripheral Features:

- High current sink/source
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler
- TMR1: 16-bit timer/counter (time-base for capture/compare). TMR1 can be incremented during sleep via external crystal/clock (for real-time clock)
- TMR2: 8-bit timer/counter with 8-bit period register (time-base for PWM), prescaler and postscaler
- ★ Two CCP pins that can be configured as capture input, PWM output, or compare output
  - Capture is 16-bit, max resolution 12.5 ns
  - Compare is 16-bit, max resolution 200 ns
  - PWM resolution is 1- to 10-bit. Maximum PWM frequency @: 8-bit resolution = 80 kHz, 10-bit resolution = 20 kHz
- Synchronous Serial Port (SSP) with two modes of operation:
  - 3-wire SPI™ (Supports all 4 SPI modes)
  - I^2C™ slave mode
- ★ USART (supports high and low speed)/SCI
- Parallel Slave Port (PSP), 8-bits wide with external RD, WR, and CS controls (PIC16C67 only)

Special Microcontroller Features:

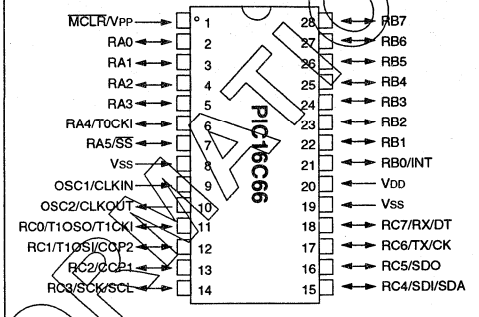
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Brown-out Reset circuitry

CMOS Technology:

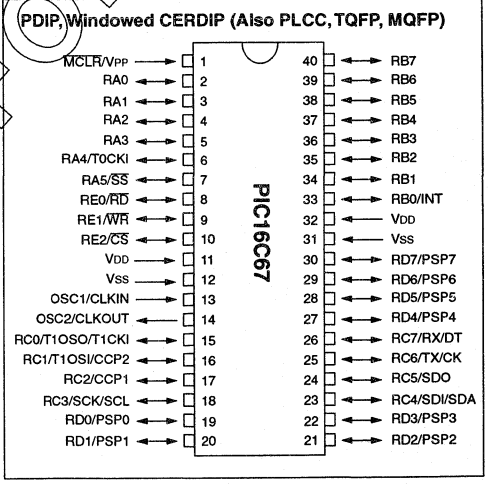
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range (2.5V to 6.0V)

Pin Diagrams

PDIP, SOIC, Windowed CERDIP



PDIP, Windowed CERDIP (Also PLCC, TQFP, MQFP)



- Commercial, industrial and automotive temperature ranges
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - < 1.0 µA typical standby current @ 3.0V

I^2C is a trademark of Philips Corporation. SPI is a trademark of Motorola Corporation. * PIC16C76/77 devices available with A/D.

ADVANCE INFORMATION

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SECTION 10
PIC16C7X MICROCONTROLLER PRODUCT SPECIFICATIONS

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PIC16CR72 28-Pin 8-Bit ROM-Based Microcontroller Product Brief 10-265
PIC16C76/77 EPROM-Based 8-Bit Microcontroller Product Brief 10-267

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MICROCHIP

PIC16C7X

8-Bit CMOS Microcontrollers with A/D Converter

Devices included in this data sheet:

- PIC16C710
- PIC16C71
- PIC16C711
- PIC16C72
- PIC16C73
- PIC16C73A
- PIC16C74
- PIC16C74A

PIC16C7X Microcontroller Core Features:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- 8-bit multichannel analog-to-digital converter
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range: 2.5V to 6.0V
- High Sink/Source Current 25/25 mA
- Commercial, Industrial and Automotive temperature ranges
- Low-power consumption:
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

PIC16C7X Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module(s)
- Capture is 16-bit, max. resolution 12.5 ns, Compare is 16-bit, max. resolution 200 ns, max. PWM resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™ and I^2C™
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bits wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIC16C7X Features	710	71	711	72	73	73A	74	74A
Program Memory (EPROM) x 14	512	1K	1K	2K	4K	4K	4K	4K
Data Memory (Bytes) x 8	36	36	68	128	192	192	192	192
I/O Pins	13	13	13	22	22	22	33	33
Parallel Slave Port	—	—	—	—	—	—	Yes	Yes
Capture/Compare/PWM Modules	—	—	—	1	2	2	2	2
Timer Modules	1	1	1	3	3	3	3	3
A/D Channels	4	4	4	5	5	5	8	8
Serial Communication	—	—	—	SPI/I^2C	SPI/I^2C, USART	SPI/I^2C, USART	SPI/I^2C, USART	SPI/I^2C, USART
In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset	Yes	—	Yes	Yes	—	Yes	—	Yes
Interrupt Sources	4	4	4	8	11	11	12	12

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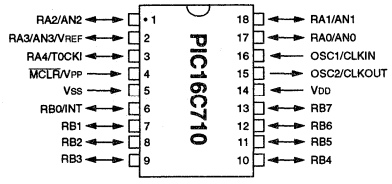
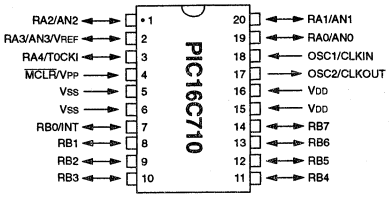
Pin Diagrams

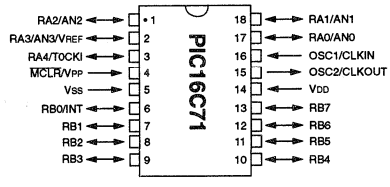
PDIP, SOIC, Windowed CERDIP



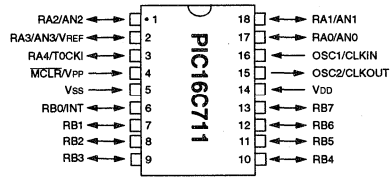
SSOP



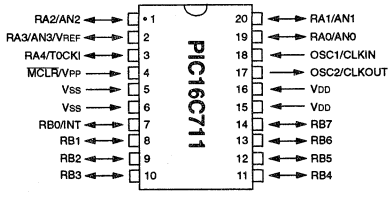
PDIP, SOIC, Windowed CERDIP



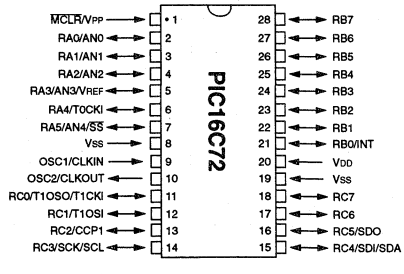
PDIP, SOIC, Windowed CERDIP



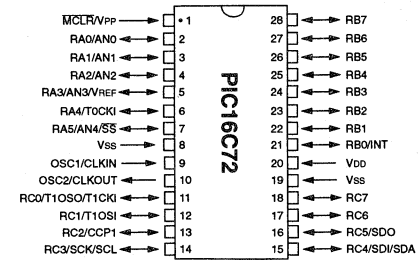
SSOP



SDIP, SOIC, Windowed Side Brazed Ceramic



SSOP



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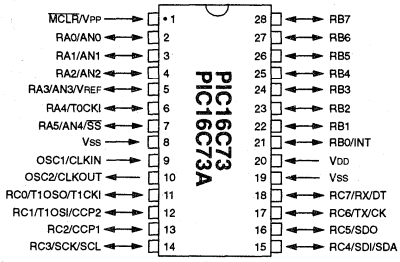
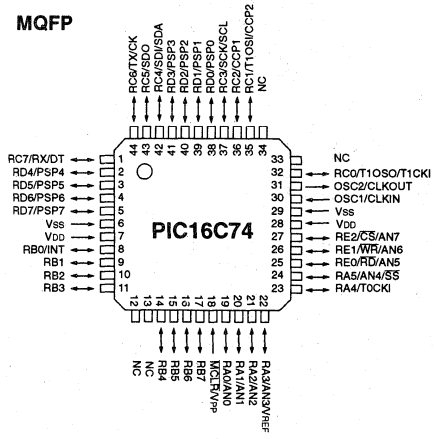
Pin Diagrams (Cont.'d)

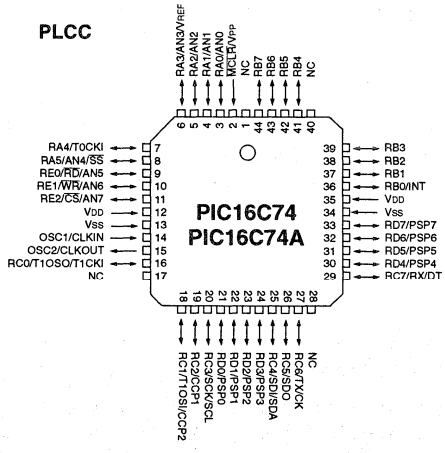
SDIP, SOIC, Windowed Side Brazed Ceramic



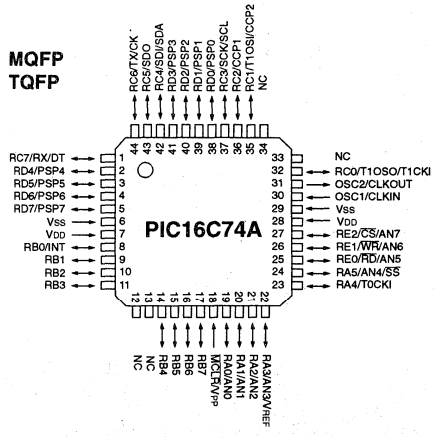
MQFP



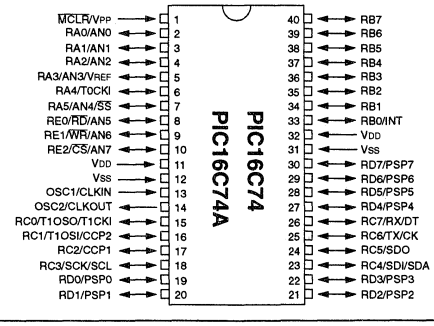
PLCC



MQFP
TQFP



PDIP, Windowed CERDIP



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For register and module descriptions in this data sheet, device legends show which devices apply to those sections. As an example, the legend below would mean that the following section applies only to the PIC16C711, PIC16C72, PIC16C73A and PIC16C74A devices.

Applicable Devices							
710	71	711	72	73	73A	74	74A

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1.0 GENERAL DESCRIPTION

The PIC16C7X is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers with integrated analog-to-digital (A/D) converters, in the PIC16CXX mid-range family.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16CXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches which require two cycles. A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C710/71** devices have 36 bytes of RAM, and the **PIC16C711** has 68 bytes of RAM. The **PIC16C710/71/711** devices have 13 I/O pins. In addition a timer/counter is available. Also a 4-channel high-speed 8-bit A/D is provided. The 8-bit resolution is ideally suited for applications requiring low-cost analog interface, e.g. thermostat control, pressure sensing, etc.

The **PIC16C72** device has 128 bytes of RAM and 22 I/O pins. In addition several peripheral features are available including: three timer/counters, one Capture/Compare/PWM module and one serial port. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. Also a 5-channel high-speed 8-bit A/D is provided. The 8-bit resolution is ideally suited for applications requiring low-cost analog interface, e.g. thermostat control, pressure sensing, etc.

The **PIC16C73/73A** devices have 192 bytes of RAM and 22 I/O pins. In addition, several peripheral features are available including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also known as the Serial Communications Interface or SCI. Also a 5-channel high-speed 8-bit A/D is provided.The 8-bit resolution is ideally suited for applications requiring low-cost analog interface, e.g. thermostat control, pressure sensing, etc.

The **PIC16C74/74A** devices have 192 bytes of RAM and 33 I/O pins. In addition several peripheral features are available including: three timer/counters, two Capture/Compare/PWM modules and two serial ports. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The Universal Synchronous Asynchronous Receiver Transmitter (USART) is also known as the Serial Communications Interface or SCI. An 8-bit Parallel Slave Port is provided. Also an 8-channel high-speed 8-bit A/D is provided. The 8-bit resolution is ideally suited for applications requiring low-cost analog interface, e.g. thermostat control, pressure sensing, etc.

The PIC16C7X family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) feature provides a power saving mode. The user can wake up the chip from SLEEP through several external and internal interrupts and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

A UV erasable CERDIP packaged version is ideal for code development while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C7X family fits perfectly in applications ranging from security and remote sensors to appliance control and automotive. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16C7X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, serial communication, capture and compare, PWM functions and coprocessor applications).

1.1 Family and Upward Compatibility

Users familiar with the PIC16C5X microcontroller family will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for the PIC16C5X can be easily ported to the PIC16CXX family of devices (Appendix B).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available. (Section 15.0)

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TABLE 1-1: PIC16C7X FAMILY OF DEVICES

	Clock	Memory			Peripherals					Features				
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (x14 words)	Data Memory (bytes)	Timer Module(s)	Capture/Compare/PWM Module(s)	Serial Port(s) (SPI/I²C, USART)	Parallel Slave Port	A/D Converter (8-bit) Channels	Interrupt Sources	I/O Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Brown-out Reset	Packages
PIC16C710	20	512	36	TMR0	—	—	—	4	4	13	3.0-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C71	20	1K	36	TMR0	—	—	—	4	4	13	3.0-6.0	Yes	—	18-pin DIP, SOIC
PIC16C711	20	1K	68	TMR0	—	—	—	4	4	13	3.0-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C72	20	2K	128	TMR0, TMR1, TMR2	1	SPI/I²C	—	5	8	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP
PIC16C73	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	—	5	11	22	3.0-6.0	Yes	—	28-pin SDIP, SOIC
PIC16C73A(1)	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	—	5	11	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16C74	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	Yes	8	12	33	3.0-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP
PIC16C74A(1)	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I²C, USART	Yes	8	12	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16C7X Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

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2.0 PIC16C7X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C7X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C7X family, there are two device "types" as indicated in the device number:

1. **C**, as in PIC16**C**74. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**74. These devices have EPROM type memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes. Microchip's PICSTART® and PRO MATE™ programmers both support the PIC16C7X. Third party programmers also are available; refer to the Microchip Third Party Guide for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

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NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM) and data memory (RAM) for each PIC16C7X device.

Device	Program Memory	Data Memory
PIC16C710	512 x 14	36 x 8
PIC16C71	1K x 14	36 x 8
PIC16C711	1K x 14	68 x 8
PIC16C72	2K x 14	128 x 8
PIC16C73	4K x 14	192 x 8
PIC16C73A	4K x 14	192 x 8
PIC16C74	4K x 14	192 x 8
PIC16C74A	4K x 14	192 x 8

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ bit and a $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

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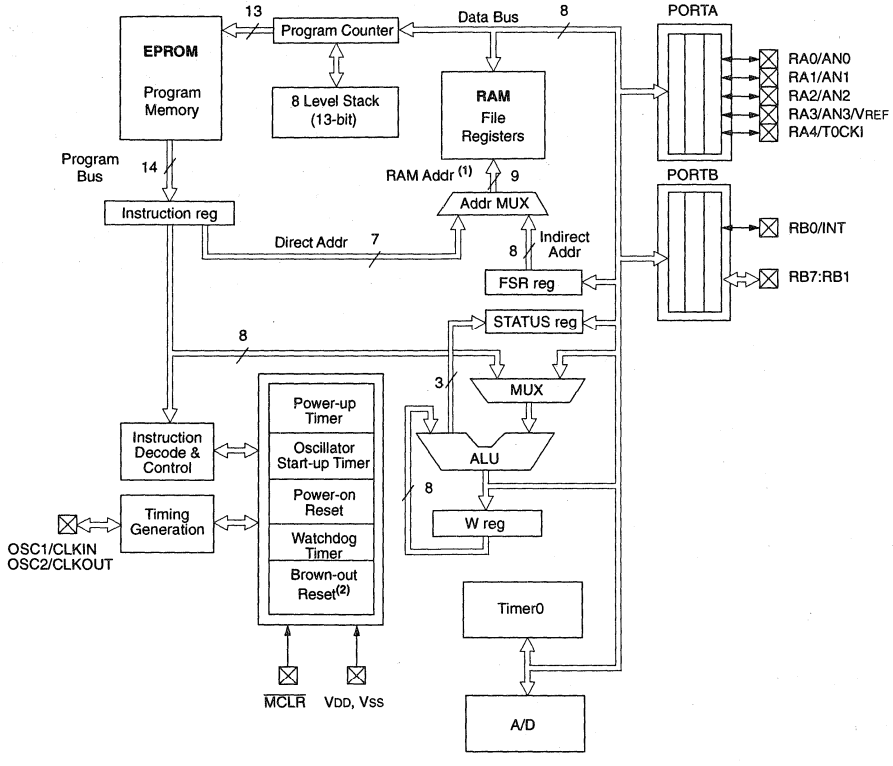
FIGURE 3-1: PIC16C710/71/711 BLOCK DIAGRAM

Device	Program Memory	Data Memory (RAM)
PIC16C710	512 x 14	36 x 8
PIC16C71	1K x 14	36 x 8
PIC16C711	1K x 14	68 x 8



Note 1: Higher order bits are from the STATUS register.
2: Brown-out Reset is not available on the PIC16C71.

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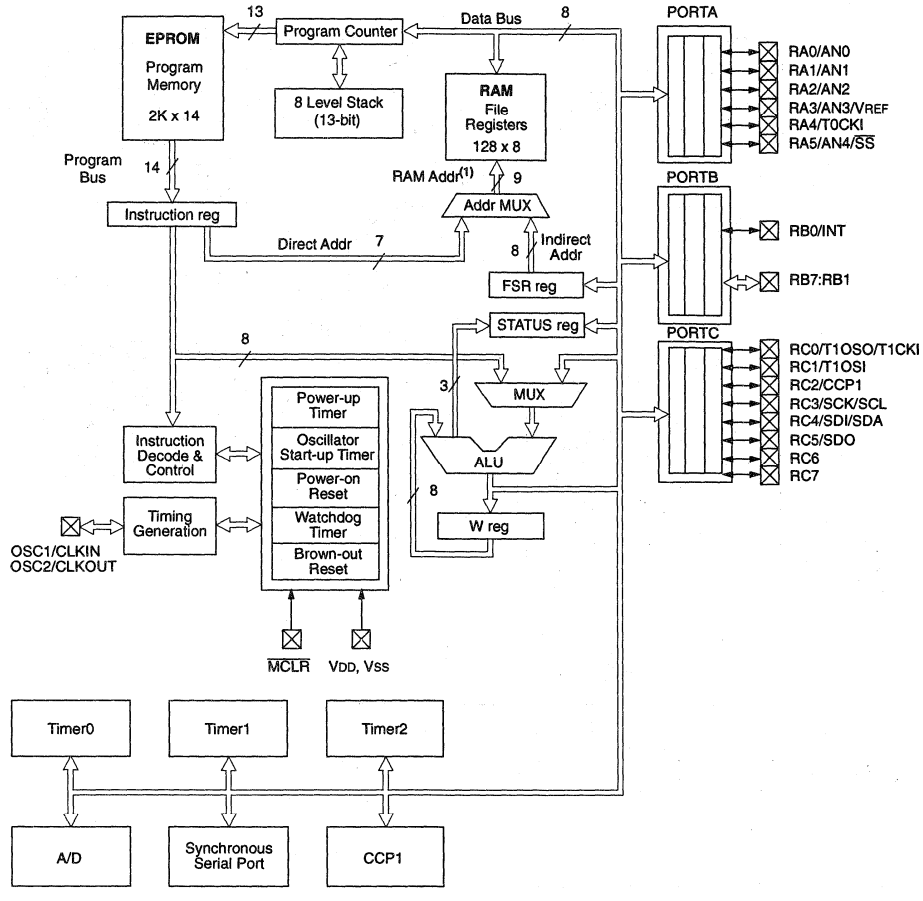
FIGURE 3-2: PIC16C72 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.

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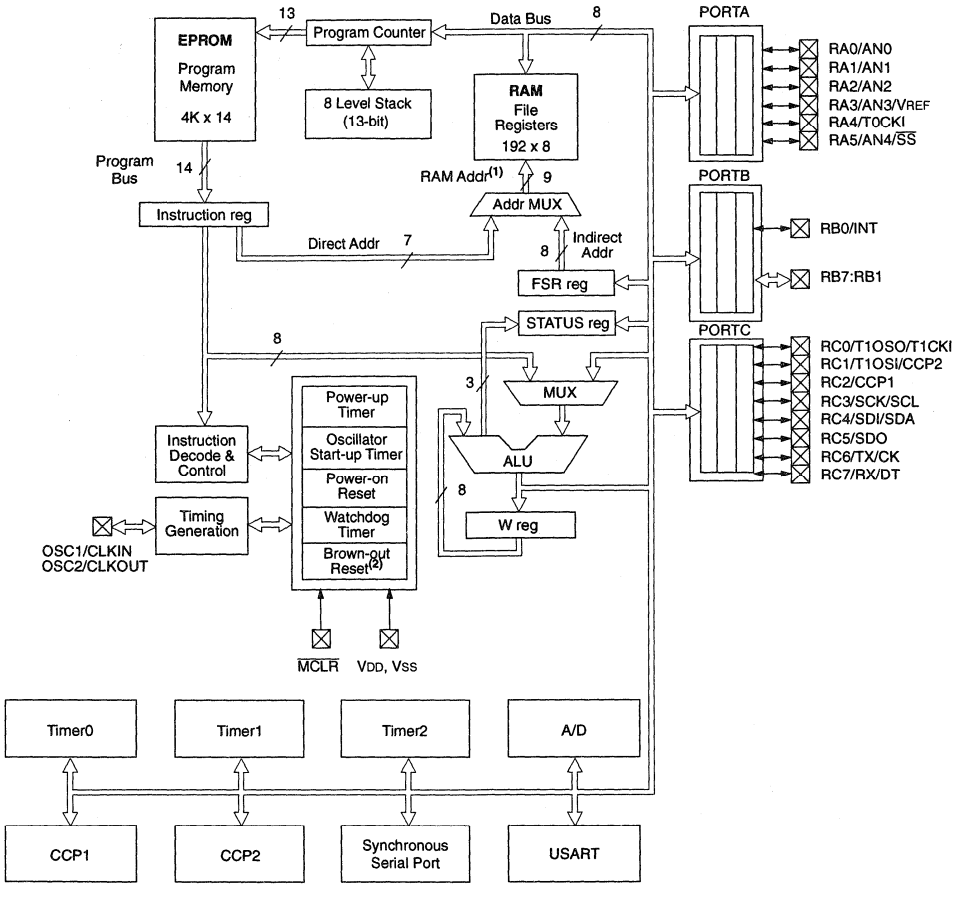
FIGURE 3-3: PIC16C73/73A BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.
2: Brown-out Reset is not available on the PIC16C73.

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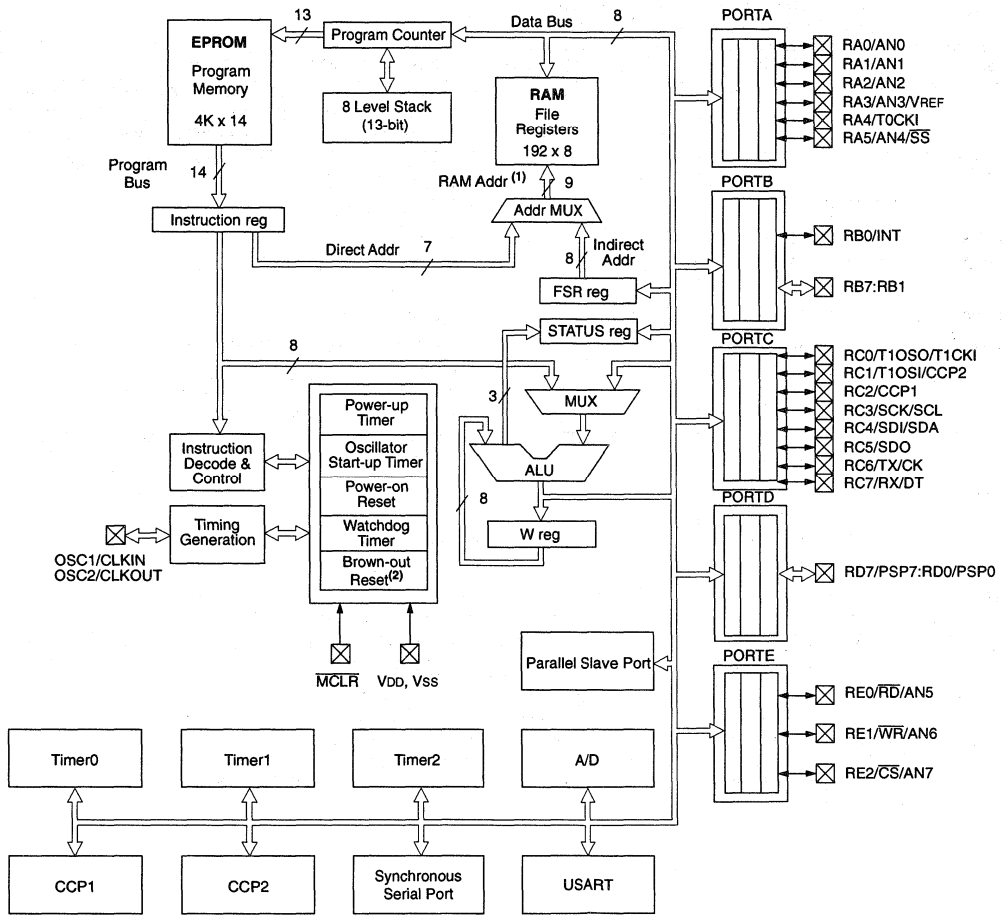
FIGURE 3-4: PIC16C74/74A BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.
2: Brown-out Reset is not available on the PIC16C74.

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TABLE 3-1: PIC16C710/711 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SSOP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	16	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	17	19	17	I/O	TTL	Analog input0
RA1/AN1	18	20	18	I/O	TTL	Analog input1
RA2/AN2	1	1	1	I/O	TTL	Analog input2
RA3/AN3/VREF	2	2	2	I/O	TTL	Analog input3/VREF
RA4/T0CKI	3	3	3	I/O	ST	Can also be selected to be the clock input to the Timer0 module. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	7	6	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	8	7	I/O	TTL	
RB2	8	9	8	I/O	TTL	
RB3	9	10	9	I/O	TTL	
RB4	10	11	10	I/O	TTL	Interrupt on change pin.
RB5	11	12	11	I/O	TTL	Interrupt on change pin.
RB6	12	13	12	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.
RB7	13	14	13	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.
VSS	5	4, 6	5	P	—	Ground reference for logic and I/O pins.
VDD	14	15, 16	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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TABLE 3-2: PIC16C71 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0/AN0	17	17	I/O	TTL	Analog input0
RA1/AN1	18	18	I/O	TTL	Analog input1
RA2/AN2	1	1	I/O	TTL	Analog input2
RA3/AN3/VREF	2	2	I/O	TTL	Analog input3/VREF
RA4/T0CKI	3	3	I/O	ST	Can also be selected to be the clock input to the Timer0 module. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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TABLE 3-3: PIC16C72 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SSOP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	9	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	1	1	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	2	2	I/O	TTL	Analog input0
RA1/AN1	3	3	3	I/O	TTL	Analog input1
RA2/AN2	4	4	4	I/O	TTL	Analog input2
RA3/AN3/VREF	5	5	5	I/O	TTL	Analog input3/VREF
RA4/T0CKI	6	6	6	I/O	ST	Can also be selected to be the clock input to the Timer0 module. Output is open drain type.
RA5/AN4/$\overline{SS}$	7	7	7	I/O	TTL	Analog input4 can also be the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	21	21	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	22	22	22	I/O	TTL	
RB2	23	23	23	I/O	TTL	
RB3	24	24	24	I/O	TTL	
RB4	25	25	25	I/O	TTL	Interrupt on change pin.
RB5	26	26	26	I/O	TTL	Interrupt on change pin.
RB6	27	27	27	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.
RB7	28	28	28	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11	11	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI	12	12	12	I/O	ST	RC1/T1OSI can also be selected as a Timer1 oscillator input.
RC2/CCP1	13	13	13	I/O	ST	RC2/CCP1 can also be selected as a Capture1 input/ Compare1 output/PWM1 output.
RC3/SCK/SCL	14	14	14	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	15	15	15	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	16	16	16	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6	17	17	17	I/O	ST	
RC7	18	18	18	I/O	ST	
VSS	8, 19	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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TABLE 3-4: PIC16C73/73A PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	1	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0/AN0	2	2	I/O	TTL	Analog input0
RA1/AN1	3	3	I/O	TTL	Analog input1
RA2/AN2	4	4	I/O	TTL	Analog input2
RA3/AN3/VREF	5	5	I/O	TTL	Analog input3/VREF
RA4/T0CKI	6	6	I/O	ST	Can also be selected to be the clock input to the Timer0 module. Output is open drain type.
RA5/AN4/$\overline{SS}$	7	7	I/O	TTL	Analog input4 can also be the slave select for the synchronous serial port.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	21	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	22	22	I/O	TTL	
RB2	23	23	I/O	TTL	
RB3	24	24	I/O	TTL	
RB4	25	25	I/O	TTL	Interrupt on change pin.
RB5	26	26	I/O	TTL	Interrupt on change pin.
RB6	27	27	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.
RB7	28	28	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.
					PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	12	12	I/O	ST	RC1/T1OSI/CCP2 can also be selected as a Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	13	13	I/O	ST	RC2/CCP1 can also be selected as a Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	14	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	15	15	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	16	16	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK	17	17	I/O	ST	RC6/TX/CK can also be selected as Asynchronous Transmit or USART Synchronous Clock.
RC7/RX/DT	18	18	I/O	ST	RC7/RX/DT can also be selected as the Asynchronous Receive or USART Synchronous Data.
VSS	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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TABLE 3-5: PIC16C74/74A PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(4)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	Analog input0
RA1/AN1	3	4	20	I/O	TTL	Analog input1
RA2/AN2	4	5	21	I/O	TTL	Analog input2
RA3/AN3/VREF	5	6	22	I/O	TTL	Analog input3/VREF
RA4/T0CKI	6	7	23	I/O	ST	Can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/AN4/$\overline{SS}$	7	8	24	I/O	TTL	Analog input4 can also be the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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TABLE 3-5: PIC16C74/74A PINOUT DESCRIPTION (Cont.'d)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1/T1OSI/CCP2 can also be selected as a Timer1 oscillator input or Capture2 input/Compare2 output/ PWM2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2/CCP1 can also be selected as a Capture1 input/ Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	24	26	43	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6/TX/CK can also be selected as Asynchronous Transmit or USART Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7/RX/DT can also be selected as the Asynchronous Receive or USART Synchronous Data.
						PORTD is a bi-directional I/O port or parallel slave port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(3)	
RD1/PSP1	20	22	39	I/O	ST/TTL(3)	
RD2/PSP2	21	23	40	I/O	ST/TTL(3)	
RD3/PSP3	22	24	41	I/O	ST/TTL(3)	
RD4/PSP4	27	30	2	I/O	ST/TTL(3)	
RD5/PSP5	28	31	3	I/O	ST/TTL(3)	
RD6/PSP6	29	32	4	I/O	ST/TTL(3)	
RD7/PSP7	30	33	5	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port.
RE0/$\overline{RD}$/AN5	8	9	25	I/O	ST/TTL(3)	RE0/$\overline{RD}$/AN5 read control for parallel slave port, or analog input5.
RE1/$\overline{WR}$/AN6	9	10	26	I/O	ST/TTL(3)	RE1/$\overline{WR}$/AN6 write control for parallel slave port, or analog input6.
RE2/$\overline{CS}$/AN7	10	11	27	I/O	ST/TTL(3)	RE2/$\overline{CS}$/AN7 select control for parallel slave port, or analog input7.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17,28, 40	12,13, 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

10

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-5.

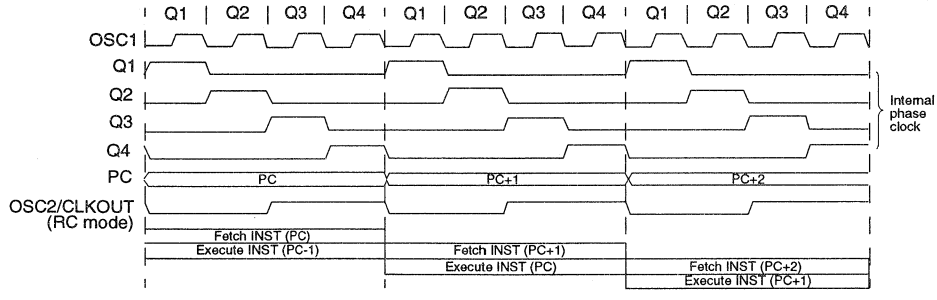
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

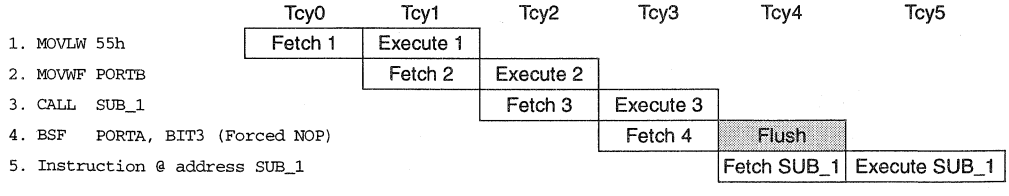
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-5: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 MEMORY ORGANIZATION

Applicable Devices							
710	71	711	72	73	73A	74	74A

4.1 Program Memory Organization

The PIC16C7X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space.

For the PIC16C710, only the first 512 x 14 (0000h-01FFh) is physically implemented. For the PIC16C71/711 only the first 1K x 14 (0000h-03FFh) is implemented. For the PIC16C72, only the first 2K x 14 (0000h-07FFh) is implemented. For the PIC16C73, PIC16C73A, PIC16C74, and PIC16C74A, only the first 4K x 14 (0000h-0FFFh) is physically implemented. Accessing a location above the physically implemented address will cause a wraparound. The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC16C710 PROGRAM MEMORY MAP AND STACK

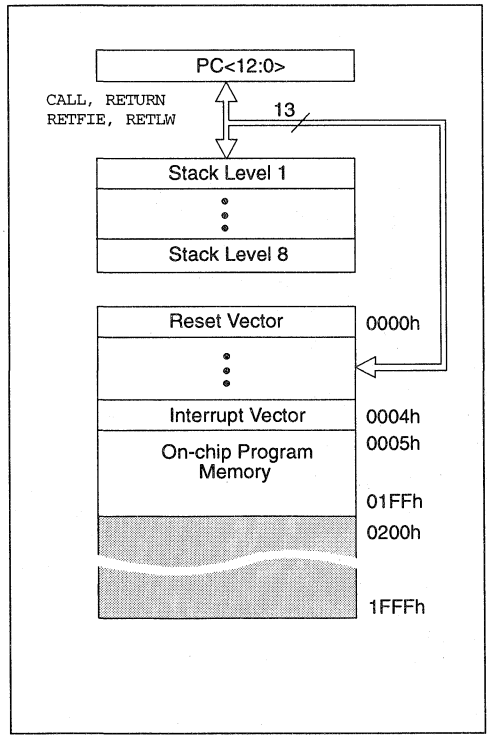

FIGURE 4-2: PIC16C71/711 PROGRAM MEMORY MAP AND STACK

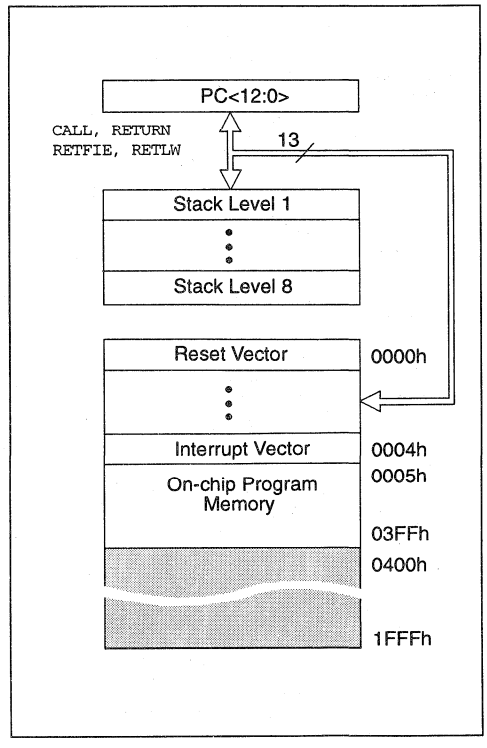

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FIGURE 4-3: PIC16C72 PROGRAM MEMORY MAP AND STACK

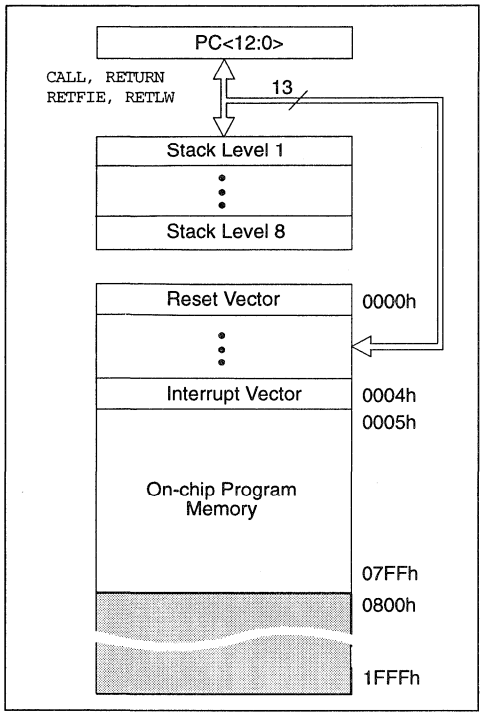
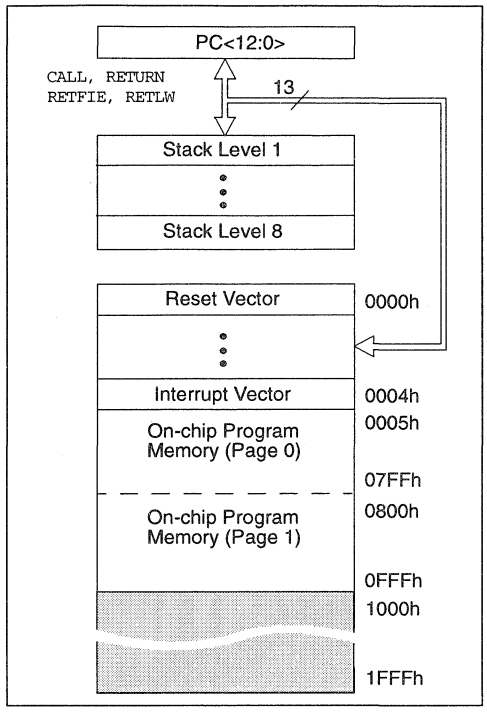


FIGURE 4-4: PIC16C73/73A/74/74A PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Applicable Devices								
710	71	711	72	73	73A	74	74A

The data memory is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bit RP0 is the bank select bit.

RP0 (STATUS<5>) = 1 → Bank 1

RP0 (STATUS<5>) = 0 → Bank 0

Each Bank extends up to 7Fh (128 bytes). The lower locations of each Bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers implemented as static RAM. Both Bank 0 and Bank 1 contain special function registers. Some "high use" special function registers from Bank 0 are mirrored in Bank 1 for code reduction and quicker access.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

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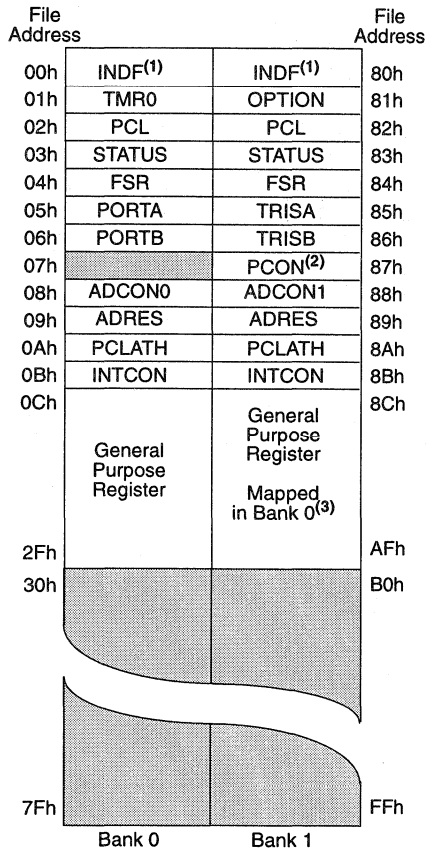
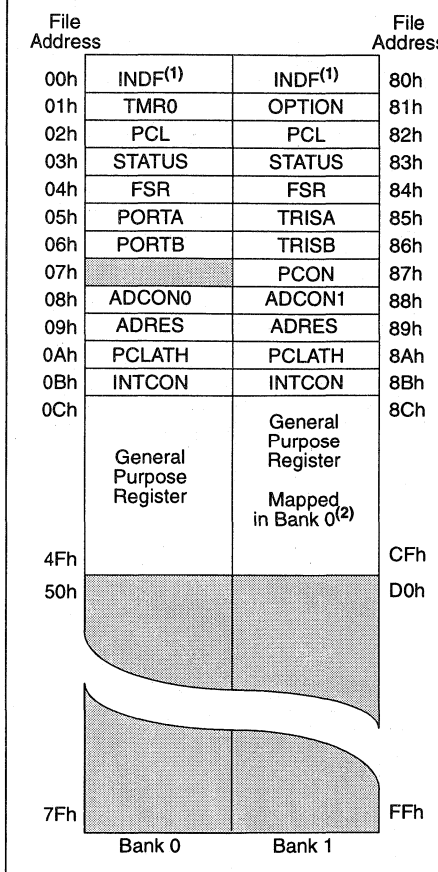
FIGURE 4-5: PIC16C710/71 REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.
2: The PCON register is not implemented on the PIC16C71.
3: These locations are unimplemented in Bank 1. Any access to these locations will access the corresponding Bank 0 register.

FIGURE 4-6: PIC16C711 REGISTER FILE MAP

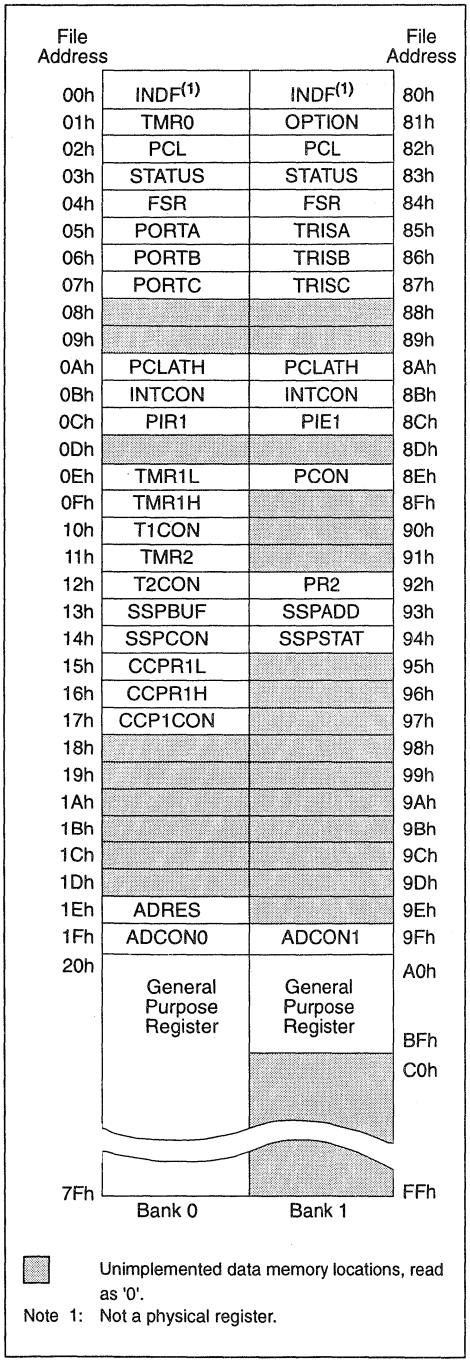


Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.
2: These locations are unimplemented in Bank 1. Any access to these locations will access the corresponding Bank 0 register.

10

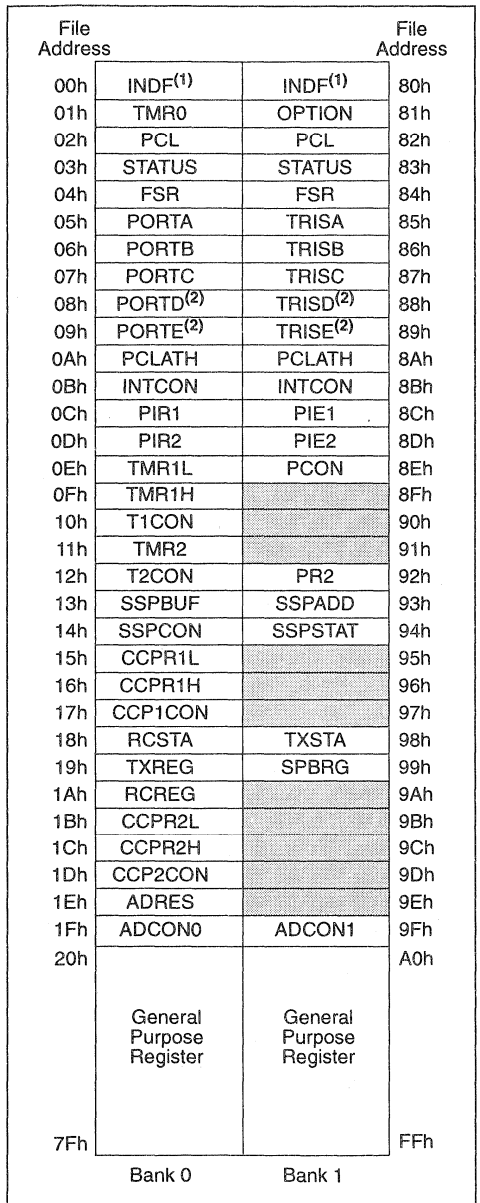
FIGURE 4-7: PIC16C72 REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

FIGURE 4-8: PIC16C73/73A/74/74A REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: These registers are not physically implemented on the PIC16C73/73A, read as '0'.

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4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). Those registers associated with the "core" functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: PIC16C710/71/711 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (1)
Bank 0											
00h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(3)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(3)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(3)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	PORTA Data Latch when written: PORTA pins when read					---x 0000	---u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	—	Unimplemented								—	—
08h	ADCON0	ADCS1	ADCS0	(6)	CHS1	CHS0	GO/$\overline{DONE}$	ADIF	ADON	00-0 0000	00-0 0000
09h(3)	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
0Ah(2,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(3)	INTCON	GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(3)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(3)	STATUS	IRP(5)	RP1(5)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(3)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111
86h	TRISB	PORTB Data Direction Control Register								1111 1111	1111 1111
87h(4)	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
88h	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	---- --00	---- --00
89h(3)	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
8Ah(2,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(3)	INTCON	GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: Other (non power-up) resets include external reset through $\overline{MCLR}$ and Watchdog Timer Reset.
2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
3: These registers can be addressed from either bank.
4: The PCON register is not physically implemented in the PIC16C71, read as '0'.
5: The IRP and RP1 bits are reserved on the PIC16C7X, always maintain these bits clear.
6: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C71 only. For the PIC16C710/711, this bit is unimplemented, read as '0'.

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TABLE 4-2: PIC16C72 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (3)
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C7X, always maintain these bits clear.

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TABLE 4-2: PIC16C72 SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (3)
Bank 1											
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(1)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC					---0 0000	---0 0000
8Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	—	Unimplemented								—	—
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.
2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
3: Other (non power-up) resets include external reset through $\overline{MCLR}$ and Watchdog Timer Reset.
4: The IRP and RP1 bits are reserved on the PIC16C7X, always maintain these bits clear.

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TABLE 4-3: PIC16C73/73A/74/74A SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 0											
00h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h(4)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h(4)	STATUS	IRP(7)	RP1(7)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h(4)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h(5)	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
09h(5)	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
0Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(4)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(3)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	–	—	—	—	CCP2IF	---- ---0	---- ---0
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
2: Other (non power-up) resets include external reset through $\overline{MCLR}$ and Watchdog Timer Reset.
3: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.
4: These registers can be addressed from either bank.
5: PORTD and PORTE are not physically implemented on the PIC16C73/73A, read as '0'.
6: Brown-out Reset is not implemented on the PIC16C73 or the PIC16C74, read as '0'.
7: The IRP and RP1 bits are reserved on the PIC16C7X, always maintain these bits clear.

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TABLE 4-3: PIC16C73/73A/74/74A SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 1											
80h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h(4)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h(4)	STATUS	IRP(7)	RP1(7)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h(4)	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h(5)	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h(5)	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
8Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh(4)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE(3)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$(6)	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
2: Other (non power-up) resets include external reset through $\overline{MCLR}$ and Watchdog Timer Reset.
3: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.
4: These registers can be addressed from either bank.
5: PORTD and PORTE are not physically implemented on the PIC16C73/73A, read as '0'.
6: Brown-out Reset is not implemented on the PIC16C73 or the PIC16C74, read as '0'.
7: The IRP and RP1 bits are reserved on the PIC16C7X, always maintain these bits clear.

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4.2.2.1 STATUS REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

The STATUS register, shown in Figure 4-9, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u uluu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

Note 1: Bits IRP and RP1 (STATUS<7:6>) are not used by the PIC16C7X and should be maintained clear. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{borrow}$ and digit $\overline{borrow}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 4-9: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)
The IRP bit is reserved on the PIC16C7X, always maintain this bit clear.

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h - 1FFh)
`10` = Bank 2 (100h - 17Fh)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)
Each bank is 128 bytes. The RP1 bit is reserved on the PIC16C7X, always maintain this bit clear.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

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4.2.2.2 OPTION REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer by setting bit PSA (OPTION<3>).

FIGURE 4-10: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.2.2.3 INTCON REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT Pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-11: INTCON REGISTER FOR PIC16C710/71/711 (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:**(1) Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **ADIE**: A/D Converter Interrupt Enable bit
1 = Enables A/D interrupt
0 = Disables A/D interrupt

bit 5: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note 1: For the PIC16C71, if an interrupt occurs while the GIE bit is being cleared, the GIE bit may be unintentionally re-enabled by the `RETFIE` instruction in the user's Interrupt Service Routine. Refer to Section 14.5 for a detailed description.

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FIGURE 4-12: INTCON REGISTER FOR PIC16C72/73/73A/74/74A (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R	= Readable bit
W	= Writable bit
U	= Unimplemented bit, read as '0'
- n	= Value at POR reset

bit 7: **GIE:**(1) Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note 1: For the PIC16C73 and PIC16C74, if an interrupt occurs while the GIE bit is being cleared, the GIE bit may be unintentionally re-enabled by the `RETFIE` instruction in the user's Interrupt Service Routine. Refer to Section 14.5 for a detailed description.

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4.2.2.4 PIE1 REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

This register contains the individual enable bits for the Peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

FIGURE 4-13: PIE1 REGISTER PIC16C72 (ADDRESS 8Ch)

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6: **ADIE**: A/D Converter Interrupt Enable bit
1 = Enables the A/D interrupt
0 = Disables the A/D interrupt

bit 5-4: **Unimplemented**: Read as '0'

bit 3: **SSPIE**: Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE**: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE**: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: **TMR1IE**: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

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FIGURE 4-14: PIE1 REGISTER PIC16C73/73A/74/74A (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIE(1):** Parallel Slave Port Read/Write Interrupt Enable bit
1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

bit 6: **ADIE:** A/D Converter Interrupt Enable bit
1 = Enables the A/D interrupt
0 = Disables the A/D interrupt

bit 5: **RCIE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4: **TXIE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3: **SSPIE:** Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Note 1: PIC16C73 and PIC16C73A devices do not have a Parallel Slave Port implemented, this bit location is reserved on these two devices, always maintain this bit clear.

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4.2.2.5 PIR1 REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

This register contains the individual flag bits for the Peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-15: PIR1 REGISTER PIC16C72 (ADDRESS 0Ch)

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6: **ADIF**: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed
0 = The A/D conversion is not complete

bit 5-4: **Unimplemented**: Read as '0'

bit 3: **SSPIF**: Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete
0 = Waiting to transmit/receive

bit 2: **CCP1IF**: CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

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FIGURE 4-16: PIR1 REGISTER PIC16C73/73A/74/74A (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIF(1):** Parallel Slave Port Read/Write Interrupt Flag bit
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

bit 6: **ADIF**: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed
0 = The A/D conversion is not complete

bit 5: **RCIF**: USART Receive Interrupt Flag bit
1 = The USART receive buffer is full
0 = The USART receive buffer is empty

bit 4: **TXIF**: USART Transmit Interrupt Flag bit
1 = The USART transmit buffer is empty
0 = The USART transmit buffer is full

bit 3: **SSPIF**: Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete
0 = Waiting to transmit/receive

bit 2: **CCP1IF**: CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Note 1: PIC16C73 and PIC16C73A devices do not have a Parallel Slave Port implemented, this bit location is reserved on these two devices, always maintain this bit clear.

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4.2.2.6 PIE2 REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

This register contains the individual enable bit for the CCP2 peripheral interrupt.

FIGURE 4-17: PIE2 REGISTER (ADDRESS 8Dh)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-1: **Unimplemented:** Read as '0'

bit 0: **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

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4.2.2.7 PIR2 REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

This register contains the CCP2 interrupt flag bit.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-18: PIR2 REGISTER (ADDRESS 0Dh)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-1: **Unimplemented:** Read as '0'

bit 0: **CCP2IF**: CCP2 Interrupt Flag bit

Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

PWM Mode
Unused

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4.2.2.8 PCON REGISTER

Applicable Devices							
710	71	711	72	73	73A	74	74A

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external $\overline{MCLR}$ Reset or WDT Reset. It also contains a status bit to determine if a Brown-out Reset (BOR) occurred.

Note: $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

FIGURE 4-19: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-q
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}^{(1)}$
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1: **$\overline{POR}$**: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0: **$\overline{BOR}^{(1)}$**: Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: Brown-out Reset is not implemented on the PIC16C73/74.

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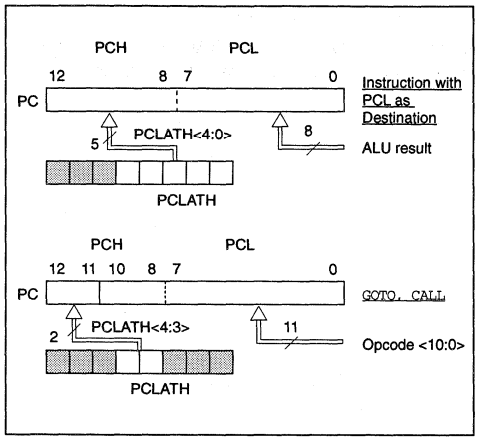
4.3 PCL and PCLATH

Applicable Devices							
710	71	711	72	73	73A	74	74A

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-20 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-20: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16CXX family has an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

4.4 Program Memory Paging

Applicable Devices							
710	71	711	72	73	73A	74	74A

The PIC16C73/73A and the PIC16C74/74A have 4K of program memory, but the CALL and GOTO instructions only have a 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 4K program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (Figure 4-20). When doing a CALL or GOTO instruction, the user must ensure that this page bit (PCLATH<3>) is programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is PUSHed onto the stack. Therefore, manipulation of the PCLATH<3> is not required for the return instructions (which POPs the address from the stack).

Note 1: The PIC16C710/71/711/72 ignore both paging bits (PCLATH<4:3>, which are used to access program memory when more than one page is available. The use of PCLATH<4:3> as general purpose read/write bits for the PIC16C7X is not recommended since this may affect upward compatibility with future products.

The PIC16C73/73A/74/74A ignores paging bit (PCLATH<4>), which is used to access program memory pages 2 and 3 (1000h - 1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

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Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0x500
BSF     PCLATH,3  ;Select page 1 (800h-FFFh)
CALL    SUB1_P1   ;Call subroutine in
        :         ;page 1 (800h-FFFh)
        :
        :
ORG 0x900
SUB1_P1:          ;called subroutine
        :         ;page 1 (800h-FFFh)
        :
RETURN            ;return to Call subroutine
                  ;in page 0 (000h-7FFh)
```

4.5 Indirect Addressing, INDF and FSR Registers

Applicable Devices							
710	71	711	72	73	73A	74	74A

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

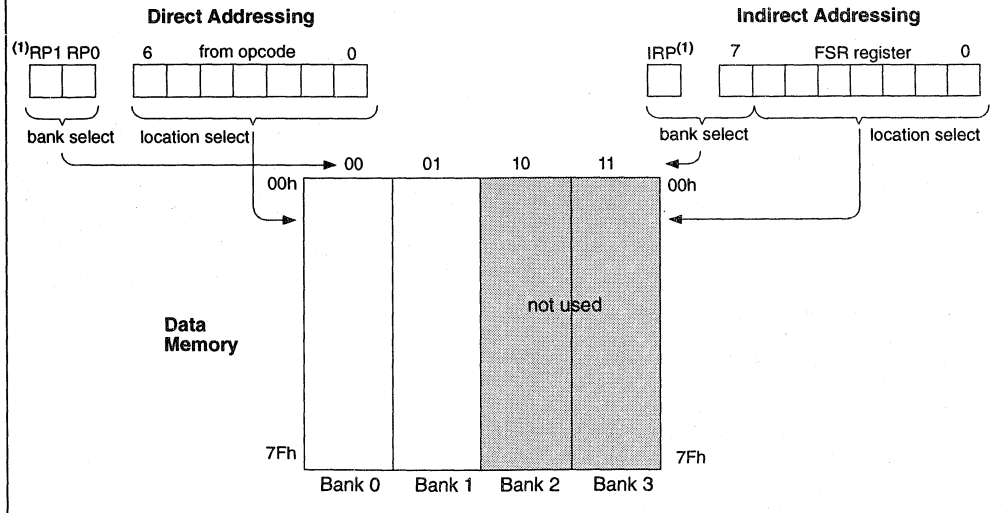
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-21. However, IRP is not used in the PIC16C7X.

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR,F   ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;no clear next
CONTINUE
        :               ;yes continue
```

FIGURE 4-21: DIRECT/INDIRECT ADDRESSING



For register file map detail see Figure 4-5, Figure 4-6, Figure 4-7, and Figure 4-8.

Note 1: The RP1 and IRP bits are reserved, always maintain these bits clear.

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5.0 I/O PORTS

Applicable Devices								
710	71	711	72	73	73A	74	74A	

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

5.1 PORTA and TRISA Registers

Applicable Devices								
710	71	711	72	73	73A	74	74A	

PORTA is a 5-bit latch for PIC16C710/71/711.

PORTA is a 6-bit latch for PIC16C72/73/73A/74/74A.

The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a TRISA register bit puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin.

Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

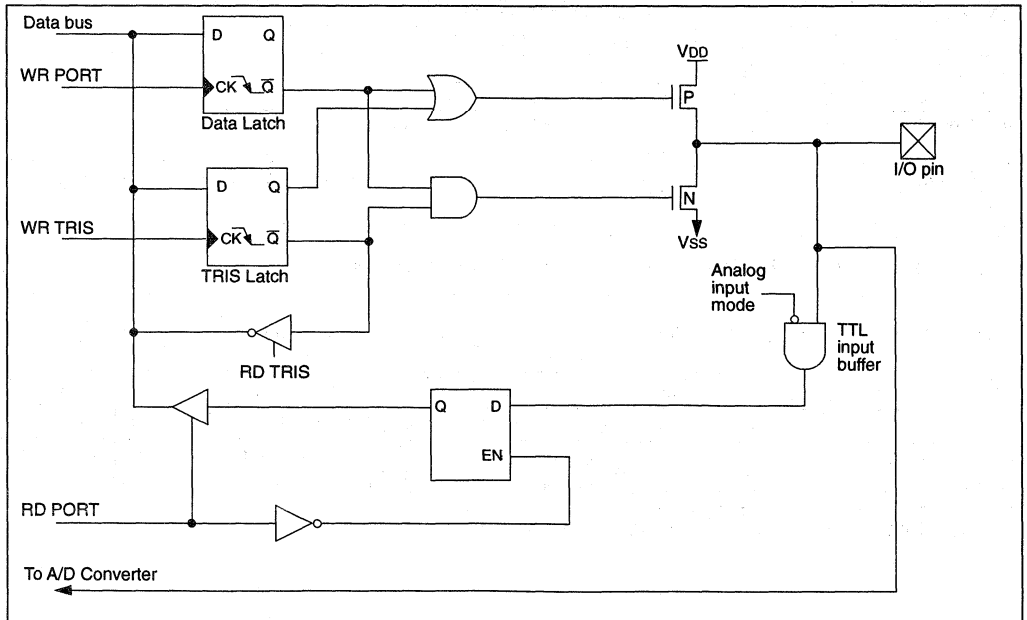
Note: On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF    PORTA           ; Initialize PORTA by
                        ; clearing output
                        ; data latches
BSF     STATUS, RP0     ; Select Bank 1
MOVLW   0xCF            ; Value used to
                        ; initialize data
                        ; direction
MOVWF   TRISA           ; Set RA<3:0> as inputs
                        ; RA<5:4> as outputs
                        ; TRISA<7:6> are always
                        ; read as '0'.
```

FIGURE 5-1: BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS



Note: I/O pin has protection diodes to VDD and VSS. The PIC16C710/71/711 devices do not have a pin RA5.

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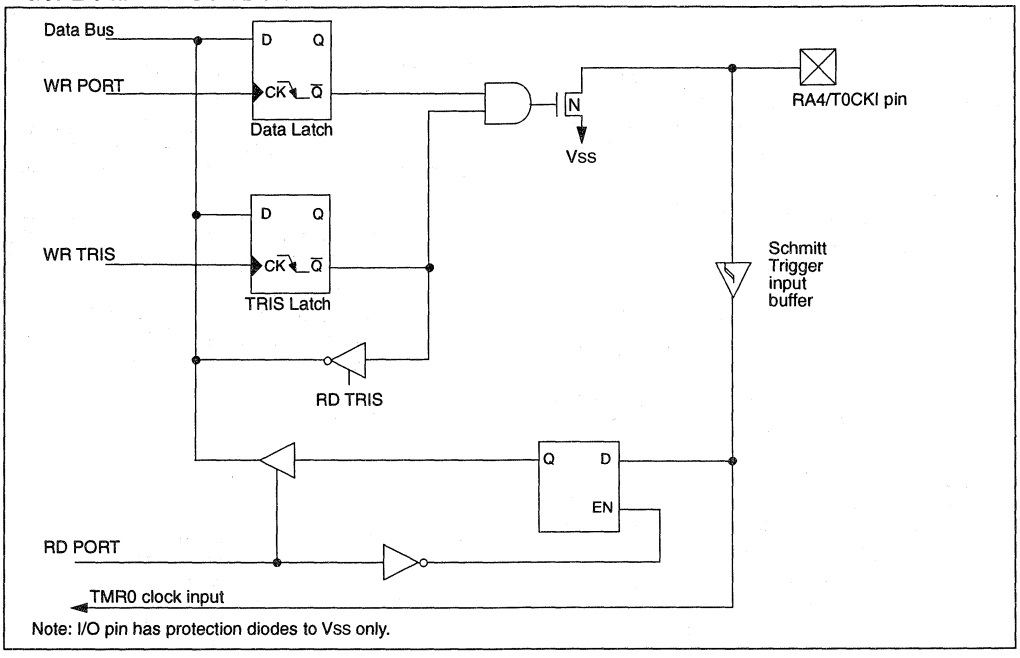
FIGURE 5-2: BLOCK DIAGRAM OF RA4/T0CKI PIN



Note: I/O pin has protection diodes to Vss only.

TABLE 5-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input/VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/AN4/$\overline{SS}$ (1)	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input

Legend: TTL = TTL input, ST = Schmitt Trigger input
Note 1: The PIC16C710/71/711 does not have PORTA<5> or TRISA<5>, read as '0'.

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	RA5(1)	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	TRISA5(1)	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
9Fh	ADCON1	—	—	—	—	—	PCFG2(2)	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.
Note 1: PORTA<5> and TRISA<5> are not implemented on the PIC16C710/71/711.
2: Bit PCFG2 is not implemented on the PIC16C710/71/711.

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5.2 PORTB and TRISB Registers

Applicable Devices								
710	71	711	72	73	73A	74	74A

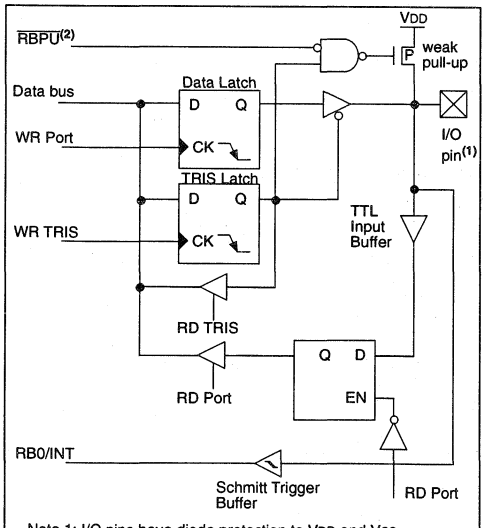
PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a bit in the TRISB register puts the corresponding output driver in a hi-impedance input mode. Clearing a bit in the TRISB register puts the contents of the output latch on the selected pin(s).

EXAMPLE 5-2: INITIALIZING PORTB

```
CLRF    PORTB           ; Initialize PORTB by
                        ; clearing output
                        ; data latches
BSF     STATUS, RP0     ; Select Bank 1
MOVLW   0xCF            ; Value used to
                        ; initialize data
                        ; direction
MOVWF   TRISB           ; Set RB<3:0> as inputs
                        ; RB<5:4> as outputs
                        ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBPU}}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

FIGURE 5-3: BLOCK DIAGRAM OF RB3:RB0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if $\overline{\text{RBPU}}$ = '0' (OPTION<7>).

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.
b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

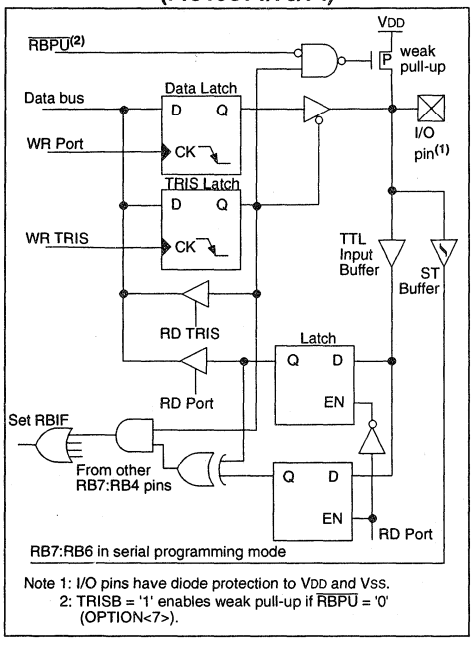
This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a keypad and make it possible for wake-up on key-depression. Refer to the Embedded Control Handbook, *"Implementing Wake-Up on Key Stroke"* (AN552).

Note: For the PIC16C71/73/74 if a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then interrupt flag bit RBIF may not get set.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

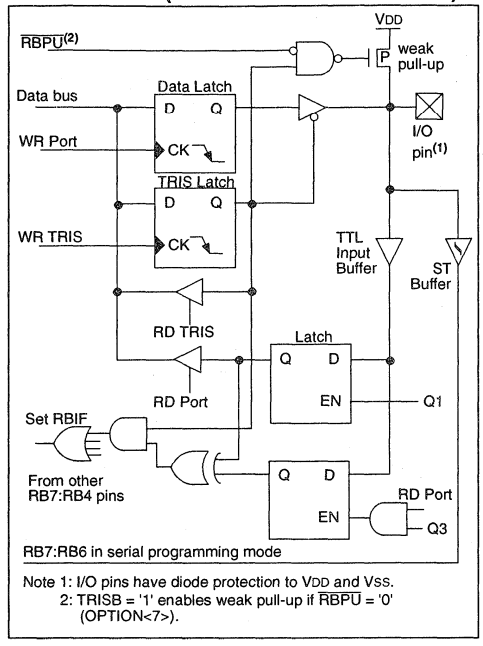
10

FIGURE 5-4: BLOCK DIAGRAM OF RB7:RB4 PINS (PIC16C71/73/74)



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if $\overline{RBPU}$ = '0' (OPTION<7>).

FIGURE 5-5: BLOCK DIAGRAM OF RB7:RB4 PINS (PIC16C710/711/72/73A/74A)



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if $\overline{RBPU}$ = '0' (OPTION<7>).

TABLE 5-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.

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TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

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5.3 PORTC and TRISC Registers

Applicable Devices							
710	71	711	72	73	73A	74	74A

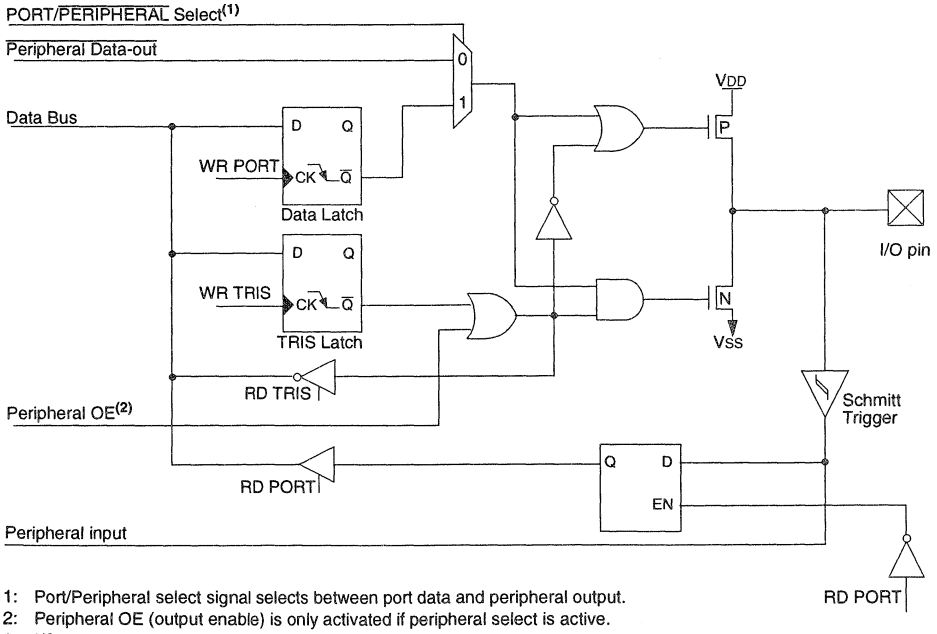
PORTC is an 8-bit bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

EXAMPLE 5-3: INITIALIZING PORTC

```
CLRF    PORTC       ; Initialize PORTC by
                    ; clearing output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISC       ; Set RC<3:0> as inputs
                    ; RC<5:4> as outputs
                    ; RC<7:6> as inputs
```

FIGURE 5-6: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only activated if peripheral select is active.
3: I/O pins have diode protection to VDD and VSS.

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TABLE 5-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input
RC1/T1OSI/CCP2(1)	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output
RC6/TX/CK(2)	bit6	ST	Input/output port pin or USART Asynchronous Transmit, or USART Synchronous Clock
RC7/RX/DT(2)	bit7	ST	Input/output port pin or USART Asynchronous Receive, or USART Synchronous Data

Legend: ST = Schmitt Trigger input

Note 1: The CCP2 multiplexed function is not enabled on the PIC16C72.

2: The TX/CK and RX/DT multiplexed functions are not enabled on the PIC16C72.

TABLE 5-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged.

10

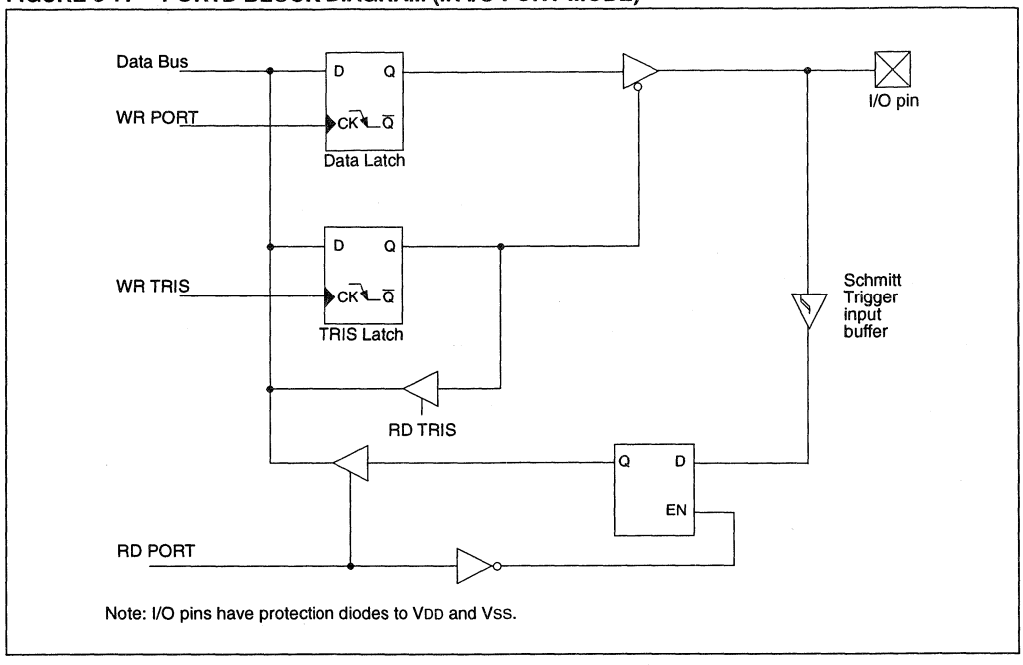
5.4 PORTD and TRISD Registers

Applicable Devices							
710	71	711	72	73	73A	74	74A

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 5-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and VSS.

TABLE 5-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL(1)	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL(1)	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL(1)	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL(1)	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL(1)	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL(1)	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL(1)	Input/output port pin or parallel slave port bit7

Legend: ST = Schmitt Trigger input TTL = TTL input
Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffer when in Parallel Slave Port Mode.

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TABLE 5-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTD.

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5.5 PORTE and TRISE Register

Applicable Devices							
710	71	711	72	73	73A	74	74A

PORTE has three pins RE0/$\overline{RD}$/AN5, RE1/$\overline{WR}$/AN6 and RE2/$\overline{CS}$/AN7, which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs) and that register ADCON1 is configured for digital I/O. In this mode the input buffers are TTL.

Figure 5-8 shows the TRISE register, which also controls the parallel slave port operation.

PORTE pins are multiplexed with analog inputs. The operation of these pins is selected by control bits in the ADCON1 register. When selected as an analog input, these pins will read as '0's.

TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note: On a Power-on Reset these pins are configured as analog inputs.

FIGURE 5-8: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IBF:** Input Buffer Full Status bit
1 = A word has been received and waiting to be read by the CPU
0 = No word has been received

bit 6: **OBF**: Output Buffer Full Status bit
1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5: **IBOV**: Input Buffer Overflow Detect bit (in microprocessor mode)
1 = A write occurred when a previously input word has not been read (must be cleared in software)
0 = No overflow occurred

bit 4: **PSPMODE**: Parallel Slave Port Mode Select bit
1 = Parallel slave port mode
0 = General purpose I/O mode

bit 3: **Unimplemented**: Read as '0'

bit 2: **TRISE2**: Direction control bit for pin RE2/$\overline{CS}$/AN7
1 = Input
0 = Output

bit 1: **TRISE1**: Direction control bit for pin RE1/$\overline{WR}$/AN6
1 = Input
0 = Output

bit 0: **TRISE0**: Direction control bit for pin RE0/$\overline{RD}$/AN5
1 = Input
0 = Output

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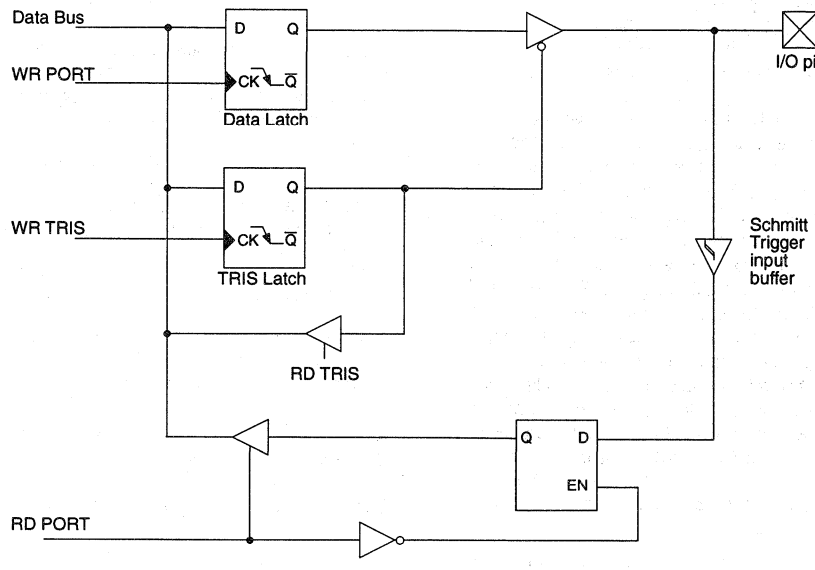
FIGURE 5-9: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and VSS.

TABLE 5-9: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/$\overline{RD}$/AN5	bit0	ST/TTL(1)	Input/output port pin or read control input in parallel slave port mode or analog input: $\overline{RD}$ 1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
RE1/$\overline{WR}$/AN6	bit1	ST/TTL(1)	Input/output port pin or write control input in parallel slave port mode or analog input: $\overline{WR}$ 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected)
RE2/$\overline{CS}$/AN7	bit2	ST/TTL(1)	Input/output port pin or chip select control input in parallel slave port mode or analog input: $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input TTL = TTL input
Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port Mode.

TABLE 5-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTE.

10

5.6 I/O Programming Considerations

Applicable Devices							
710	71	711	72	73	73A	74	74A

5.6.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched to an output, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-4 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 5-4: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

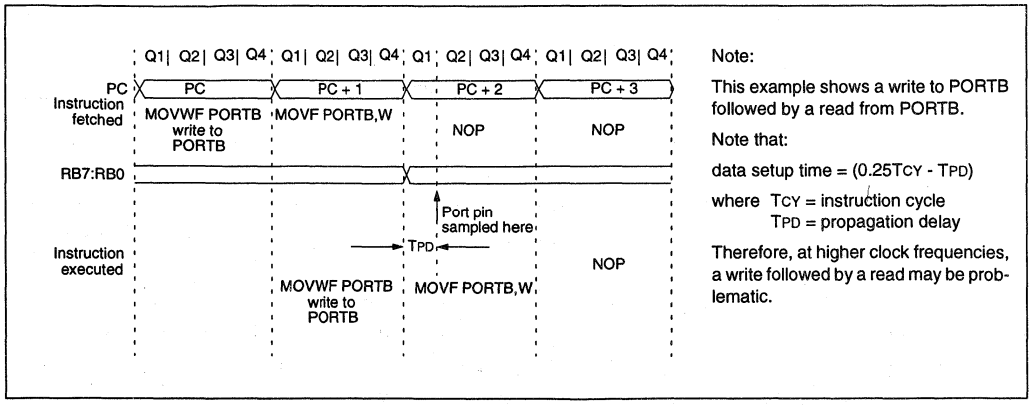
```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                       PORT latch  PORT pins
;                       ----------  ---------
  BCF PORTB, 7      ; 01pp pppp    11pp pppp
  BCF PORTB, 6      ; 10pp pppp    11pp pppp
  BSF STATUS, RP0   ;
  BCF TRISB, 7      ; 10pp pppp    11pp pppp
  BCF TRISB, 6      ; 10pp pppp    10pp pppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-10). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-10: SUCCESSIVE I/O OPERATION



Note:

This example shows a write to PORTB followed by a read from PORTB.

Note that:

data setup time = (0.25TCY - TPD)

where TCY = instruction cycle
TPD = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

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5.7 Parallel Slave Port

Applicable Devices							
710	71	711	72	73	73A	74	74A

PORTD operates as an 8-bit wide Parallel Slave Port, or microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through $\overline{RD}$ control input pin RE0/$\overline{RD}$/AN5 and $\overline{WR}$ control input pin RE1/$\overline{WR}$/AN6.

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/$\overline{RD}$/AN5 to be the $\overline{RD}$ input, RE1/$\overline{WR}$/AN6 to be the $\overline{WR}$ input and RE2/$\overline{CS}$/AN7 to be the $\overline{CS}$ (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set) and the A/D port configuration bits PCFG2:PCFG0 (ADCON1<2:0>) must be set, which will configure pins RE2:RE0 as digital I/O.

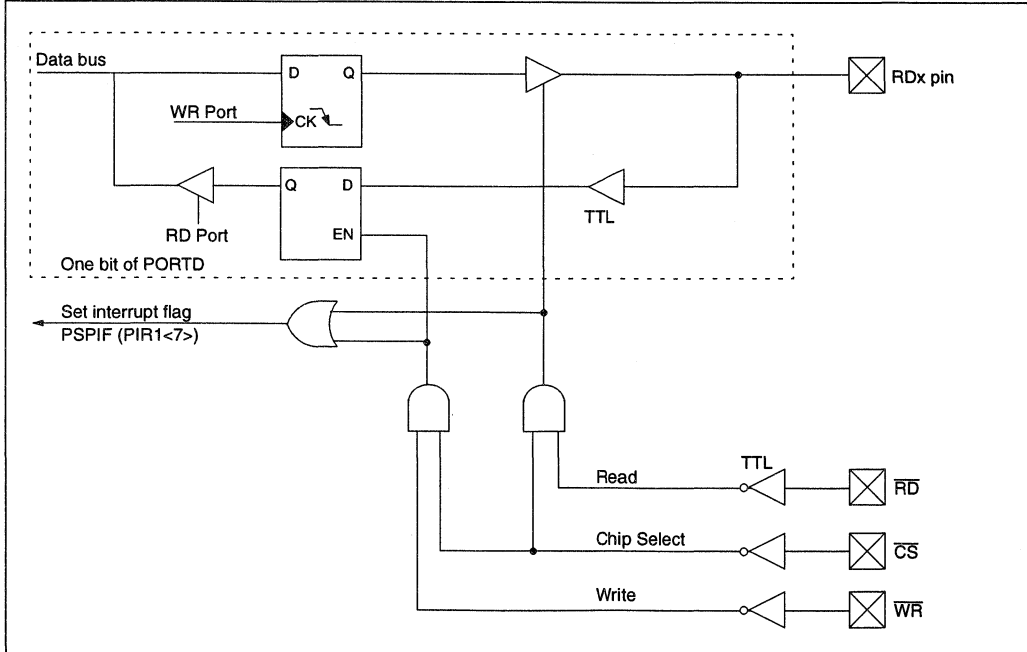
There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored, since the microprocessor is controlling the direction of data flow.

Input Buffer Full Status Flag bit IBF (TRISE<7>), is set if a received word is waiting to be read by the CPU. Once the PORTD input latch is read, IBF is cleared. IBF is a read only status bit. Output Buffer Full Status Flag bit OBF (TRISE<6>), is set if a word written to PORTD latch is waiting to be read by the external bus. Once the PORTD output latch is read by the microprocessor, OBF is cleared. Input Buffer Overflow Status Flag bit IBOV (TRISE<5>) is set if a second write to the microprocessor port is attempted when the previous word has not been read by the CPU (the first word is retained in the buffer).

When not in Parallel Slave Port mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in the software.

An interrupt is generated and latched into flag bit PSPIF (PIR1<7>) when a read or a write operation is completed. Interrupt flag bit PSPIF must be cleared by user software and the interrupt can be disabled by clearing interrupt enable bit PSPIE (PIE1<7>).

FIGURE 5-11: PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE PORT)



Note: I/O pins have protection diodes to VDD and VSS.

TABLE 5-11: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	PSP7	PSP6	PSP5	PSP4	PSP3	PSP2	PSP1	PSP0	xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111
0Ch	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Parallel Slave Port.

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6.0 OVERVIEW OF TIMER MODULES

Applicable Devices							
710	71	711	72	73	73A	74	74A

The PIC16C710 and PIC16C71/711 have one timer module.

The PIC16C72, PIC16C73/73A and PIC16C74/74A each have three timer modules.

Each module can generate an interrupt to indicate that an event has occurred (i.e. timer overflow). Each of these modules is explained in full detail in the following sections. The timer modules are:

- Timer0 Module (Section 7.0)
- Timer1 Module (Section 8.0)
- Timer2 Module (Section 9.0)

6.1 Timer0 Overview

Applicable Devices							
710	71	711	72	73	73A	74	74A

The Timer0 module (previously known as RTCC) is a simple 8-bit overflow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. Timer0 can increment at the following rates: 1:1 (when prescaler assigned to Watchdog timer), 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256 (Timer0 only).

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

6.2 Timer1 Overview

Applicable Devices							
710	71	711	72	73	73A	74	74A

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock (Fosc/4), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

Timer1 also has a prescaler option which allows Timer1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. Timer1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit Capture or the 16-bit Compare and must be synchronized to the device.

6.3 Timer2 Overview

Applicable Devices							
710	71	711	72	73	73A	74	74A

Timer2 is an 8-bit timer with a programmable prescaler and postscaler, as well as an 8-bit period register (PR2). Timer2 can be used with the CCP1 module (in PWM mode) as well as the Baud Rate Generator for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, 1:16.

The postscaler allows the TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP Overview

Applicable Devices							
710	71	711	72	73	73A	74	74A

The CCP module(s) can operate in one of these three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or the sixteenth rising edge of the CCPx pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs an interrupt can be generated, and the output pin CCPx can be forced to given state (High or Low), TMR1 can be reset (CCP1), or TMR1 reset and start A/D conversion (CCP2). This depends on the control bits CCPxM3:CCPxM0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPRxH:CCPRxL<5:4>) as well as to an 8-bit period register (PR2). When the TMR2 register = Duty Cycle register, the CCPx pin will be forced low. When TMR2 = PR2, TMR2 is cleared to 00h, an interrupt can be generated, and the CCPx pin (if an output) will be forced high.

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NOTES:

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7.0 TIMER0 MODULE

Applicable Devices								
710	71	711	72	73	73A	74	74A

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit T0CS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

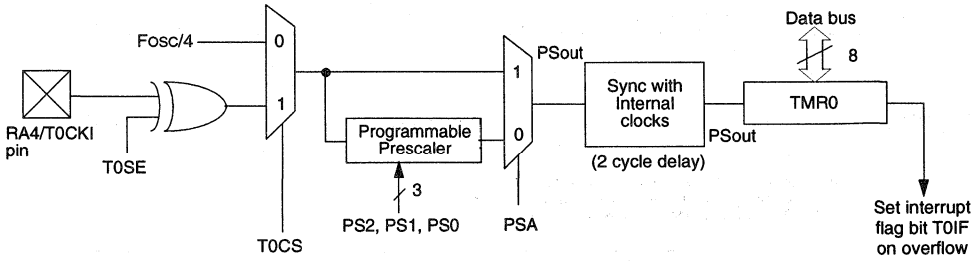
The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 Timer0 Interrupt

Applicable Devices								
710	71	711	72	73	73A	74	74A

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for Timer0 interrupt timing.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS2:PS0 (OPTION<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 7-6 for detailed block diagram).

FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

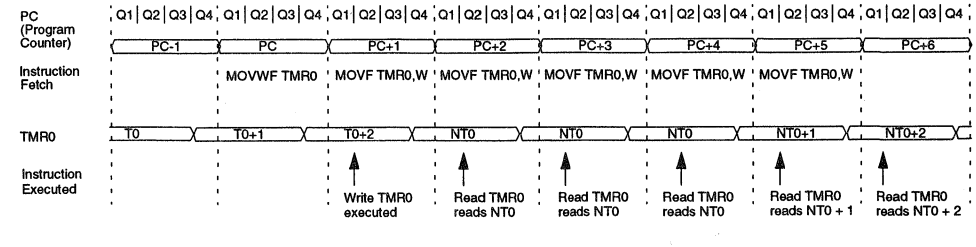


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FIGURE 7-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

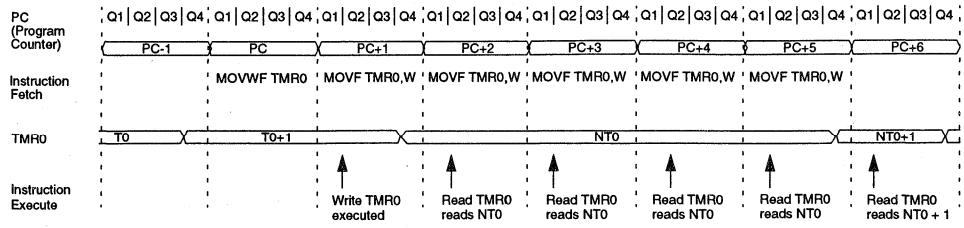
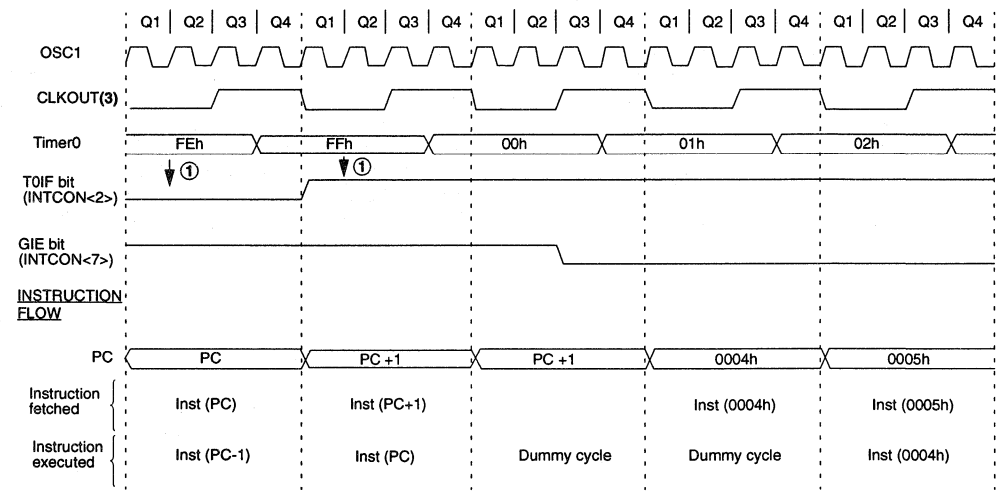


FIGURE 7-4: TIMER0 INTERRUPT TIMING



Note 1: Interrupt flag bit T0IF is sampled here (every Q1).
2: Interrupt latency = 4Tcy where Tcy = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.

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7.2 Using Timer0 with an External Clock

Applicable Devices							
710	71	711	72	73	73A	74	74A

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

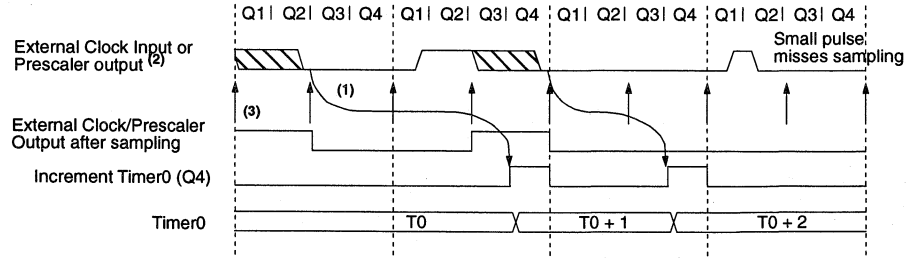
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TMR0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

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7.3 Prescaler

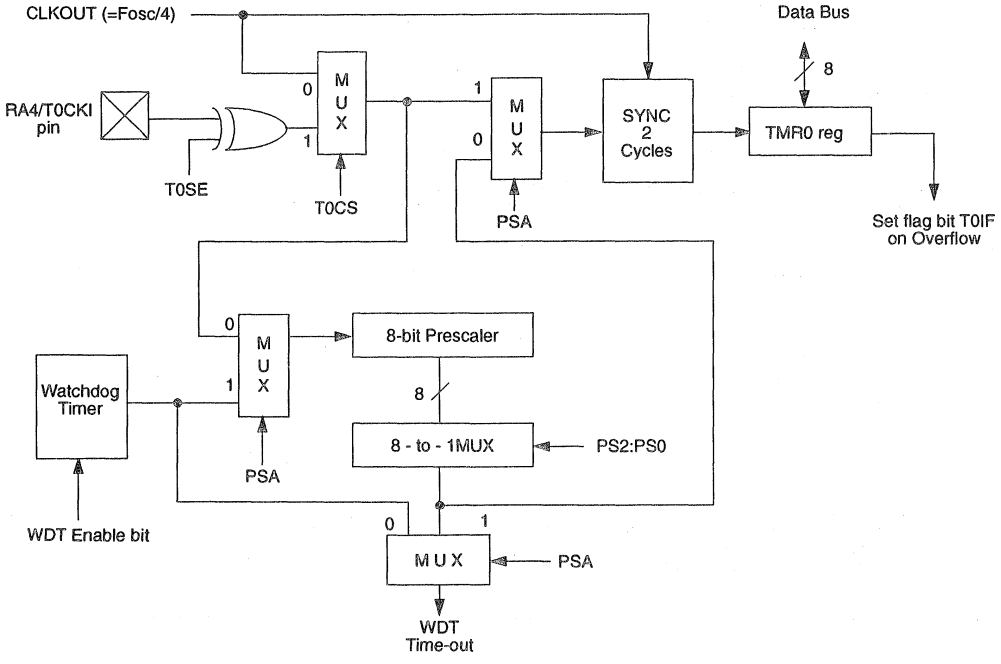
Applicable Devices							
710	71	711	72	73	73A	74	74A

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. `CLRF 1`, `MOVWF 1`, `BSF 1,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 7-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are (OPTION<5:0>).

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7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution.

Note: To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS, RP0  ;Bank 0
CLRF    TMR0         ;Clear TMR0 & Prescaler
BSF     STATUS, RP0  ;Bank 1
CLRWDT               ;Clears WDT
MOVLW   b'xxxx1xxx'  ;Select new prescale
MOVWF   OPTION_REG   ;value & WDT
BCF     STATUS, RP0  ;Bank 0
```

To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 7-2.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT               ;Clear WDT and
                     ;prescaler
BSF     STATUS, RP0  ;Bank 1
MOVLW   b'xxxx0xxx'  ;Select TMR0, new
                     ;prescale value and
MOVWF   OPTION_REG   ;clock source
BCF     STATUS, RP0  ;Bank 0
```

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0, PIC16C710/71/711

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

TABLE 7-2: REGISTERS ASSOCIATED WITH TIMER0, PIC16C72/73/73A/74/74A

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

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NOTES:

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8.0 TIMER1 MODULE

Applicable Devices								
710	71	711	72	73	73A	74	74A

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. The TMR1 Register pair (TMR1H + TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input on pin RC0/T1OSO/T1CKI.

Timer1 can be turned on and off using the control bit TMR1ON (T1CON<0>).

Timer1 also has an internal "reset input". This reset can be generated by either of the two CCP modules (Section 10.0). Figure 8-1 shows the Timer1 control register.

For the PIC16C72/73A/74A, when the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI/CCP2 and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored.

For the PIC16C73/74, when the Timer1 oscillator is enabled (T1OSCEN is set), RC1/T1OSI/CCP2 pin becomes an input, however the RC0/T1OSO/T1CKI pin will have to be configured as an input by setting the TRISC<0> bit.

FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off
Note: The oscillator inverter and feedback resistor are turned off to eliminate power drain

bit 2: **$\overline{\text{T1SYNC}}$**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input

TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit
1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)
0 = Internal clock (Fosc/4)

bit 0: **TMR1ON**: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

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8.1 Timer1 Operation in Timer Mode

Applicable Devices							
710	71	711	72	73	73A	74	74A

Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is FOSC/4. The synchronize control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 Timer1 Operation in Synchronized Counter Mode

Applicable Devices							
710	71	711	72	73	73A	74	74A

Counter mode is selected by setting bit TMR1CS. In this mode the timer increments on every rising edge of clock input on pin RC1/T1OSI/CCP2 when bit T1OSCEN is set or pin RC0/T1OSO/T1CKI when bit T1OSCEN is cleared.

If $\overline{\text{T1SYNC}}$ is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple-counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if the external clock is present, since the synchronization circuit is shut off. The prescaler however will continue to increment.

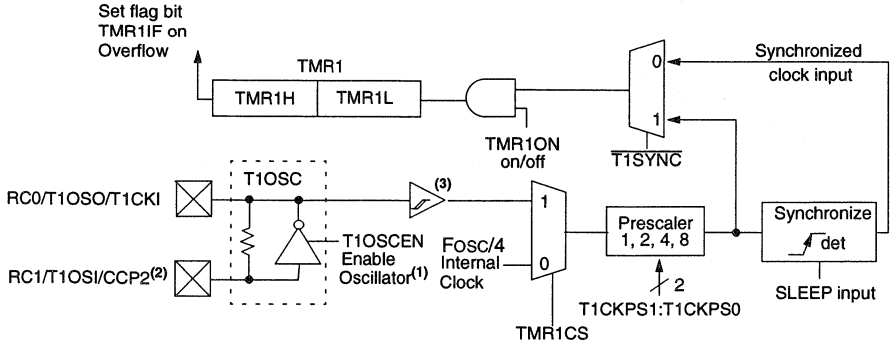
8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

When an external clock input is used for Timer1 in synchronized counter mode, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of TMR1 after synchronization.

When the prescaler is 1:1, the external clock input is the same as the prescaler output. The synchronization of T1CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T1CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the appropriate electrical specifications, parameters 45, 46, and 47.

When a prescaler other than 1:1 is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. In order for the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T1CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T1CKI high and low time is that they do not violate the minimum pulse width requirements of 10 ns). Refer to the appropriate electrical specifications, parameters 40, 42, 45, 46, and 47.

FIGURE 8-2: TIMER1 BLOCK DIAGRAM



Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.
2: The CCP2 module is not implemented in the PIC16C72.
3: For the PIC16C73 and PIC16C74, the Schmitt Trigger is not implemented in external clock mode.

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8.3 Timer1 Operation in Asynchronous Counter Mode

Applicable Devices								
710	71	711	72	73	73A	74	74A	

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 8.3.2).

In asynchronous counter mode, Timer1 can not be used as a time-base for capture or compare operations.

8.3.1 EXTERNAL CLOCK INPUT TIMING WITH UNSYNCHRONIZED CLOCK

If control bit $\overline{\text{T1SYNC}}$ is set, the timer will increment completely asynchronously. The input clock must meet certain minimum high time and low time requirements. Refer to the appropriate Electrical Specifications Section, timing parameters 45, 46, and 47.

8.3.2 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running, from an external asynchronous clock, will guarantee a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

```
; All interrupts are disabled
   MOVF   TMR1H, W  ;Read high byte
   MOVWF  TMPH      ;
   MOVF   TMR1L, W  ;Read low byte
   MOVWF  TMPL      ;
   MOVF   TMR1H, W  ;Read high byte
   SUBWF  TMPH,  W  ;Sub 1st read
                    ; with 2nd read
   BTFSC  STATUS,Z  ;Is result = 0
   GOTO   CONTINUE  ;Good 16-bit read
;
; TMR1L may have rolled over between the read
; of the high and low bytes. Reading the high
; and low bytes now will read a good value.
;
   MOVF   TMR1H, W  ;Read high byte
   MOVWF  TMPH      ;
   MOVF   TMR1L, W  ;Read low byte
   MOVWF  TMPL      ;
; Re-enable the Interrupt (if required)
CONTINUE            ;Continue with your code
```

8.4 Timer1 Oscillator

Applicable Devices								
710	71	711	72	73	73A	74	74A	

A crystal oscillator circuit is built in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

TABLE 8-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz(1)	15 pF	15 pF
	100 kHz	15 pF	15 pF
	200 kHz	0 - 15 pF	0 - 15 pF
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.			
Crystals Tested:			
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM	
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM	
200 kHz	STD XTL 200.000 kHz	± 20 PPM	

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8.5 Resetting Timer1 using a CCP Trigger Output

Applicable Devices							
710	71	711	72	73	73A	74	74A

The CCP2 module is not implemented on the PIC16C72 device.

If the CCP1 or CCP2 module is configured in compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1.

Note: The special event triggers from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL registers pair effectively becomes the period register for Timer1.

8.6 Resetting of Timer1 Register Pair (TMR1H, TMR1L)

Applicable Devices							
710	71	711	72	73	73A	74	74A

TMR1H and TMR1L registers are not reset on a POR or any other reset except by the CCP1 and CCP2 special event triggers.

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset. In any other reset, the register is unaffected.

8.7 Timer1 Prescaler

Applicable Devices							
710	71	711	72	73	73A	74	74A

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1,2)	ADIF	RCIF(2)	TXIF(2)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1,2)	ADIE	RCIE(2)	TXIE(2)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

2: The PIC16C72 does not have a Parallel Slave Port or a USART, these bits are unimplemented, read as '0'.

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9.0 TIMER2 MODULE

Applicable Devices							
710	71	711	72	73	73A	74	74A

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device reset.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4 or 1:16 (selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is set during RESET.

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 9-2 shows the Timer2 control register.

9.1 Timer2 Prescaler and Postscaler

Applicable Devices							
710	71	711	72	73	73A	74	74A

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device reset (Power-on Reset, $\overline{MCLR}$ reset, Watchdog Timer reset, or Brown-out Reset

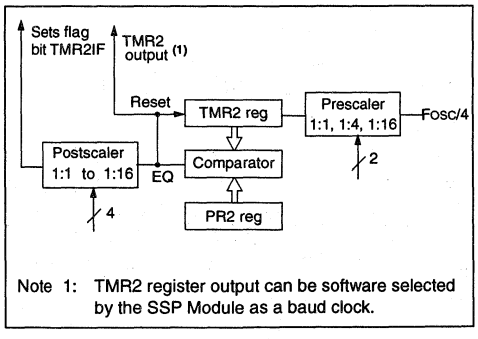
TMR2 will not clear when T2CON is written, only for a WDT, POR, $\overline{MCLR}$, and BOR reset.

9.2 Output of TMR2

Applicable Devices							
710	71	711	72	73	73A	74	74A

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

FIGURE 9-1: TIMER2 BLOCK DIAGRAM



Note 1: TMR2 register output can be software selected by the SSP Module as a baud clock.

10

FIGURE 9-2: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2: **TMR2ON**: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0: **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1,2)	ADIF	RCIF(2)	TXIF(2)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1,2)	ADIE	RCIE(2)	TXIE(2)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.
2: The PIC16C72 does not have a Parallel Slave Port or a USART, these bits are unimplemented, read as '0'.

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10.0 CAPTURE/COMPARE/PWM MODULE(s)

Applicable Devices									
710	71	711	72	73	73A	74	74A	CCP1
710	71	711	72	73	73A	74	74A	CCP2

Each CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register or as a PWM master/slave Duty Cycle register. Both the CCP1 and CCP2 modules are identical in operation, with the exception of the operation of the special event trigger. Table 10-1 and Table 10-2 show the resources and interactions of the CCP module(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

CCP2 module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

For use of the CCP modules, refer to the Embedded Control Handbook, *"Using the CCP Modules"* (AN594).

TABLE 10-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

TABLE 10-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base.
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1.
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1.
PWM	PWM	The PWMs will have the same frequency, and update rate (TMR2 interrupt).
PWM	Capture	None
PWM	Compare	None

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FIGURE 10-1: CCP1CON REGISTER (ADDRESS 17h)/CCP2CON REGISTER (ADDRESS 1Dh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX:CCPxY**: PWM Least Significant bits
Capture Mode: Unused
Compare Mode: Unused
PWM Mode: These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits
0000 = Capture/Compare/PWM off (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set; CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled))
11xx = PWM mode

10.1 Capture Mode

Applicable Devices							
710	71	711	72	73	73A	74	74A

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1. An event is defined as:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

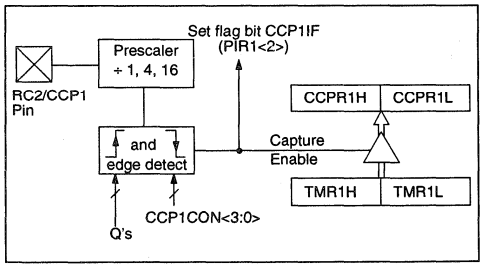
An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

10.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting its corresponding TRIS bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

FIGURE 10-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP module to use the capture feature. In asynchronous counter mode, the capture operation may not work.

10.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in operating mode.

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10.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON      ;Turn CCP module off
MOVLW   NEW_CAPT_PS  ;Load the W reg with
                     ; the new prescaler
                     ; mode value and CCP ON
MOVWF   CCP1CON      ;Load CCP1CON with this
                     ; value
```

10.2 Compare Mode

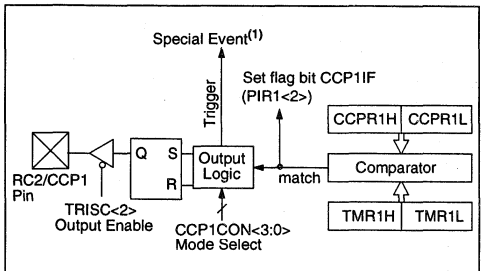
Applicable Devices							
710	71	711	72	73	73A	74	74A

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven High
- Driven Low
- Remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, a compare interrupt is also generated.

FIGURE 10-3: COMPARE MODE OPERATION BLOCK DIAGRAM



Note 1: For CCP1 (if enabled), reset Timer1, but not set TMR1IF(PIR<0>).
For CCP2 (if enabled), reset Timer1, but not set TMR1IF(PIR<0>), and set bit GO/$\overline{\text{DONE}}$ (ADCON0<2>), which starts an A/D conversion.

10.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

10.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

10.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

10.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special trigger output of CCP2 resets the TMR1 register pair, and starts an A/D conversion (if the A/D module is enabled).

For the PIC16C72 only, the special event trigger output of CCP1 resets the TMR1 register pair, and starts an A/D conversion (if the A/D module is enabled).

Note: The special event trigger from the CCP1and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

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10.3 PWM Mode

Applicable Devices									
61	62	62A	R62	63	64	64A	R64	65	65A

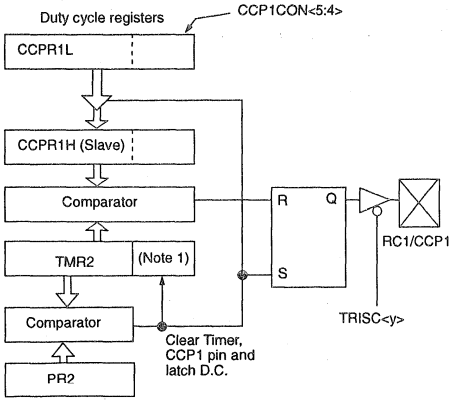
In Pulse Width Modulation (PWM) mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCPx pin is multiplexed with the PORTC data latch, the corresponding TRISC bit must be cleared to make the CCPx pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 10-4 shows a simplified block diagram of the CCP module in PWM mode.

For a step by step procedure on how to set up the CCP module for PWM operation, see Section 10.3.3.

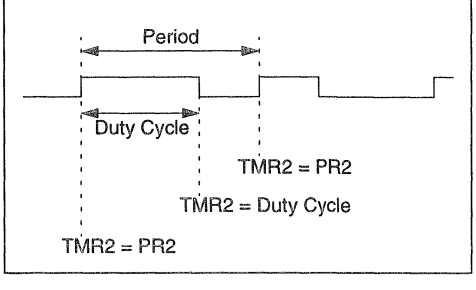
FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base.

A PWM output (Figure 10-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 10-5: PWM OUTPUT



10.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see Section 9.1) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

10.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle:

$$\text{PWM duty cycle} = (CCPR1L{:}CCP1CON<5:4>) \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period (PWM duty cycle = 100%), the CCP1 pin will not be cleared.

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EXAMPLE 10-2: PWM PERIOD AND DUTY CYCLE CALCULATION

Desired PWM frequency is 78.125 kHz,
Fosc = 20 MHz
TMR2 prescale = 1

$$1/78.125\ kHz = [(PR2) + 1] \cdot 4 \cdot 1/20\ MHz \cdot 1$$
$$12.8\ \mu s = [(PR2) + 1] \cdot 4 \cdot 50\ ns \cdot 1$$
$$PR2 = 63$$

Find the maximum resolution of the duty cycle that can be used with a 78.125 kHz frequency and 20 MHz oscillator:

$$1/78.125\ kHz = 2^{PWM\ RESOLUTION} \cdot 1/20\ MHz \cdot 1$$
$$12.8\ \mu s = 2^{PWM\ RESOLUTION} \cdot 50\ ns \cdot 1$$
$$256 = 2^{PWM\ RESOLUTION}$$
$$\log(256) = (PWM\ Resolution) \cdot \log(2)$$
$$8.0 = PWM\ Resolution$$

At most, an 8-bit resolution duty cycle can be obtained from a 78.125 kHz frequency and a 20 MHz oscillator, i.e., 0 ≤ CCPR1L:CCP1CON<5:4> ≤ 255. Any value greater than 255 will result in a 100% duty cycle.

In order to achieve higher resolution, the PWM frequency must be decreased. In order to achieve higher PWM frequency, the resolution must be decreased.

Table 10-3 lists example PWM frequencies and resolutions for Fosc = 20 MHz. TMR2 prescaler and PR2 values are also shown.

10.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the appropriate TRISC bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP module for PWM operation.

TABLE 10-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 10-4: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1,2)	ADIF	RCIF(2)	TXIF(2)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh(2)	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE(1,2)	ADIE	RCIE(2)	TXIE(2)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh(2)	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh(2)	CCPR2L	Capture/Compare/PWM register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch(2)	CCPR2H	Capture/Compare/PWM register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh(2)	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.
2: The PIC16C72 does not have a Parallel Slave Port, USART or CCP2 module, these bits are unimplemented, read as '0'.

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TABLE 10-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1,2)	ADIF	RCIF(2)	TXIF(2)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh(2)	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE(1,2)	ADIE	RCIE(2)	TXIE(2)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh(2)	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh(2)	CCPR2L	Capture/Compare/PWM register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch(2)	CCPR2H	Capture/Compare/PWM register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh(2)	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

2: The PIC16C72 does not have a Parallel Slave Port, USART or CCP2 module, these bits are unimplemented, read as '0'.

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11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

Applicable Devices							
710	71	711	72	73	73A	74	74A

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

Refer to Application Note AN578, *"Use of the SSP Module in the I^2C Multi-Master Environment."*

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5: **D/$\overline{A}$**: Data/$\overline{Address}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)
0 = Stop bit was not detected last

bit 3: **S**: Start bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)
0 = Start bit was not detected last

bit 2: **R/$\overline{W}$**: Read/Write bit information (I^2C mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid during the transmission.
1 = Read
0 = Write

bit 1: **UA**: Update Address (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit

Receive (SPI and I^2C modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit (I^2C mode only)
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

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FIGURE 11-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **WCOL**: Write Collision Detect bit
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6: **SSPOV**: Receive Overflow Indicator bit

In SPI mode
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In master mode the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
0 = No overflow

In I^2C mode
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in transmit mode. SSPOV must be cleared in software in either mode.
0 = No overflow

bit 5: **SSPEN**: Synchronous Serial Port Enable bit

In SPI mode
1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins
0 = Disables serial port and configures these pins as I/O port pins

In I^2C mode
1 = Enables the serial port and configures the SDA and SCL pins as serial port pins
0 = Disables serial port and configures these pins as I/O port pins
In both modes, when enabled, these pins must be properly configured as input or output.

bit 4: **CKP**: Clock Polarity Select bit
In SPI mode
1 = Transmit happens on falling edge, receive on rising edge. Idle state for clock is a high level
0 = Transmit happens on rising edge, receive on falling edge. Idle state for clock is a low level
In I^2C mode
SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch) (Used to ensure data setup time)

bit 3-0: **SSPM3:SSPM0**: Synchronous Serial Port Mode Select bits
0000 = SPI master mode, clock = FOSC/4
0001 = SPI master mode, clock = FOSC/16
0010 = SPI master mode, clock = FOSC/64
0011 = SPI master mode, clock = TMR2 output/2
0100 = SPI slave mode, clock = SCK pin. $\overline{SS}$ pin control enabled.
0101 = SPI slave mode, clock = SCK pin. $\overline{SS}$ pin control disabled. $\overline{SS}$ can be used as I/O pin
0110 = I^2C slave mode, 7-bit address
0111 = I^2C slave mode, 10-bit address
1011 = I^2C start and stop bit interrupts enabled (slave idle)
1110 = I^2C slave mode, 7-bit address with start and stop bit interrupts enabled
1111 = I^2C slave mode, 10-bit address with start and stop bit interrupts enabled

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11.1 SPI Mode

Applicable Devices							
710	71	711	72	73	73A	74	74A

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI
- Serial Clock (SCK) RC3/SCK

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select ($\overline{SS}$) RA5/AN4/$\overline{SS}$

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>). These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Output/Input data on the Rising/Falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select Mode (Slave mode only)

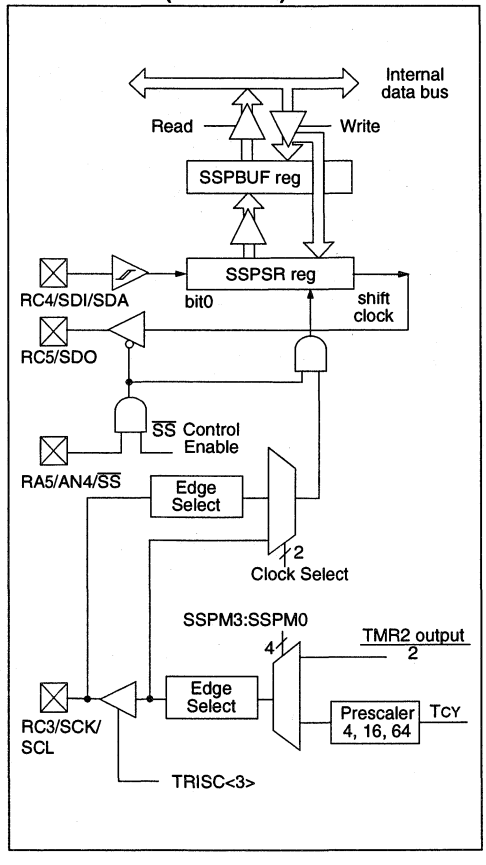
The SSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSB first. The SSPBUF holds the data that was previously written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that information is moved to the SSPBUF register. Then the buffer full detect bit BF (SSPSTAT <0>) and interrupt flag bit SSPIF (PIR1<3>) are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit WCOL (SSPCON<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully. When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit BF (SSPSTAT<0>) indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF can then be read (if data is meaningful) and/or the SSPBUF (SSPSR) can be written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-1 shows the loading of the SSPBUF (SSPSR) for data transmission. The shaded instruction is only required if the received data is meaningful.

EXAMPLE 11-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
     BSF   STATUS, RP0    ;Specify Bank 1
LOOP BTFSS SSPSTAT, BF    ;Has data been
                          ;received
                          ;(transmit
                          ;complete)?
     GOTO  LOOP           ;No
     BCF   STATUS, RP0    ;Specify Bank 0
     MOVF  SSPBUF, W      ;W reg = contents
                          ; of SSPBUF
     MOVWF RXDATA         ;Save in user RAM
     MOVF  TXDATA, W      ;W reg = contents
                          ; of TXDATA
     MOVWF SSPBUF         ;New data to xmit
```

The block diagram of the SSP module, when in SPI mode (Figure 11-3), shows that the SSPSR is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

FIGURE 11-3: SSP BLOCK DIAGRAM (SPI MODE)



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To enable the serial port, SSP enable bit SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- $\overline{SS}$ must have TRISA<5> set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and $\overline{SS}$ could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) wishes to broadcast data by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

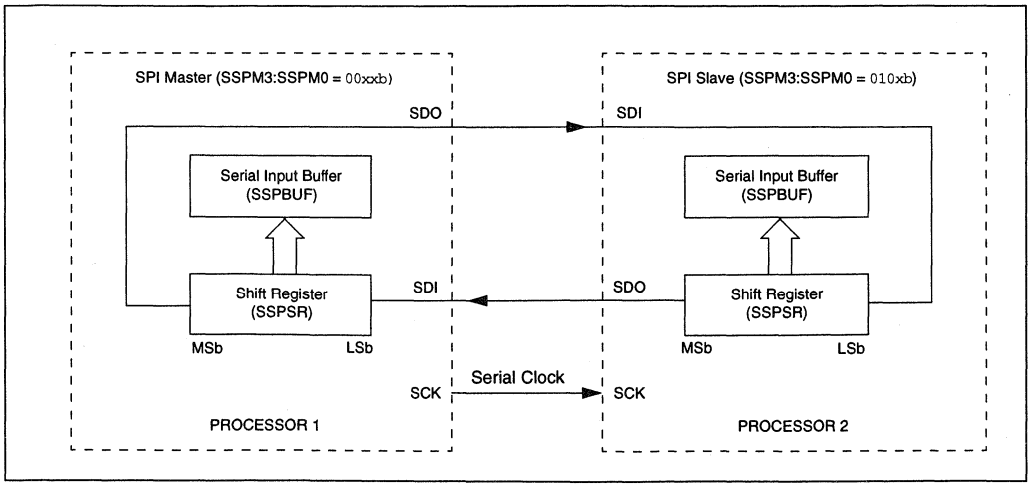
The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-5 and Figure 11-6 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 • TCY)
- FOSC/64 (or 16 • TCY)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

FIGURE 11-4: SPI MASTER/SLAVE CONNECTION



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The $\overline{SS}$ pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set the for the synchronous slave mode to be enabled. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. If the $\overline{SS}$ pin is taken low without resetting SPI mode, the transmission will continue from the point at which it was taken high. External pull-up/pull-down resistors may be desirable, depending on the application.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-5: SPI MODE TIMING (MASTER MODE OR SLAVE MODE W/O $\overline{SS}$ CONTROL)

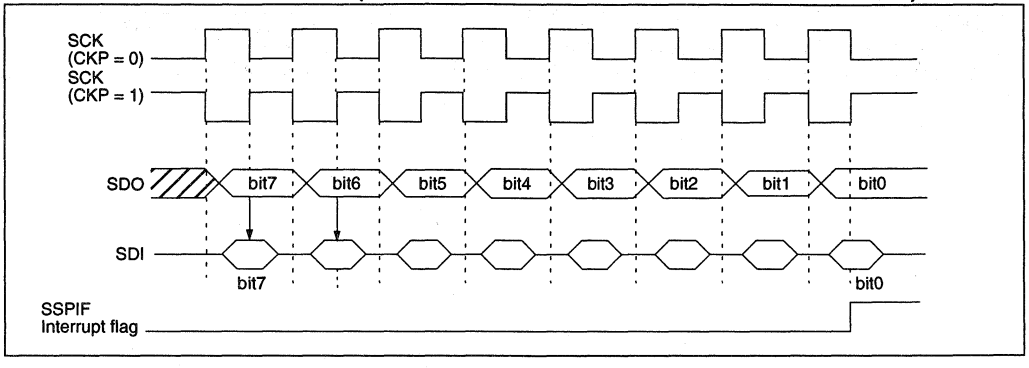

FIGURE 11-6: SPI MODE TIMING (SLAVE MODE WITH $\overline{SS}$ CONTROL)

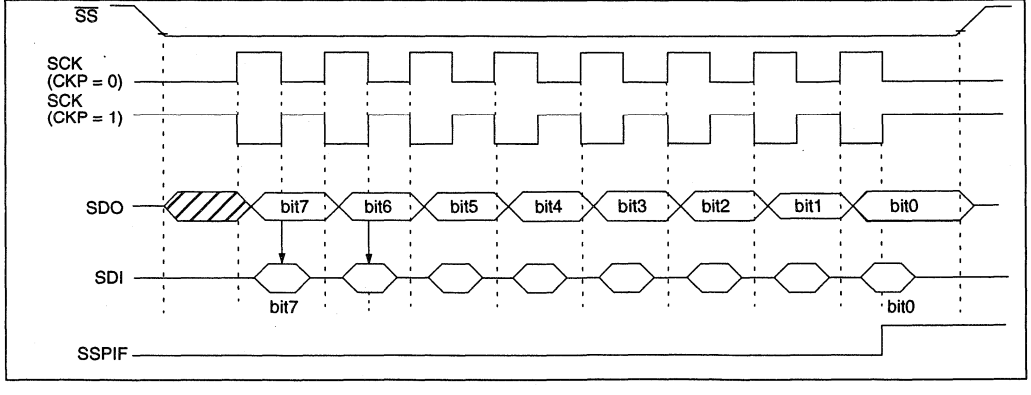

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TABLE 11-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1,2)	ADIF	RCIF(2)	TXIF(2)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1,2)	ADIE	RCIE(2)	TXIE(2)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the SSP in SPI mode.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.
2: The PIC16C72 does not have a Parallel Slave Port or USART, these bits are unimplemented, read as '0'.

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11.2 I²C™ Overview

Applicable Devices								
710	71	711	72	73	73A	74	74A	

This section provides an overview of the Inter-Integrated Circuit (I^2C) bus, with Section 11.3 discussing the operation of the SSP module in I^2C mode.

The I^2C bus is a two-wire serial interface developed by the Philips Corporation. The original specification, or standard mode, was for data transfers of up to 100 Kbps. An enhanced specification, or fast mode, supports data transmission up to 400 Kbps. Both standard mode and fast mode devices will inter-operate if attached to the same bus.

The I^2C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master" (generates the clock), while the other device(s) acts as the "slave." All portions of the slave protocol are implemented in the SSP module's hardware, while portions of the master protocol need to be addressed in the PIC16CXX software. Table 11-2 defines some of the I^2C bus terminology. For additional information on the I^2C interface specification, refer to the Philips document *"The I^2C bus and how to use it."*, which can be obtained from the Philips Corporation.

In the I^2C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to "talk" to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read-from/write-to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of operating in either of these two relations:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level when no device is pulling the line down. The number of devices that may be attached to the I^2C bus is limited only by the maximum bus loading specification of 400 pF.

11.2.1 INITIATING AND TERMINATING DATA TRANSFER

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure 11-7 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

FIGURE 11-7: START AND STOP CONDITIONS

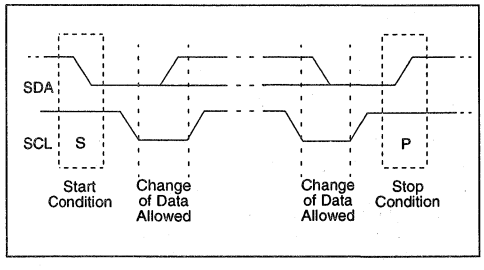

TABLE 11-2: I^2C BUS TERMINOLOGY

Term	Description
Transmitter	The device that sends the data to the bus.
Receiver	The device that receives the data from the bus.
Master	The device which initiates the transfer, generates the clock and terminates the transfer.
Slave	The device addressed by a master.
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensure that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

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11.2.2 ADDRESSING I²C DEVICES

There are two address formats. The simplest is the 7-bit address format with a R/$\overline{W}$ bit (Figure 11-8). The more complex is the 10-bit address with a R/$\overline{W}$ bit (Figure 11-9). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

FIGURE 11-8: 7-BIT ADDRESS FORMAT

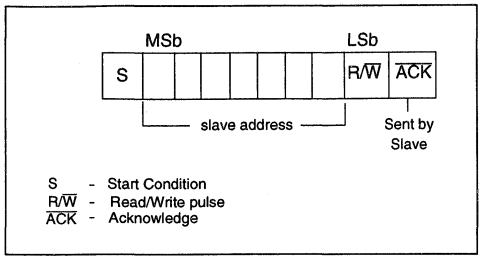
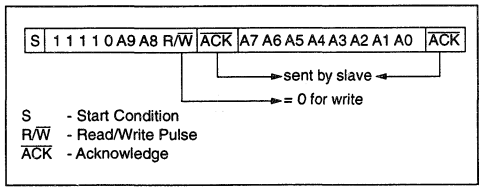


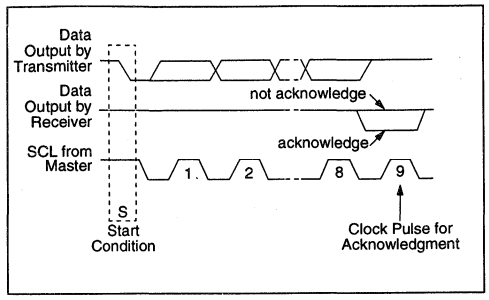
FIGURE 11-9: I²C 10-BIT ADDRESS FORMAT



11.2.3 TRANSFER ACKNOWLEDGE

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit ($\overline{ACK}$) (Figure 11-10). When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP condition (Figure 11-7).

FIGURE 11-10: SLAVE-RECEIVER ACKNOWLEDGE



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level, Figure 11-11. The slave will inherently stretch the clock when it is a transmitter but will not when it is a receiver. The slave will have to clear the SSPCON<4> bit to enable clock stretching when it is a receiver.

FIGURE 11-11: DATA TRANSFER WAIT STATE

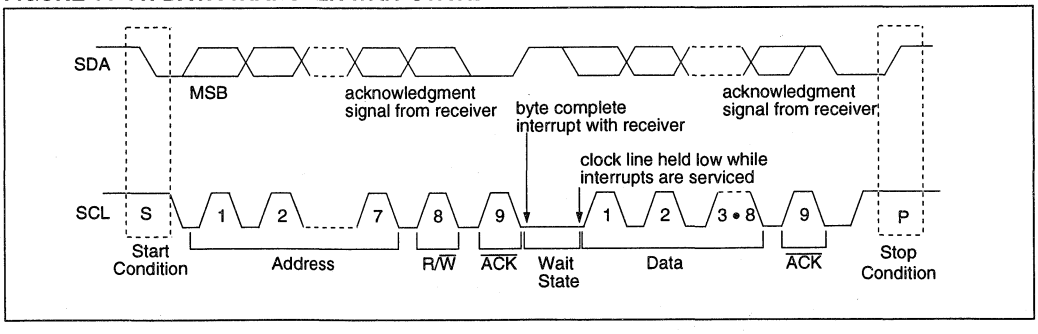


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Figure 11-12 and Figure 11-13 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-14.

FIGURE 11-12: MASTER-TRANSMITTER SEQUENCE

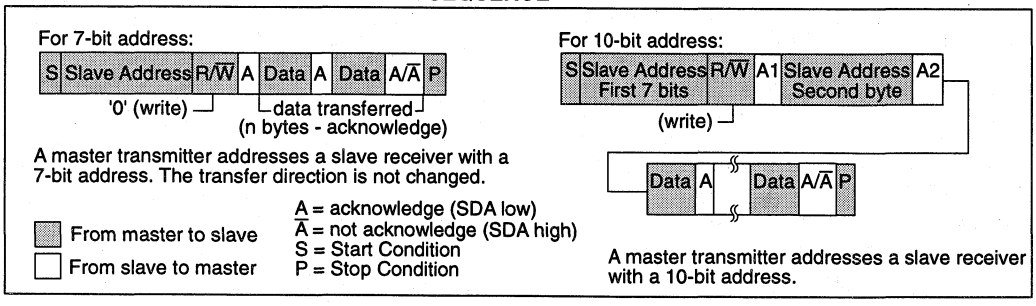


FIGURE 11-13: MASTER-RECEIVER SEQUENCE

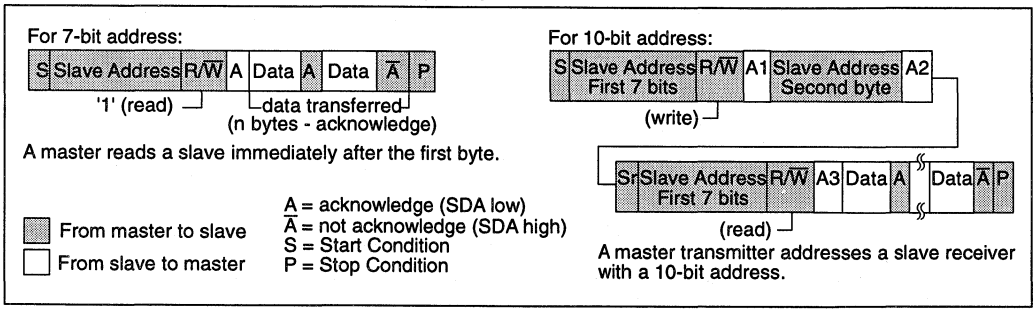
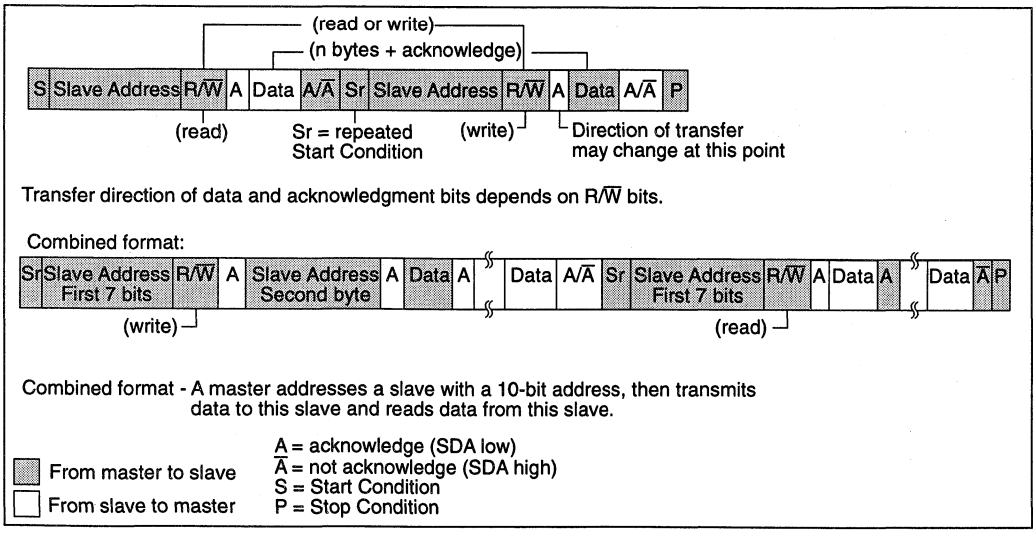


FIGURE 11-14: COMBINED FORMAT



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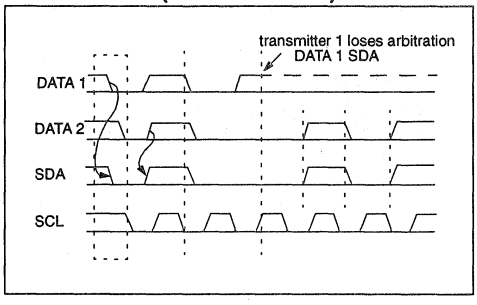
11.2.4 MULTI-MASTER

The I^2C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

11.2.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure 11-15), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

FIGURE 11-15: MULTI-MASTER ARBITRATION (TWO MASTERS)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

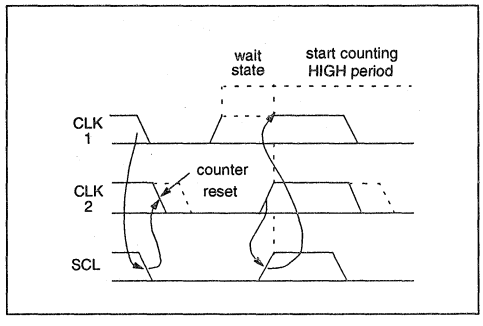
- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

11.2.4.2 CLOCK SYNCHRONIZATION

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period, Figure 11-16.

FIGURE 11-16: CLOCK SYNCHRONIZATION



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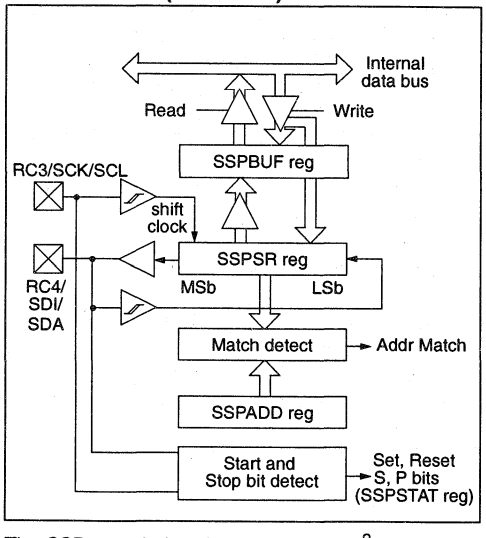
11.3 SSP I²C Operation

Applicable Devices							
710	71	711	72	73	73A	74	74A

The SSP module in I²C mode fully implements all slave functions, and provides interrupts on start and stop bits in hardware to facilitate software implementations of the master functions. The SSP module implements the standard and fast mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

FIGURE 11-17: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
- I²C start and stop bit interrupts enabled, slave is idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (`1111 0 A9 A8 0`). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

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11.3.1 SLAVE MODE

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge ($\overline{ACK}$) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this $\overline{ACK}$ pulse. These are if either (or both):

a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.

b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 11-3 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I^2C specification as well as the requirement of the SSP module is shown in timing parameter #100 and parameter #101 (see Electrical Specification section).

11.3.1.1 ADDRESSING

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

a) The SSPSR register value is loaded into the SSPBUF register.

b) The buffer full bit, BF is set.

c) An $\overline{ACK}$ pulse is generated.

d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave (Figure 11-9). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/$\overline{W}$ (SSPSTAT<2>) must specify a write, so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for a 10-bit address is as follows, with steps 7- 9 for slave-transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
5. Update the SSPADD register with the first (high) byte of Address (clears bit UA, if match releases SCL line).
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive repeated START condition.
8. Receive first (high) byte of Address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

TABLE 11-3: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received				
BF	SSPOV	SSPSR → SSPBUF	Generate $\overline{ACK}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if Enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

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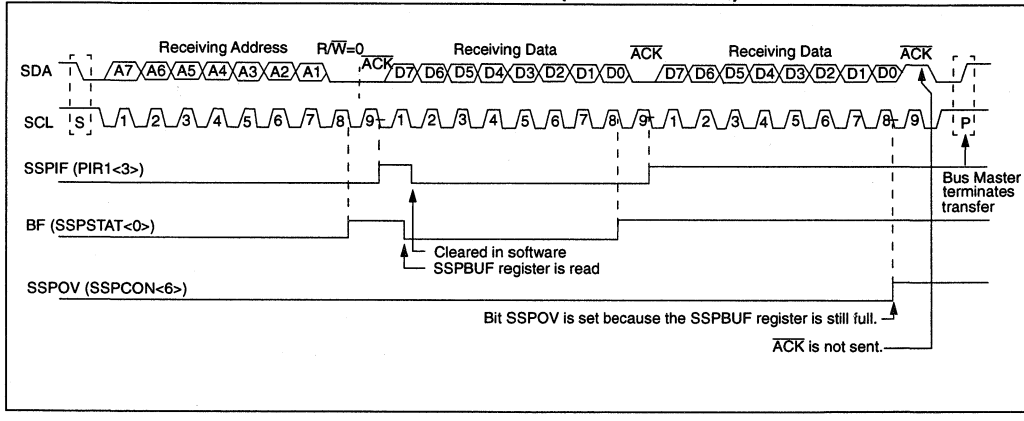
11.3.1.2 RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software, and the SSPSTAT register is used to determine the status of the byte.

FIGURE 11-18: I^2C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



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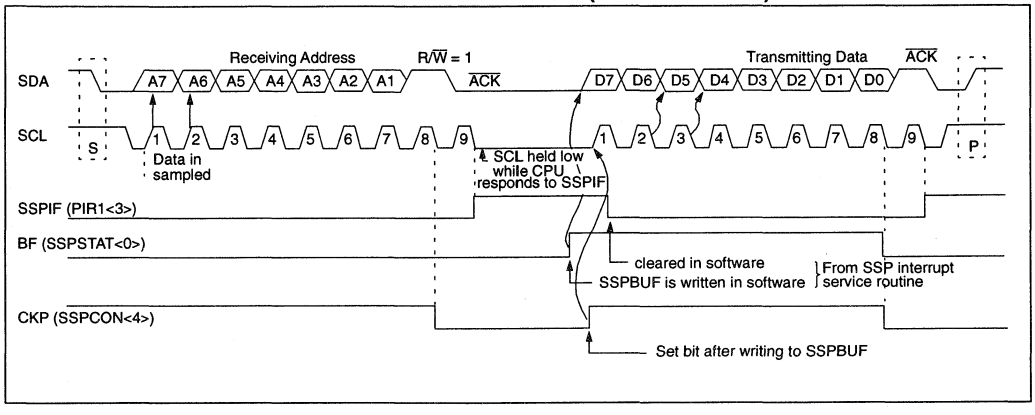
11.3.1.3 TRANSMISSION

When the R/$\overline{W}$ bit of the incoming address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The $\overline{ACK}$ pulse will be sent on the ninth bit, and pin RC3/SCK/SCL is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 11-19).

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. The slave then monitors for another occurrence of the START bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP.

FIGURE 11-19: I^2C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



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11.3.2 MASTER MODE

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is idle with both the S and P bits clear.

In master mode the SCL and SDA lines are manipulated by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause the SSP Interrupt Flag bit SSPIF to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

11.3.3 MULTI-MASTER MODE

In multi-master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, they are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, the device may be being addressed. If addressed an $\overline{ACK}$ pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

TABLE 11-4: REGISTERS ASSOCIATED WITH I^2C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1,2)	ADIF	RCIF(2)	TXIF(2)	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1,2)	ADIE	RCIE(2)	TXIE(2)	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	--00 0000	--00 0000
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by SSP in I^2C mode.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.
2: The PIC16C72 does not have a Parallel Slave Port or USART, these bits are unimplemented, read as '0'.

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FIGURE 11-20: OPERATION OF THE I²C MODULE IN IDLE_MODE, RCV_MODE OR XMIT_MODE

```
IDLE_MODE (7-bit):
if (Addr_match)                 {       Set interrupt;
                                        if (R/W = 1)    {       Send ACK = 0;
                                                                set XMIT_MODE;
                                                        }
                                        else if (R/W = 0) set RCV_MODE;
                                }
RCV_MODE:
if ((SSPBUF=Full) OR (SSPOV = 1))
        {       Set SSPOV;
                Do not acknowledge;
        }
else    {       transfer SSPSR → SSPBUF;
                send ACK = 0;
        }
Receive 8-bits in SSPSR;
Set interrupt;
XMIT_MODE:
While ((SSPBUF = Empty) AND (CKP=0)) Hold SCL Low;
Send byte;
Set interrupt;
if ( ACK Received = 1)          {       End of transmission;
                                        Go back to IDLE_MODE;
                                }
else if ( ACK Received = 0)   Go back to XMIT_MODE;
IDLE_MODE (10-Bit):
If (High_byte_addr_match AND (R/W = 0))
        {       PRIOR_ADDR_MATCH = FALSE;
                Set interrupt;
                if ((SSPBUF = Full) OR ((SSPOV = 1))
                        {       Set SSPOV;
                                Do not acknowledge;
                        }
                else    {       Set UA = 1;
                                Send ACK = 0;
                                While (SSPADD not updated) Hold SCL low;
                                Clear UA = 0;
                                Receive Low_addr_byte;
                                Set interrupt;
                                Set UA = 1;
                                If (Low_byte_addr_match)
                                        {       PRIOR_ADDR_MATCH = TRUE;
                                                Send ACK = 0;
                                                while (SSPADD not updated) Hold SCL low;
                                                Clear UA = 0;
                                                Set RCV_MODE;
                                        }
                        }
        }
else if (High_byte_addr_match AND (R/W = 1)
        {       if (PRIOR_ADDR_MATCH)
                        {       send ACK = 0;
                                set XMIT_MODE;
                        }
        else PRIOR_ADDR_MATCH = FALSE;
        }
```


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12.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

Applicable Devices							
710	71	711	72	73	73A	74	74A

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also know as a Serial Communications Interface or SCI). The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

Bit SPEN (RCSTA<7>), and bits TRISC<7:6>, have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT for the Serial Communication Interface.

FIGURE 12-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **CSRC**: Clock Source Select bit

Asynchronous mode
Don't care

Synchronous mode
1 = Master mode (Clock generated internally from BRG)
0 = Slave mode (Clock from external source)

bit 6: **TX9**: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5: **TXEN**: Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled
Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4: **SYNC**: USART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3: **Unimplemented:** Read as '0'

bit 2: **BRGH**: High Baud Rate Select bit

Asynchronous mode
1 = High speed

Note: At the time of this printing, the asynchronous high speed mode (BRGH is set) may experience a high rate of receive errors. It is recommended to have the BRGH bit cleared. If you desire a higher baud rate than BRGH=0 can support, refer to the device errata for additional information.

0 = Low speed

Synchronous mode
Unused in this mode

bit 1: **TRMT**: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0: **TX9D**: 9th bit of transmit data. Can be parity bit.

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FIGURE 12-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **SPEN**: Serial Port Enable bit
1 = Serial port enabled (Configures RC7/RX/DT and RC6/TX/CK pins as serial port pins)
0 = Serial port disabled

bit 6: **RX9**: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5: **SREN**: Single Receive Enable bit

Asynchronous mode
Don't care

Synchronous mode - master
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.

Synchronous mode - slave
Unused in this mode

bit 4: **CREN**: Continuous Receive Enable bit

Asynchronous mode
1 = Enables continuous receive
0 = Disables continuous receive

Synchronous mode
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3: **Unimplemented:** Read as '0'

bit 2: **FERR**: Framing Error bit
1 = Framing error (Can be updated by reading RCREG register and receive next valid byte)
0 = No framing error

bit 1: **OERR**: Overrun Error bit
1 = Overrun error (Can be cleared by clearing bit CREN)
0 = No overrun error

bit 0: **RX9D**: 9th bit of received data (Can be parity bit)

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12.1 USART Baud Rate Generator (BRG)

Applicable Devices							
710	71	711	72	73	73A	74	74A

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 12-1. From this, the error in baud rate can be determined.

Example 12-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz
Desired Baud Rate = 9600
BRGH = 0
SYNC = 0

EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))

9600 = 16000000 /(64 (X + 1))

X = ⌊25.042⌋ = 25

Calculated Baud Rate=16000000 / (64 (25 + 1))

= 9615

$$\text{Error} = \frac{\text{(Calculated Baud Rate - Desired Baud Rate)}}{\text{Desired Baud Rate}}$$

= (9615 - 9600) / 9600

= 0.16%

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the Fosc/(16(X + 1)) equation can reduce the baud rate error in some cases.

Note: At the time of this printing, the asynchronous high speed mode (BRGH is set) may experience a high rate of receive errors. It is recommended to have the BRGH bit cleared. If you desire a higher baud rate than BRGH=0 can support, refer to the device errata for additional information.

Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

TABLE 12-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate= Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	NA

X = value in SPBRG (0 to 255)

TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the BRG.

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TABLE 12-3: BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	Fosc = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-	NA	-	-
9.6	NA	-	-	NA	-	-	9.766	+1.73	255	9.622	+0.23	185
19.2	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129	19.24	+0.23	92
76.8	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32	77.82	+1.32	22
96	96.15	+0.16	51	95.24	-0.79	41	96.15	+0.16	25	94.20	-1.88	18
300	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7	298.3	-0.57	5
500	500	0	9	500	0	7	500	0	4	NA	-	-
HIGH	5000	-	0	4000	-	0	2500	-	0	1789.8	-	0
LOW	19.53	-	255	15.625	-	255	9.766	-	255	6.991	-	255

BAUD RATE (K)	Fosc = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-	0.303	+1.14	26
1.2	NA	-	-	NA	-	-	NA	-	-	1.202	+0.16	207	1.170	-2.48	6
2.4	NA	-	-	NA	-	-	NA	-	-	2.404	+0.16	103	NA	-	-
9.6	9.6	0	131	9.615	+0.16	103	9.622	+0.23	92	9.615	+0.16	25	NA	-	-
19.2	19.2	0	65	19.231	+0.16	51	19.04	-0.83	46	19.24	+0.16	12	NA	-	-
76.8	79.2	+3.13	15	76.923	+0.16	12	74.57	-2.90	11	83.34	+8.51	2	NA	-	-
96	97.48	+1.54	12	1000	+4.17	9	99.43	+3.57	8	NA	-	-	NA	-	-
300	316.8	+5.60	3	NA	-	-	298.3	-0.57	2	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	1267	-	0	100	-	0	894.9	-	0	250	-	0	8.192	-	0
LOW	4.950	-	255	3.906	-	255	3.496	-	255	0.9766	-	255	0.032	-	255

TABLE 12-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD RATE (K)	Fosc = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129	1.203	+0.23	92
2.4	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64	2.380	-0.83	46
9.6	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15	9.322	-2.90	11
19.2	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5
76.8	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1	NA	-	-
96	104.2	+8.51	2	NA	-	-	NA	-	-	NA	-	-
300	312.5	+4.17	0	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	312.5	-	0	250	-	0	156.3	-	0	111.9	-	0
LOW	1.221	-	255	0.977	-	255	0.6104	-	255	0.437	-	255

BAUD RATE (K)	Fosc = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	0.31	+3.13	255	0.3005	-0.17	207	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.2	0	65	1.202	+1.67	51	1.190	-0.83	46	1.202	+0.16	12	NA	-	-
2.4	2.4	0	32	2.404	+1.67	25	2.432	+1.32	22	2.232	-6.99	6	NA	-	-
9.6	9.9	+3.13	7	NA	-	-	9.322	-2.90	5	NA	-	-	NA	-	-
19.2	19.8	+3.13	3	NA	-	-	18.64	-2.90	2	NA	-	-	NA	-	-
76.8	79.2	+3.13	0	NA	-	-	NA	-	-	NA	-	-	NA	-	-
96	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	79.2	-	0	62.500	-	0	55.93	-	0	15.63	-	0	0.512	-	0
LOW	0.3094	-	255	3.906	-	255	0.2185	-	255	0.0610	-	255	0.0020	-	255

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TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD RATE (K)	FOSC = 20 MHz			16 MHz			10 MHz			7.16 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64	9.520	-0.83	46
19.2	19.230	+0.16	64	19.230	+0.16	51	18.939	-1.36	32	19.454	+1.32	22
38.4	37.878	-1.36	32	38.461	+0.16	25	39.062	+1.7	15	37.286	-2.90	11
57.6	56.818	-1.36	21	58.823	+2.12	16	56.818	-1.36	10	55.930	-2.90	7
115.2	113.636	-1.36	10	111.111	-3.55	8	125	+8.51	4	111.860	-2.90	3
250	250	0	4	250	0	3	NA	-	-	NA	-	-
625	625	0	1	NA	-	-	625	0	0	NA	-	-
1250	1250	0	0	NA	-	-	NA	-	-	NA	-	-

BAUD RATE (K)	FOSC = 5.068 MHz			4 MHz			3.579 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.6	0	32	NA	-	-	9.727	+1.32	22	8.928	-6.99	6	NA	-	-
19.2	18.645	-2.94	16	1.202	+0.17	207	18.643	-2.90	11	20.833	+8.51	2	NA	-	-
38.4	39.6	+3.12	7	2.403	+0.13	103	37.286	-2.90	5	31.25	-18.61	1	NA	-	-
57.6	52.8	-8.33	5	9.615	+0.16	25	55.930	-2.90	3	62.5	+8.51	0	NA	-	-
115.2	105.6	-8.33	2	19.231	+0.16	12	111.860	-2.90	1	NA	-	-	NA	-	-
250	NA	-	-	NA	-	-	223.721	-10.51	0	NA	-	-	NA	-	-
625	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1250	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-

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12.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin. If bit BRGH (TXSTA<2>) is clear (i.e., at the low baud rates), the sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 12-3). If bit BRGH is set (i.e., at the high baud rates), the sampling is done on the 3 clock edges preceding the second rising edge after the first falling edge of a x4 clock (Figure 12-4 and Figure 12-5).

FIGURE 12-3: RX PIN SAMPLING SCHEME (BRGH = 0)

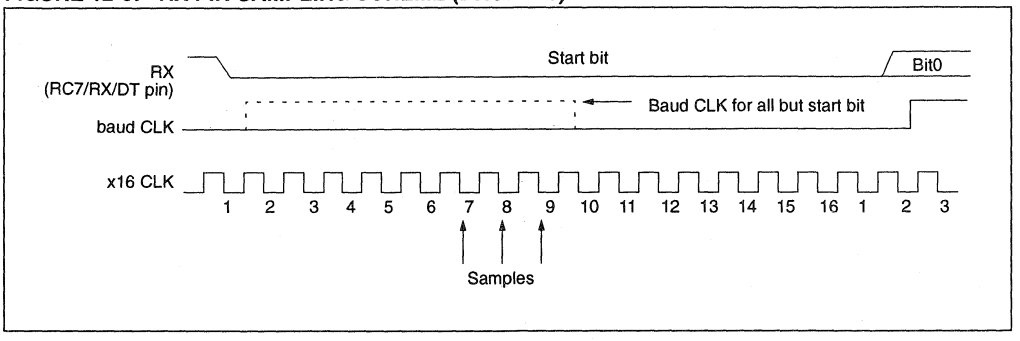


FIGURE 12-4: RX PIN SAMPLING SCHEME (BRGH = 1)

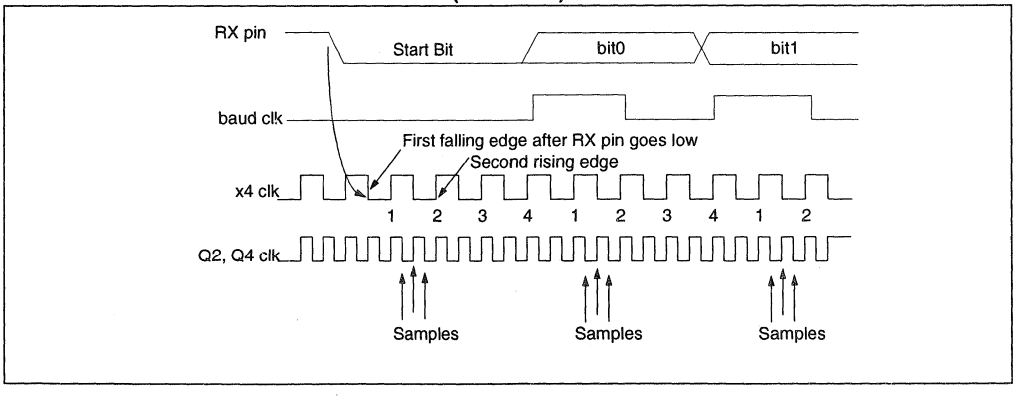
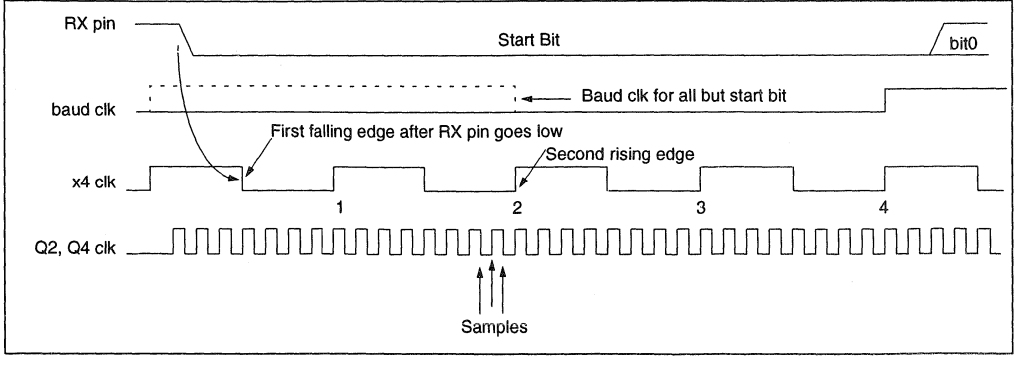


FIGURE 12-5: RX PIN SAMPLING SCHEME (BRGH = 1)



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12.2 USART Asynchronous Mode

Applicable Devices							
710	71	711	72	73	73A	74	74A

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

12.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 12-6. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCY), the TXREG register is empty and flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicated the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

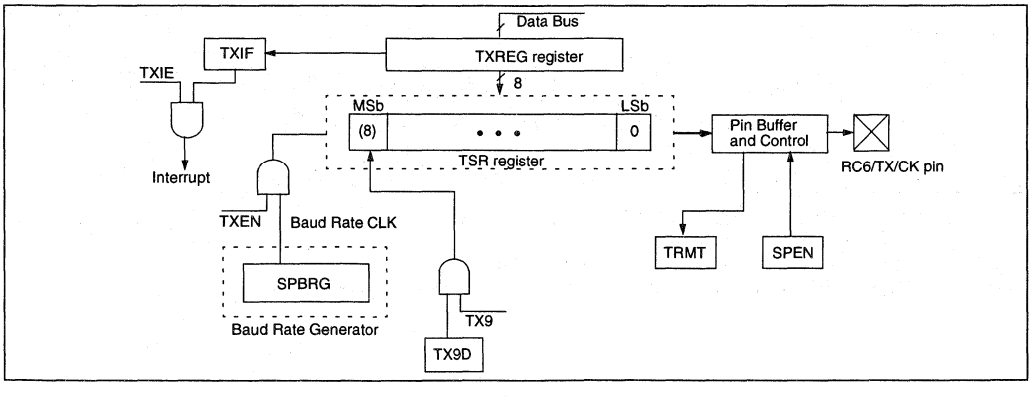
Note 1: The TSR register is not mapped in data memory so it is not available to the user.

Note 2: Flag bit TXIF is set when enable bit TXEN is set.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 12-6). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 12-8). Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. As a result the RC6/TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, transmit bit TX9 (TXSTA<6>) should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). In such a case, an incorrect ninth data bit maybe loaded in the TSR register.

FIGURE 12-6: USART TRANSMIT BLOCK DIAGRAM



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Steps to follow when setting up a Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH. (Section 12.1)
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).

FIGURE 12-7: ASYNCHRONOUS MASTER TRANSMISSION

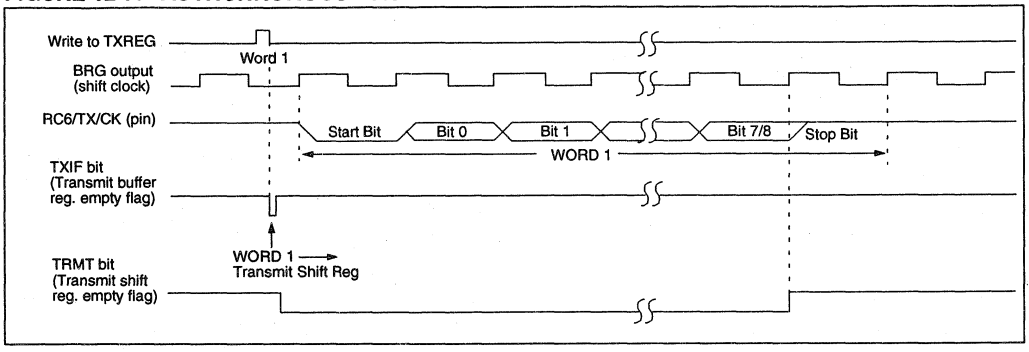
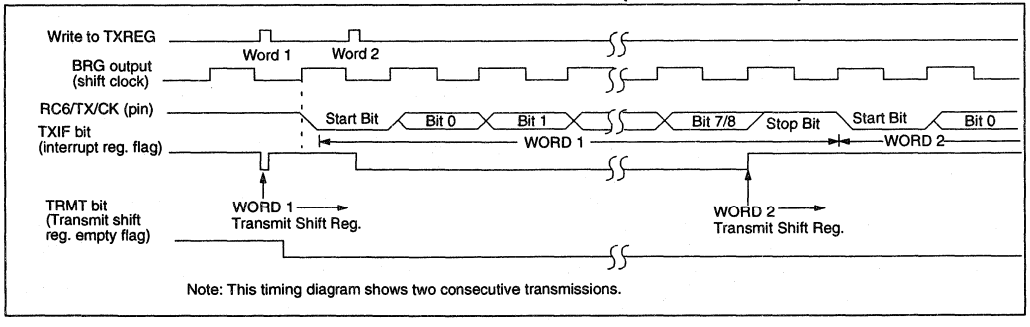


FIGURE 12-8: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 12-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

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12.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 12-9. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double buffered register, i.e. it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG register is still full then overrun error bit OERR (RCSTA<1>) will be set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited, so it is essential to clear error bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a stop bit is detected as clear. Bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG, will load bits RX9D and FERR with new values, therefore it is essential for the user to read the RCSTA register before reading RCREG register in order not to lose the old FERR and RX9D information.

FIGURE 12-9: USART RECEIVE BLOCK DIAGRAM

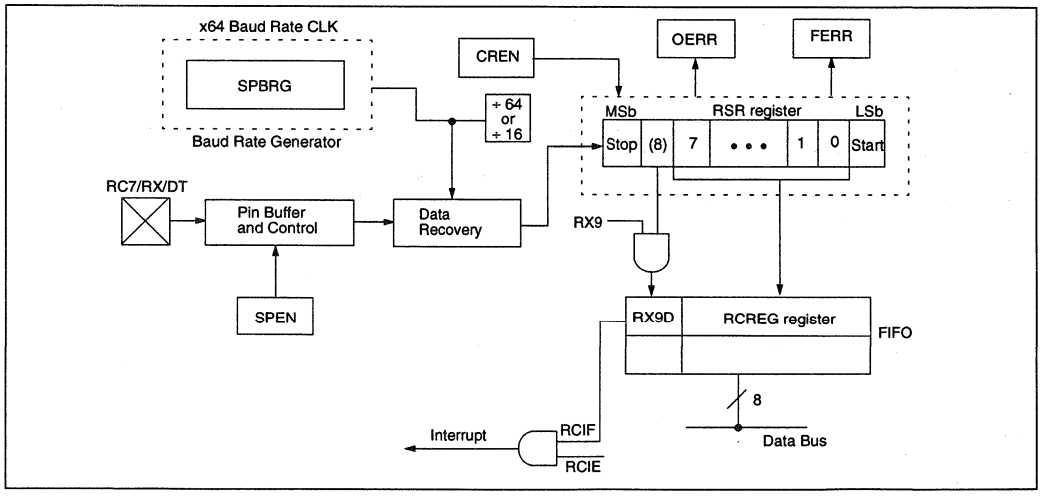
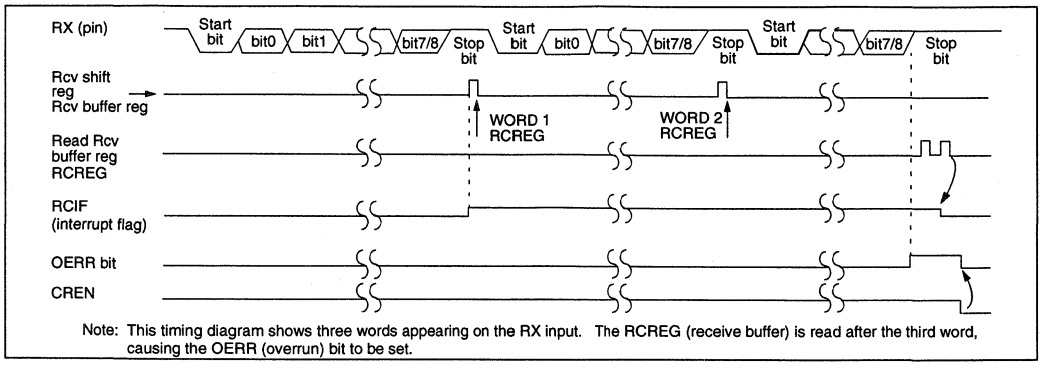


FIGURE 12-10: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

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Steps to follow when setting up an Asynchronous Reception:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH. (Section 12.1).
2. Enable the asynchronous serial port by clearing bit SYNC, and setting bit SPEN.
3. If interrupts are desired, then set enable bit RCIE.
4. If 9-bit reception is desired, then set bit RX9.
5. Enable the reception by setting bit CREN.
6. Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading the RCREG register.
9. If any error occurred, clear the error by clearing enable bit CREN.

TABLE 12-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

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12.3 USART Synchronous Master Mode

Applicable Devices							
710	71	711	72	73	73A	74	74A

In Synchronous Master mode, the data is transmitted in a half-duplex manner i.e. transmission and reception do not occur at the same time. When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition enable bit SPEN (RCSTA<7>) is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

12.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 12-6. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcycle), the TXREG is empty and interrupt bit, TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 12-11). The transmission can also be started by first loading the TXREG register and then setting bit TXEN. This is advantageous when slow baud rates are selected, since the BRG is kept in reset when bits TXEN, CREN, and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing enable bit TXEN, during a transmission, will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hi-impedance. If either bit CREN or bit SREN is set, during a transmission, the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic however is not reset although it is disconnected from the pins. In order to reset the transmitter, the user has to clear bit TXEN. If bit SREN is set (to interrupt an on-going transmission and receive a single word), then after the single word is received, bit SREN will be cleared and the serial port will revert back to transmitting since bit TXEN is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, bit TXEN should be cleared.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR was empty and the TXREG was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set bit TX9.
5. Enable the transmission by setting bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.

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TABLE 12-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for Synchronous Master Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

FIGURE 12-11: SYNCHRONOUS TRANSMISSION

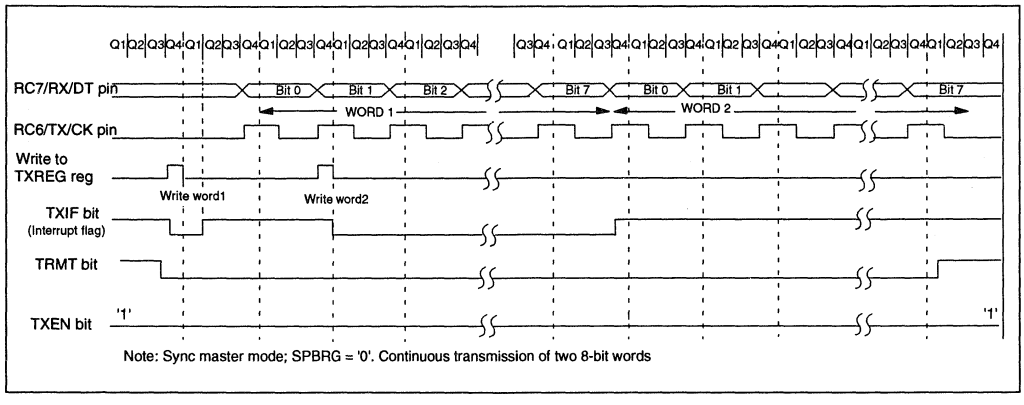
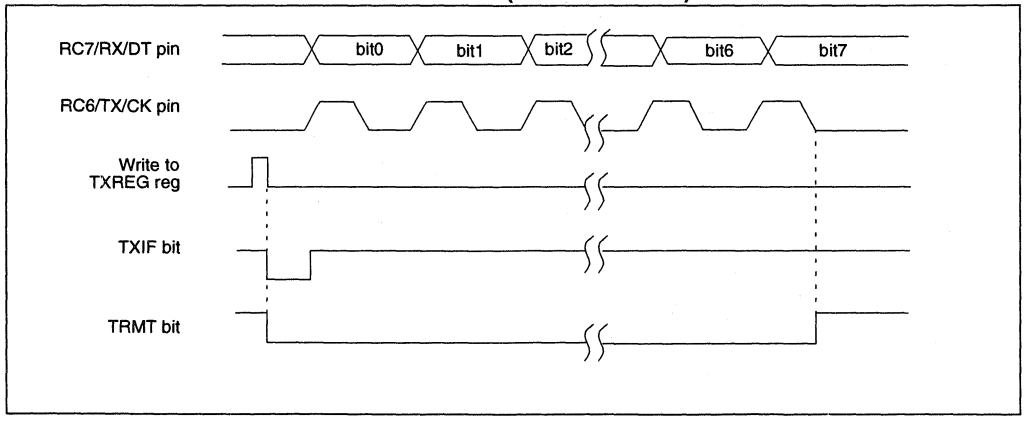


FIGURE 12-12: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



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12.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either enable bit SREN (RCSTA<5>) or enable bit CREN (RCSTA<4>). Data is sampled on the RC7/RX/DT pin on the falling edge of the clock. If enable bit SREN is set, then only a single word is received. If enable bit CREN is set, the reception is continuous until CREN is cleared. If both bits are set then CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to the RCREG register (if it is empty). When the transfer is complete, interrupt flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is reset by the hardware. In this case it is reset when the RCREG register has been read and is empty. The RCREG is a double buffered register, i.e. it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR register. On the clocking of the last bit of the third byte, if the RCREG register is still full then overrun error bit OERR (RCSTA<1>) is set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Bit OERR has to be cleared in software (by clearing bit CREN). If bit OERR is set, transfers from the RSR to the RCREG are inhibited, so it is essential to clear bit OERR if it is set. The 9th receive bit is buffered the same way as the receive data. Reading the RCREG register, will load bit RX9D with a new value, therefore it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old RX9D information.

Steps to follow when setting up a Synchronous Master Reception:

1. Initialize the SPBRG register for the appropriate baud rate. (Section 12.1)
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. Ensure bits CREN and SREN are clear.
4. If interrupts are desired, then set enable bit RCIE.
5. If 9-bit reception is desired, then set bit RX9.
6. If a single reception is required, set bit SREN. For continuous reception set bit CREN.
7. Interrupt flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
8. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
9. Read the 8-bit received data by reading the RCREG register.
10. If any error occurred, clear the error by clearing bit CREN.

TABLE 12-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Master Reception.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

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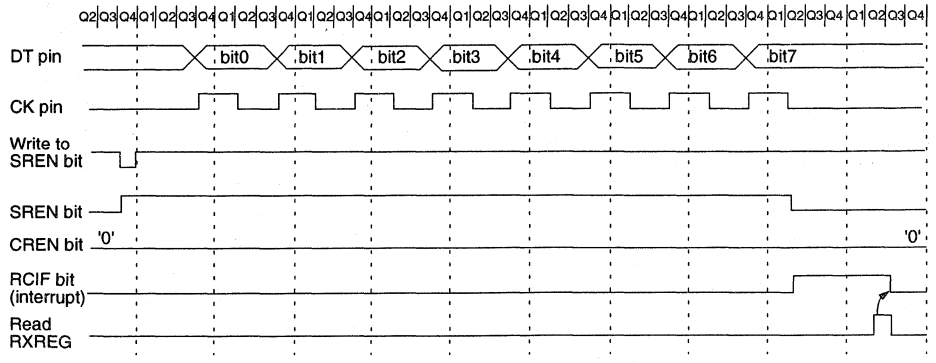
FIGURE 12-13: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates SYNC master mode with SREN = '1' and BRG = '0'.

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12.4 USART Synchronous Slave Mode

Applicable Devices							
710	71	711	72	73	73A	74	74A

Synchronous slave mode differs from the Master mode in the fact that the shift clock is supplied externally at the RC6/TX/CK pin (instead of being supplied internally in master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

12.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

a) The first word will immediately transfer to the TSR register and transmit.
b) The second word will remain in TXREG register.
c) Flag bit TXIF will not be set.
d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
e) If enable bit TXIE is set, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Transmission:

1. Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
2. Clear bits CREN and SREN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set bit TX9.
5. Enable the transmission by setting enable bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.

12.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, bit SREN is a don't care in slave mode.

If receive is enabled, by setting bit CREN, prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

1. Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
2. If interrupts are desired, then set enable bit RCIE.
3. If 9-bit reception is desired, then set bit RX9.
4. To enable reception, set enable bit CREN.
5. Flag bit RCIF will be set when reception is complete and an interrupt will be generated, if enable bit RCIE was set.
6. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREG register.
8. If any error occurred, clear the error by clearing bit CREN.

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TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

TABLE 12-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

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13.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

Applicable Devices							
710	71	711	72	73	73A	74	74A

The analog-to-digital (A/D) converter module has four analog inputs for the PIC16C710/71/711, five inputs for the PIC16C72/73/73A, and eight for the PIC16C74/74A.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Figure 13-1 and Figure 13-2, controls the operation of the A/D module. The ADCON1 register, shown in Figure 13-3 and Figure 13-4, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

FIGURE 13-1: ADCON0 REGISTER, PIC16C710/71/711 (ADDRESS 08h)

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	— (1)	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADIF	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from an RC oscillation)

bit 5: **Unimplemented:** Read as '0'.

bit 4-3: **CHS2:CHS0:** Analog Channel Select bits
00 = channel 0, (RA0/AN0)
01 = channel 1, (RA1/AN1)
10 = channel 2, (RA2/AN2)
11 = channel 3, (RA3/AN3)

bit 2: **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

If ADON = 1
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **ADIF:** A/D Conversion Complete Interrupt Flag bit
1 = conversion is complete (must be cleared in software)
0 = conversion is not complete

bit 0: **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Note 1: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C71 only. For the PIC16C710/711, this bit is unimplemented, read as '0'.

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FIGURE 13-2: ADCON0 REGISTER, PIC16C72/73/73A/74/74A (ADDRESS 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from an RC oscillation)

bit 5-3: **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)
101 = channel 5, (RE0/AN5)(1)
110 = channel 6, (RE1/AN6)(1)
111 = channel 7, (RE2/AN7)(1)

bit 2: **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
If ADON = 1
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **Unimplemented:** Read as '0'

bit 0: **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Note 1: A/D channels 5, 6, and 7 are implemented on the PIC16C74/74A only.

FIGURE 13-3: ADCON1 REGISTER FOR PIC16C710/71/711 (ADDRESS 88h)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1-0: **PCFG1:PCFG0:** A/D Port Configuration Control bits

PCFG1:PCFG0	RA1 & RA0	RA2	RA3	VREF
00	A	A	A	VDD
01	A	A	VREF	RA3
10	A	D	D	VDD
11	D	D	D	VDD

A = Analog input
D = Digital I/O

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FIGURE 13-4: ADCON1 REGISTER, PIC16C72/73/73A/74/74A (ADDRESS 9Fh)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-3: **Unimplemented:** Read as '0'

bit 2-0: **PCFG2:PCFG0**: A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA5	RA3	RE0(1)	RE1(1)	RE2(1)	VREF
000	A	A	A	A	A	A	A	A	VDD
001	A	A	A	A	VREF	A	A	A	RA3
010	A	A	A	A	A	D	D	D	VDD
011	A	A	A	A	VREF	D	D	D	RA3
100	A	A	D	D	A	D	D	D	VDD
101	A	A	D	D	VREF	D	D	D	RA3
11x	D	D	D	D	D	D	D	D	—

A = Analog input

D = Digital I/O

Note 1: RE0, RE1, and RE2 are implemented on the PIC16C74/74A only.

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The ADRES register contains the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF is set. The block diagrams of the A/D module are shown in Figure 13-5 and Figure 13-6.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine sample time, see Section 13.1. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins / voltage reference / and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

FIGURE 13-5: A/D BLOCK DIAGRAM, PIC16C710/71/711

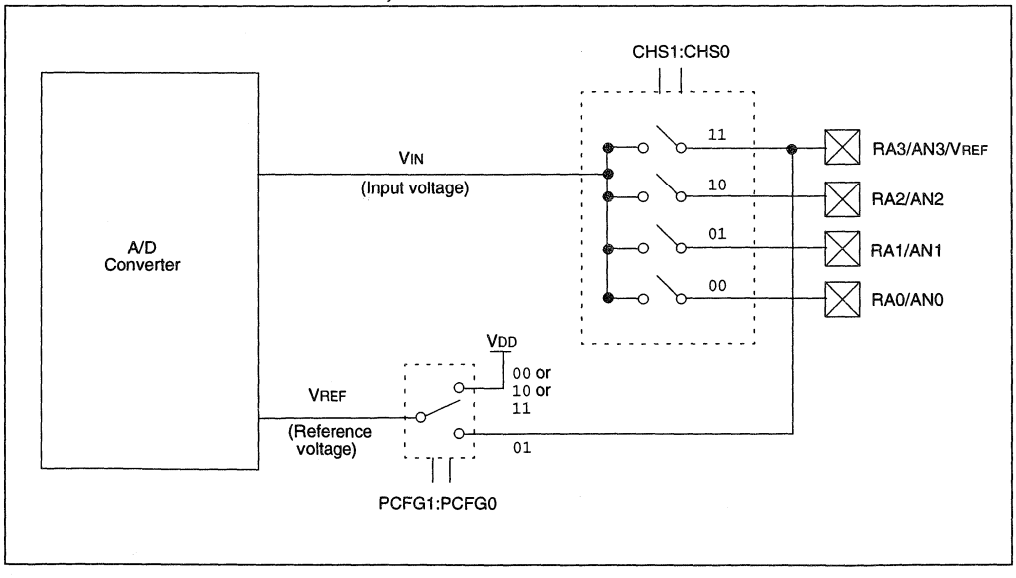

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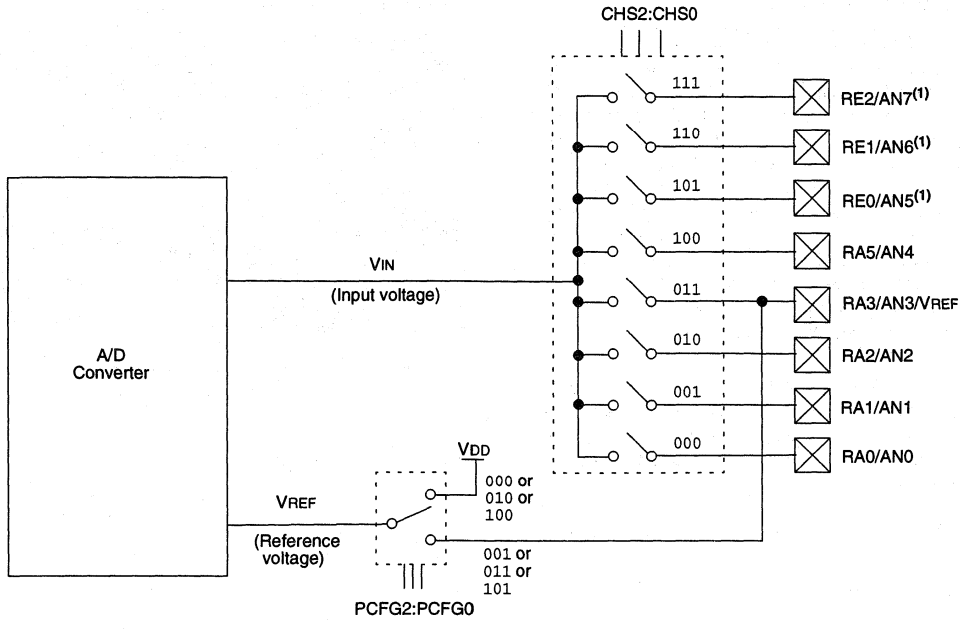
FIGURE 13-6: A/D BLOCK DIAGRAM, PIC16C72/73/73A/74/74A



Note 1: Not available on PIC16C72/73/73A.

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13.1 A/D Sampling Requirements

Applicable Devices							
710	71	711	72	73	73A	74	74A

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 13-7. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 13-7. **The maximum recommended impedance for analog sources is 10 kΩ.** After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 13-1 may be used. This equation assumes that 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

EQUATION 13-1: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/512)) \cdot (1 - e^{(-Tc/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$

or

$$Tc = -(51.2\ pF)(1\ k\Omega + R_{SS} + R_S)\ \ln(1/511)$$

Example 13-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

RS = 10 kΩ

1/2 LSb error

VDD = 5V → RSS = 7 kΩ

Temp (system max.) = 50°C

VHOLD = 0 @ t = 0

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

Note 3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

Note 4: After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

EXAMPLE 13-1: CALCULATING THE MINIMUM REQUIRED SAMPLE TIME

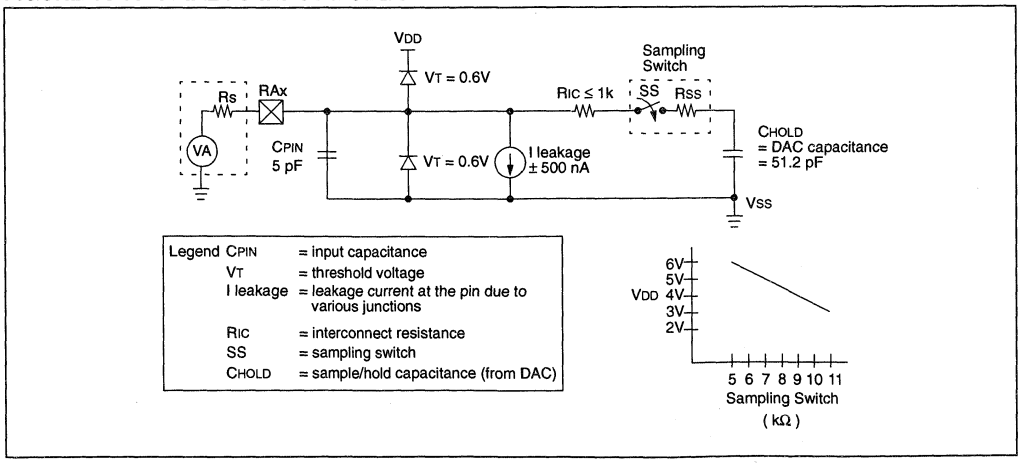
TACQ = Amplifier Settling Time +
Holding Capacitor Charging Time +
Temperature Coefficient

TACQ = 5 µs + Tc + [(Temp - 25°C)(0.05 µs/°C)]

Tc = -CHOLD (RIC + RSS + RS) ln(1/512)
-51.2 pF (1 kΩ + 7 kΩ + 10 kΩ) ln(0.0020)
-51.2 pF (18 kΩ) ln(0.0020)
-0.921 µs (-6.2146)
5.724 µs

TACQ = 5 µs + 5.724 µs + [(50°C - 25°C)(0.05 µs/°C)]
10.724 µs + 1.25 µs
11.974 µs

FIGURE 13-7: ANALOG INPUT MODEL



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13.2 Selecting the A/D Conversion Clock

Applicable Devices							
710	71	711	72	73	73A	74	74A

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5 TAD per 8-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for TAD are:

- 2TOSC
- 8TOSC
- 32TOSC
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of:

2.0 µs for the PIC16C71

1.6 µs for all other PIC16C7X devices

Table 13-2 and Table 13-1 show the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

13.3 Configuring Analog Port Pins

Applicable Devices							
710	71	711	72	73	73A	74	74A

The ADCON1, TRISA, and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, all pins configured as analog input channel will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the AN7:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

TABLE 13-1: TAD vs. DEVICE OPERATING FREQUENCIES, PIC16C71

AD Clock Source (TAD)		Device Frequency				
Operation	**ADCS1:ADCS0**	**20 MHz**	**16 MHz**	**4 MHz**	**1 MHz**	**333.33 kHz**
2TOSC	00	100 ns(2)	125 ns(2)	500 ns(2)	2.0 µs	6 µs
8TOSC	01	400 ns(2)	500 ns(2)	2.0 µs	8.0 µs	24 µs(3)
32TOSC	10	1.6 µs(2)	2.0 µs	8.0 µs	32.0 µs(3)	96 µs(3)
RC(5)	11	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1)	2 - 6 µs(1)

Note 1: The RC source has a typical TAD time of 4 µs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: While in RC mode, with device frequency above 1 MHz, conversion accuracy is out of specification.
5: For extended voltage devices (LC), please refer to Electrical Specifications section.

TABLE 13-2: TAD vs. DEVICE OPERATING FREQUENCIES, PIC16C710/711/72/73/73A/74/74A

AD Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**20 MHz**	**5 MHz**	**1.25 MHz**	**333.33 kHz**
2TOSC	00	100 ns(2)	400 ns(2)	1.6 µs	6 µs
8TOSC	01	400 ns(2)	1.6 µs	6.4 µs	24 µs(3)
32TOSC	10	1.6 µs	6.4 µs	25.6 µs(3)	96 µs(3)
RC(5)	11	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1)

Note 1: The RC source has a typical TAD time of 4 µs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: While in RC mode, with device frequency above 1 MHz, conversion accuracy is out of specification.
5: For extended voltage devices (LC), please refer to Electrical Specifications section.

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13.4 A/D Conversions

Applicable Devices							
710	71	711	72	73	73A	74	74A

Example 13-2 and Example 13-3 show how to perform an A/D conversion. The RA pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the RA0 channel.

Note: The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

EXAMPLE 13-2: DOING AN A/D CONVERSION (PIC16C710/71/711)

```
    BSF     STATUS, RP0         ; Select Page 1
    CLRF    ADCON1              ; Configure A/D inputs
    BCF     STATUS, RP0         ; Select Page 0
    MOVLW   0xC1                ; RC Clock, A/D is on, Channel 0 is selected
    MOVWF   ADCON0              ;
    BSF     INTCON, ADIE        ; Enable A/D Interrupt
    BSF     INTCON, GIE         ; Enable all interrupts
;
;  Ensure that the required sampling time for the selected input channel has elapsed.
;  Then the conversion may be started.
;
    BSF     ADCON0, GO          ; Start A/D Conversion
      :                         ; The ADIF bit will be set and the GO/DONE bit
      :                         ;  is cleared upon completion of the A/D Conversion.
```

EXAMPLE 13-3: DOING AN A/D CONVERSION (PIC16C72/73/73A/74/74A)

```
    BSF     STATUS, RP0         ; Select Page 1
    CLRF    ADCON1              ; Configure A/D inputs
    BSF     PIE1,   ADIE        ; Enable A/D interrupts
    BCF     STATUS, RP0         ; Select Page 0
    MOVLW   0xC1                ; RC Clock, A/D is on, Channel 0 is selected
    MOVWF   ADCON0              ;
    BCF     PIR1,   ADIF        ; Clear A/D interrupt flag bit
    BSF     INTCON, PEIE        ; Enable peripheral interrupts
    BSF     INTCON, GIE         ; Enable all interrupts
;
;  Ensure that the required sampling time for the selected input channel has elapsed.
;  Then the conversion may be started.
;
    BSF     ADCON0, GO          ; Start A/D Conversion
      :                         ; The ADIF bit will be set and the GO/DONE bit
      :                         ;  is cleared upon completion of the A/D Conversion.
```


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13.4.1 FASTER CONVERSION - LOWER RESOLUTION TRADE-OFF

Not all applications require a result with 8-bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the A/D module may be switched so that the TAD time violates the minimum specified time (see the applicable electrical specification). Once the TAD time violates the minimum specified time, all the following A/D result bits are not valid (see A/D Conversion Timing in the Electrical Specifications section.) The clock sources may only be switched between the three oscillator versions (cannot be switched from/to RC). The equation to determine the time before the oscillator can be switched is as follows:

Conversion time = $2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$
Where: N = number of bits of resolution required.

Since the TAD is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D oscillator may be changed. Example 13-4 shows a comparison of time required for a conversion with 4-bits of resolution, versus the 8-bit resolution conversion. The example is for devices operating at 20 MHz and 16 MHz (The A/D clock is programmed for 32TOSC), and assumes that immediately after 6TAD, the A/D clock is programmed for 2TOSC.

The 2TOSC violates the minimum TAD time since the last 4-bits will not be converted to correct values.

EXAMPLE 13-4: 4-BIT vs. 8-BIT CONVERSION TIMES

	Freq. (MHz)(1)	Resolution	
		4-bit	8-bit
TAD	20	1.6 µs	1.6 µs
	16	2.0 µs	2.0 µs
TOSC	20	50 ns	50 ns
	16	62.5 ns	62.5 ns
$2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$	20	10 µs	16 µs
	16	12.5 µs	20 µs

Note 1: The PIC16C71 has a minimum TAD time of 2.0 µs.
All other PIC16C7X devices have a minimum TAD time of 1.6 µs.

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13.5 A/D Operation During Sleep

Applicable Devices							
710	71	711	72	73	73A	74	74A

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/$\overline{\text{DONE}}$ bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in SLEEP, the GO/$\overline{\text{DONE}}$ bit must be set, followed by the SLEEP instruction.

13.6 A/D Accuracy/Error

Applicable Devices							
710	71	711	72	73	73A	74	74A

The overall accuracy of the A/D is less than ± 1 LSb for V_{DD} = 5V ± 10% and the analog V_{REF} = V_{DD}. This overall accuracy includes offset error, full scale error, and integral error. The A/D converter is guaranteed to be monotonic. The resolution and accuracy may be less when either the analog reference (V_{DD}) is less than 5.0V or when the analog reference (V_{REF}) is less than V_{DD}.

The maximum pin leakage current is ± 5 µA.

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, T_{AD} should be derived from the device oscillator. T_{AD} must not violate the minimum and should be ≤ 8 µs for preferred operation. This is because T_{AD}, when derived from T_{OSC}, is kept away from on-chip phase clock transitions. This reduces, to a large extent, the effects of digital switching noise. This is not possible with the RC derived clock. The loss of accuracy due to digital switching noise can be significant if many I/O pins are active.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

13.7 Effects of a RESET

Applicable Devices							
710	71	711	72	73	73A	74	74A

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRES register is not modified for a Power-on Reset. The ADRES register will contain unknown data after a Power-on Reset.

13.8 Use of the CCP Trigger

Applicable Devices							
710	71	711	72	73	73A	74	74A

Note: In the PIC16C72 the "special event trigger" is implemented in the CCP1 module.

An A/D conversion can be started by the "special event trigger" of the CCP2 module (CCP1 on the PIC16C72 only). This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as 1011 and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving the ADRES to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the "special event trigger" sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 counter.

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13.9 Connection Considerations

Applicable Devices							
710	71	711	72	73	73A	74	74A

If the input voltage exceeds the rail values (VSS or VDD) by greater than 0.2V, then the accuracy of the conversion is out of specification.

Note: For the PIC16C710/71/711, care must be taken when using the RA0 pin in A/D conversions due to its proximity to the OSC1 pin.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 kΩ recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

13.10 Transfer Function

Applicable Devices							
710	71	711	72	73	73A	74	74A

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) is 1 LSb (or Analog VREF / 256) (Figure 13-8).

FIGURE 13-8: A/D TRANSFER FUNCTION

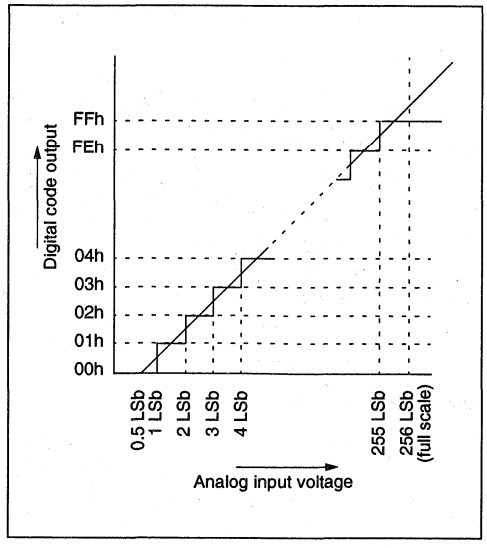

FIGURE 13-9: FLOWCHART OF A/D OPERATION

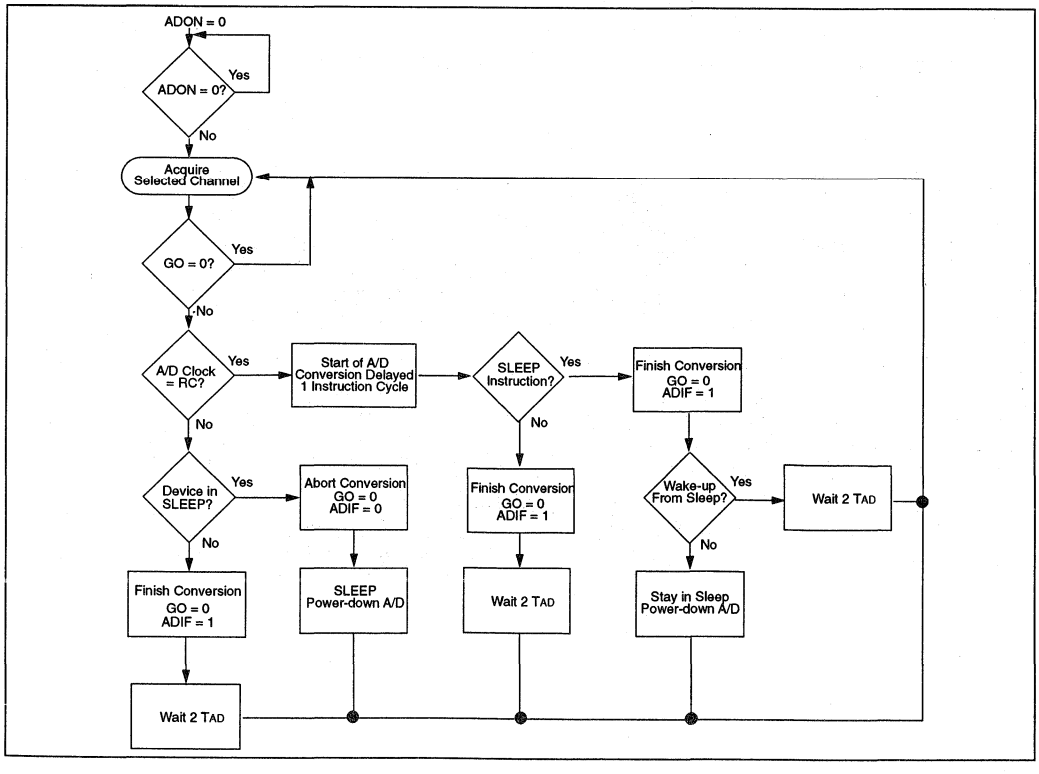

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TABLE 13-3: SUMMARY OF A/D REGISTERS, PIC16C710/71/711

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
89h	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
08h	ADCON0	ADCS1	ADCS0	—	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADIF	ADON	00-0 0000	00-0 0000
88h	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	---- --00	---- --00
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

TABLE 13-4: SUMMARY OF A/D REGISTERS, PIC16C72

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

TABLE 13-5: SUMMARY OF A/D REGISTERS, PIC16C73/73A/74/74A

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC6C73/73A, always maintain these bits clear.

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14.0 SPECIAL FEATURES OF THE CPU

Applicable Devices							
710	71	711	72	73	73A	74	74A

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

14.1 Configuration Bits

Applicable Devices							
710	71	711	72	73	73A	74	74A

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 14-1: CONFIGURATION WORD FOR PIC16C71

—	—	—	—	—	—	—	—	—	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-5: **Unimplemented**: Read as '1'

bit 4: **CP0**: Code protection bit
1 = Code protection off
0 = All memory is code protected, but 00h - 3Fh is writable

bit 3: **PWRTE**: Power-up Timer Enable bit
1 = Power-up Timer enabled
0 = Power-up Timer disabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

10

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FIGURE 14-2: CONFIGURATION WORD FOR PIC16C710/711

CP0	CP0	CP0	CP0	CP0	CP0	CP0	BODEN	CP0	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-7 **CP0**: Code protection bits (2)
5-4: 1 = Code protection off
0 = All memory is code protected, but 00h - 3Fh is writable

bit 6: **BODEN**: Brown-out Reset Enable bit (1)
1 = BOR enabled
0 = BOR disabled

bit 3: **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit (1)
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRTE}}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.
2: All of the CP0 bits have to be given the same value to enable the code protection scheme listed.

FIGURE 14-3: CONFIGURATION WORD FOR PIC16C73/74

—	—	—	—	—	—	—	—	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-5: **Unimplemented**: Read as '1'

bit 4: **CP1:CP0**: Code protection bits
11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 3: **PWRTE**: Power-up Timer Enable bit
1 = Power-up Timer enabled
0 = Power-up Timer disabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

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FIGURE 14-4: CONFIGURATION WORD FOR PIC16C72/73A/74A

CP1	CP0	CP1	CP0	CP1	CP0	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-8 **CP1:CP0**: Code Protection bits (2)
5-4: 11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 7: **Unimplemented**: Read as '1'

bit 6: **BODEN**: Brown-out Reset Enable bit (1)
1 = BOR enabled
0 = BOR disabled

bit 3: **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit (1)
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRTE}}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.
2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

14.2 Oscillator Configurations

Applicable Devices								
710	71	711	72	73	73A	74	74A

14.2.1 OSCILLATOR TYPES

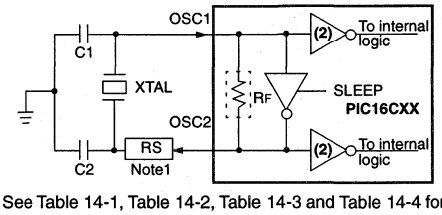
The PIC16CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

14.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 14-5). The PIC16CXX Oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 14-6).

FIGURE 14-5: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



See Table 14-1, Table 14-2, Table 14-3 and Table 14-4 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.
2: For the PIC16C710/71/711 the buffer is on the OSC2 pin, all other devices have the buffer on the OSC1 pin.

FIGURE 14-6: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

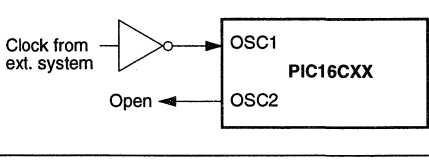


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TABLE 14-1: CERAMIC RESONATORS PIC16C71

Ranges Tested:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	47 - 100 pF 15 - 68 pF 15 - 68 pF	47 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	15 - 68 pF 10 - 47 pF	15 - 68 pF 10 - 47 pF
Note: Recommended values of C1 and C2 are identical to the ranges tested table. Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.			
Resonators Used:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%	
All resonators used did not have built-in capacitors.			

TABLE 14-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C71

Mode	Freq	OSC1	OSC2
LP	32 kHz 200 kHz	33 - 68 pF 15 - 47 pF	33 - 68 pF 15 - 47 pF
XT	100 kHz 500 kHz 1 MHz 2 MHz 4 MHz	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF
HS	8 MHz 20 MHz	15 - 47 pF 15 - 47 pF	15 - 47 pF 15 - 47 pF
Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.			

TABLE 14-3: CERAMIC RESONATORS PIC16C710/711/72/73/73A/74/74A

Ranges Tested:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF
Note: Recommended values of C1 and C2 are identical to the ranges tested table. Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.			
Resonators Used:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%	
All resonators used did not have built-in capacitors.			

TABLE 14-4: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR FOR PIC16C710/711/72/73/73A/74/74A

Mode	Freq	OSC1	OSC2
LP	32 kHz(1) 200 kHz	15 - 47 pF 15 - 33 pF	15 - 47 pF 15 - 33 pF
XT	100 kHz 500 kHz 1 MHz 2 MHz 4 MHz	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF
HS	8 MHz 20 MHz	15 - 47 pF 15 - 47 pF	15 - 47 pF 15 - 47 pF
Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components. Note 1: For $V_{DD} > 4.5V$, $C1 = C2 \approx 30$ pF is recommended.			

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14.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 14-7 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 14-7: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

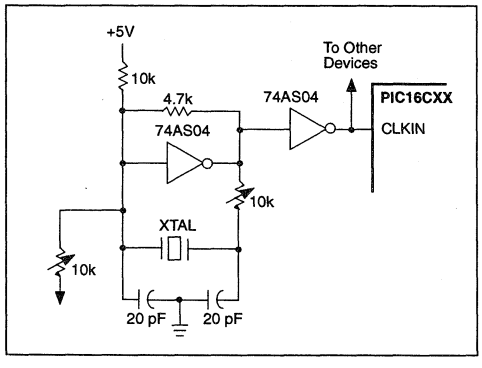
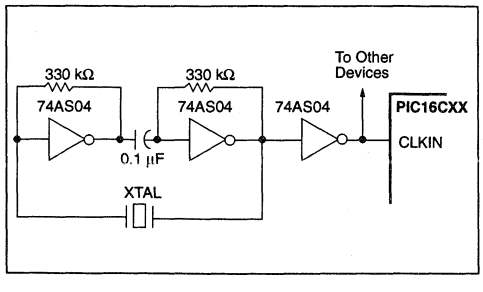


Figure 14-8 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 14-8: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



14.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 14-9 shows how the R/C combination is connected to the PIC16CXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kΩ and 100 kΩ.

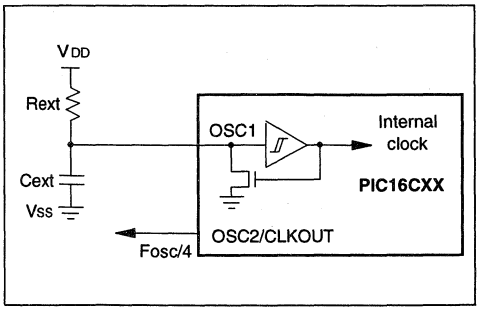
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See characterization data for desired device for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characterization data for desired device for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-5 for waveform).

FIGURE 14-9: RC OSCILLATOR MODE



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14.3 Reset

Applicable Devices							
710	71	711	72	73	73A	74	74A

The PIC16CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{MCLR}$ reset during normal operation
- $\overline{MCLR}$ reset during SLEEP
- WDT Reset (normal operation)
- Brown-out Reset (BOR) (PIC16C710/711/72/73A/74A)

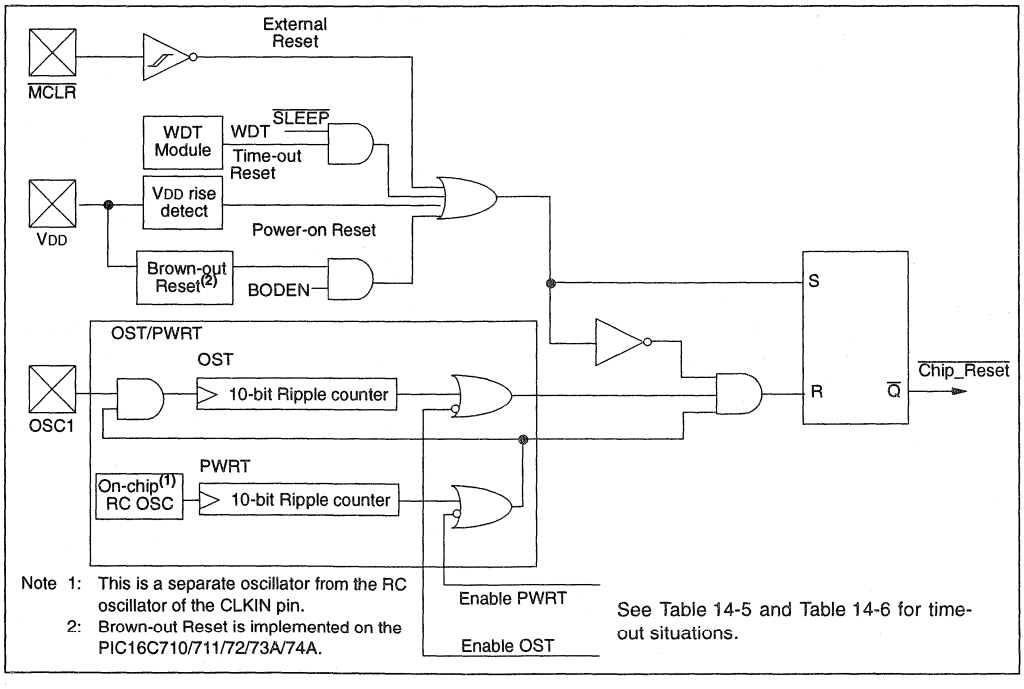
Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on the $\overline{MCLR}$ and WDT Reset, on $\overline{MCLR}$ reset during SLEEP, and Brown-out Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 14-7 and Table 14-8. These bits are used in software to determine the nature of the reset. See Table 14-10 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 14-10.

The PIC16C710/711/72/73A/74A have a $\overline{MCLR}$ noise filter in the $\overline{MCLR}$ reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

FIGURE 14-10: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



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14.4 Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST), Brown-out Reset (BOR)

Applicable Devices							
710	71	711	72	73	73A	74	74A

14.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting.*"

14.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

14.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

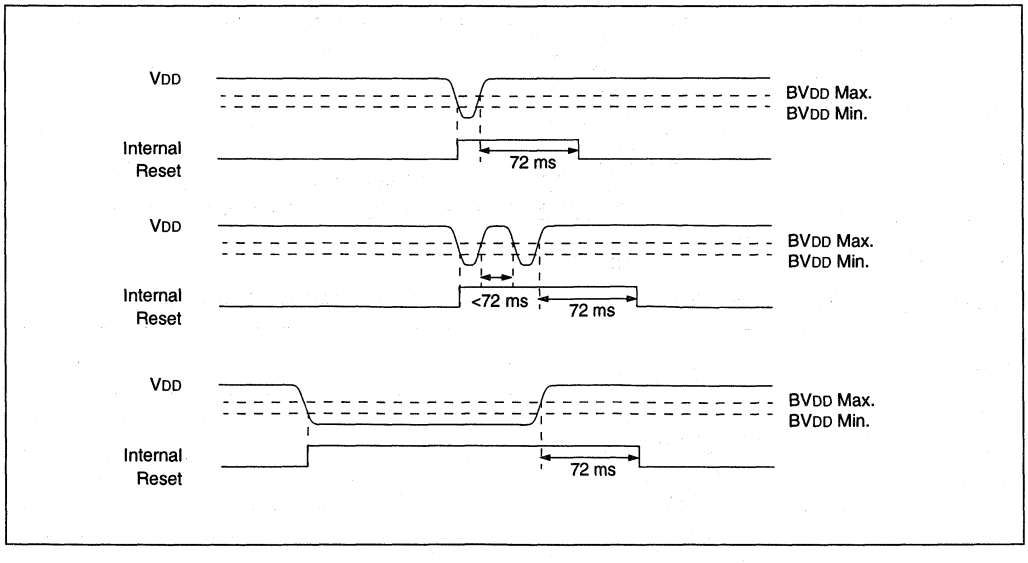
The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

14.4.4 BROWN-OUT RESET (BOR)

Applicable Devices							
710	71	711	72	73	73A	74	74A

A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (3.8V - 4.2V range) for greater than parameter #35, the brown-out situation will reset the chip. A reset may not occur if VDD falls below 4.0V for less than parameter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 14-11 shows typical brown-out situations.

FIGURE 14-11: BROWN-OUT SITUATIONS



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14.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 14-12, Figure 14-13, and Figure 14-14 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (Figure 14-13). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 14-9 shows the reset conditions for some special function registers, while Table 14-10 shows the reset conditions for all the registers.

14.4.6 POWER CONTROL/STATUS REGISTER (PCON)

Applicable Devices							
710	71	711	72	73	73A	74	74A

The Power Control/Status Register, PCON has up to 2 bits, depending upon the device. Bit0 is not implemented on the PIC16C73 or PIC16C74.

Bit0 is Brown-out Reset Status bit, $\overline{BOR}$. Bit $\overline{BOR}$ is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{BOR}$ cleared, indicating a BOR occurred. The $\overline{BOR}$ bit is a "Don't Care" bit and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is Power-on Reset Status bit $\overline{POR}$. It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 14-5: TIME-OUT IN VARIOUS SITUATIONS, PIC16C71/73/74

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024 TOSC
RC	72 ms	—	—

TABLE 14-6: TIME-OUT IN VARIOUS SITUATIONS, PIC16C710/711/72/73A/74A

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024TOSC
RC	72 ms	—	72 ms	—

TABLE 14-7: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C71/73/74

$\overline{POR}$(1)	$\overline{TO}$	$\overline{PD}$	
0	1	1	Power-on Reset
0	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	1	WDT Reset
1	0	0	WDT Wake-up
1	u	u	$\overline{MCLR}$ Reset during normal operation
1	1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

Legend: u = unchanged, x = unknown
Note 1: Bit $\overline{POR}$ is not implemented on the PIC16C71.

TABLE 14-8: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C710/711/72/73A/74A

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{MCLR}$ Reset during normal operation
1	1	1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

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TABLE 14-9: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register PIC16C710/711	PCON Register PIC16C73/74	PCON Register PIC16C72/73A/74A
Power-on Reset	000h	0001 1xxx	---- --0x	---- --0-	---- --0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- --uu	---- --u-	---- --uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---- --uu	---- --u-	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu	---- --u-	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu	---- --u-	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0	N/A	---- --u0
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --uu	---- --u-	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 14-10: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices								Power-on Reset, Brown-out Reset	$\overline{MCLR}$ Resets WDT Reset	Wake-up via WDT or Interrupt
W	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	710	71	711	72	73	73A	74	74A	N/A	N/A	N/A
TMR0	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	710	71	711	72	73	73A	74	74A	0000h	0000h	PC + 1(2)
STATUS	710	71	711	72	73	73A	74	74A	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	710	71	711	72	73	73A	74	74A	---x 0000	---u 0000	---u uuuu
	710	71	711	72	73	73A	74	74A	--0x 0000	--0u 0000	--uu uuuu
PORTB	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	710	71	711	72	73	73A	74	74A	---- -xxx	---- -uuu	---- -uuu
PCLATH	710	71	711	72	73	73A	74	74A	---0 0000	---0 0000	---u uuuu
INTCON	710	71	711	72	73	73A	74	74A	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	710	71	711	72	73	73A	74	74A	-0-- 0000	-0-- 0000	-u-- uuuu(1)
	710	71	711	72	73	73A	74	74A	-000 0000	-000 0000	-uuu uuuu(1)
	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu(1)
PIR2	710	71	711	72	73	73A	74	74A	---- ---0	---- ---0	---- ---u(1)
TMR1L	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	710	71	711	72	73	73A	74	74A	--00 0000	--uu uuuu	--uu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition
Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: See Table 14-9 for reset value for specific condition.

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TABLE 14-10: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Register	Applicable Devices								Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
TMR2	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
T2CON	710	71	711	72	73	73A	74	74A	-000 0000	-000 0000	-uuu uuuu
SSPBUF	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
CCPR1L	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	710	71	711	72	73	73A	74	74A	--00 0000	--00 0000	--uu uuuu
RCSTA	710	71	711	72	73	73A	74	74A	0000 -00x	0000 -00x	uuuu -uuu
TXREG	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
RCREG	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
CCPR2L	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2H	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
ADRES	710	71	711	72	73	73A	74	74A	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	710	71	711	72	73	73A	74	74A	00-0 0000	00-0 0000	uu-u uuuu
	710	71	711	72	73	73A	74	74A	0000 00-0	0000 00-0	uuuu uu-u
OPTION	710	71	711	72	73	73A	74	74A	1111 1111	1111 1111	uuuu uuuu
TRISA	710	71	711	72	73	73A	74	74A	---1 1111	---1 1111	---u uuuu
	710	71	711	72	73	73A	74	74A	--11 1111	--11 1111	--uu uuuu
TRISB	710	71	711	72	73	73A	74	74A	1111 1111	1111 1111	uuuu uuuu
TRISC	710	71	711	72	73	73A	74	74A	1111 1111	1111 1111	uuuu uuuu
TRISD	710	71	711	72	73	73A	74	74A	1111 1111	1111 1111	uuuu uuuu
TRISE	710	71	711	72	73	73A	74	74A	0000 -111	0000 -111	uuuu -uuu
PIE1	710	71	711	72	73	73A	74	74A	-0-- 0000	-0-- 0000	-u-- uuuu
	710	71	711	72	73	73A	74	74A	-000 0000	-000 0000	-uuu uuuu
	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
PIE2	710	71	711	72	73	73A	74	74A	---- ---0	---- ---0	---- ---u
PCON	710	71	711	72	73	73A	74	74A	---- --0-	---- --u-	---- --u-
	710	71	711	72	73	73A	74	74A	---- --0u	---- --uu	---- --uu
PR2	710	71	711	72	73	73A	74	74A	1111 1111	1111 1111	1111 1111
SSPADD	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	710	71	711	72	73	73A	74	74A	--00 0000	--00 0000	--uu uuuu
TXSTA	710	71	711	72	73	73A	74	74A	0000 -010	0000 -010	uuuu -uuu
SPBRG	710	71	711	72	73	73A	74	74A	0000 0000	0000 0000	uuuu uuuu
ADCON1	710	71	711	72	73	73A	74	74A	---- --00	---- --00	---- --uu
	710	71	711	72	73	73A	74	74A	---- -000	---- -000	---- -uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 14-9 for reset value for specific condition.

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FIGURE 14-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

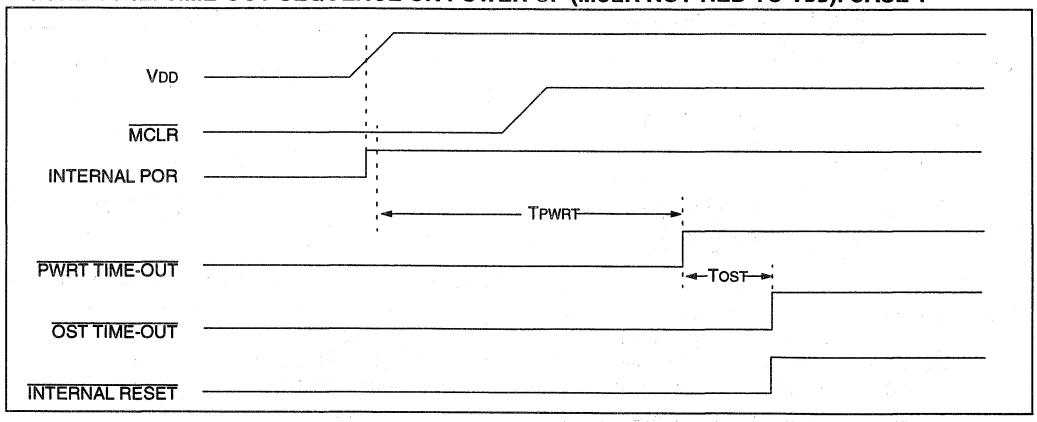

FIGURE 14-13: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

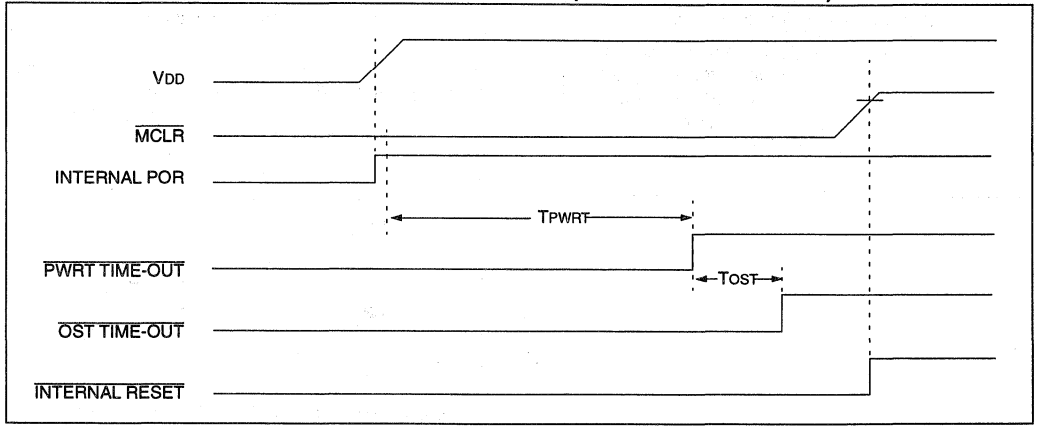

FIGURE 14-14: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

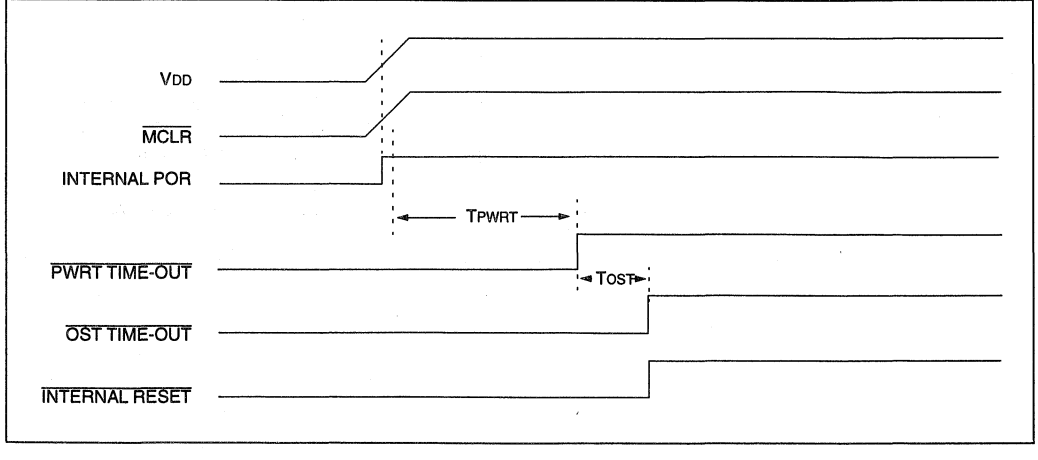

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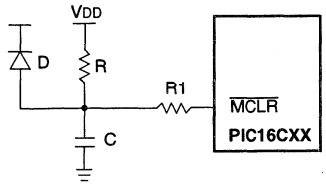
FIGURE 14-15: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

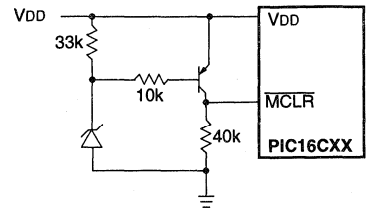


Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 14-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

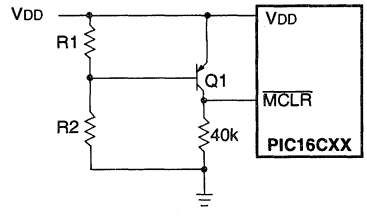


Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

2: Internal brown-out detection on the PIC16C710/711/72/73A/74A should be disabled when using this circuit.

3: Resistors should be adjusted for the characteristics of the transistor.

FIGURE 14-17: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Internal brown-out detection on the PIC16C710/711/72/73A/74A should be disabled when using this circuit.

3: Resistors should be adjusted for the characteristics of the transistor.

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14.5 Interrupts

Applicable Devices							
710	71	711	72	73	73A	74	74A

The PIC16C7X family has up to 12 sources of interrupt:

Interrupt Sources	Applicable Devices							
External interrupt RB0/INT	710	71	711	72	73	73A	74	74A
TMR0 overflow interrupt	710	71	711	72	73	73A	74	74A
PORTB change interrupts (pins RB7:RB4)	710	71	711	72	73	73A	74	74A
A/D Interrupt	710	71	711	72	73	73A	74	74A
TMR1 overflow interrupt	710	71	711	72	73	73A	74	74A
TMR2 matches period interrupt	710	71	711	72	73	73A	74	74A
CCP1 interrupt	710	71	711	72	73	73A	74	74A
CCP2 interrupt	710	71	711	72	73	73A	74	74A
USART Receive	710	71	711	72	73	73A	74	74A
USART Transmit	710	71	711	72	73	73A	74	74A
Synchronous serial port interrupt	710	71	711	72	73	73A	74	74A
Parallel slave port read/write interrupt	710	71	711	72	73	73A	74	74A

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set regardless of the status of the GIE bit. The GIE bit is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2, and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 14-22). The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note: For the PIC16C71/73/74

If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction). The events that would cause this to occur are:

1. An instruction clears the GIE bit while an interrupt is acknowledged.
2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the RETFIE instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

Perform the following to ensure that interrupts are globally disabled:

```
LOOP BCF    INTCON, GIE  ; Disable global
                         ;  interrupt bit
     BTFSC  INTCON, GIE  ; Global interrupt
                         ;   disabled?
     GOTO   LOOP         ; NO, try again
       :                 ;   Yes, continue
                         ;   with program
                         ;   flow
```

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FIGURE 14-18: INTERRUPT LOGIC FOR PIC16C710/71/711

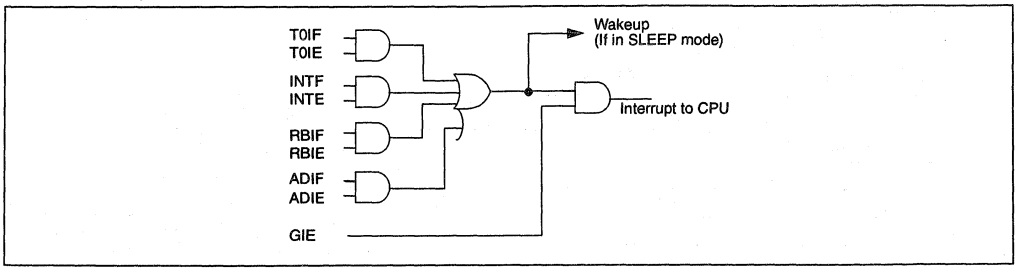

FIGURE 14-19: INTERRUPT LOGIC FOR PIC16C72

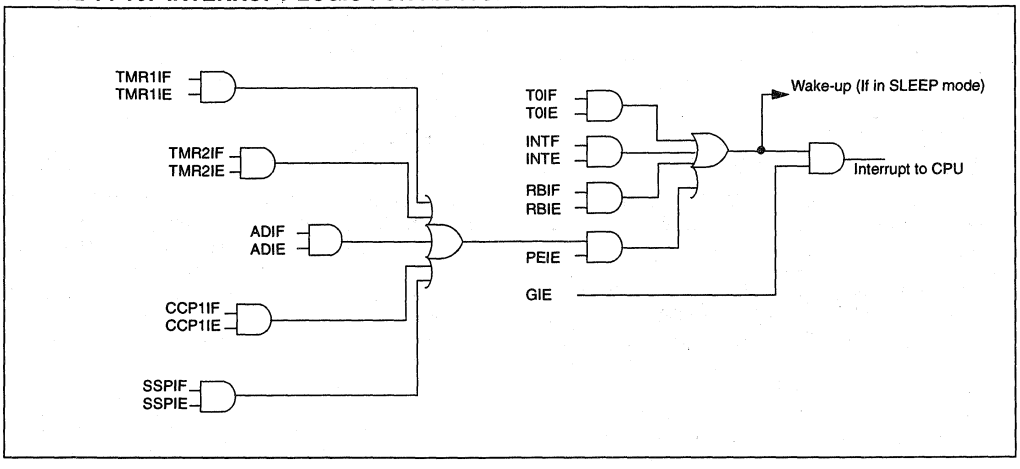

FIGURE 14-20: INTERRUPT LOGIC FOR PIC16C73/73A

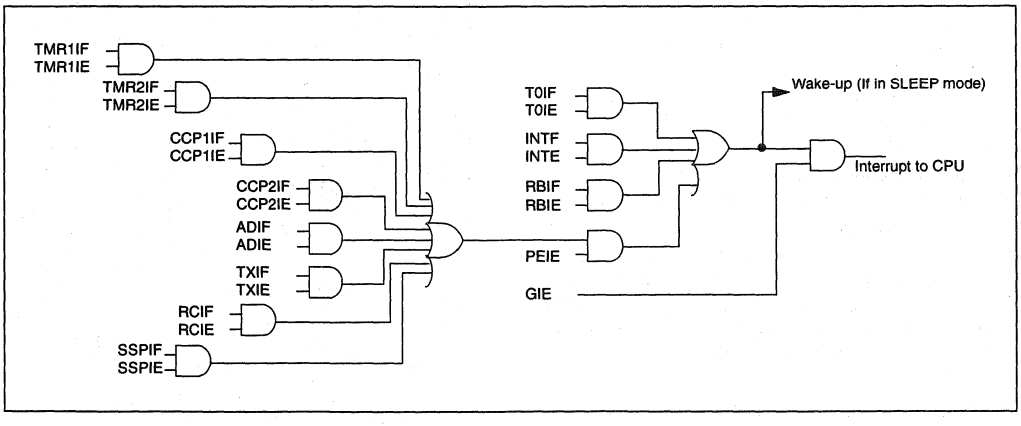

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FIGURE 14-21: INTERRUPT LOGIC FOR PIC16C74/74A

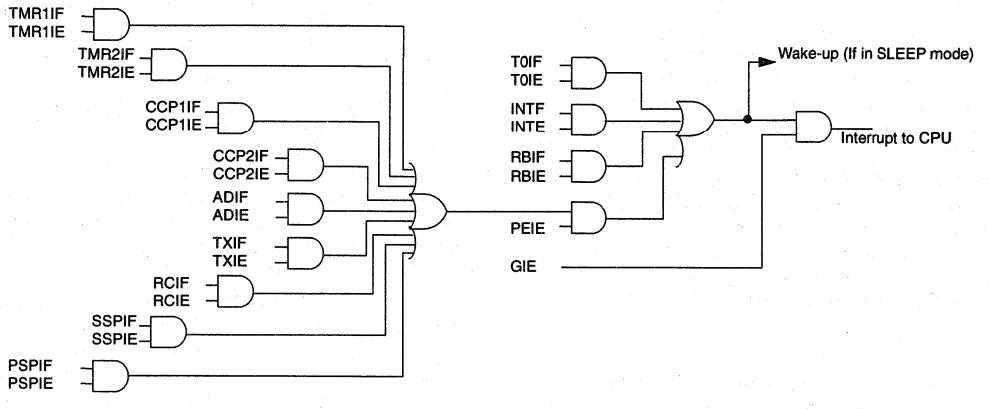
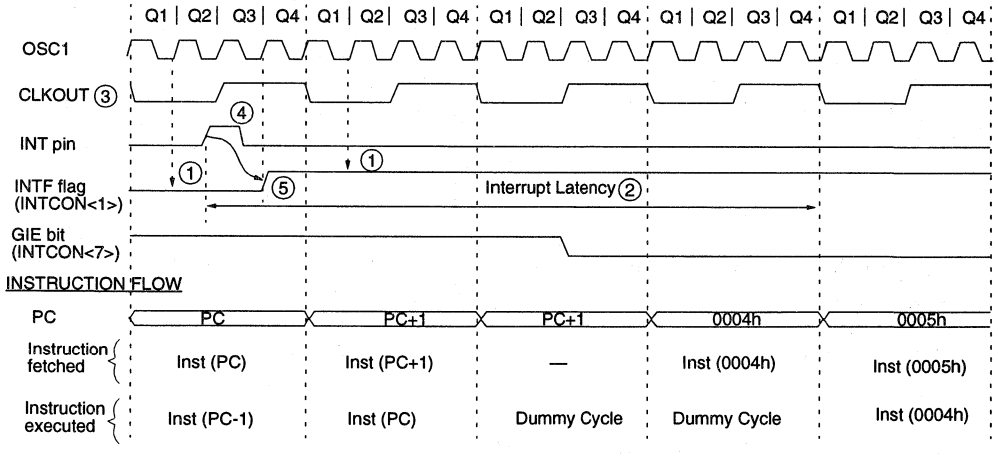


FIGURE 14-22: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

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14.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 14.8 for details on SLEEP mode.

14.5.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 7.0)

14.5.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 5.2)

Note: For the PIC16C71/73/74 if a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

14.6 Context Saving During Interrupts

Applicable Devices							
710	71	711	72	73	73A	74	74A

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 14-1 and Example 14-2 store and restore the STATUS and W registers. For PIC16C72/73/73A/74/74A, the register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1). For PIC16C710/71/711, the user register, STATUS_TEMP, must be defined in bank 0.

The example:

a) Stores the W register.
b) Stores the STATUS register in bank 0.
c) Executes the ISR code.
d) Restores the STATUS register (and bank select bit).
e) Restores the W register.

EXAMPLE 14-1: SAVING STATUS AND W REGISTERS IN RAM (PIC16C710/71/711)

```
MOVWF   W_TEMP          ;Copy W to TEMP register, could be bank one or zero
SWAPF   STATUS,W        ;Swap status to be saved into W
MOVWF   STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF   STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF   STATUS          ;Move W into STATUS register
SWAPF   W_TEMP,F        ;Swap W_TEMP
SWAPF   W_TEMP,W        ;Swap W_TEMP into W
```

EXAMPLE 14-2: SAVING STATUS AND W REGISTERS IN RAM (PIC16C72/73/73A/74/74A)

```
MOVWF   W_TEMP          ;Copy W to TEMP register, could be bank one or zero
SWAPF   STATUS,W        ;Swap status to be saved into W
BCF     STATUS,RP0      ;Change to bank zero, regardless of current bank
MOVWF   STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF   STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF   STATUS          ;Move W into STATUS register
SWAPF   W_TEMP,F        ;Swap W_TEMP
SWAPF   W_TEMP,W        ;Swap W_TEMP into W
```


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14.7 Watchdog Timer (WDT)

Applicable Devices							
710	71	711	72	73	73A	74	74A

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 14.1).

14.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

14.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When the prescaler is assigned to the WDT, always execute a CLRWDT instruction before changing the prescale value, otherwise a WDT reset may occur.

FIGURE 14-23: WATCHDOG TIMER BLOCK DIAGRAM

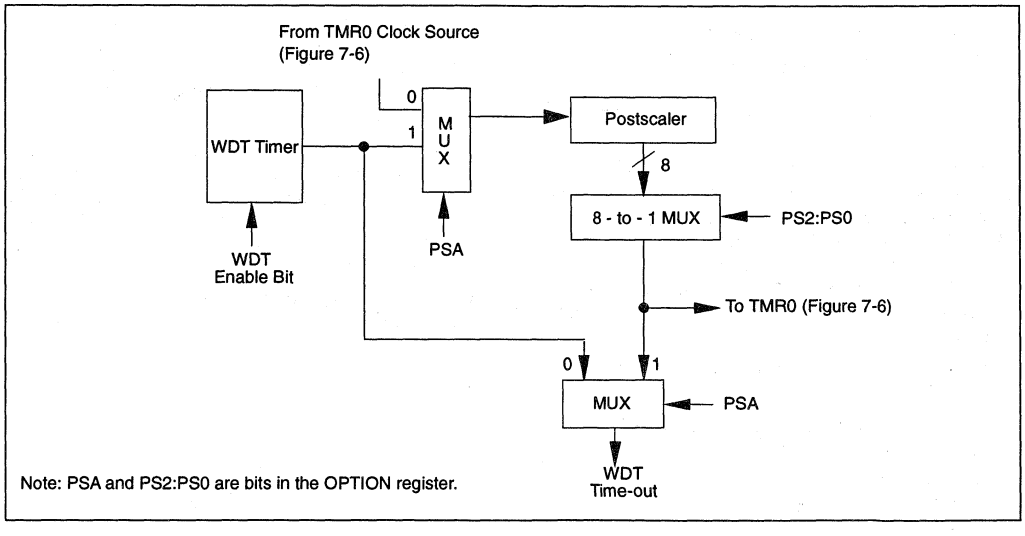

FIGURE 14-24: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN(1)	CP1	CP0	PWRTE(1)	WDTE	FOSC1	FOSC0
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 14-1, Figure 14-2, Figure 14-3, and Figure 14-4 for operation of these bits.

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14.8 Power-down Mode (SLEEP)

Applicable Devices							
710	71	711	72	73	73A	74	74A

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D, disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

14.8.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from INT pin, RB port change, or some Peripheral Interrupts.

External $\overline{MCLR}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. SSP (Start/Stop) bit detect interrupt.
3. SSP transmit or receive in slave mode (SPI/ I^2C).
4. CCP capture mode interrupt.
5. Parallel Slave Port read or write.
6. A/D conversion (when A/D clock source is RC).
7. Special event trigger (Timer1 in asynchronous mode using an external clock).
8. USART TX or RX (synchronous slave mode).

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

14.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep . The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

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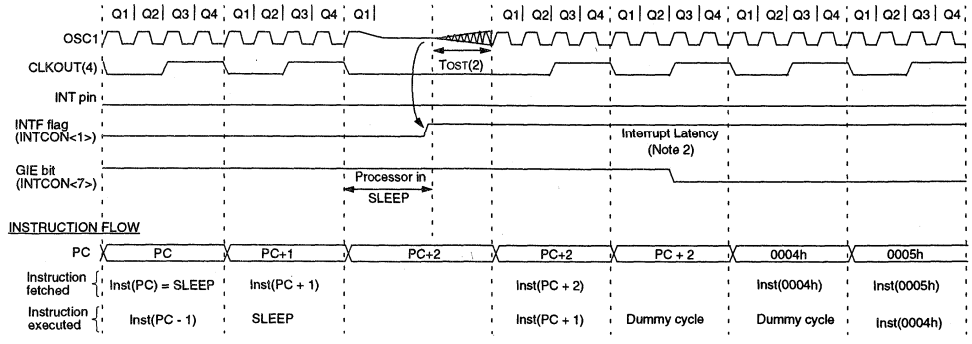
FIGURE 14-25: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

14.9 Program Verification/Code Protection

Applicable Devices							
710	71	711	72	73	73A	74	74A

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

14.10 ID Locations

Applicable Devices							
710	71	711	72	73	73A	74	74A

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

14.11 In-Circuit Serial Programming

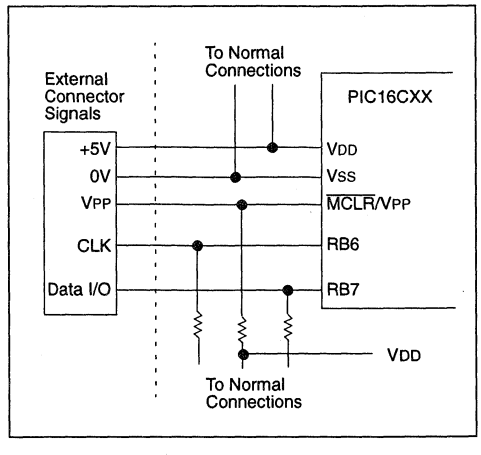
Applicable Devices							
710	71	711	72	73	73A	74	74A

PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

FIGURE 14-26: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



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NOTES:

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Applicable Devices | 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

15.0 ELECTRICAL CHARACTERISTICS FOR PIC16C710 AND PIC16C711

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V
Total power dissipation (Note 1) 1.0W
Maximum current out of VSS pin ..... 300 mA
Maximum current into VDD pin ..... 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA ..... 200 mA
Maximum current sourced by PORTA ..... 200 mA
Maximum current sunk by PORTB ..... 200 mA
Maximum current sourced by PORTB ..... 200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD - VOH) x IOH} + Σ(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

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Applicable Devices	710	71	711	72	73	73A	74	74A

TABLE 15-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C710-04 PIC16C711-04	PIC16C710-10 PIC16C711-10	PIC16C710-20 PIC16C711-20	PIC16LC710-04 PIC16LC711-04	PIC16C710/JW PIC16C711/JW
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

PRELIMINARY

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Applicable Devices	710	71	711	72	73	73A	74	74A

15.1 DC Characteristics: PIC16C710-04 (Commercial, Industrial, Automotive(5)) PIC16C711-04 (Commercial, Industrial, Automotive(5)) PIC16C710-10 (Commercial, Industrial, Automotive(5)) PIC16C711-10 (Commercial, Industrial, Automotive(5)) PIC16C710-20 (Commercial, Industrial, Automotive(5)) PIC16C711-20 (Commercial, Industrial, Automotive(5))

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +710°C for commercial				
Param. No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2)	IDD	-	2.7	5	mA	XT, RC osc configuration (PIC16C710/711-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration (PIC16C710/711-20) FOSC = 20 MHz, VDD = 5.5V
D015	Brown-out Reset Current (Note 6)	ΔIBOR	-	300*	500	µA	BOR enabled VDD = 5.0V
D020	Power-down Current (Note 3)	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.5	21	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.5	24	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			-	1.5	TBD	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C
D023	Brown-out Reset Current (Note 6)	ΔIBOR	-	300*	500	µA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Automotive operating range is Advance Information for this device.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PRELIMINARY

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Applicable Devices 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

15.2 DC Characteristics: PIC16LC710-04 (Commercial, Industrial) PIC16LC711-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	3.0	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	µA	BOR enabled VDD = 3.0V
D020	Power-down Current (Note 3)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D021B			-	0.9	10	µA	VDD = 3.0V, WDT disabled, -40°C to +125°C
D023	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	µA	BOR enabled VDD = 3.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PRELIMINARY

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Applicable Devices | 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

15.3 DC Characteristics:

PIC16C710-04 (Commercial, Industrial, Automotive(4))
PIC16C711-04 (Commercial, Industrial, Automotive(4))
PIC16C710-10 (Commercial, Industrial, Automotive(4))
PIC16C711-10 (Commercial, Industrial, Automotive(4))
PIC16C710-20 (Commercial, Industrial, Automotive(4))
PIC16C711-20 (Commercial, Industrial, Automotive(4))
PIC16LC710-04 (Commercial, Industrial)
PIC16LC711-04 (Commercial, Industrial)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI,OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR, RA4/T0CKI RB0/INT		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Automotive operating range is Advance Information for this device.

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Applicable Devices	710	71	711	72	73	73A	74	74A

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD - 0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD - 0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Automotive operating range is Advance Information for this device.

PRELIMINARY

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15.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

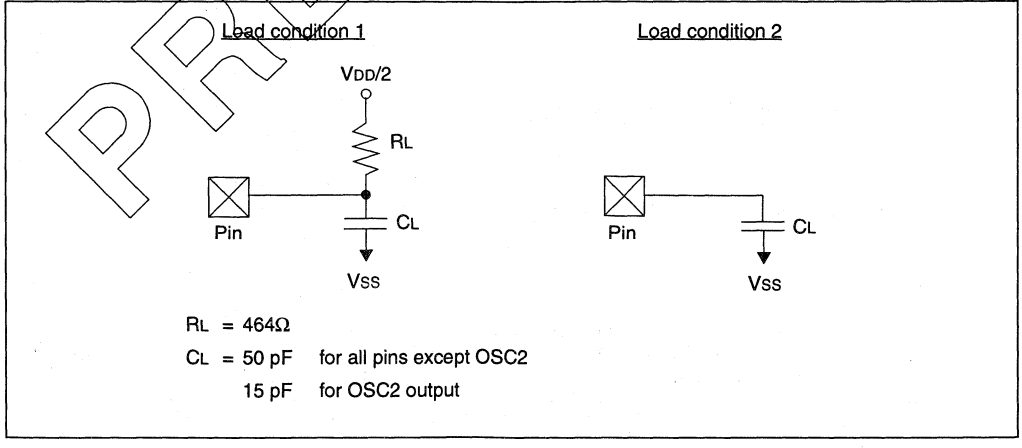
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 15-1: LOAD CONDITIONS



RL = 464Ω
CL = 50 pF for all pins except OSC2
15 pF for OSC2 output

PRELIMINARY

Applicable Devices 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

15.5 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING

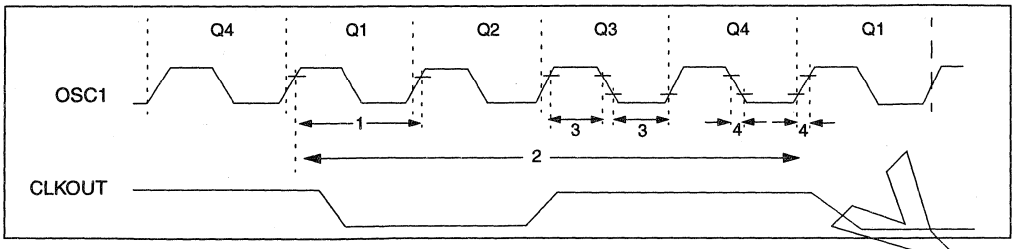


TABLE 15-2: CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C710/711-04,)
			DC	—	20	MHz	HS osc mode (PIC16C710/711-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C710/711-04)
			4	—	10	MHz	HS osc mode (PIC16C710/711-10)
			4	—	20	MHz	HS osc mode (PIC16C710/711-20)
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C710/711-04)
			100	—	—	ns	HS osc mode (PIC16C710/711-10)
			50	—	—	ns	HS osc mode (PIC16C710/711-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C710/711-04)
			100	—	250	ns	HS osc mode (PIC16C710/711-10)
			50	—	250	ns	HS osc mode (PIC16C710/711-20)
			5	—	—	µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	50	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			10	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC16C710/711.

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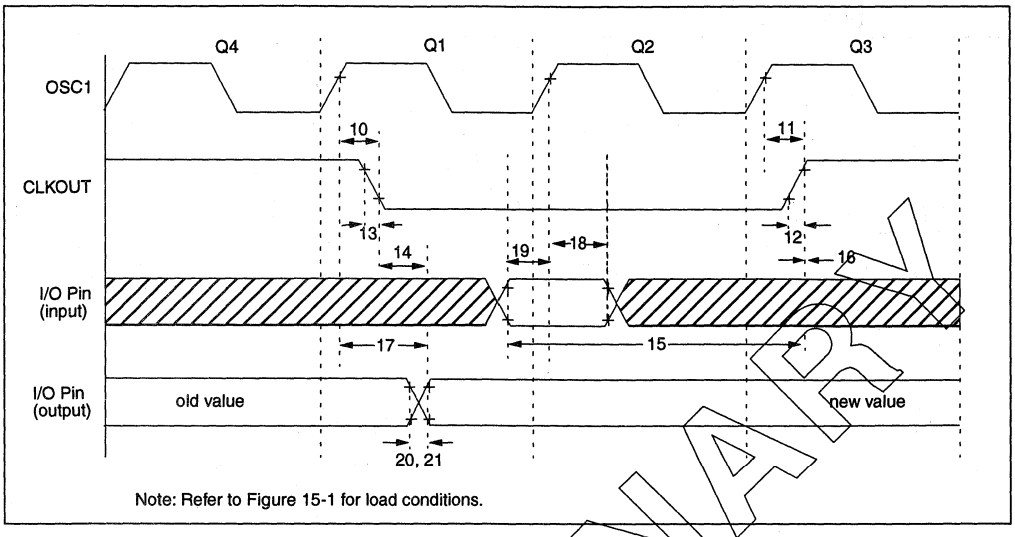
Applicable Devices | 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

FIGURE 15-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 15-1 for load conditions.

TABLE 15-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time		—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	—	80 - 100	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		TBD	—	—	ns	
20*	TioR	Port output rise time	PIC16C710/711	—	10	25	ns	
			PIC16LC710/711	—	—	60	ns	
21*	TioF	Port output fall time	PIC16C710/711	—	10	25	ns	
			PIC16LC710/711	—	—	60	ns	
22††*	Tinp	INT pin high or low time		20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		20	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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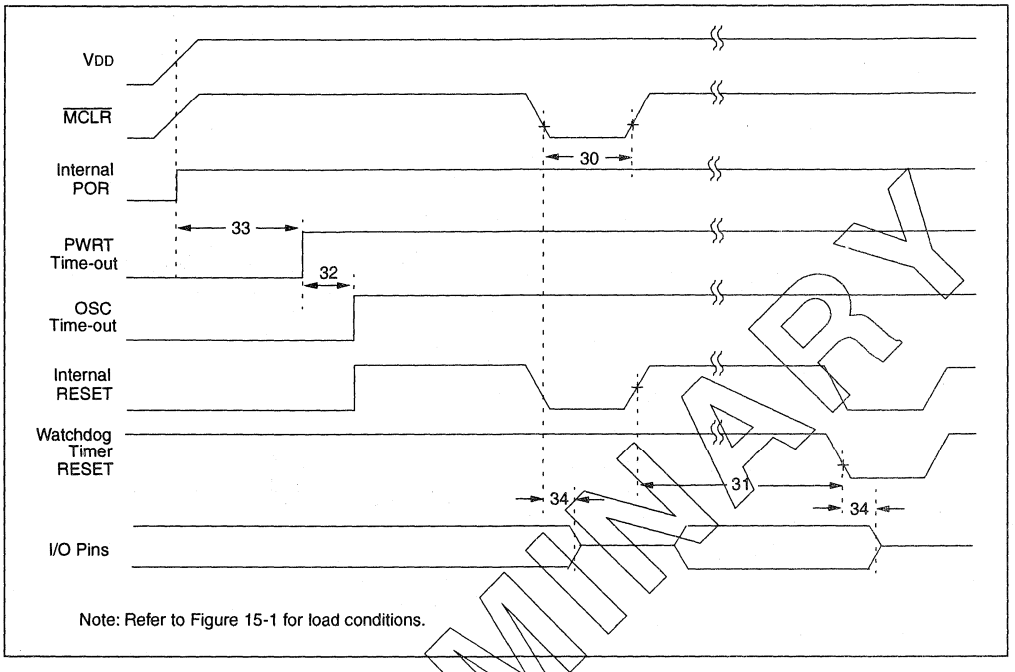
Applicable Devices 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

FIGURE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 15-1 for load conditions.

FIGURE 15-5: BROWN-OUT RESET TIMING

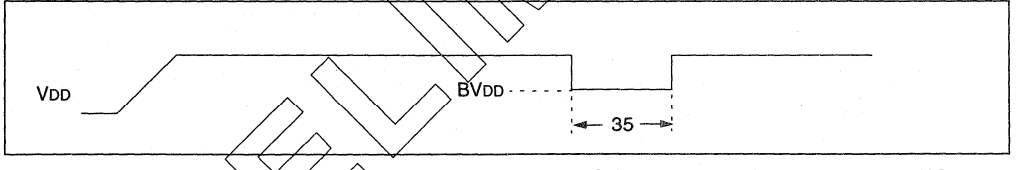


TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1	—	—	µs	VDD = 5V, -40°C to +125°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—	—	Tosc = OSC1 period
33	Tpwrt	Power up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	1.1	µs	
35	TBOR	Brown-out Reset pulse width	100	—	—	µs	3.8V ≤ VDD ≤ 4.2V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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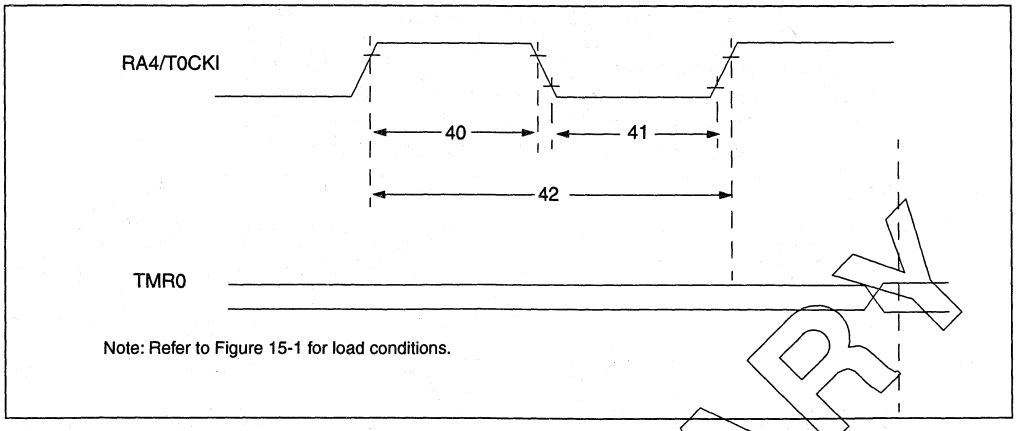
FIGURE 15-6: TIMER0 CLOCK TIMINGS



Note: Refer to Figure 15-1 for load conditions.

TABLE 15-5: TIMER0 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		Greater of: 20µs or $\frac{T_{CY} + 40^*}{N}$	—	—	ns	N = prescale value (1, 2, 4,..., 256)
48	Tcke2tmrl	Delay from external clock edge to timer increment		2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 15-6: A/D CONVERTER CHARACTERISTICS:
PIC16C710-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(3))
PIC16C711-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(3))
PIC16C710-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(3))
PIC16C711-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(3))
PIC16C710-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(3))
PIC16C711-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(3))

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 5.42V, VSS ≤ AIN ≤ VREF
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	µA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

3: Automotive operating range is Advance Information for this device.

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Applicable Devices 710 71 711 72 73 73A 74 74A

TABLE 15-7: A/D CONVERTER CHARACTERISTICS: PIC16LC710-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(4)) PIC16LC711-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE(4))

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 3.0V (Note 1)
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	µA	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 3)	—	—	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V. VIN must be between VSS and VREF

2: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

4: Automotive operating range is Advance Information for this device.

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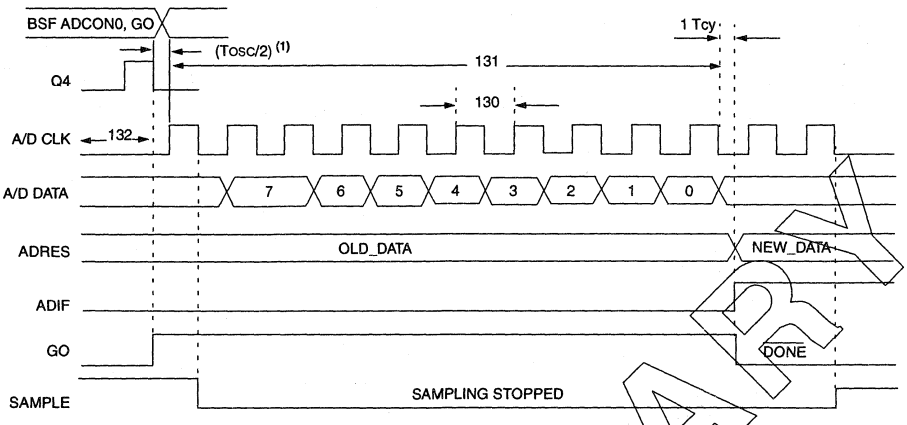
FIGURE 15-7: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-8: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	1.6		—	µs	VREF ≥ 3.0V
			2.0		—	µs	VREF full range
130	TAD	A/D Internal RC Oscillator source					ADCS1:ADCS0 = 11 (RC oscillator source)
			3.0	6.0	9.0	µs	PIC16LC710, VDD = 3.0V
			2.0	4.0	6.0	µs	PIC16C710
131	TCNV	Conversion time (not including S/H time). Note 1	—	9.5TAD	—	—	
132	TACQ	Acquisition time	Note 2	20	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

PRELIMINARY

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Applicable Devices	710	71	711	72	73	73A	74	74A

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C710 AND PIC16C711

NOT AVAILABLE AT THIS TIME

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NOTES:

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17.0 ELECTRICAL CHARACTERISTICS FOR PIC16C71

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V
Total power dissipation (Note 1) ..... 800 mW
Maximum current out of VSS pin ..... 150 mA
Maximum current into VDD pin ..... 100 mA
Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 20 mA
Maximum current sunk by PORTA ..... 80 mA
Maximum current sourced by PORTA ..... 50 mA
Maximum current sunk by PORTB ..... 150 mA
Maximum current sourced by PORTB ..... 100 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 17-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C71-04	PIC16C71-20	PIC16LC71-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.0 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 15 µA typ. at 32 kHz, 4.0V IPD: 0.6 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 9 µA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 9 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices	710	71	711	72	73	73A	74	74A

17.1 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration (PIC16C71-20) FOSC = 20 MHz, VDD = 5.5V
D020	Power-down Current	IPD	-	7	28	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021	(Note 3)		-	1.0	14	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.0	16	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

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17.2 DC Characteristics: PIC16LC71-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	3.0	-	6.0	V	XT, RC, and LP osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	1.4	2.5	mA	FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	15	32	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-down Current (Note 3)	IPD	-	5	20	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.6	9	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.6	12	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

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Applicable Devices	710	71	711	72	73	73A	74	74A

17.3 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial) PIC16LC71-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 17.1 and Section 17.2.				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI,OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports (Note 4)	VIH		-			
D040	with TTL buffer		0.36VDD	-	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.45VDD	-	VDD		For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.85VDD	-	VDD		For entire VDD range
D042	MCLR RA4/T0CKI		0.85VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	†400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6mA, VDD = 4.5V, -40°C to +85°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3mA, VDD = 4.5V, -40°C to +85°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: PIC16C71 Rev. "Ax" INT pin has a TTL input buffer. PIC16C71 Rev. "Bx" INT pin has a Schmitt Trigger input buffer.

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17.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

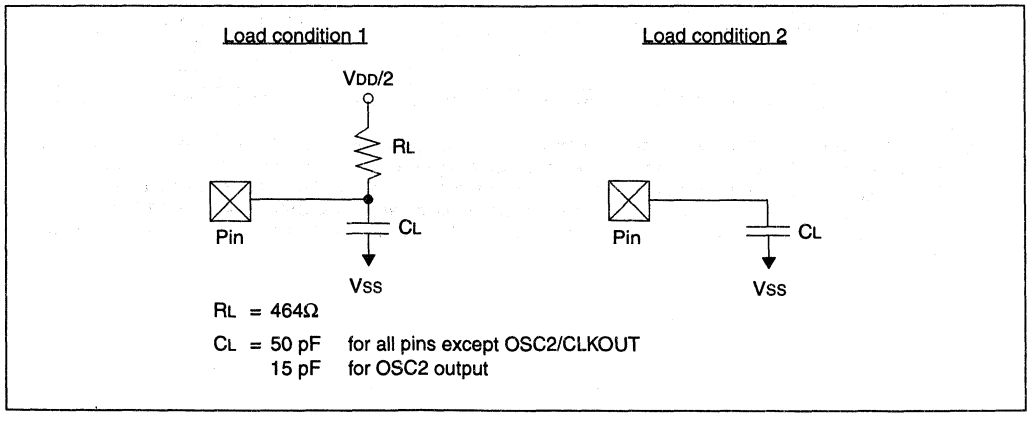
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 17-1: LOAD CONDITIONS



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17.5 Timing Diagrams and Specifications

FIGURE 17-2: EXTERNAL CLOCK TIMING

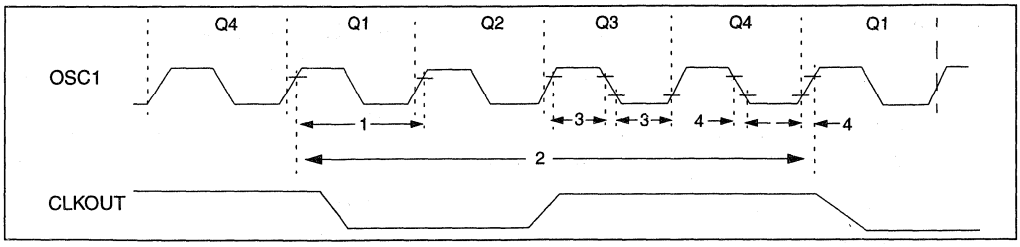

TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C71-04)
			DC	—	20	MHz	HS osc mode (PIC16C71-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			1	—	4	MHz	HS osc mode (PIC16C71-04)
			1	—	20	MHz	HS osc mode (PIC16C71-20)
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C71-04)
			50	—	—	ns	HS osc mode (PIC16C71-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	1,000	ns	HS osc mode (PIC16C71-04)
			50	—	1,000	ns	HS osc mode (PIC16C71-20)
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	1.0	Tcy	DC	µs	Tcy = 4/Fosc
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	50	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			10	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	25	—	—	ns	XT oscillator
			50	—	—	ns	LP oscillator
			15	—	—	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC16C71.

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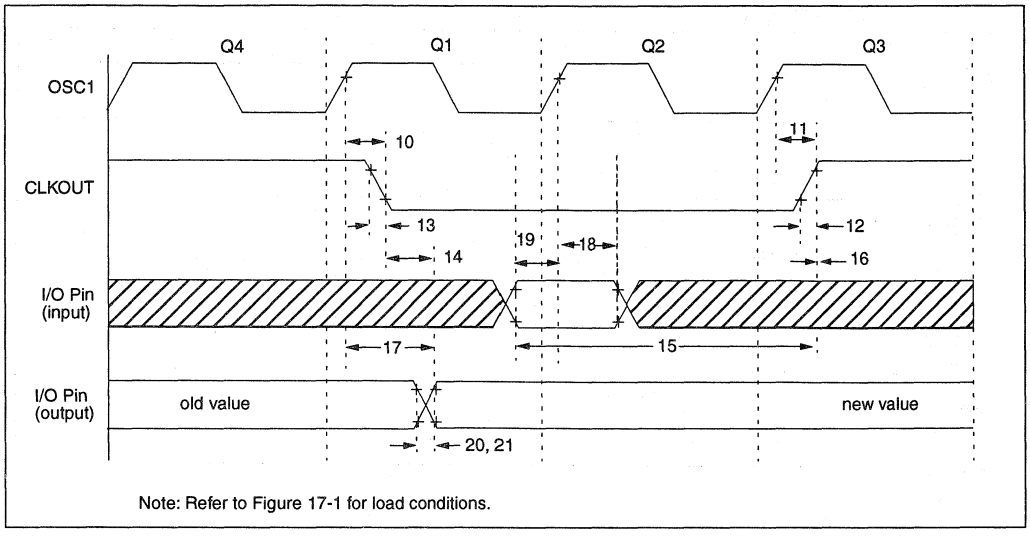
FIGURE 17-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 17-1 for load conditions.

TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time		—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	—	80 - 100	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C71	100	—	—	ns	
			PIC16LC71	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C71	—	10	25	ns	
			PIC16LC71	—	—	60	ns	
21*	TioF	Port output fall time	PIC16C71	—	10	25	ns	
			PIC16LC71	—	—	60	ns	
22††*	Tinp	INT pin high or low time		20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		20	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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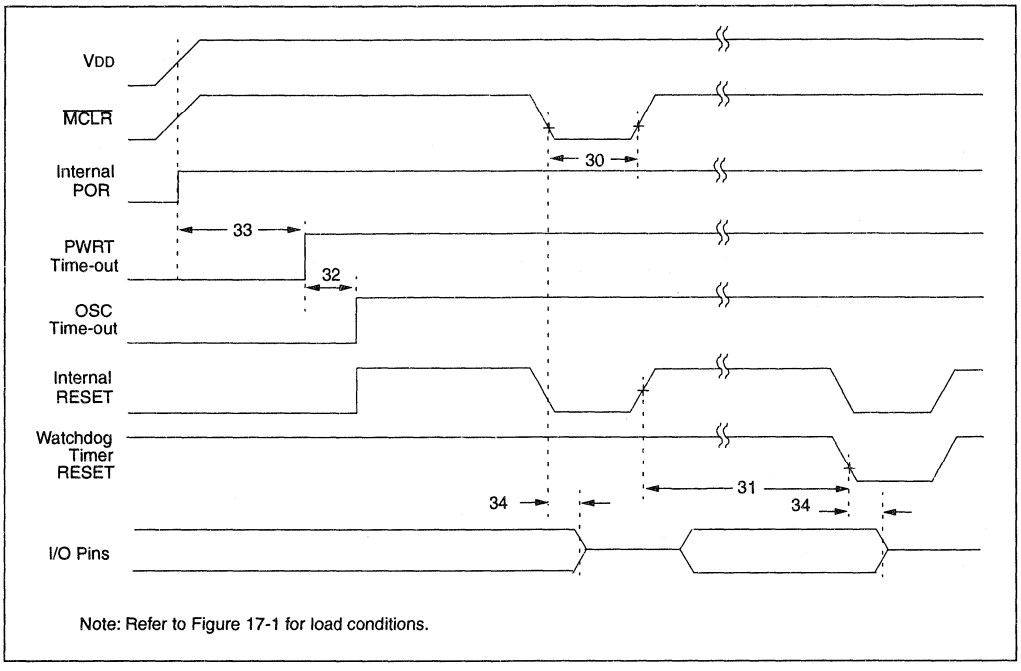
FIGURE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 17-1 for load conditions.

TABLE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	200	—	—	ns	VDD = 5V, -40°C to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +85°C
34	Tioz	I/O High Impedance from $\overline{MCLR}$ Low	—	—	100	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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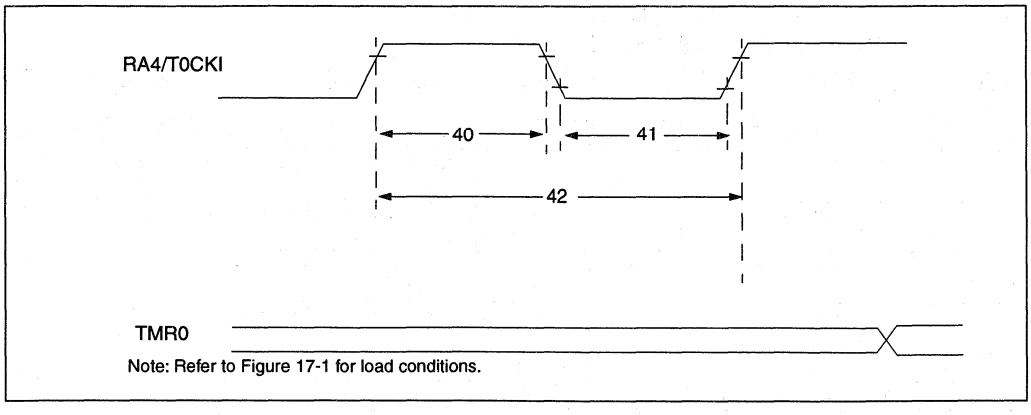
FIGURE 17-5: TIMER0 CLOCK TIMINGS



Note: Refer to Figure 17-1 for load conditions.

TABLE 17-5: TIMER0 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	T0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	T0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	T0P	T0CKI Period		Greater of: 20µs or $\frac{T_{CY} + 40^*}{N}$	—	—	ns	N = prescale value (2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Applicable Devices	710	71	711	72	73	73A	74	74A

TABLE 17-6: A/D CONVERTER CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL) PIC16C71-20 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8 bits	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 40	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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TABLE 17-7: A/D CONVERTER CHARACTERISTICS: PIC16LC71-04 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8 bits	—	VREF = VDD = 3.0V (Note 1)
	NINT	integral error	—	—	less than ±2 LSb	—	VREF = VDD = 3.0V (Note 1)
	NDIF	Differential error	—	—	less than ±2 LSb	—	VREF = VDD = 3.0V (Note 1)
	NFS	Full scale error	—	—	less than ±2 LSb	—	VREF = VDD = 3.0V (Note 1)
	NOFF	Offset error	—	—	less than ±2 LSb	—	VREF = VDD = 3.0V (Note 1)
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	µA	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 3)	—	—	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V. VIN must be between VSS and VREF

2: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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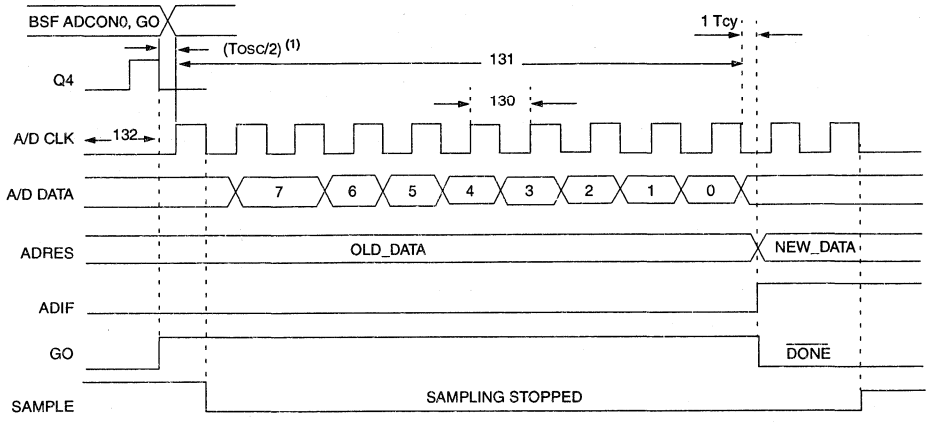
FIGURE 17-6: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 17-8: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period		2.0	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16C71	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16LC71	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	10TAD	—	—	
132	TACQ	Acquisition time		Note 2	20	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

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18.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C71

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. **In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.**

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

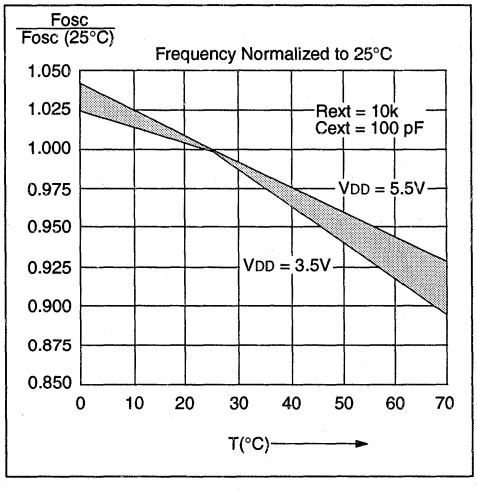


FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

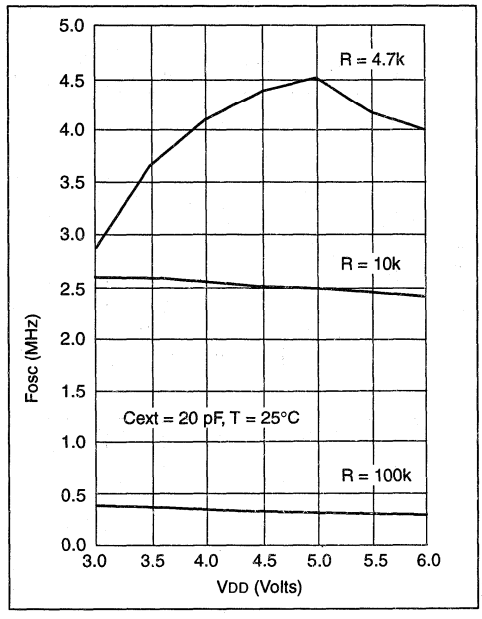
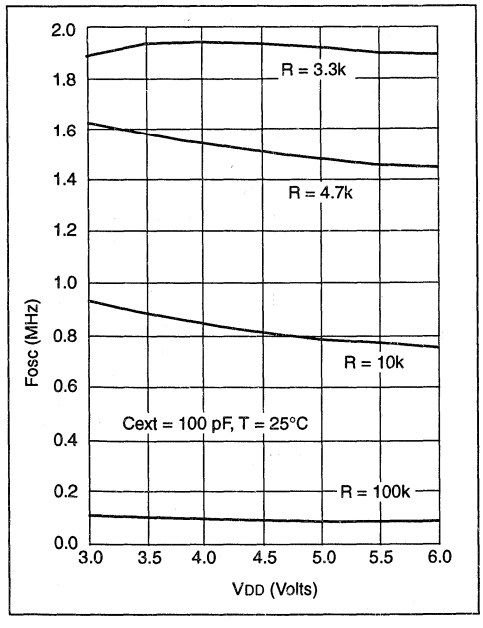


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



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Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

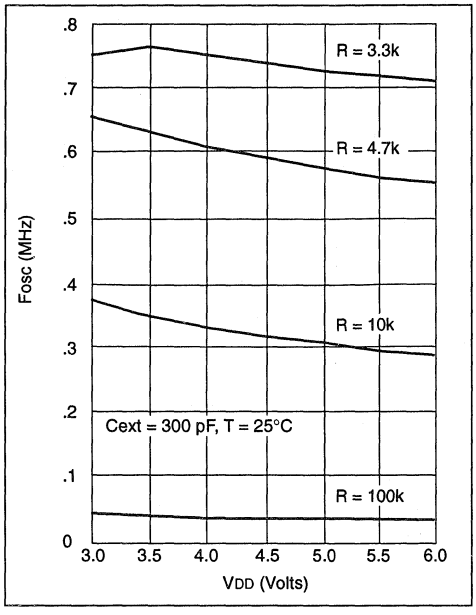


FIGURE 18-5: TYPICAL IPD vs. VDD WATCHDOG TIMER DISABLED 25°C

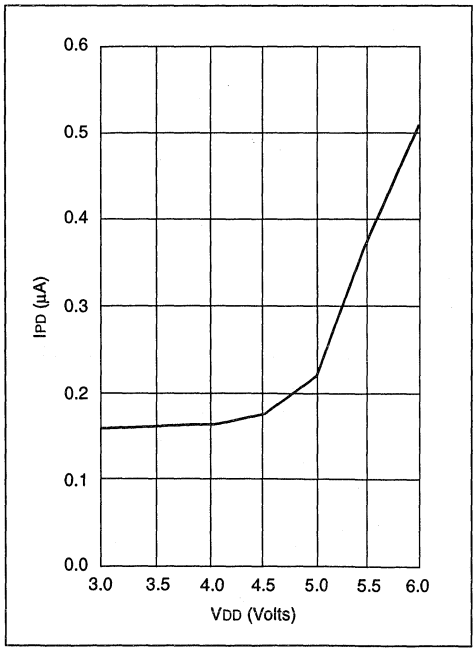
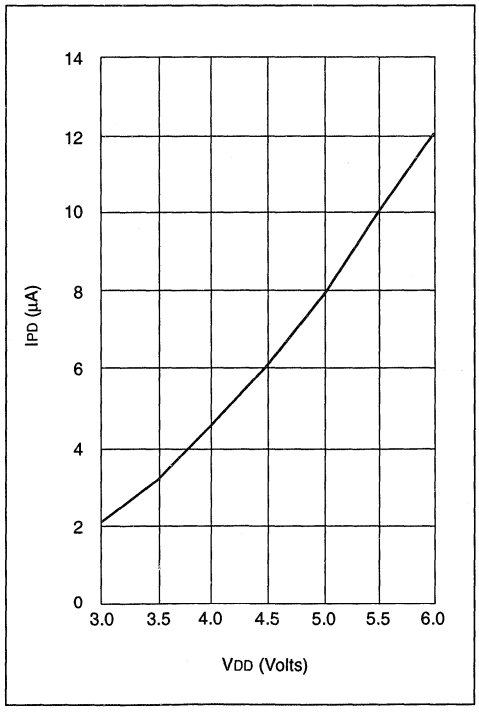


TABLE 18-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20 pf	4.7k	4.52 MHz	±17.35%
	10k	2.47 MHz	±10.10%
	100k	290.86 kHz	±11.90%
100 pf	3.3k	1.92 MHz	±9.43%
	4.7k	1.49 MHz	±9.83%
	10k	788.77 kHz	±10.92%
	100k	88.11 kHz	±16.03%
300 pf	3.3k	726.89 kHz	±10.97%
	4.7k	573.95 kHz	±10.14%
	10k	307.31 kHz	±10.43%
	100k	33.82 kHz	±11.24%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

FIGURE 18-6: TYPICAL IPD vs. VDD WATCHDOG TIMER ENABLED 25°C



Data based on matrix samples. See first page of this section for details.

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FIGURE 18-7: MAXIMUM IPD VS. VDD WATCHDOG DISABLED

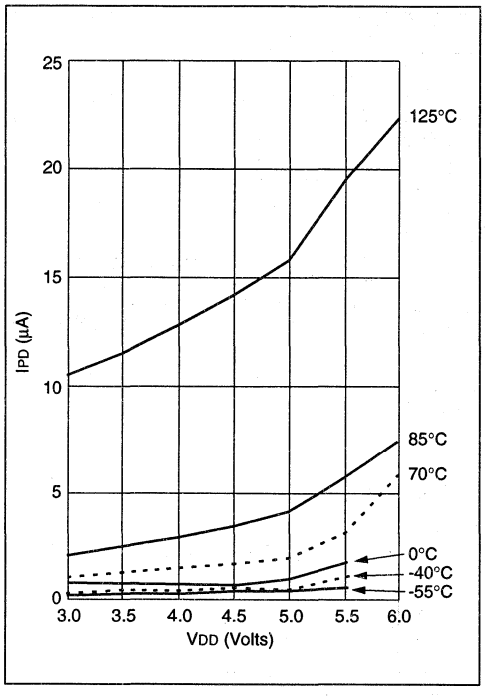
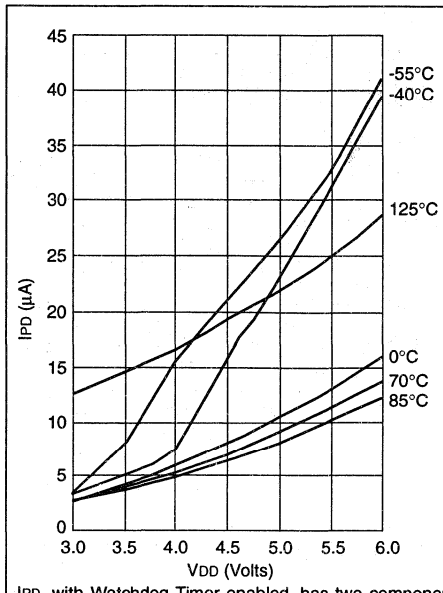
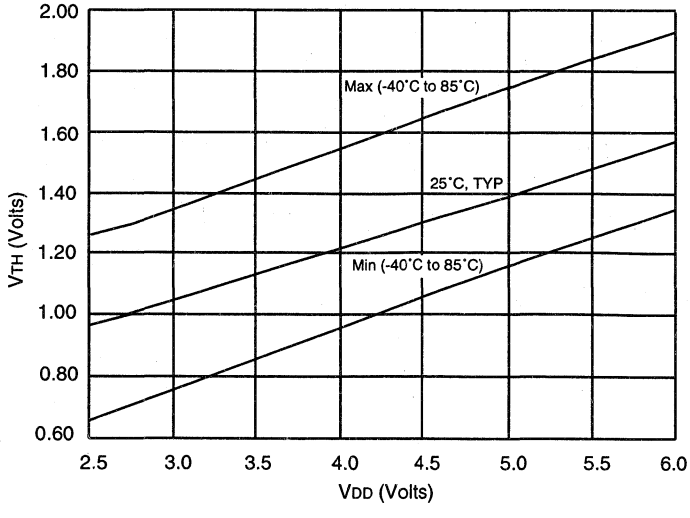


FIGURE 18-8: MAXIMUM IPD VS. VDD WATCHDOG ENABLED



IPD, with Watchdog Timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the Watchdog Timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 18-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS VS. VDD



Data based on matrix samples. See first page of this section for details.

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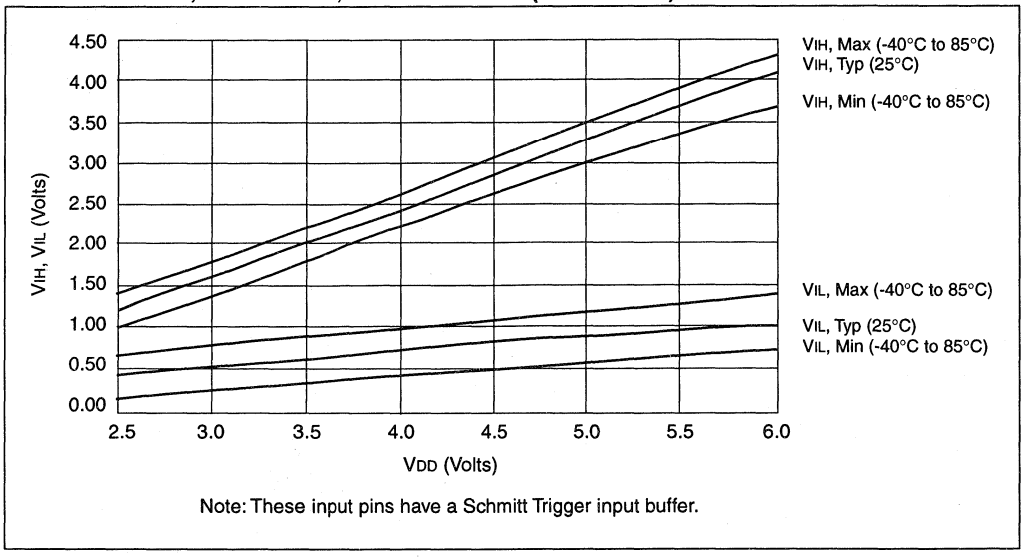
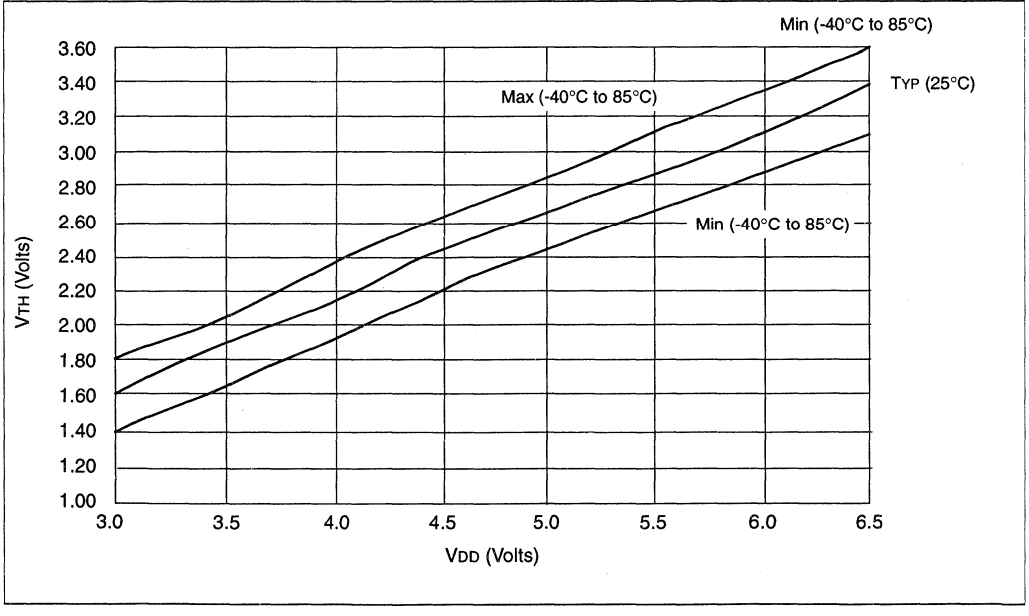
Applicable Devices 70 | 71 | 71A | 72 | 73 | 73A | 74 | 74A

FIGURE 18-10: VIH, VIL OF $\overline{MCLR}$, T0CKI AND OSC1 (IN RC MODE) VS. VDD



Note: These input pins have a Schmitt Trigger input buffer.

FIGURE 18-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) VS. VDD



Data based on matrix samples. See first page of this section for details.

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Applicable Devices | 70 | 71 | 71A | 72 | 73 | 73A | 74 | 74A

FIGURE 18-12: TYPICAL IDD vs. FREQ (EXT CLOCK, 25°C)

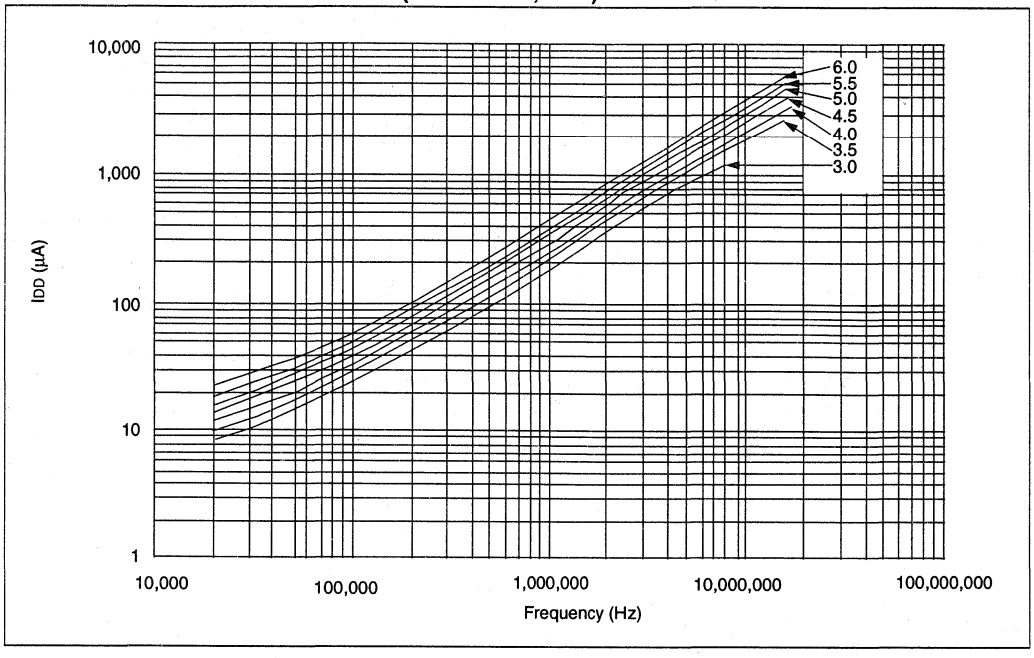
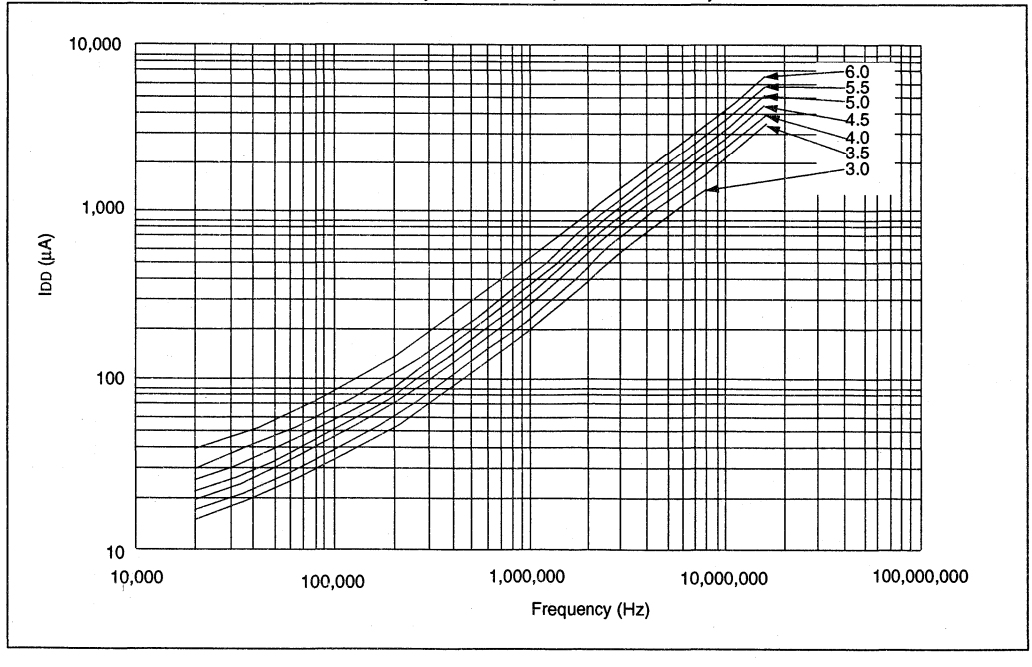


FIGURE 18-13: MAXIMUM, IDD vs. FREQ (EXT CLOCK, -40° TO +85°C)



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	70	71	71A	72	73	73A	74	74A

FIGURE 18-14: MAXIMUM IDD VS. FREQ WITH A/D OFF (EXT CLOCK, -55° TO +125°C)

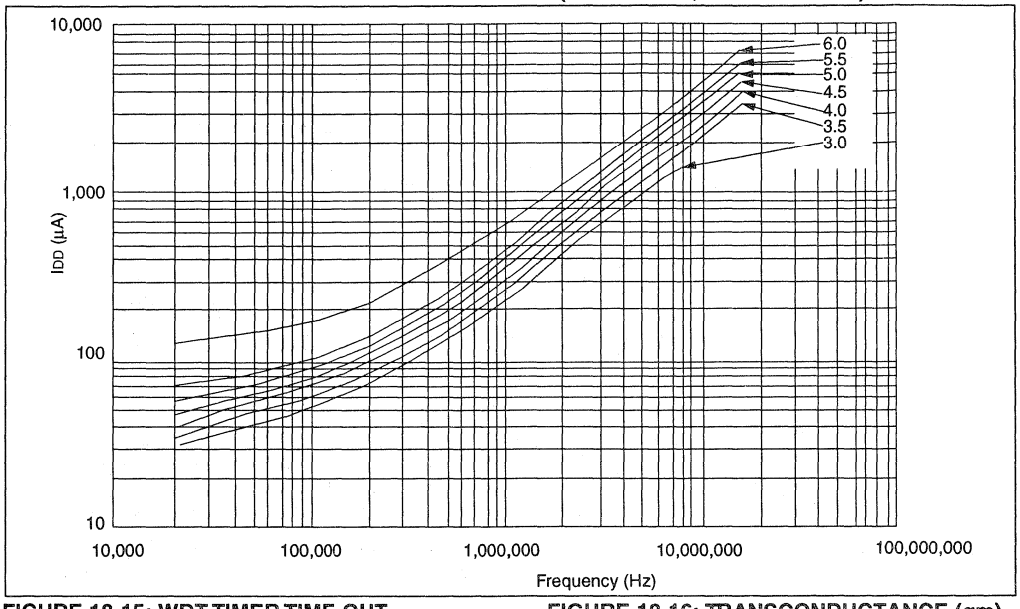


FIGURE 18-15: WDT TIMER TIME-OUT PERIOD VS. VDD

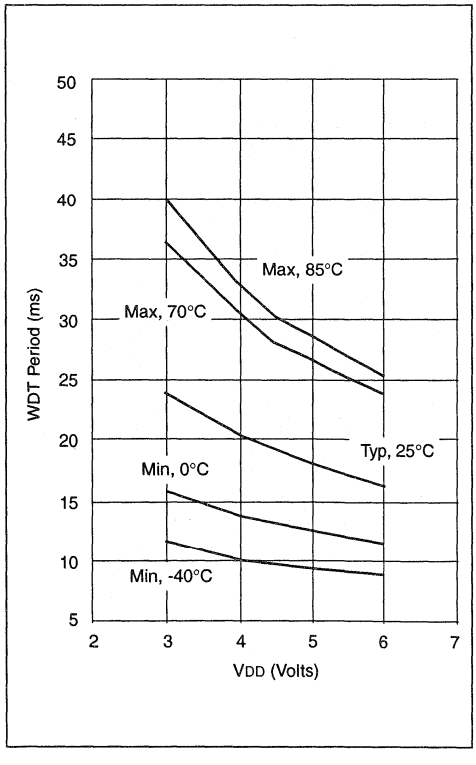
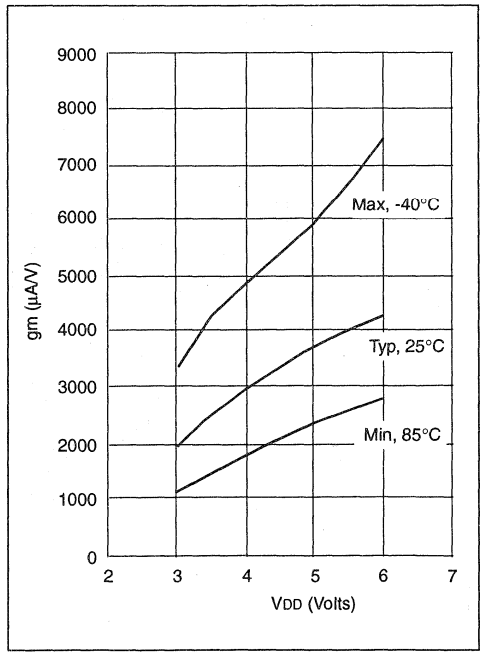


FIGURE 18-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR VS. VDD



Data based on matrix samples. See first page of this section for details.

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FIGURE 18-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

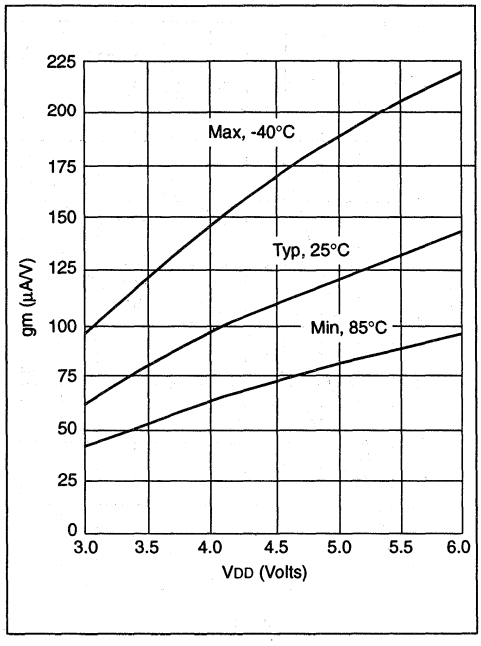


FIGURE 18-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

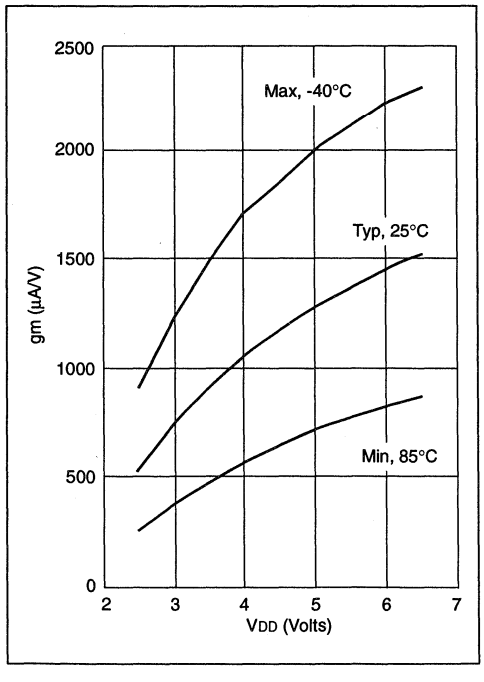


FIGURE 18-19: IOH vs. VOH, VDD = 3V

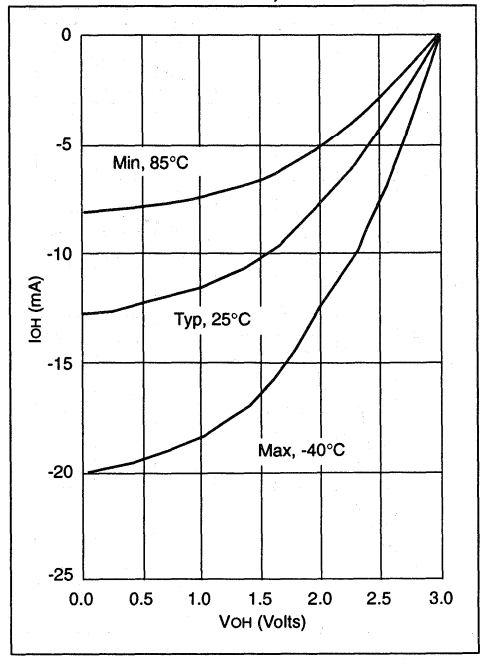
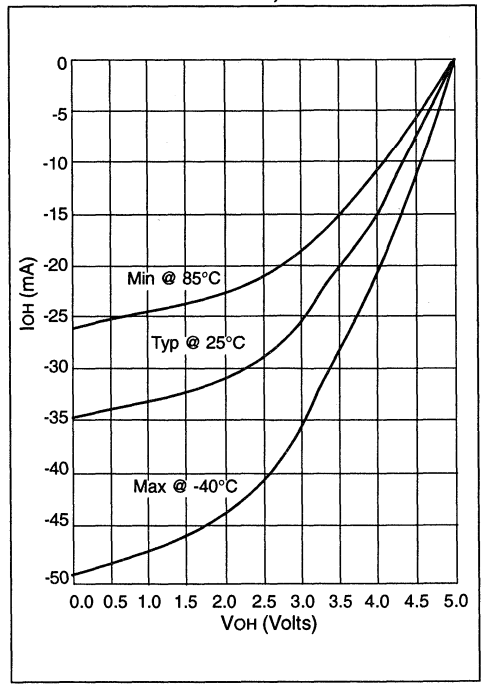


FIGURE 18-20: IOH vs. VOH, VDD = 5V



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 18-21: IOL VS. VOL, VDD = 3V

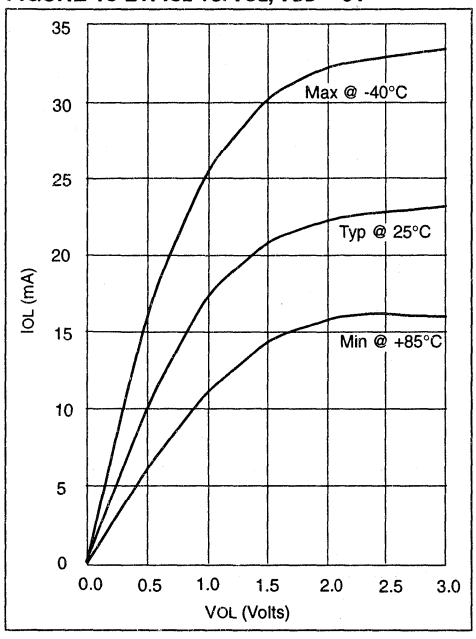
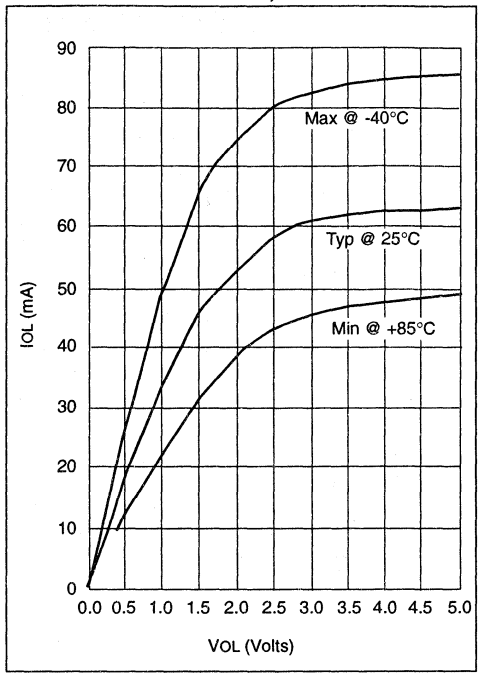


FIGURE 18-22: IOL VS. VOL, VDD = 5V



Data based on matrix samples. See first page of this section for details.

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19.0 ELECTRICAL CHARACTERISTICS FOR PIC16C72

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.3V to (V_{DD} + 0.3V)

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2) ..... 0 to +14V

Total power dissipation (Note 1) 1.0W

Maximum current out of V_{SS} pin ..... 300 mA

Maximum current into V_{DD} pin ..... 250 mA

Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) ..... ±20 mA

Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by PORTA and PORTB (combined) ..... 200 mA

Maximum current sourced by PORTA and PORTB (combined) ..... 200 mA

Maximum current sunk by PORTC ..... 200 mA

Maximum current sourced by PORTC ..... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C72-04	PIC16C72-10	PIC16C72-20	PIC16LC72-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices | 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

19.1 DC Characteristics: PIC16C72-04 (Commercial, Industrial, Automotive) PIC16C72-10 (Commercial, Industrial, Automotive) PIC16C72-20 (Commercial, Industrial, Automotive)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset Signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset Signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
D010	Supply Current (Note 2,5)	IDD	-	2.7	5	mA	XT, RC osc configuration (PIC16C72-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	10	20	mA	HS osc configuration (PIC16C72-20) FOSC = 20 MHz, VDD = 5.5V
D015	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled VDD = 5.0V
D020	Power-down Current (Note 3,5)	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.5	16	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.5	19	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			-	2.5	19	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C
D023	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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Applicable Devices	710	71	711	72	73	73A	74	74A

19.2 DC Characteristics: PIC16LC72-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
D010	Supply Current (Note 2,5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled VDD = 3.0V
D020	Power-down Current (Note 3,5)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	300	500	µA	BOR enabled VDD = 3.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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19.3 DC Characteristics: PIC16C72-04 (Commercial, Industrial, Automotive)
PIC16C72-10 (Commercial, Industrial, Automotive)
PIC16C72-20 (Commercial, Industrial, Automotive)
PIC16LC72-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2.				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI,OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR, RA4/T0CKI, RC7:RC4, RB0/INT		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	†400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2.

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD - 0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD - 0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	
D102	SCL, SDA in I^2C mode	CB	-	-	400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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19.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

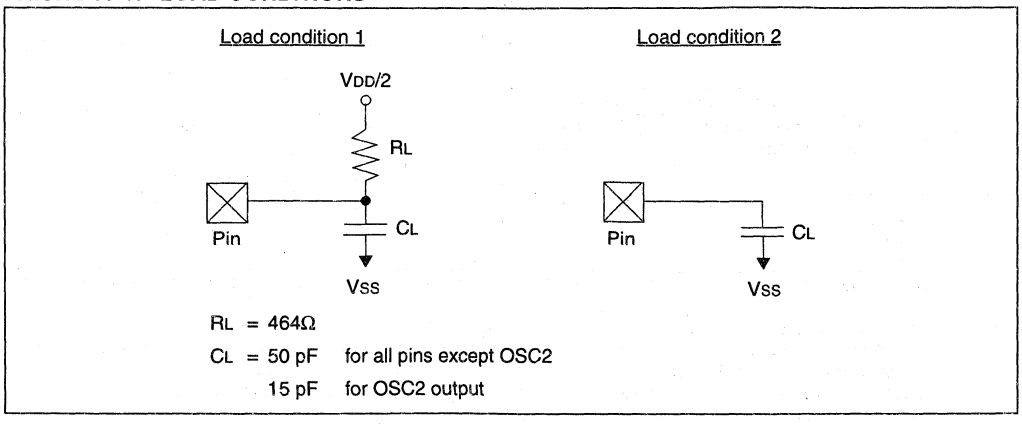
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 19-1: LOAD CONDITIONS



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Applicable Devices 710 71 711 72 73 73A 74 74A

19.5 Timing Diagrams and Specifications

FIGURE 19-2: EXTERNAL CLOCK TIMING

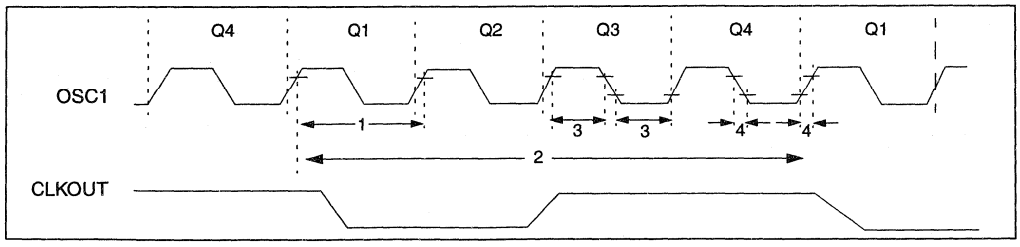

TABLE 19-2: CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C72-04)
			DC	—	20	MHz	HS osc mode (PIC16C72-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C72-04)
			4	—	10	MHz	HS osc mode (PIC16C72-10)
			4	—	20	MHz	HS osc mode (PIC16C72-20)
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C72-04)
			100	—	—	ns	HS osc mode (PIC16C72-10)
			50	—	—	ns	HS osc mode (PIC16C72-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C72-04)
			100	—	250	ns	HS osc mode (PIC16C72-10)
			50	—	250	ns	HS osc mode (PIC16C72-20)
			5	—	—	µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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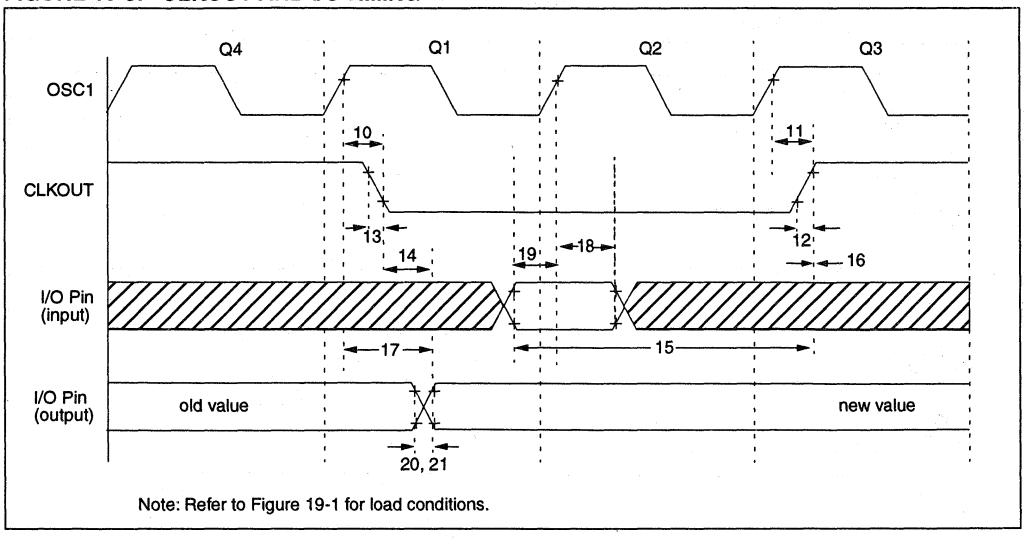
FIGURE 19-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 19-1 for load conditions.

TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		TOSC + 200	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C72	100	—	—	ns	
			PIC16LC72	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C72	—	10	40	ns	
			PIC16LC72	—	—	80	ns	
21*	TioF	Port output fall time	PIC16C72	—	10	40	ns	
			PIC16LC72	—	—	80	ns	
22††*	Tinp	INT pin high or low time		TCY	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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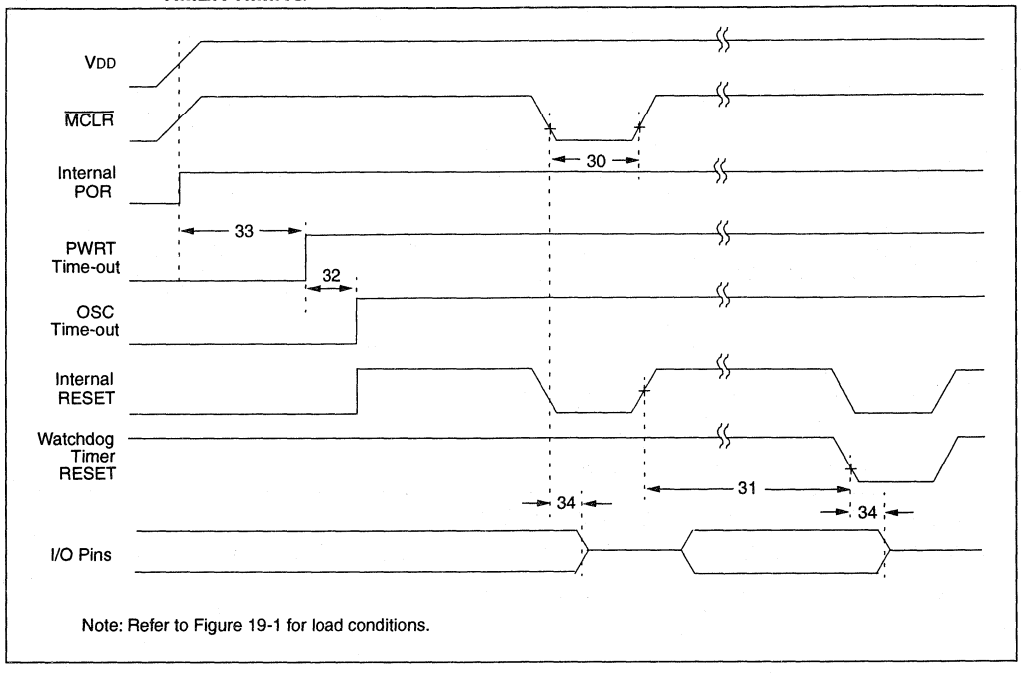
FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 19-1 for load conditions.

FIGURE 19-5: BROWN-OUT RESET TIMING

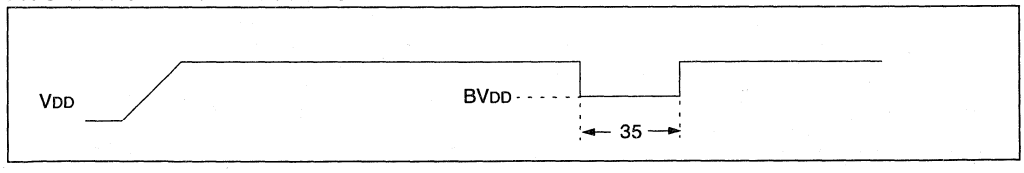


TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset pulse width	100	—	—	µs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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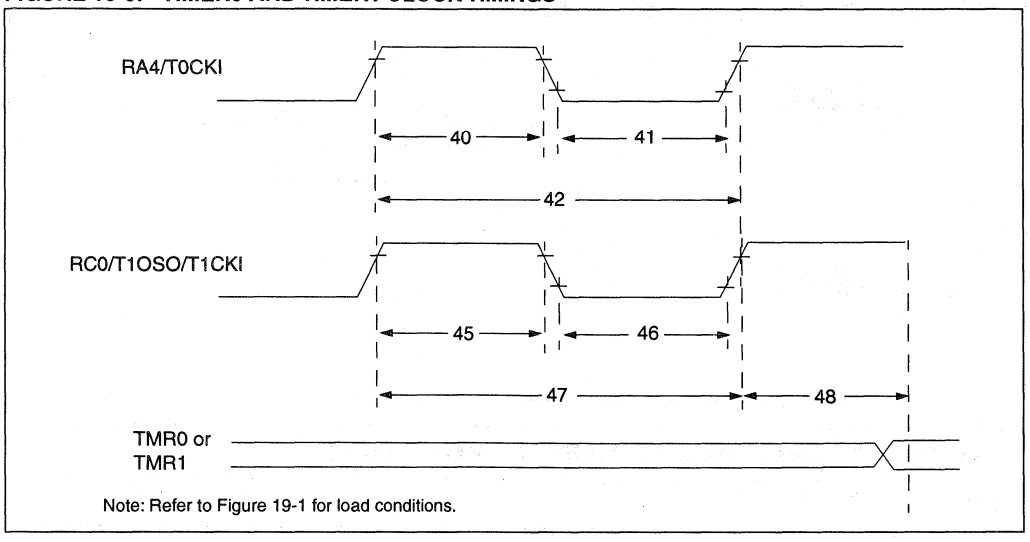
FIGURE 19-6: TIMER0 AND TIMER1 CLOCK TIMINGS



Note: Refer to Figure 19-1 for load conditions.

TABLE 19-5: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler		10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler		10	—	—	ns	
42*	Tt0P	T0CKI Period			TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C72	15	—	—	ns	
				PIC16LC72	25	—	—		
			Asynchronous		2TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C72	15	—	—	ns	
				PIC16LC72	25	—	—		
			Asynchronous		2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous		TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)			DC	—	200	kHz	
48	Tcke2tmrl	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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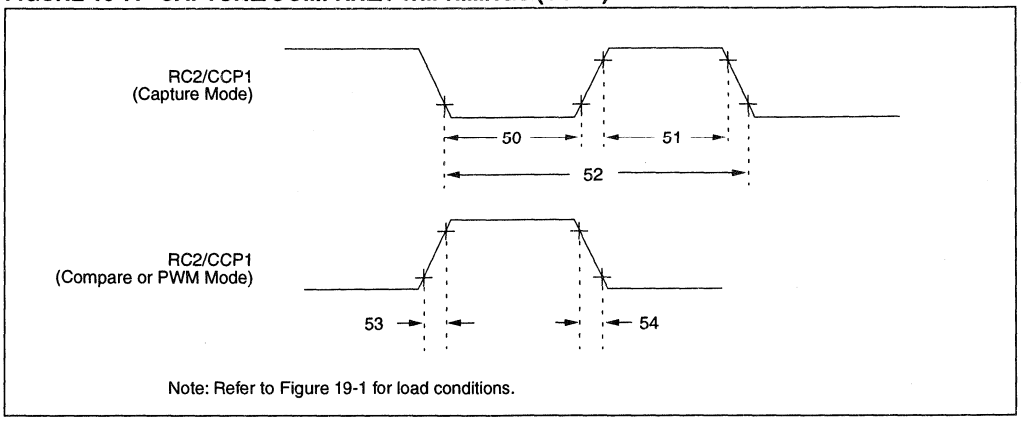
FIGURE 19-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1)



Note: Refer to Figure 19-1 for load conditions.

TABLE 19-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C72	10	—	—	ns	
				PIC16LC72	20	—	—	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C72	10	—	—	ns	
				PIC16LC72	20	—	—	ns	
52*	TccP	CCP1 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 output rise time		PIC16C72	—	10	25	ns	
				PIC16LC72	—	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16C72	—	10	25	ns	
				PIC16LC72	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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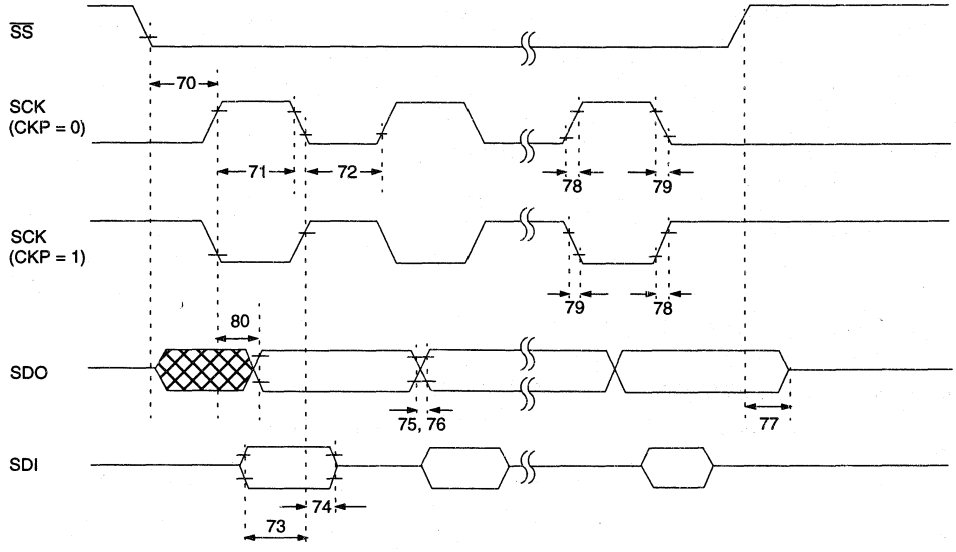
FIGURE 19-8: SPI MODE TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-7: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK↓ or SCK↑ input	TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75	TdoR	SDO data output rise time	—	10	25	ns	
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	$\overline{SS}\downarrow$ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	—	10	25	ns	
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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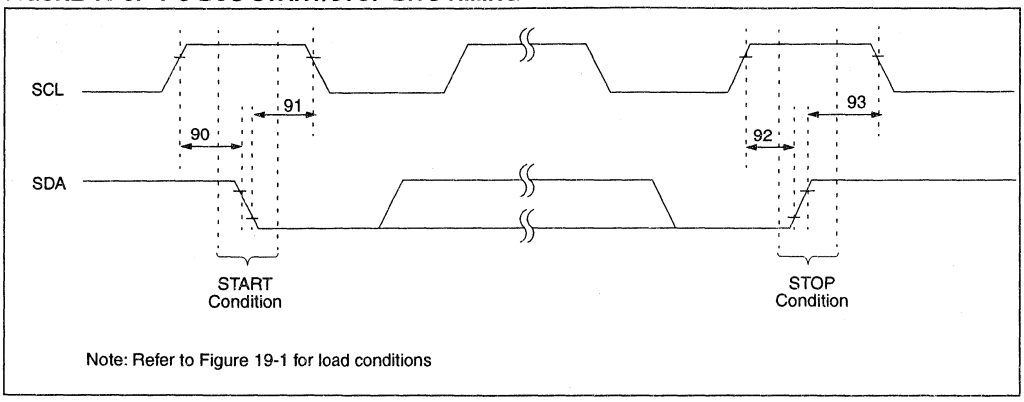
FIGURE 19-9: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-8: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

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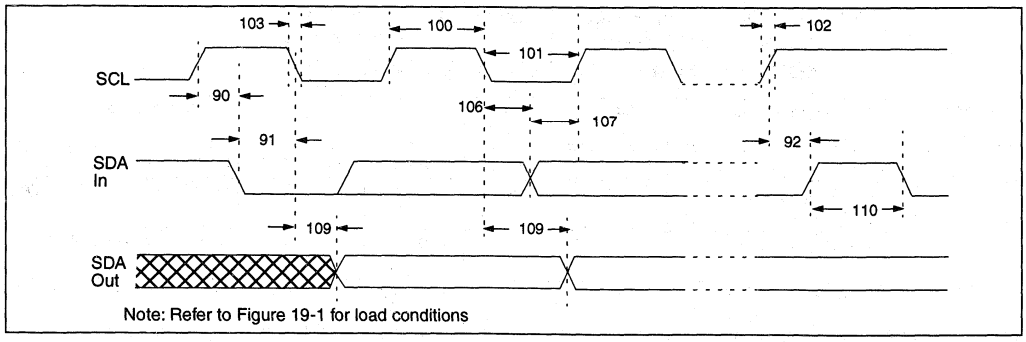
FIGURE 19-10: I^2C BUS DATA TIMING



Note: Refer to Figure 19-1 for load conditions

TABLE 19-9: I^2C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C72 must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16C72 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C72 must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16C72 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

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TABLE 19-10: A/D CONVERTER CHARACTERISTICS: PIC16C72-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C72-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C72-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 10	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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TABLE 19-11: A/D CONVERTER CHARACTERISTICS: PIC16LC72-04 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 3.0V (Note 1)
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	μA	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 3)	—	—	1 10	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V. Vin must be between VSS and VREF

2: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

4: Automotive operating range is Advance Information for this device.

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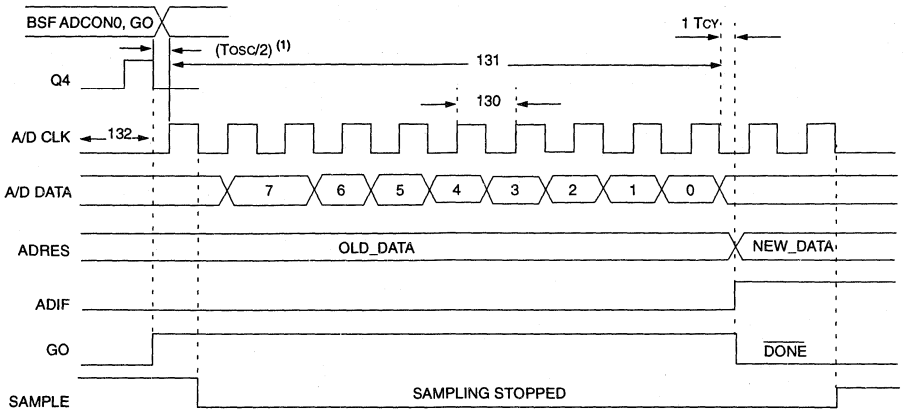
FIGURE 19-11: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 19-12: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16C72	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16LC72	2.0	—	—	µs	TOSC based, VREF full range
			PIC16C72	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16LC72	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	9.5TAD	—	—	
132	TACQ	Acquisition time		Note 2	20	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

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20.0 ELECTRICAL CHARACTERISTICS FOR PIC16C73/74

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V

Total power dissipation (Note 1) 1.0W

Maximum current out of VSS pin ..... 300 mA

Maximum current into VDD pin ..... 250 mA

Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3) ..... 200 mA

Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3) ..... 200 mA

Maximum current sunk by PORTC and PORTD (combined) (Note 3) ..... 200 mA

Maximum current sourced by PORTC and PORTD (combined) (Note 3) ..... 200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD - VOH) x IOH} + Σ(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

Note 3: PORTD and PORTE are not implemented on the PIC16C73.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 20-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C73-04 PIC16C74-04	PIC16C73-10 PIC16C74-10	PIC16C73-20 PIC16C74-20	PIC16LC73-04 PIC16LC74-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 13.5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 13.5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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20.1 DC Characteristics: PIC16C73-04 (Commercial, Industrial) PIC16C74-04 (Commercial, Industrial) PIC16C73-10 (Commercial, Industrial) PIC16C74-10 (Commercial, Industrial) PIC16C73-20 (Commercial, Industrial) PIC16C74-20 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2,5)	IDD	-	2.7	5	mA	XT, RC osc configuration (PIC16C74-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration (PIC16C74-20) FOSC = 20 MHz, VDD = 5.5V
D020	Power-down Current (Note 3,5)	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.5	21	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.5	24	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

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20.2 DC Characteristics: PIC16LC73-04 (Commercial, Industrial) PIC16LC74-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	3.0	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2,5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-down Current (Note 3,5)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	13.5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	18	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

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20.3 DC Characteristics: PIC16C73-04 (Commercial, Industrial)
PIC16C74-04 (Commercial, Industrial)
PIC16C73-10 (Commercial, Industrial)
PIC16C74-10 (Commercial, Industrial)
PIC16C73-20 (Commercial, Industrial)
PIC16C74-20 (Commercial, Industrial)
PIC16LC73-04 (Commercial, Industrial)
PIC16LC74-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 20.1 and Section 20.2.				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, RA4/T0CKI,OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR, RA4/T0CKI, RC7:RC4, RD7:RD4, RB0/INT, RE2:RE0		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 20.1 and Section 20.2.

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC	CIO	-	-	50	pF	
D102	mode) SCL, SDA in I²C mode	CB	-	-	400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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20.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

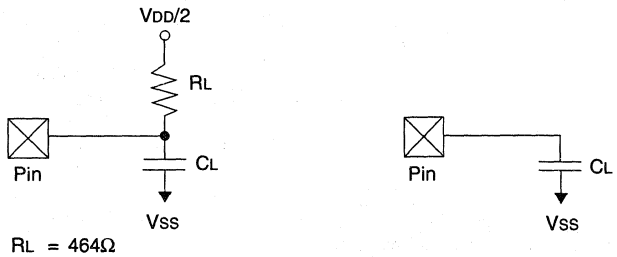
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 20-1: LOAD CONDITIONS



RL = 464Ω

CL = 50 pF for all pins except OSC2, but including PORTD and PORTE outputs as ports

15 pF for OSC2 output

Note: PORTD and PORTE are not implemented on the PIC16C73.

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20.5 Timing Diagrams and Specifications

FIGURE 20-2: EXTERNAL CLOCK TIMING

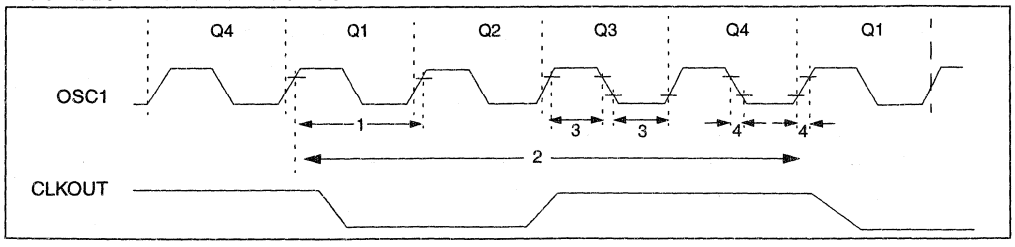

TABLE 20-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C73-04, PIC16C74-04)
			DC	—	20	MHz	HS osc mode (PIC16C73-20, PIC16C74-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C73-04, PIC16C74-04)
			4	—	10	MHz	HS osc mode (PIC16C73-10, PIC16C74-10)
			4	—	20	MHz	HS osc mode (PIC16C73-20, PIC16C74-20)
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C73-04, PIC16C74-04)
			100	—	—	ns	HS osc mode (PIC16C73-10, PIC16C74-10)
			50	—	—	ns	HS osc mode (PIC16C73-20, PIC16C74-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C73-04, PIC16C74-04)
			100	—	250	ns	HS osc mode (PIC16C73-10, PIC16C74-10)
			50	—	250	ns	HS osc mode (PIC16C73-20, PIC16C74-20)
			5	—	—	µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	Tcy = 4/Fosc

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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TABLE 20-2: EXTERNAL CLOCK TIMING REQUIREMENTS (Cont'd)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	50	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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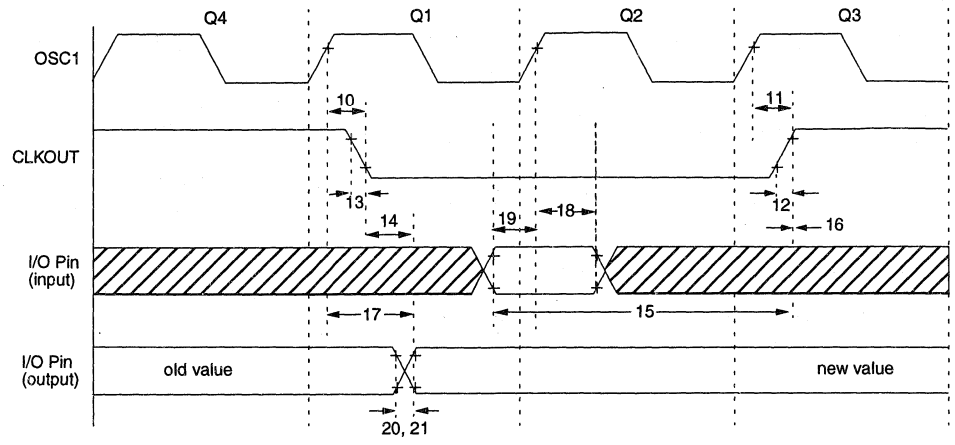
FIGURE 20-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 20-1 for load conditions.

TABLE 20-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C73/74	100	—	—	ns	
			PIC16LC73/74	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C73/74	—	10	25	ns	
			PIC16LC73/74	—	—	60	ns	
21*	TioF	Port output fall time	PIC16C73/74	—	10	25	ns	
			PIC16LC73/74	—	—	60	ns	
22††*	Tinp	INT pin high or low time		TCY	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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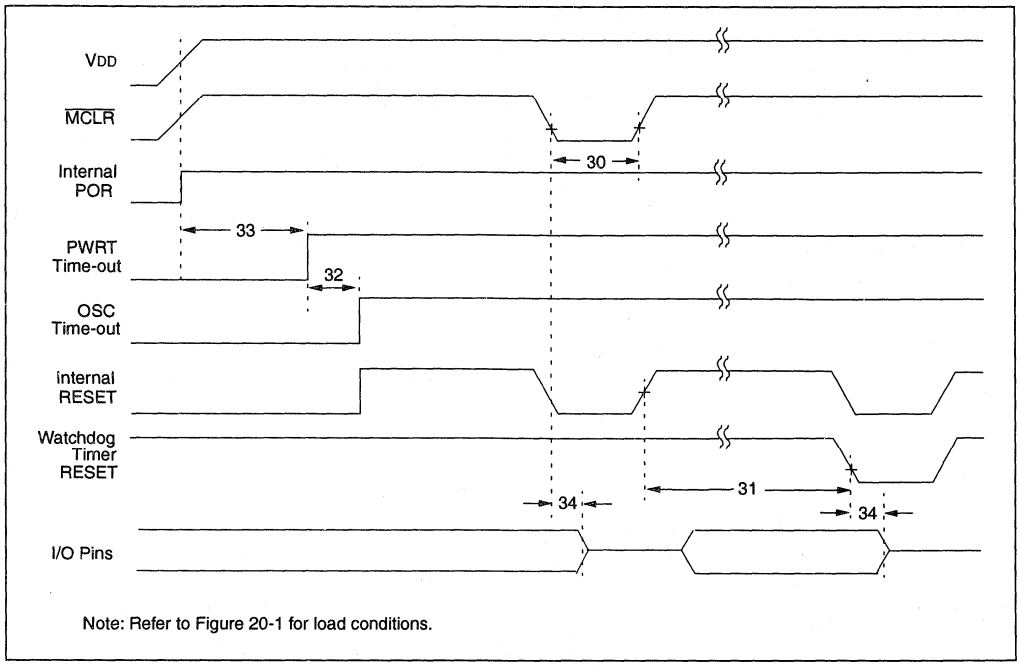
FIGURE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 20-1 for load conditions.

TABLE 20-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100	—	—	ns	VDD = 5V, -40°C to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +85°C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	100	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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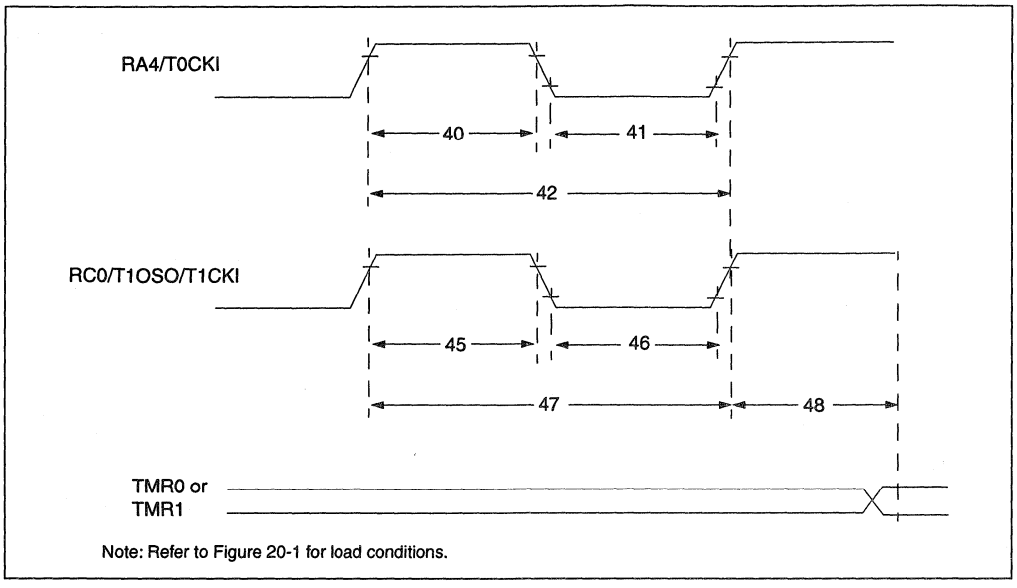
FIGURE 20-5: TIMER0 AND TIMER1 CLOCK TIMINGS



Note: Refer to Figure 20-1 for load conditions.

TABLE 20-5: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10*	—	—	ns	
42*	Tt0P	T0CKI Period			Greater of: 20µs or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4,..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C73/74	15	—	—	ns	
				PIC16LC73/74	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C73/74	15	—	—	ns	
				PIC16LC73/74	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous		Greater of: 20µs or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		Greater of: 20µs or 4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)			DC	—	200	kHz	
48	Tcke2tmrl	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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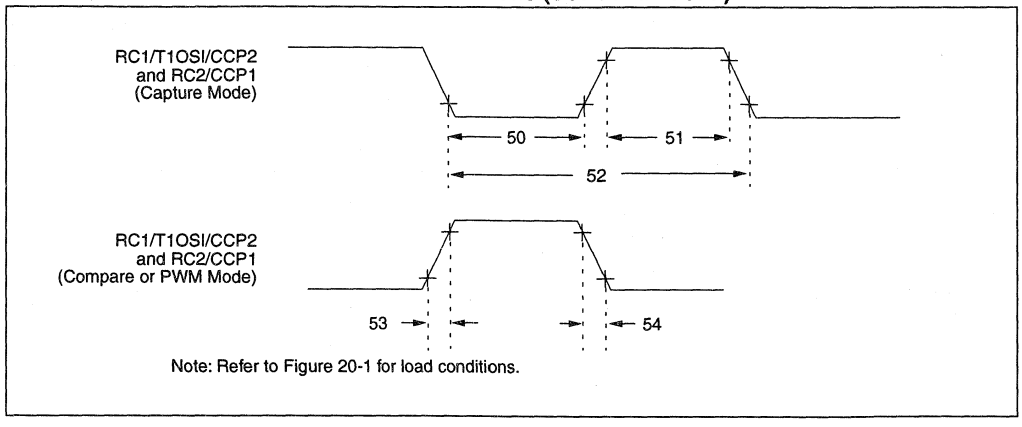
FIGURE 20-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 20-1 for load conditions.

TABLE 20-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C73/74	10	—	—	ns	
				PIC16LC73/74	20	—	—	ns	
51*	TccH	CCP1 and CCP2 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C73/74	10	—	—	ns	
				PIC16LC73/74	20	—	—	ns	
52*	TccP	CCP1 and CCP2 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 and CCP2 output fall time		PIC16C73/74	—	10	25	ns	
				PIC16LC73/74	—	25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time		PIC16C73/74	—	10	25	ns	
				PIC16LC73/74	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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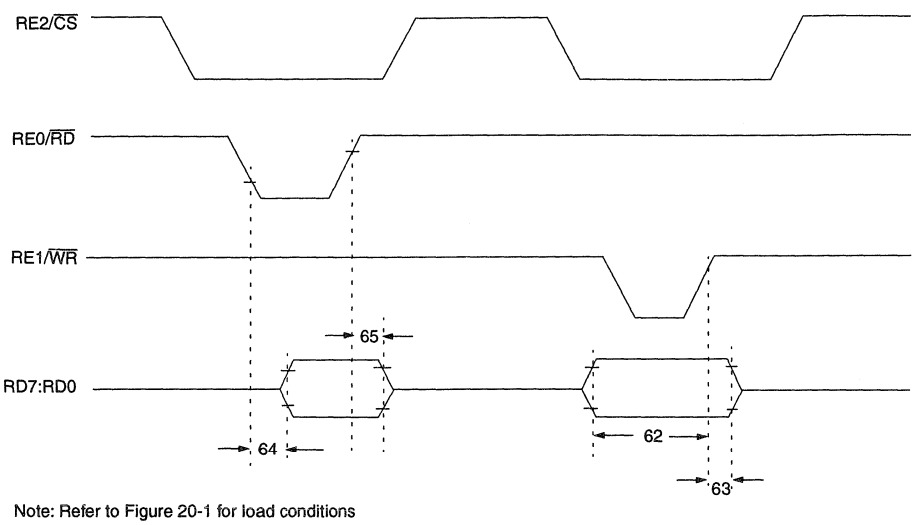
FIGURE 20-7: PARALLEL SLAVE PORT TIMING (PIC16C74)



Note: Refer to Figure 20-1 for load conditions

TABLE 20-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C74)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20	—	—	ns	
63*	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	PIC16C74	20	—	—	ns	
			PIC16LC74	35	—	—	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		—	—	80	ns	
65	TrdH2dtI	RD↑ or CS↓ to data–out invalid		10	—	30	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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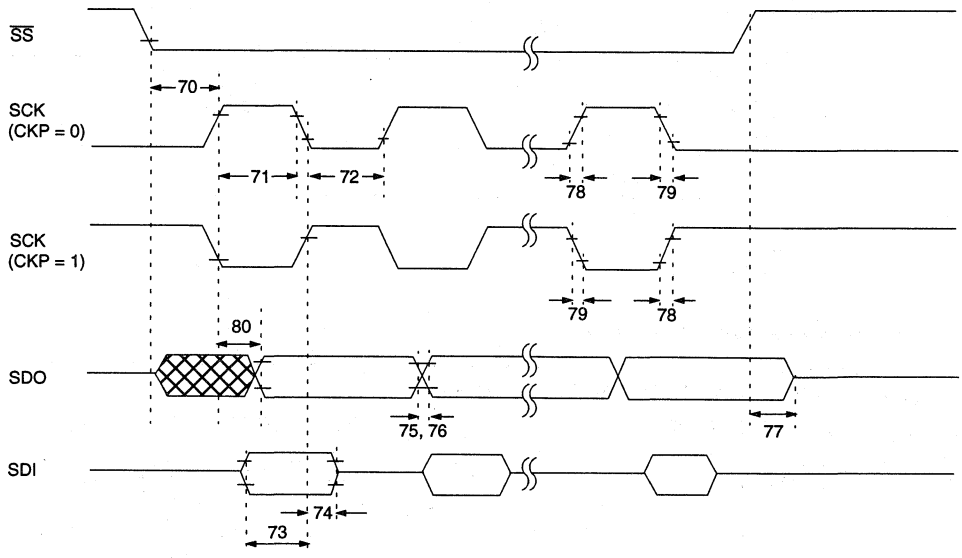
FIGURE 20-8: SPI MODE TIMING



Note: Refer to Figure 20-1 for load conditions

TABLE 20-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75	TdoR	SDO data output rise time	—	10	25	ns	
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	SS↓ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	—	10	25	ns	
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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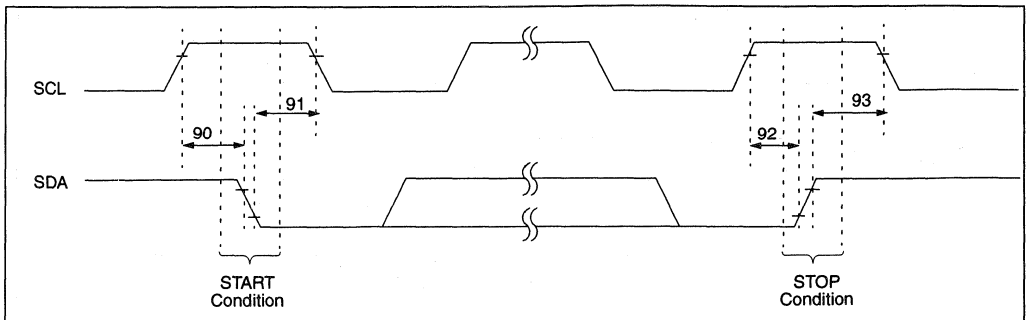
Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 20-9: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 20-1 for load conditions

TABLE 20-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

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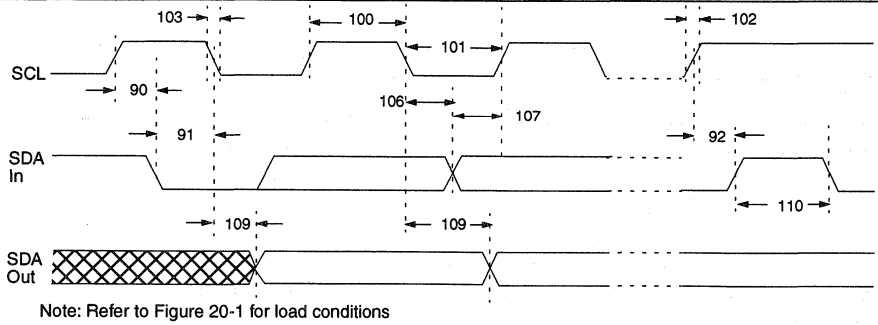
FIGURE 20-10: I^2C BUS DATA TIMING



Note: Refer to Figure 20-1 for load conditions

TABLE 20-10: I^2C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C73/74 must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16C73/74 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C73/74 must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16C73/74 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

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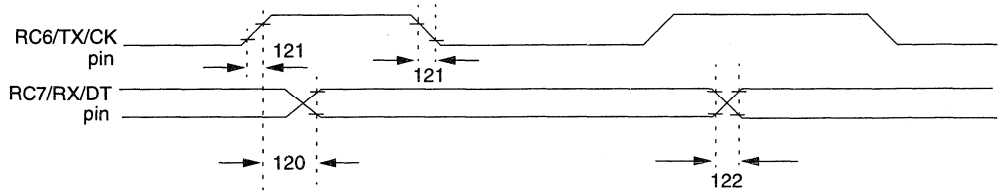
FIGURE 20-11: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



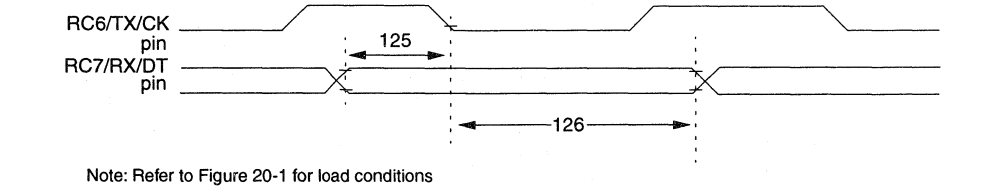
Note: Refer to Figure 20-1 for load conditions

TABLE 20-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16C73/74	—	—	80	ns	
			PIC16LC73/74	—	—	100	ns	
121	Tckrf	Clock out rise time and fall time (Master Mode)	PIC16C73/74	—	—	45	ns	
			PIC16LC73/74	—	—	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC16C73/74	—	—	45	ns	
			PIC16LC73/74	—	—	50	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-12: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 20-1 for load conditions

TABLE 20-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckl	SYNC RCV (MASTER & SLAVE) Data hold before CK ↓ (DT hold time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 20-13: A/D CONVERTER CHARACTERISTICS:
PIC16C73-04 (COMMERCIAL, INDUSTRIAL)
PIC16C74-04 (COMMERCIAL, INDUSTRIAL)
PIC16C73-10 (COMMERCIAL, INDUSTRIAL)
PIC16C74-10 (COMMERCIAL, INDUSTRIAL)
PIC16C73-20 (COMMERCIAL, INDUSTRIAL)
PIC16C74-20 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 10	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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TABLE 20-14: A/D CONVERTER CHARACTERISTICS: PIC16LC73-04 (COMMERCIAL, INDUSTRIAL) PIC16LC74-04 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 3.0V (Note 1)
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	90	—	μA	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 3)	—	—	1 10	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V. VIN must be between VSS and VREF

2: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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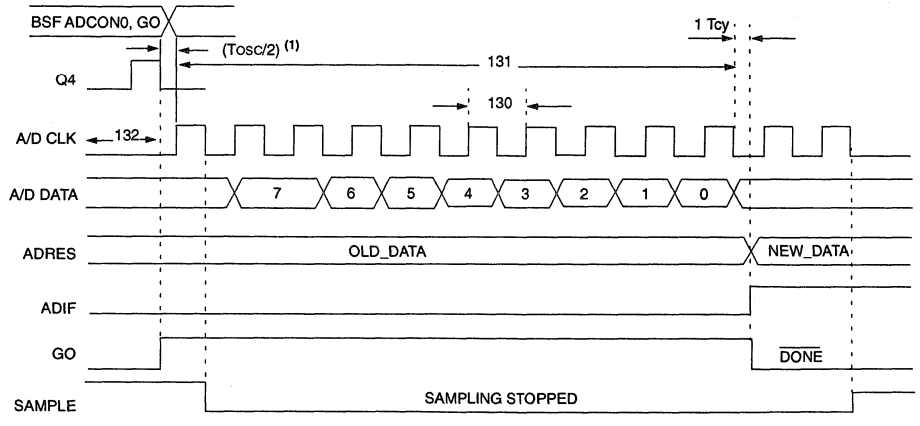
FIGURE 20-13: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 20-15: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16C73/74	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16LC73/74	2.0	—	—	µs	TOSC based, VREF full range
			PIC16C73/74	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16LC73/74	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	9.5TAD	—	—	
132	TACQ	Acquisition time		Note 2	20	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

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NOTES:

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21.0 ELECTRICAL CHARACTERISTICS FOR PIC16C73A/74A

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) ..... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V

Total power dissipation (Note 1) 1.0W

Maximum current out of VSS pin ..... 300 mA

Maximum current into VDD pin ..... 250 mA

Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3) ..... 200 mA

Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3) ..... 200 mA

Maximum current sunk by PORTC and PORTD (combined) (Note 3) ..... 200 mA

Maximum current sourced by PORTC and PORTD (combined) (Note 3) ..... 200 mA

Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

Note 3: PORTD and PORTE are not implemented on the PIC16C73A.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 21-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C73A-04 PIC16C74A-04	PIC16C73A-10 PIC16C74A-10	PIC16C73A-20 PIC16C74A-20	PIC16LC73A-04 PIC16LC74A-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices	710	71	711	72	73	73A	74	74A

21.1 DC Characteristics: PIC16C73A-04 (Commercial, Industrial, Automotive) PIC16C74A-04 (Commercial, Industrial, Automotive) PIC16C73A-10 (Commercial, Industrial, Automotive) PIC16C74A-10 (Commercial, Industrial, Automotive) PIC16C73A-20 (Commercial, Industrial, Automotive) PIC16C74A-20 (Commercial, Industrial, Automotive)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
			3.7	4.0	4.4	V	Automotive Range Only
D010	Supply Current (Note 2,5)	IDD	-	2.7	5	mA	XT, RC osc configuration (PIC16C73A-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	10	20	mA	HS osc configuration (PIC16C73A-20) FOSC = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled VDD = 5.0V
D020	Power-down Current (Note 3,5)	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.5	16	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.5	19	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			-	2.5	19	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

10

Applicable Devices	710	71	711	72	73	73A	74	74A

21.2 DC Characteristics: PIC16LC73A-04 (Commercial, Industrial) PIC16LC74A-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
D010	Supply Current (Note 2,5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled VDD = 3.0V
D020	Power-down Current (Note 3,5)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	µA	BOR enabled VDD = 3.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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Applicable Devices 710 | 71 | 711 | 72 | 73 | 73A | 74 | 74A

21.3 DC Characteristics: PIC16C73A-04 (Commercial, Industrial, Automotive)
PIC16C74A-04 (Commercial, Industrial, Automotive)
PIC16C73A-10 (Commercial, Industrial, Automotive)
PIC16C74A-10 (Commercial, Industrial, Automotive)
PIC16C73A-20 (Commercial, Industrial, Automotive)
PIC16C74A-20 (Commercial, Industrial, Automotive)
PIC16LC73A-04 (Commercial, Industrial)
PIC16LC74A-04 (Commercial, Industrial)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 21.1 and Section 21.2.

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	$\overline{MCLR}$, RA4/T0CKI, RC7:RC4, RD7:RD4, RB0/INT		0.8VDD	-	VDD	V	
D042A	RE2:RE0, OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	VSS ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

10

Applicable Devices	710	71	711	72	73	73A	74	74A

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Section 21.1 and Section 21.2.

Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD - 0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD - 0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
	Capacitive Loading Specs on Output Pins						
D100	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC	CIO	-	-	50	pF	
D102	mode) SCL, SDA in I²C mode	CB	-	-	400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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21.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I²C specifications only)
4. Ts (I²C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

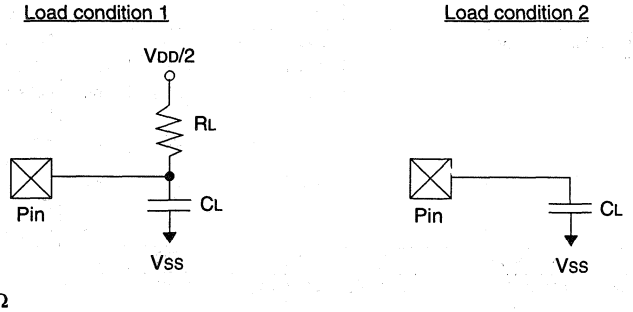
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I²C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I²C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 21-1: LOAD CONDITIONS



RL = 464Ω

CL = 50 pF for all pins except OSC2, but including PORTD and PORTE outputs as ports

15 pF for OSC2 output

Note: PORTD and PORTE are not implemented on the PIC16C73A.

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Applicable Devices	710	71	711	72	73	73A	74	74A

21.5 Timing Diagrams and Specifications

FIGURE 21-2: EXTERNAL CLOCK TIMING

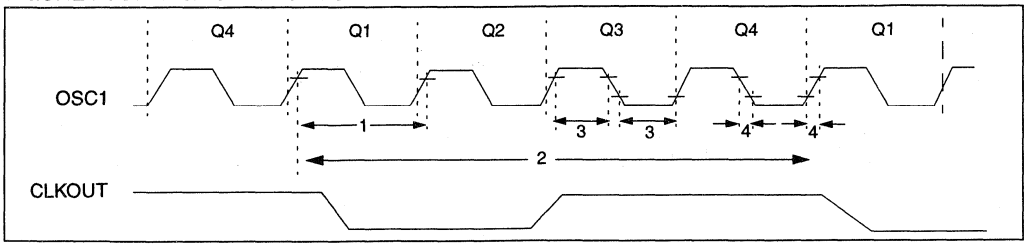

TABLE 21-2: CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (PIC16C73A-04, PIC16C74A-04)
			DC	—	20	MHz	HS osc mode (PIC16C73A-20, PIC16C74A-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C73A-04, PIC16C74A-04)
			4	—	10	MHz	HS osc mode (PIC16C73A-10, PIC16C74A-10)
			4	—	20	MHz	HS osc mode (PIC16C73A-20, PIC16C74A-20)
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period (Note 1)**	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (PIC16C73A-04, PIC16C74A-04)
			100	—	—	ns	HS osc mode (PIC16C73A-10, PIC16C74A-10)
			50	—	—	ns	HS osc mode (PIC16C73A-20, PIC16C74A-20)
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C73A-04, PIC16C74A-04)
			100	—	250	ns	HS osc mode (PIC16C73A-10, PIC16C74A-10)
			50	—	250	ns	HS osc mode (PIC16C73A-20, PIC16C74A-20)
			5	—	—	µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	200	—	DC	ns	Tcy = 4/Fosc

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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Applicable Devices	710	71	711	72	73	73A	74	74A

TABLE 21-2: CLOCK TIMING REQUIREMENTS (Cont.'d)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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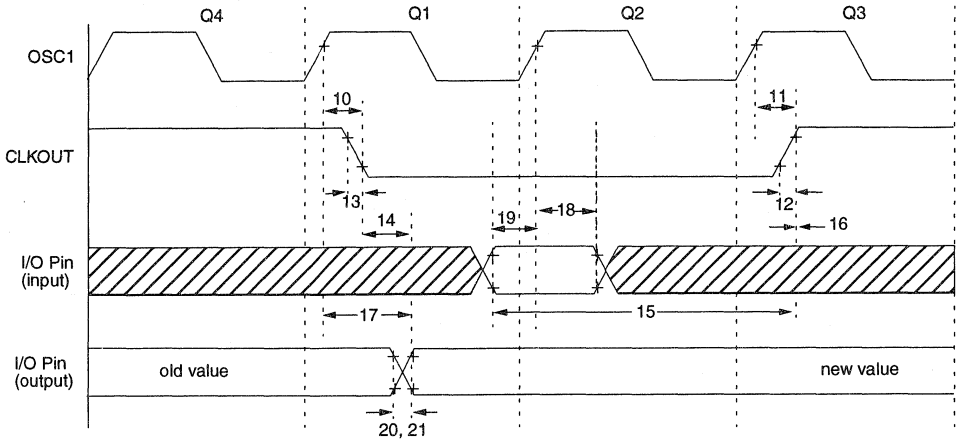
Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 21-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		TOSC + 200	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C73A/74A	100	—	—	ns	
			PIC16LC73A/74A	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C73A/74A	—	10	40	ns	
			PIC16LC73A/74A	—	—	80	ns	
21*	TioF	Port output fall time	PIC16C73A/74A	—	10	40	ns	
			PIC16LC73A/74A	—	—	80	ns	
22††*	Tinp	INT pin high or low time		TCY	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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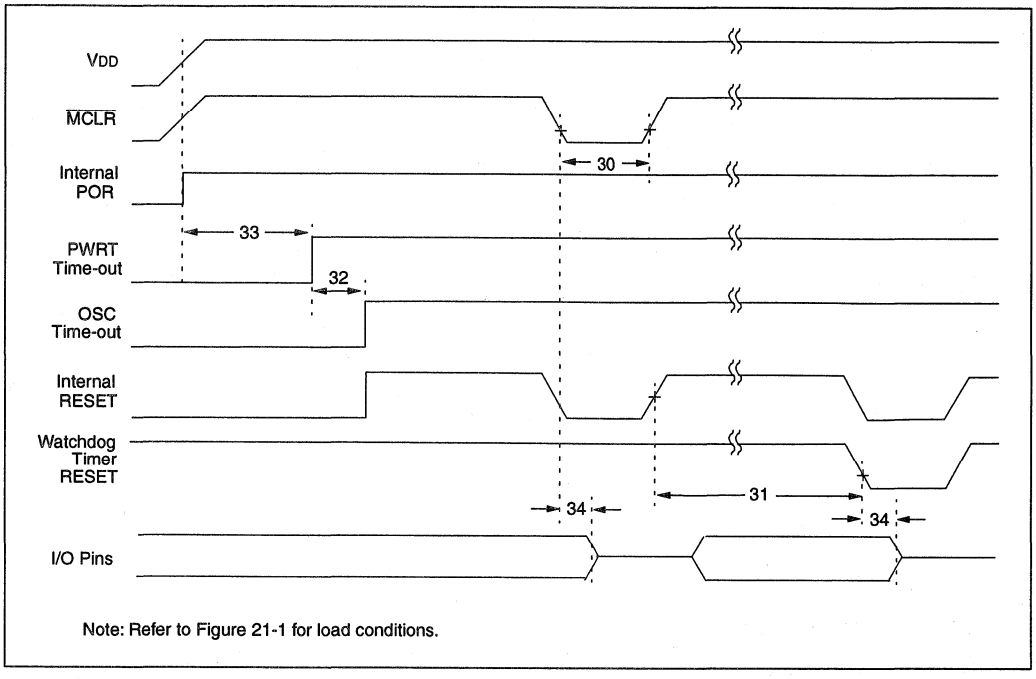
FIGURE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 21-1 for load conditions.

FIGURE 21-5: BROWN-OUT RESET TIMING

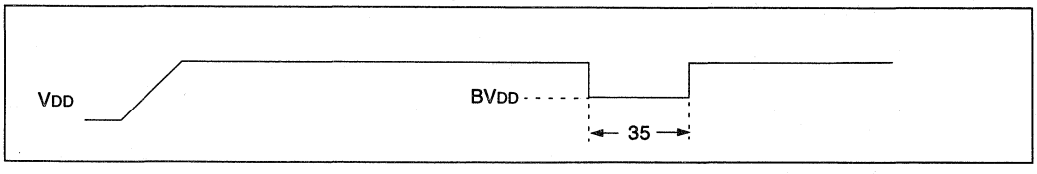


TABLE 21-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset pulse width	100	—	—	µs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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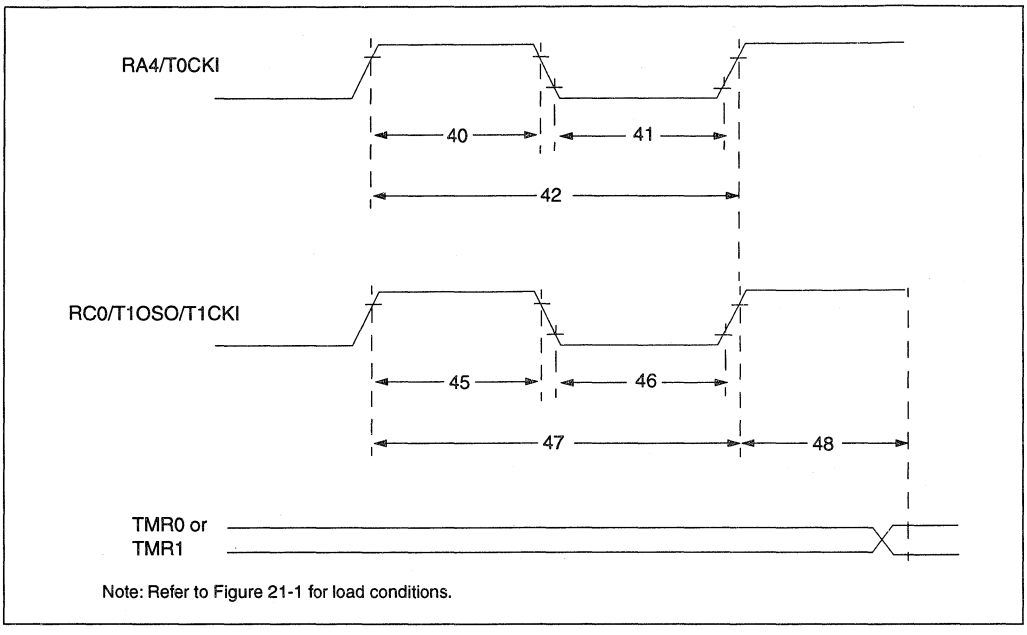
Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 21-6: TIMER0 AND TIMER1 CLOCK TIMINGS



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-5: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period			TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4,..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C73A/74A	15	—	—	ns	
				PIC16LC73A/74A	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C73A/74A	15	—	—	ns	
				PIC16LC73A/74A	25	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous		TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)			DC	—	200	kHz	
48	Tcke2tmrl	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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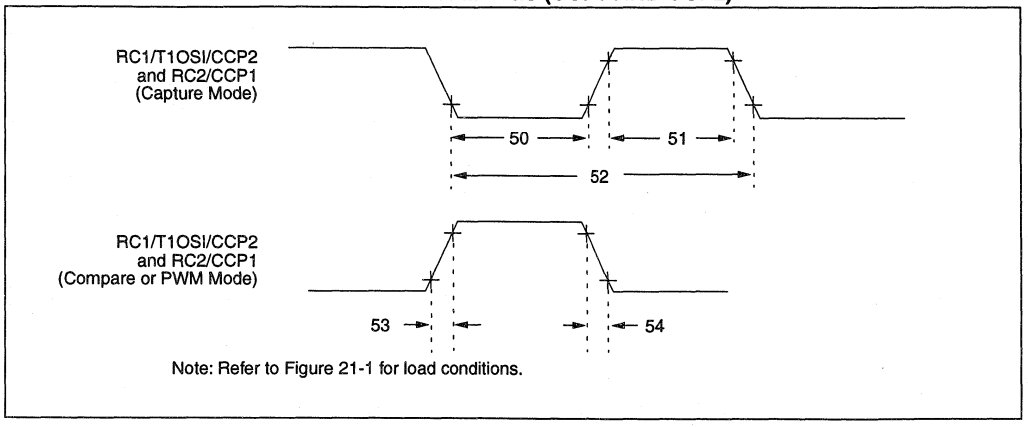
FIGURE 21-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 21-1 for load conditions.

TABLE 21-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2 input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C73A/74A	10	—	—	ns	
				PIC16LC73A/74A	20	—	—	ns	
51*	TccH	CCP1 and CCP2 input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C73A/74A	10	—	—	ns	
				PIC16LC73A/74A	20	—	—	ns	
52*	TccP	CCP1 and CCP2 input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 and CCP2 output rise time		PIC16C73A/74A		10	25	ns	
				PIC16LC73A/74A		25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time		PIC16C73A/74A		10	25	ns	
				PIC16LC73A/74A		25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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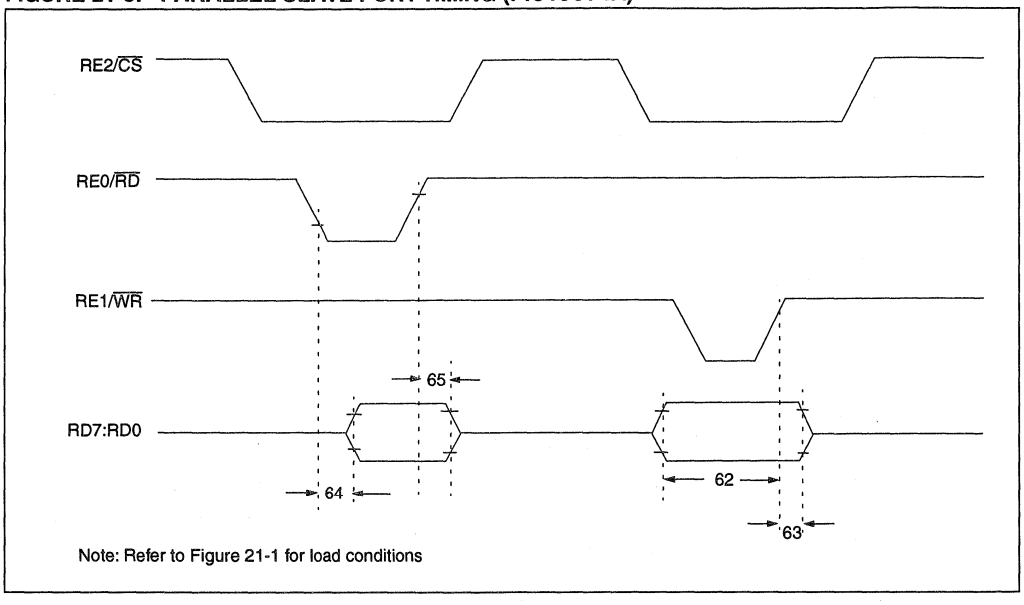
FIGURE 21-8: PARALLEL SLAVE PORT TIMING (PIC16C74A)



Note: Refer to Figure 21-1 for load conditions

TABLE 21-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C74A)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20	—	—	ns	
63*	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	PIC16C74A	20	—	—	ns	
			PIC16LC74A	35	—	—	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		—	—	80	ns	
65	TrdH2dtI	RD↑ or CS↓ to data–out invalid		10	—	30	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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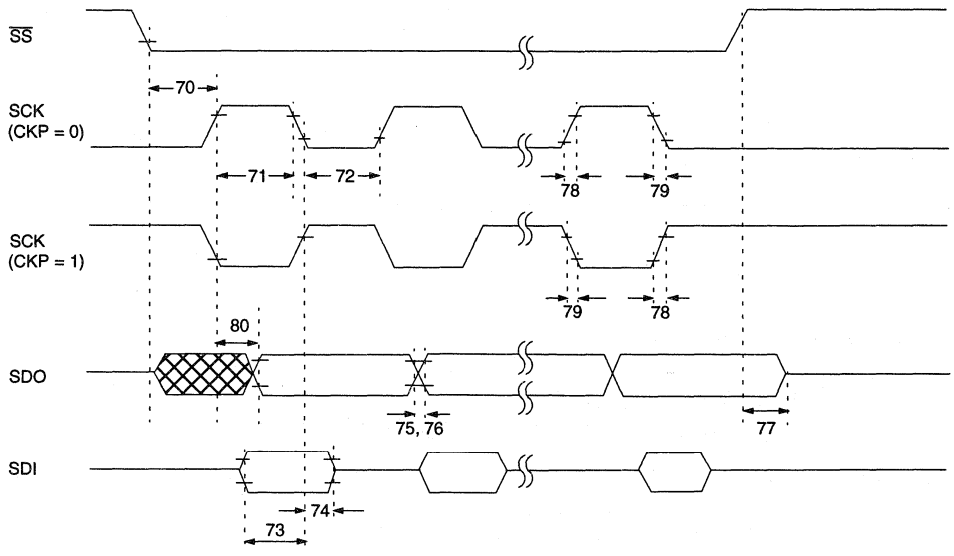
FIGURE 21-9: SPI MODE TIMING



Note: Refer to Figure 21-1 for load conditions

TABLE 21-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input	TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	ns	
75	TdoR	SDO data output rise time	—	10	25	ns	
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	$\overline{SS}$↓ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	—	10	25	ns	
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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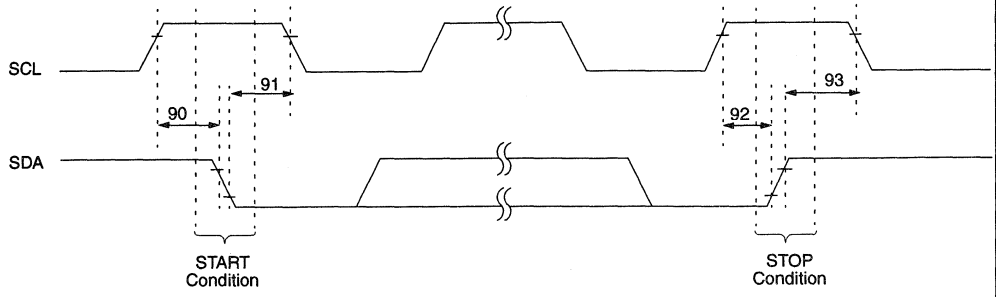
FIGURE 21-10: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 21-1 for load conditions

TABLE 21-9: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

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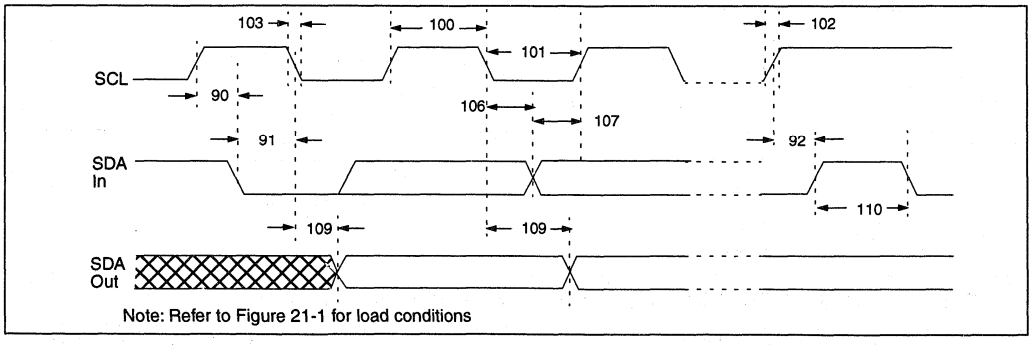
FIGURE 21-11: I²C BUS DATA TIMING



Note: Refer to Figure 21-1 for load conditions

TABLE 21-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C73A/74A must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16C73A/74A must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C73A/74A must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16C73A/74A must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

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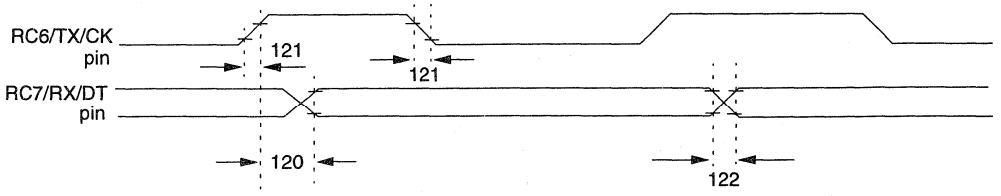
FIGURE 21-12: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



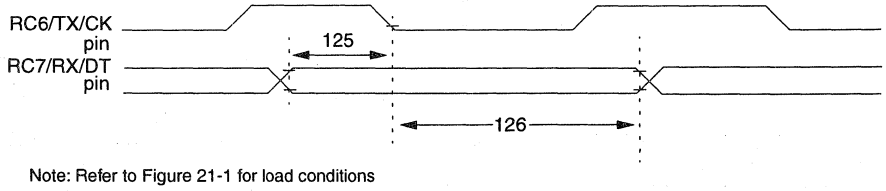
Note: Refer to Figure 21-1 for load conditions

TABLE 21-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16C73A/74A	—	—	80	ns	
			PIC16LC73A/74A	—	—	100	ns	
121	Tckrf	Clock out rise time and fall time (Master Mode)	PIC16C73A/74A	—	—	45	ns	
			PIC16LC73A/74A	—	—	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC16C73A/74A	—	—	45	ns	
			PIC16LC73A/74A	—	—	50	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-13: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 21-1 for load conditions

TABLE 21-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckl	SYNC RCV (MASTER & SLAVE) Data hold before CK ↓ (DT hold time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 21-13: A/D CONVERTER CHARACTERISTICS:
PIC16C73A-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)
PIC16C74A-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)
PIC16C73A-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)
PIC16C74A-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)
PIC16C73A-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)
PIC16C74A-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	µA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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TABLE 21-14: A/D CONVERTER CHARACTERISTICS: PIC16LC73A-04 (COMMERCIAL, INDUSTRIAL) PIC16LC74A-04 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 3.0V (Note 1)
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	μA	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 3)	—	—	1 10	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V. VIN must be between VSS and VREF

2: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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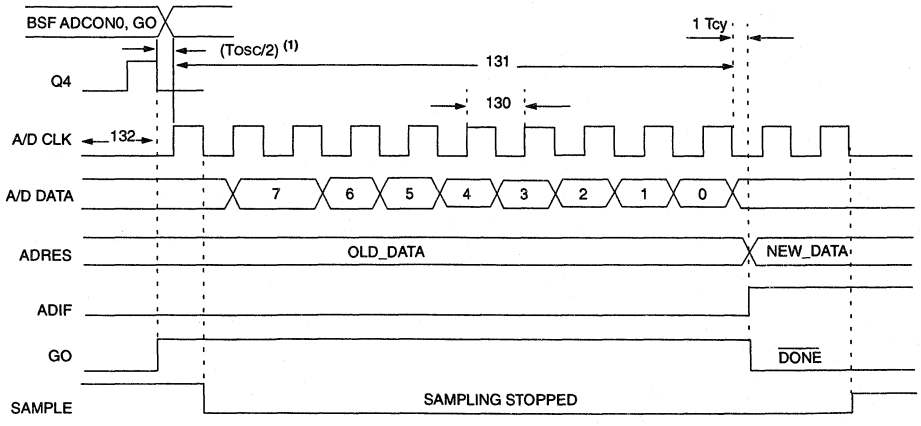
FIGURE 21-14: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 21-15: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16C73/74	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16LC73/74	2.0	—	—	µs	TOSC based, VREF full range
			PIC16C73/74	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16LC73/74	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	9.5TAD	—	—	
132	TACQ	Acquisition time		Note 2	20	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

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NOTES:

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22.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR: PIC16C72, PIC16C73, PIC16C73A, PIC16C74, PIC16C74A

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25°C, while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 22-1: TYPICAL IPD vs. VDD (WDT DISABLED, RC MODE)

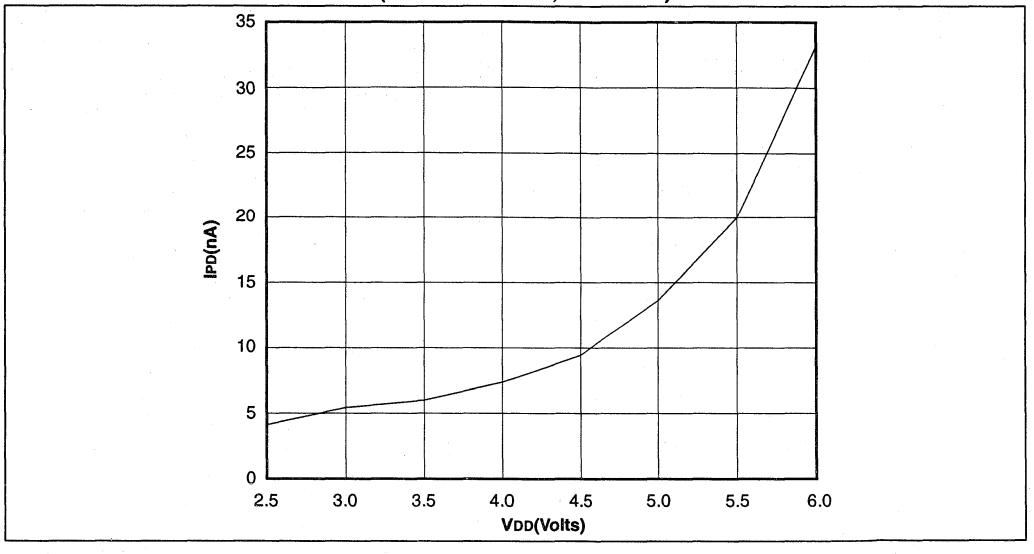
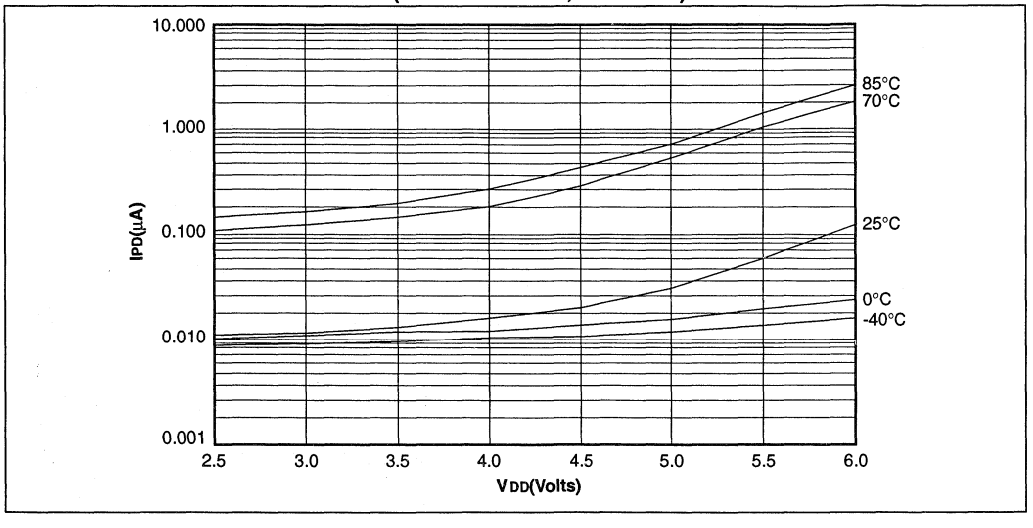


FIGURE 22-2: MAXIMUM IPD vs. VDD (WDT DISABLED, RC MODE)



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Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 22-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

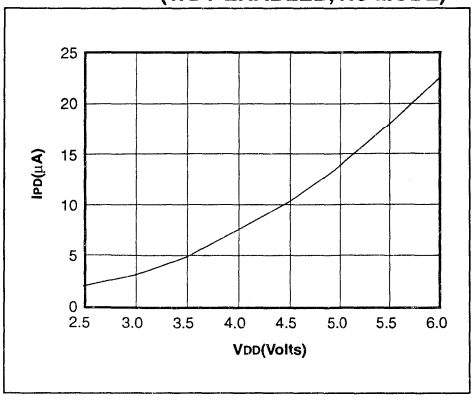


FIGURE 22-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

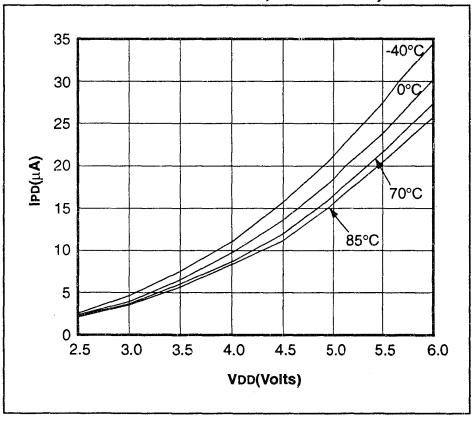
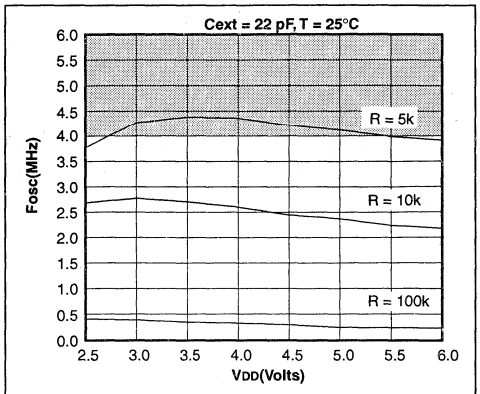


FIGURE 22-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Shaded area is beyond recommended range.

FIGURE 22-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

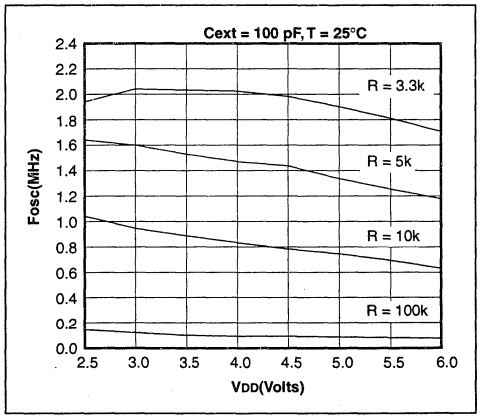
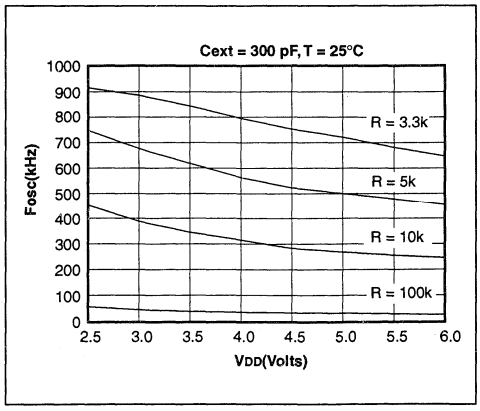


FIGURE 22-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Data based on matrix samples. See first page of this section for details.

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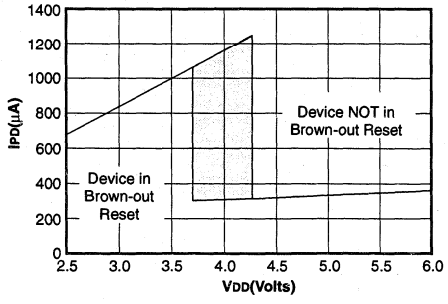
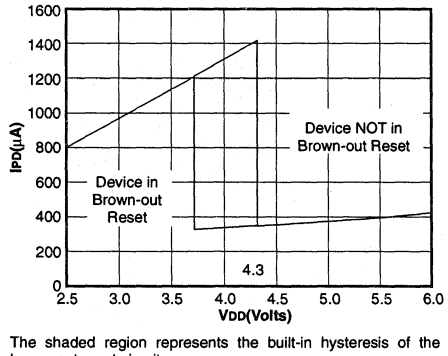
FIGURE 22-8: TYPICAL IPD vs. VDD BROWN-OUT DETECT ENABLED (RC MODE)



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

FIGURE 22-9: MAXIMUM IPD vs. VDD BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

FIGURE 22-10: TYPICAL IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

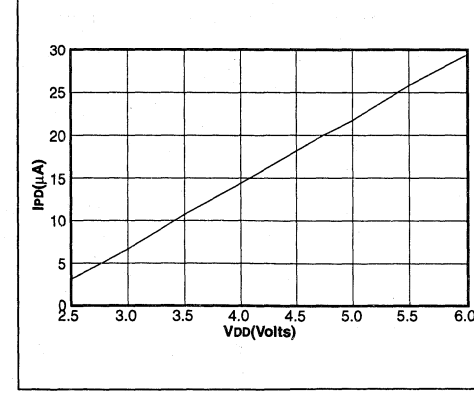
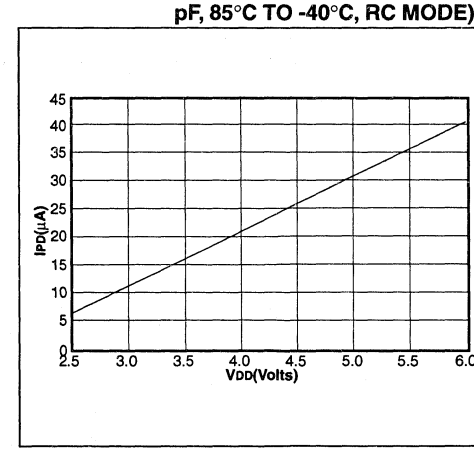


FIGURE 22-11: MAXIMUM IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)



Data based on matrix samples. See first page of this section for details.

10

Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 22-12: TYPICAL IDD vs. FREQUENCY (RC MODE @ 22 pF, 25°C)

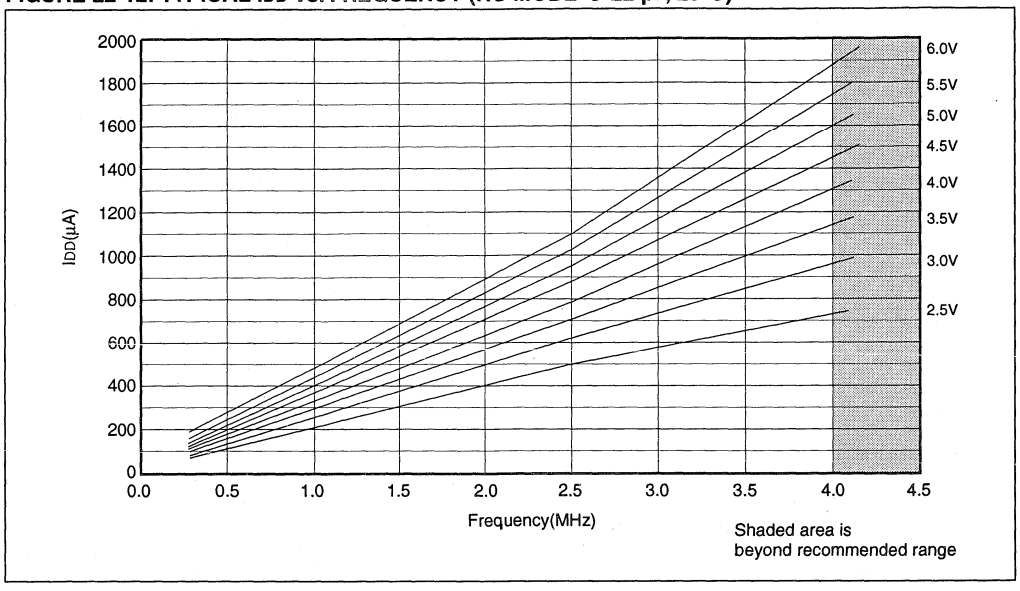
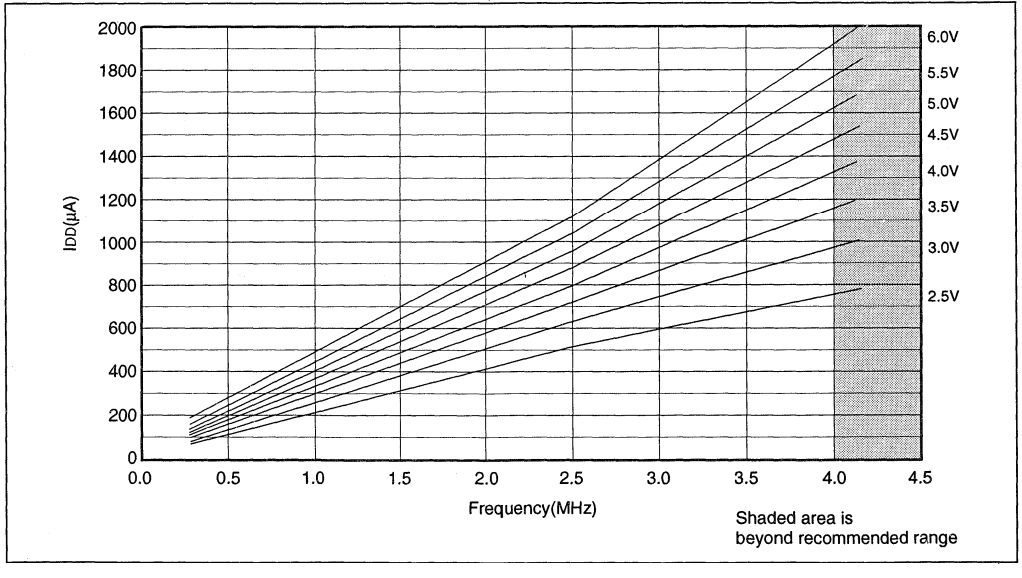


FIGURE 22-13: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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FIGURE 22-14: TYPICAL IDD vs. FREQUENCY (RC MODE @ 100 pF, 25°C)

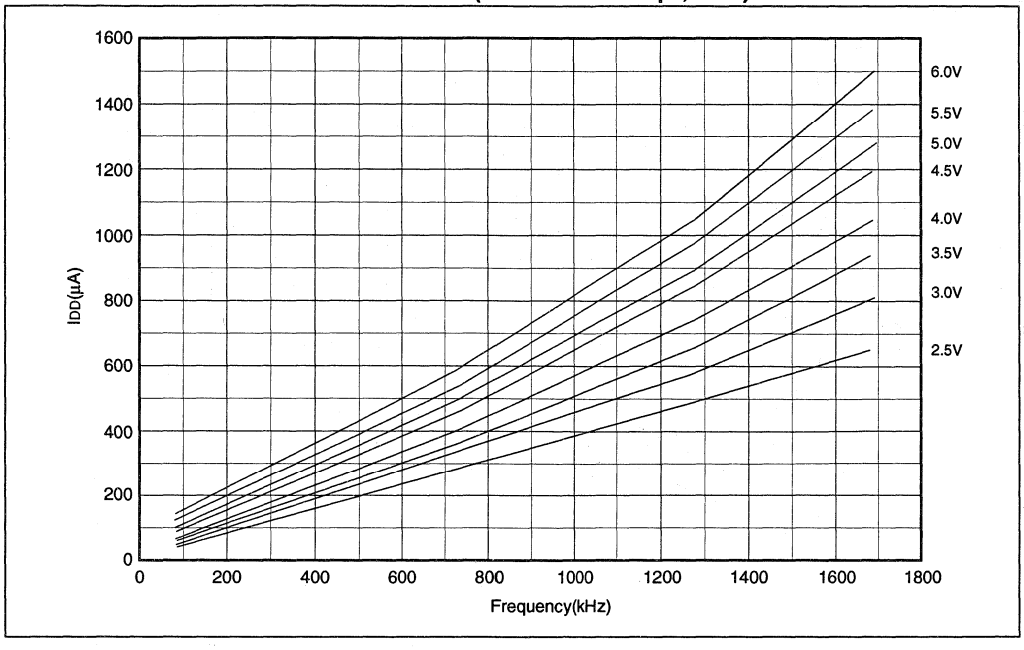
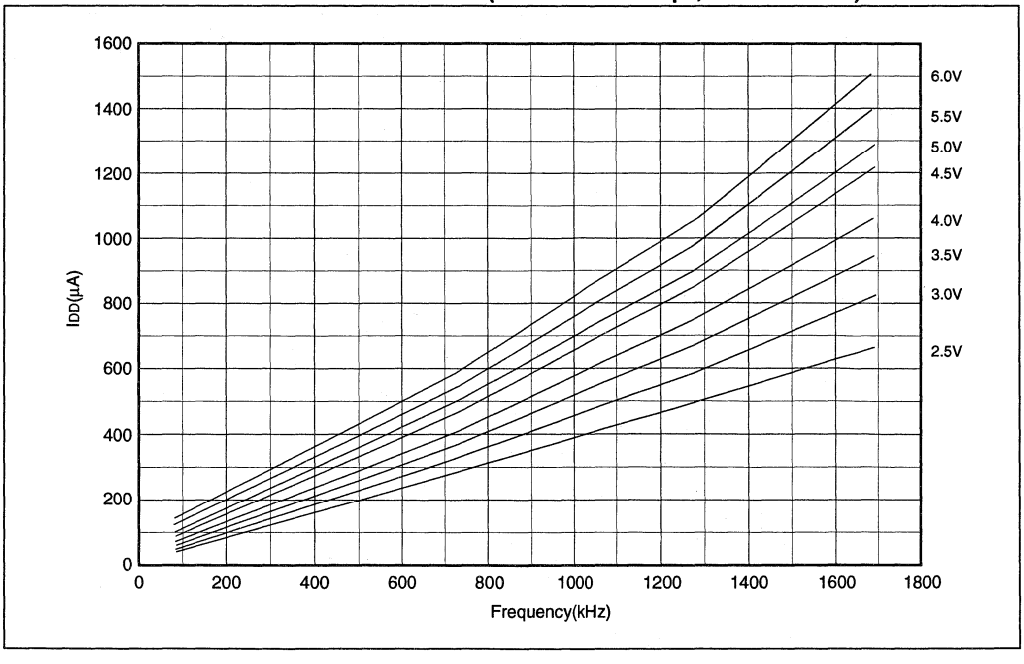


FIGURE 22-15: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 22-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

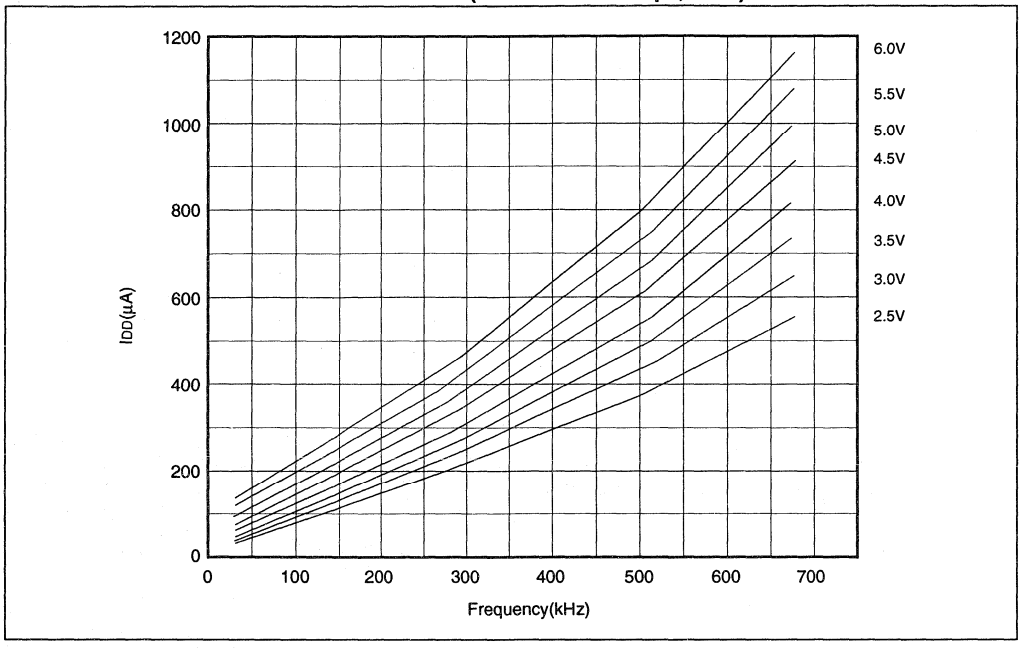
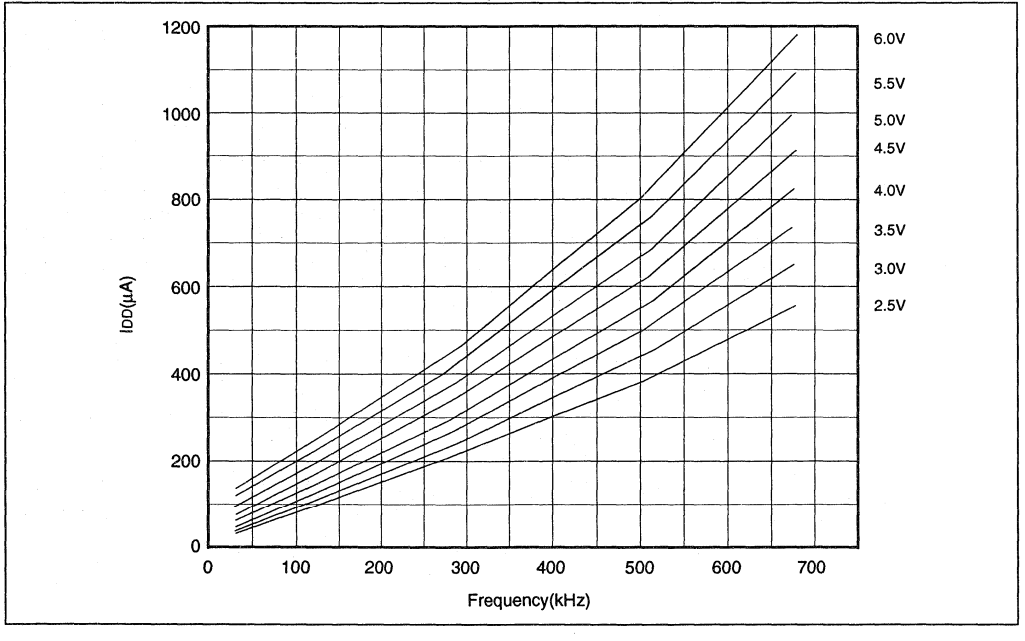


FIGURE 22-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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FIGURE 22-18: TYPICAL IDD vs. CAPACITANCE @ 500 kHz (RC MODE)

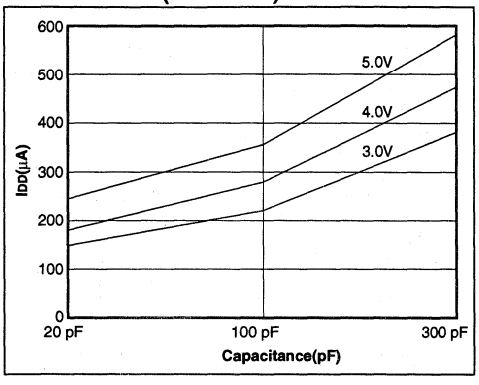


TABLE 22-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
22 pF	5k	4.12 MHz	± 1.4%
	10k	2.35 MHz	± 1.4%
	100k	268 kHz	± 1.1%
100 pF	3.3k	1.80 MHz	± 1.0%
	5k	1.27 MHz	± 1.0%
	10k	688 kHz	± 1.2%
	100k	77.2 kHz	± 1.0%
300 pF	3.3k	707 kHz	± 1.4%
	5k	501 kHz	± 1.2%
	10k	269 kHz	± 1.6%
	100k	28.3 kHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

FIGURE 22-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs. VDD

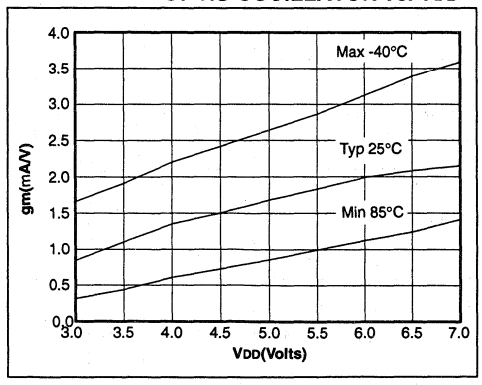


FIGURE 22-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs. VDD

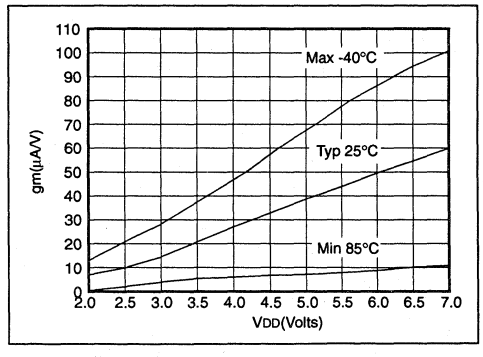
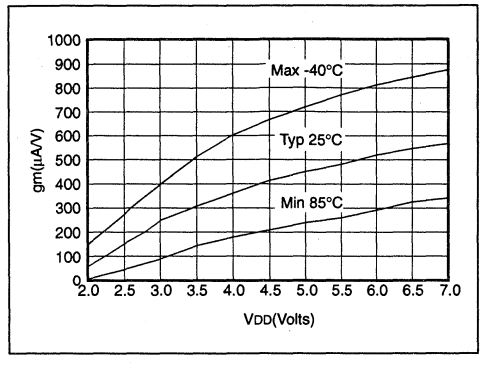


FIGURE 22-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs. VDD



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 22-22: TYPICAL XTAL STARTUP TIME vs. VDD (LP MODE, 25°C)

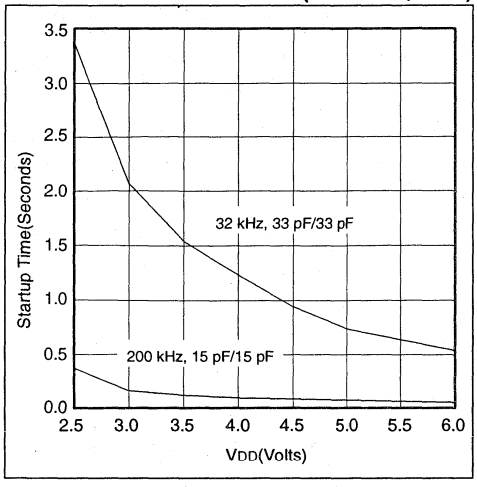

FIGURE 22-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)

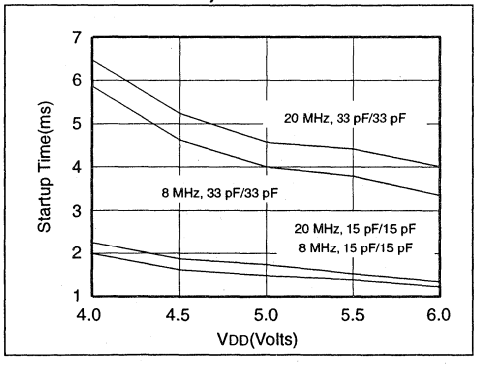

FIGURE 22-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)

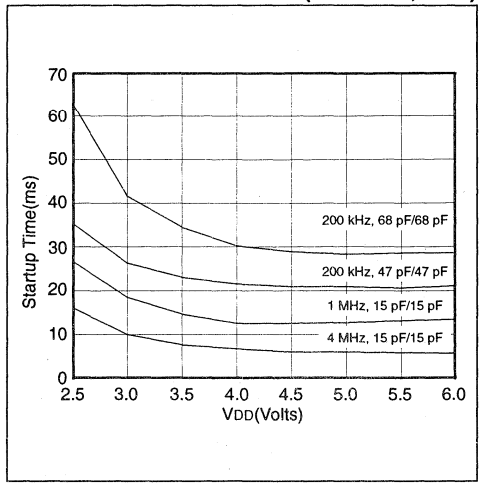

TABLE 22-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

Crystals Used		
32 kHz	Epson C-001R32.768K-A	± 20 PPM
200 kHz	STD XTL 200.000KHz	± 20 PPM
1 MHz	ECS ECS-10-13-1	± 50 PPM
4 MHz	ECS ECS-40-20-1	± 50 PPM
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM

Data based on matrix samples. See first page of this section for details.

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Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 22-25: TYPICAL IDD vs. FREQUENCY (LP MODE, 25°C)

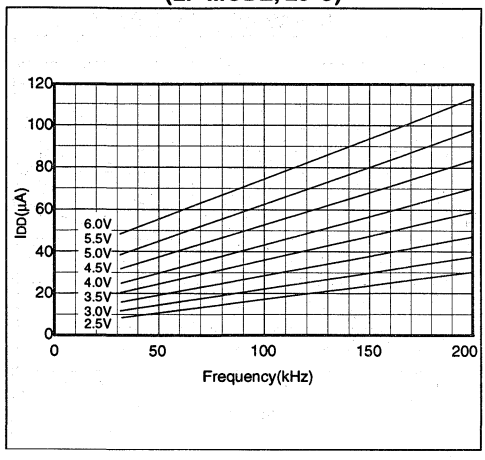


FIGURE 22-26: MAXIMUM IDD vs. FREQUENCY (LP MODE, 85°C TO -40°C)

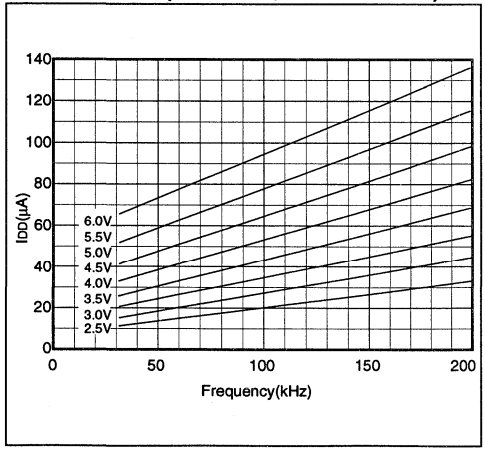


FIGURE 22-27: TYPICAL IDD vs. FREQUENCY (XT MODE, 25°C)

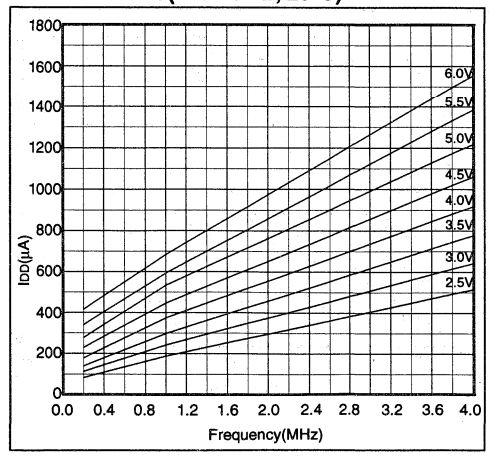
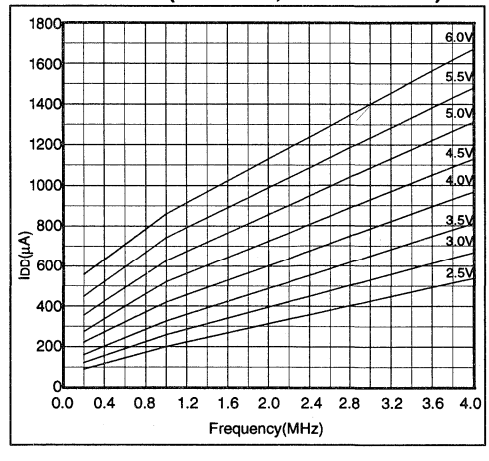


FIGURE 22-28: MAXIMUM IDD vs. FREQUENCY (XT MODE, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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Applicable Devices	710	71	711	72	73	73A	74	74A

FIGURE 22-29: TYPICAL IDD vs. FREQUENCY (HS MODE, 25°C)

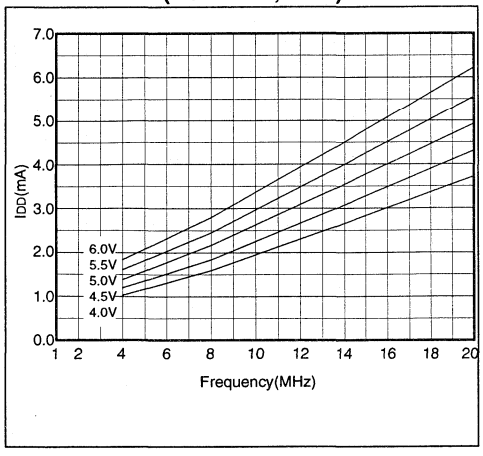
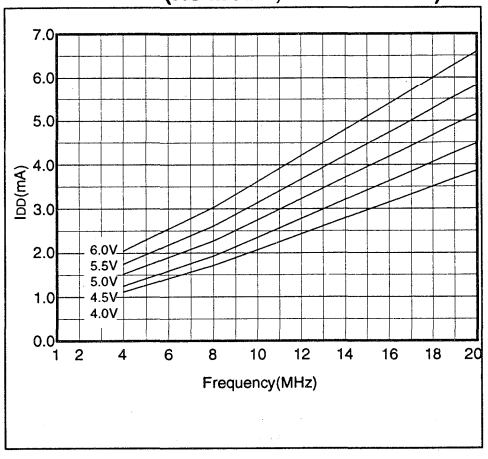


FIGURE 22-30: MAXIMUM IDD vs. FREQUENCY (HS MODE, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

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APPENDIX A:

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (192 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. Bits PA2, PA1, PA0 are removed from STATUS register.
3. Data memory paging is redefined slightly. STATUS register is modified.
4. Four new instructions have been added: `RETURN`, `RETFIE`, `ADDLW`, and `SUBLW`. Two instructions `TRIS` and `OPTION` are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. T0CKI pin is also a port pin (RA4) now.
14. FSR is made a full eight bit register.
15. "In-circuit serial programming" is made possible. The user can program PIC16CXX devices using only five pins: V_{DD}, V_{SS}, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-on Reset status bit ($\overline{POR}$).
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
18. Brown-out protection circuitry has been added. Controlled by configuration word bit BODEN. Brown-out reset ensures the device is placed in a reset condition if V_{DD} dips below a fixed setpoint.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for `CALL`, `GOTO`.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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APPENDIX C: WHAT'S NEW

Characterization data charts and graphs have been added for the following devices:

- PIC16C72
- PIC16C73
- PIC16C73A
- PIC16C74
- PIC16C74A

APPENDIX D: WHAT'S CHANGED

Minor changes, spelling and grammatical changes.

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PIC16C7X Product Identification System

To order or obtain information, e.g., on pricing or delivery refer to the factory or the listed sales office.

PART NO. -XX X /XX XXX

Pattern:	QTP, SQTP, Code or Special Requirements		
Package:	JW	=	Windowed CERDIP
	PQ	=	MQFP (Metric PQFP)
	TQ	=	TQFP (Thin Quad Flatpack)
	SO	=	SOIC
	SP	=	Skinny plastic dip
	P	=	PDIP
	L	=	PLCC
	SS	=	SSOP
Temperature Range:	-	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Frequency Range:	04	=	200 kHz (PIC16C7X-04)
	04	=	4 MHz
	10	=	10 MHz
	20	=	20 MHz
Device	PIC16C7X	:VDD range 4.0V to 6.0V	
	PIC16C7XT	:VDD range 4.0V to 6.0V (Tape/Reel)	
	PIC16LC7X	:VDD range 2.5V to 6.0V	
	PIC16LC7XT	:VDD range 2.5V to 6.0V (Tape/Reel)	

Examples

a) PIC16C71 - 04/P 301 Commercial Temp., PDIP Package, 4 MHz, normal VDD limits, QTP pattern #301

b) PIC16LC73 - 041/SO Industrial Temp., SOIC package, 4 MHz, extended VDD limits

c) PIC16C74A - 10E/P Automotive Temp., PDIP package, 10 MHz, normal VDD limits

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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PIC16CR72

28-Pin 8-Bit ROM-Based Microcontroller Product Brief

Features:

ROM Program	RAM Data	I/O	A/D Channel	PWM
2048	128	22	5	Yes

High-Performance RISC-like CPU:

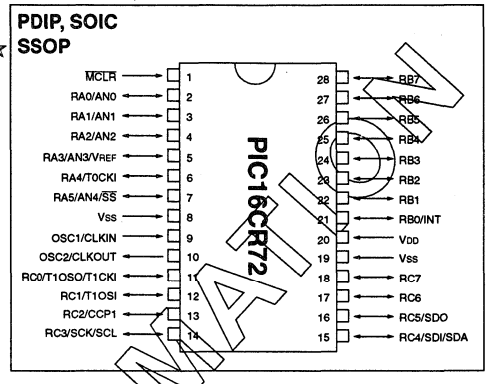
- Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed:
  - DC to 20 MHz clock input
  - DC to 200 ns instruction cycle
- 2048 x 14 on-chip ROM program memory
- 128 x 8 general purpose registers (SRAM)
- Eight levels deep hardware stack
- Interrupt capability

Peripheral Features:

- High current sink/source
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler
- TMR1: 16-bit timer/counter (time-base for capture/compare). TMR1 can be incremented during sleep via external crystal/clock (for real-time clock)
- TMR2: 8-bit timer/counter with 8-bit period register (time-base for PWM), prescaler and postscaler
- ★ One CCP pin that can be configured as capture input, PWM output, or compare output
  - 16-bit Capture, max resolution 12.5 ns (typ)
  - 16-bit Compare, max resolution 200 ns
  - 1 to 10-bit PWM resolution. Maximum PWM frequency @: 8-bit resolution = 80 kHz, 10-bit resolution = 20 kHz
- ★ 8-Bit Analog to Digital Converter (A/D) with high speed conversion rate (25 µs). Can also operate during sleep.
- Synchronous Serial Port (SSP) with two modes of operation:
  - 3-wire SPI™ (Supports all 4 SPI modes)
  - I²C™ slave mode

Pin Diagram

PDIP, SOIC
★ SSOP



Special Microcontroller Features:

- ★ Mixed Signal Microcontroller
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-system programming (via two pins)
- Brown-out protection

CMOS Technology:

- Low-power, high-speed CMOS ROM technology
- Fully static design
- ★ Wide-operating voltage range (3.0 V to 5.5 V)
- Commercial, Industrial and Automotive Temperature Ranges
- Low-power consumption
  - <2.0 mA @ 5.0 V, 4 MHz
  - 15 µA typical @ 3.0 V, 32 kHz
  - <1.0 µA typical standby current @ 3.0 V

ADVANCE INFORMATION

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PIC16C76/77

EPROM-Based 8-Bit Microcontroller Product Brief

Device	Program Memory	Data Memory	Pins	8-Bit A/D	CCP	SSP	USART	PSP
PIC16C76	8K x 14	368 x 8	28	5 ch*	2	Yes	Yes	No
PIC16C77	8K x 14	368 x 8	40-44	8 ch*	2	Yes	Yes	Yes

High Performance RISC CPU:

- Simple instruction set - 35 total
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle
- ★ 8K x 14 on-chip EPROM program memory
- ★ 368 x 8 general purpose registers (SRAM)
- Eight levels of hardware stack
- Interrupt capability

Peripheral Features:

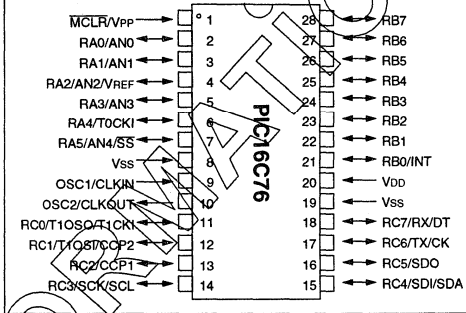
- High current sink/source
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler
- TMR1: 16-bit timer/counter (time-base for capture/compare). TMR1 can be incremented during sleep via external crystal/clock (for real-time clock)
- TMR2: 8-bit timer/counter with 8-bit period register (time-base for PWM), prescaler and postscaler
- ★ Two CCP pins that can be configured as capture input, PWM output, or compare output
  - Capture is 16-bit, max resolution 12.5 ns
  - Compare is 16-bit, max resolution 200 ns
  - PWM resolution is 1- to 10-bit. Maximum PWM frequency @: 8-bit resolution = 80 kHz, 10-bit resolution = 20 kHz
- ★ 8-Bit Analog to Digital Converter (A/D) with high speed conversion rate (25 µs). Can also operate during sleep.
- Synchronous Serial Port (SSP) with two modes of operation:
  - 3-wire SPI™ (Supports all 4 SPI modes)
  - I^2C™ slave mode
- ★ USART (supports high and low speed)/SCI
- Parallel Slave Port (PSP), 8-bits wide with external RD, WR, and CS controls (PIC16C77 only)

Special Microcontroller Features:

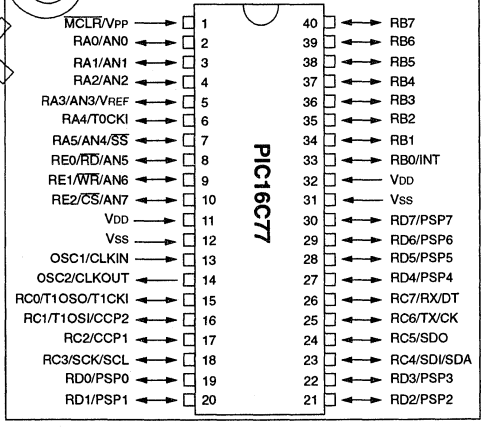
- ★ Mixed Signal Microcontroller
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Brown-out Reset circuitry

Pin Diagram

PDIP, SOIC, Windowed CERDIP



PDIP, Windowed CERDIP (Also PLCC, TQFP, MQFP)



CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range (2.5V to 6.0V)
- Commercial, industrial and automotive temperature ranges
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - < 1.0 µA typical standby current @ 3.0V

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PRELIMINARY INFORMATION

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NOTES:

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MICROCHIP

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PIC16CR8XA ROM/EEPROM 8-Bit Microcontroller Product Brief 11-177

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MICROCHIP

PIC16C84

8-Bit CMOS EEPROM Microcontroller

High Performance RISC CPU Features

- Only 35 single word instructions to learn
- All instructions single cycle (400 ns @ 10MHz) except for program branches which are two-cycle
- Operating speed: DC - 10MHz clock input
  DC - 400 ns instruction cycle
- 14-bit wide instructions
- 8-bit wide data path
- 1K x 14 EEPROM program memory
- 36 x 8 general purpose registers (SRAM)
- 64 x 8 on-chip EEPROM data memory
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt on change
  - Data EEPROM write complete
- 1,000,000 data memory EEPROM ERASE/WRITE cycles
- EEPROM Data Retention > 40 years

Peripheral Features

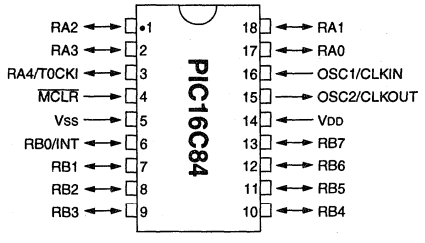
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 20 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features

- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial In-System Programming - via two pins

Pin Diagram

PDIP, SOIC



CMOS Technology

- Low-power, high-speed CMOS EEPROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 6.0V
  - Industrial: 2.0V to 6.0V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 60 µA typical @ 2V, 32 kHz
  - 26 µA typical standby current @ 2V

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1.0 GENERAL DESCRIPTION

The PIC16C84 is a low-cost, high-performance, CMOS, fully-static, 8-bit microcontroller.

All PIC16/17 microcontrollers employ an advanced RISC architecture. PIC16CXX devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with a separate 8-bit wide data bus. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set is used to achieve a very high performance level.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and up to a 2:1 speed improvement (at 10 MHz) over other 8-bit microcontrollers in their class.

The PIC16C84 has 36 bytes of RAM, 64 bytes of Data EEPROM memory, and 13 I/O pins. A timer/counter is also available.

The PIC16CXX family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake the chip from sleep through several external and internal interrupts and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

The PIC16C84 EEPROM program memory allows the same device package to be used for prototyping and production. In-circuit reprogrammability allows the code to be updated without the device being removed from the end application. This is useful in the development of many applications where the device may not be easily accessible, but the prototypes may require code updates. This is also useful for remote applications where the code may need to be updated (such as rate information).

Table 1-1 lists the features of the PIC16C84, and Appendix F: lists the features of all of the Microchip microcontrollers.

A simplified block diagram of the PIC16C84 is shown in Figure 3-1.

The PIC16C84 fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, electronic locks, security devices and smart cards. The EEPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, security codes, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C84 very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, serial communication, capture and compare, PWM functions and co-processor applications).

The serial in-system programming feature (via two pins) offers flexibility of customizing the product after complete assembly and testing. This feature can be used to serialize a product, store calibration data, or program the device with the current firmware before shipping.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A: for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to the PIC16C84 (Appendix B:).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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TABLE 1-1: PIC16C8X FAMILY OF DEVICES

	Clock	Memory				Peripherals		Features	
	Maximum Frequency of Operation (MHz)	Program Memory			Data Memory (bytes)	Data EEPROM (bytes)	Timer Module(s)	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Packages
		Flash	EEPROM	ROM							
PIC16C84	10	—	1K	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F84[1]	10	1K	—	—	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR84[1]	10	—	—	1K	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F83[1]	10	512	—	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR83[1]	10	—	—	512	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16C8X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

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2.0 PIC16C84 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in this section. When placing orders, please use the "PIC16C84 Product Identification System" at the back of this data sheet to specify the correct part number.

There are two device "types" as indicated in the device number.

1. **C**, as in PIC16**C**84. These devices have EEPROM program memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**84. These devices have EEPROM program memory and operate over an extended voltage range.

When discussing memory maps and other architectural features, the use of **C** also implies the **LC** versions.

2.1 Electrically Erasable Devices

These devices are offered in the lower cost plastic package, even though the device can be erased and reprogrammed. This allows the same device to be used for prototype development and pilot programs as well as production.

A further advantage of the electrically erasable version is that they can be erased and reprogrammed in-circuit, or by device programmers, such as Microchip's PICSTART® Plus or PRO MATE™ II programmers.

2.2 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices have all EEPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available.

For information on submitting a QTP code, please contact your Microchip Regional Sales Office.

2.3 Serialized Quick-Turnaround-Production (SQTP℠) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

For information on submitting a SQTP code, please contact your Microchip Regional Sales Office.

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NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC16CXX opcodes are 14-bits wide, enabling single word instructions. The full 14-bit wide program memory bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle (400 ns @ 10 MHz) except for program branches.

The PIC16C84 addresses 1K x 14 program memory. All program memory is internal.

PIC16CXX devices can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. An orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C84 has 36 x 8 SRAM and 64 x 8 EEPROM data memory.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), and the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

A simplified block diagram for the PIC16C84 is shown in Figure 3-1, its corresponding pin description is shown in Table 3-1.

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FIGURE 3-1: PIC16C84 BLOCK DIAGRAM

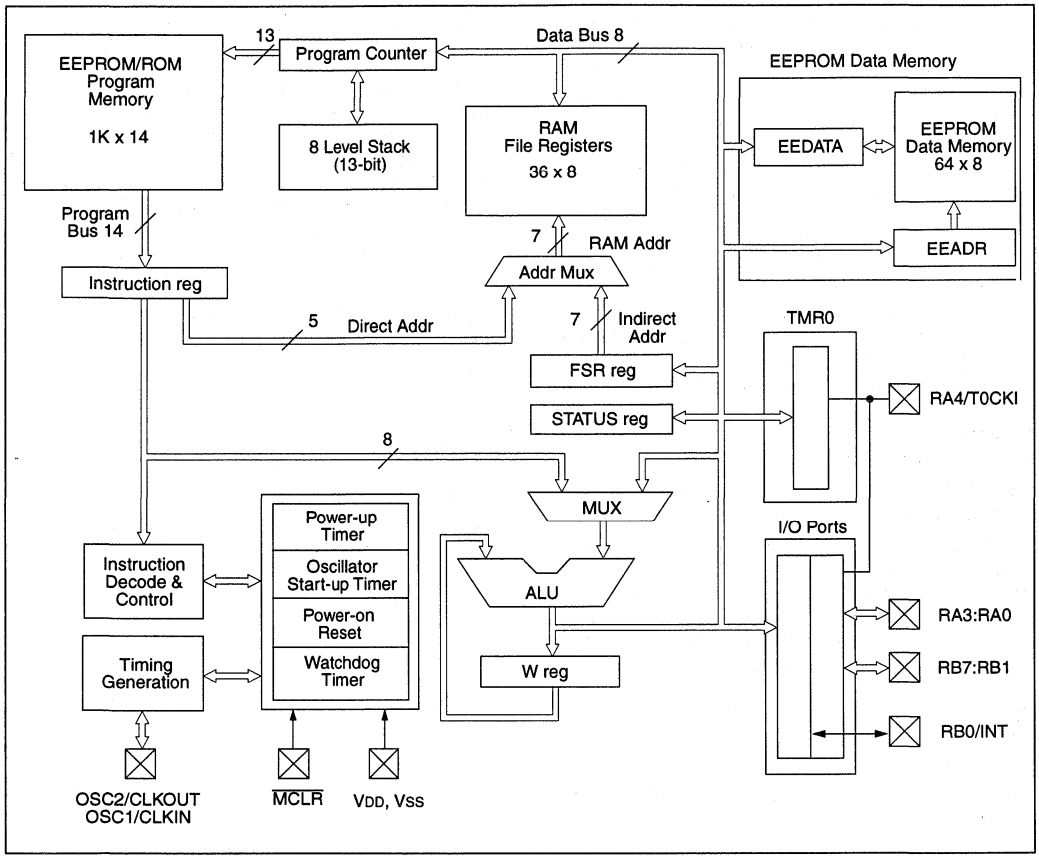

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TABLE 3-1: PIC16C8X PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS (1)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = output I/O = Input/Output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

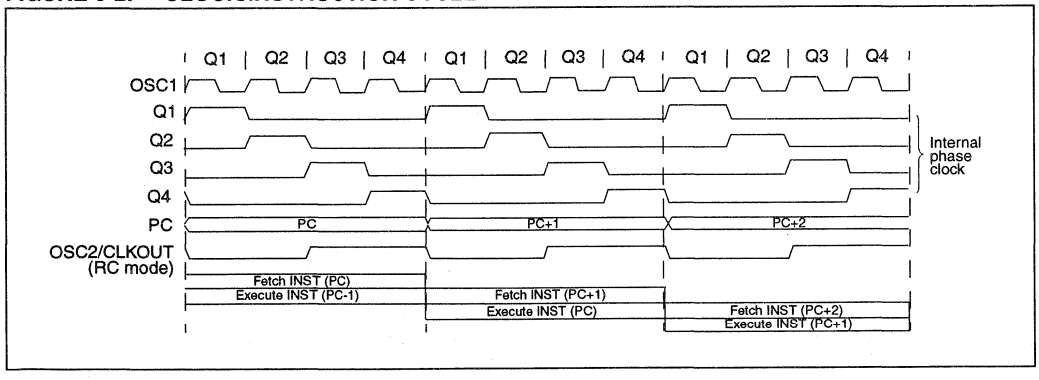
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

```
1. MOVLW 55h
2. MOVWF PORTB
3. CALL  SUB_1
4. BSF   PORTA, BIT3
```

Fetch 1	Execute 1				
	Fetch 2	Execute 2			
		Fetch 3	Execute 3		
			Fetch 4	Flush	
				Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16C84. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

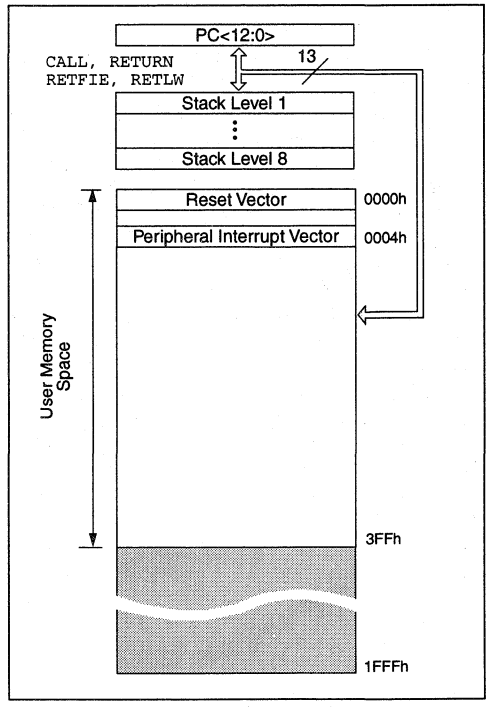
The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 7.0.

4.1 Program Memory Organization

The PIC16CXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16C84, only the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 4-1). Accessing a location above the physically implemented address will cause a wraparound. For example, locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK



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4.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 4-2 shows the data memory map organization.

Instructions `MOVWF` and `MOVF` can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 4.5). Indirect addressing uses the present value of the RP1:RP0 bits for access into the banked areas of data memory.

Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

4.2.1 GENERAL PURPOSE REGISTER FILE

All devices have some amount of General Purpose Register (GPR) area. Each GPR is 8 bits wide and is accessed either directly or indirectly through the FSR (Section 4.5).

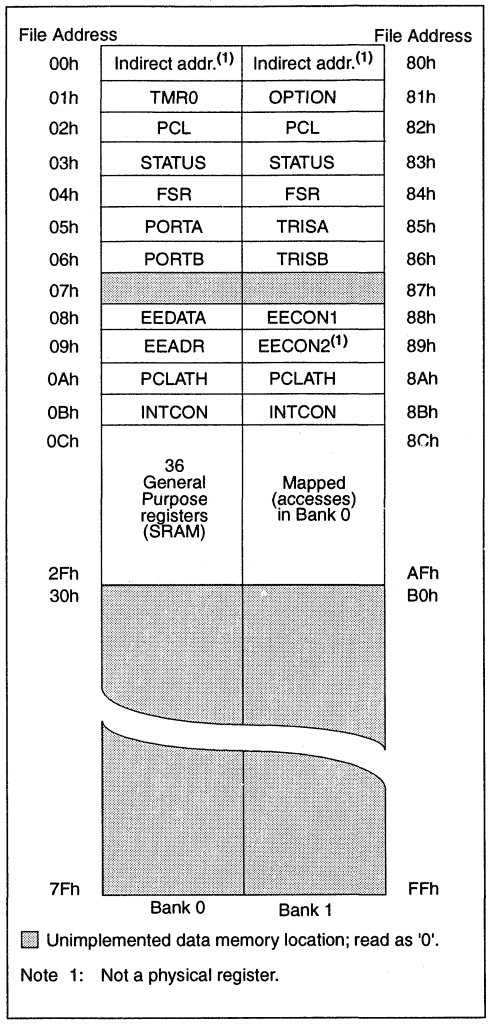
The GPR addresses in bank 1 are mapped to addresses in bank 0. As an example, addressing location 0Ch or 08h will access the same GPR.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (Figure 4-2 and Table 4-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

FIGURE 4-2: REGISTER FILE MAP



Note 1: Not a physical register.

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TABLE 4-1: REGISTER FILE SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note3)
Bank 0											
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h	PCL	Low order 8 bits of the Program Counter (PC)								0000 0000	0000 0000
03h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
07h		Unimplemented location, read as '0'								---- ----	---- ----
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC (1)					---0 0000	---0 0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	0000 0000
83h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA data direction register					---1 1111	---1 1111
86h	TRISB	PORTB data direction register								1111 1111	1111 1111
87h		Unimplemented location, read as '0'								---- ----	---- ----
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2 (not a physical register)								---- ----	---- ----
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC (1)					---0 0000	---0 0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on condition.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> is never transferred to PCLATH.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a $\overline{MCLR}$ reset.

3: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

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4.2.2.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u uluu` (where `u` = unchanged).

Only the `BCF, BSF, SWAPF` and `MOVWF` instructions should be used to alter the STATUS register (Table 9-2) because these instructions do not affect any status bit.

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C84 and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{borrow}$ and digit $\overline{borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

Note 3: When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

FIGURE 4-3: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
0 = Bank 0, 1 (00h - FFh)
1 = Bank 2, 3 (100h - 1FFh)
The IRP bit is not used by the PIC16C8X. IRP should be maintained clear.

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
10 = Bank 2 (100h - 17Fh)
11 = Bank 3 (180h - 1FFh)
Each bank is 128 bytes. Only bit RP0 is used by the PIC16C8X. RP1 should be maintained clear.

bit 4: **TO**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **PD**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `ADDLW` instructions) (For $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF` and `ADDLW` instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF, RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

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4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

FIGURE 4-4: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled (by individual port latch values)

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to TMR0

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable bits for all interrupt sources.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-5: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

Note: For the operation of the interrupt structure, please refer to Section 8.5.

bit 6: **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT Interrupt Enable bit
1 = Enables the RB0/INT interrupt
0 = Disables the RB0/INT interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 overflow interrupt flag bit
1 = TMR0 has overflowed (must be cleared in software)
0 = TMR0 did not overflow

bit 1: **INTF:** RB0/INT Interrupt Flag bit
1 = The RB0/INT interrupt occurred
0 = The RB0/INT interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

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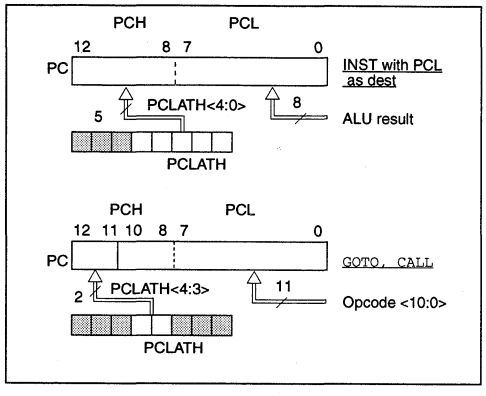
4.3 Program Counter: PCL and PCLATH

The Program Counter (PC) is 13-bits wide. The low byte is the PCL register, which is a readable and writable register. The high byte of the PC (PC<12:8>) is not directly readable nor writable and comes from the PCLATH register. The PCLATH (PC latch high) register is a holding register for PC<12:8>. The contents of PCLATH are transferred to the upper byte of the program counter when the PC is loaded with a new value. This occurs during a CALL, GOTO or a write to PCL. The high bits of PC are loaded from PCLATH as shown in Figure 4-6.

FIGURE 4-6: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 word block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 PROGRAM MEMORY PAGING

The PIC16C84 has 1K of program memory. The CALL and GOTO instructions have an 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. For future PIC16CXX program memory expansion, there must be another two bits to specify the program memory page. These paging bits come from the PCLATH<4:3> bits (Figure 4-6). When doing a CALL or a GOTO instruction, the user must ensure that these page bits (PCLATH<4:3>) are programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is "pushed" onto the stack (see next section). Therefore, manipulation of the PCLATH<4:3> is not required for the return instructions (which "pops" the PC from the stack)

Note: The PIC16C84 ignores the PCLATH<4:3> bits, which are used for program memory pages 1, 2 and 3 (0800h - 1FFFh). The use of PCLATH<4:3> as general purpose R/W bits is not recommended since this may affect upward compatibility with future products.

4.4 Stack

The PIC16C84 has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable.

The entire 13-bit PC is "pushed" onto the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is "popped" in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a push or a pop operation.

Note: There are no instruction mnemonics called push or pop. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

The stack operates as a circular buffer. That is, after the stack has been pushed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

If the stack is effectively popped nine times, the PC value is the same as the value from the first pop.

Note: There are no status bits to indicate stack overflow or stack underflow conditions.

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4.5 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

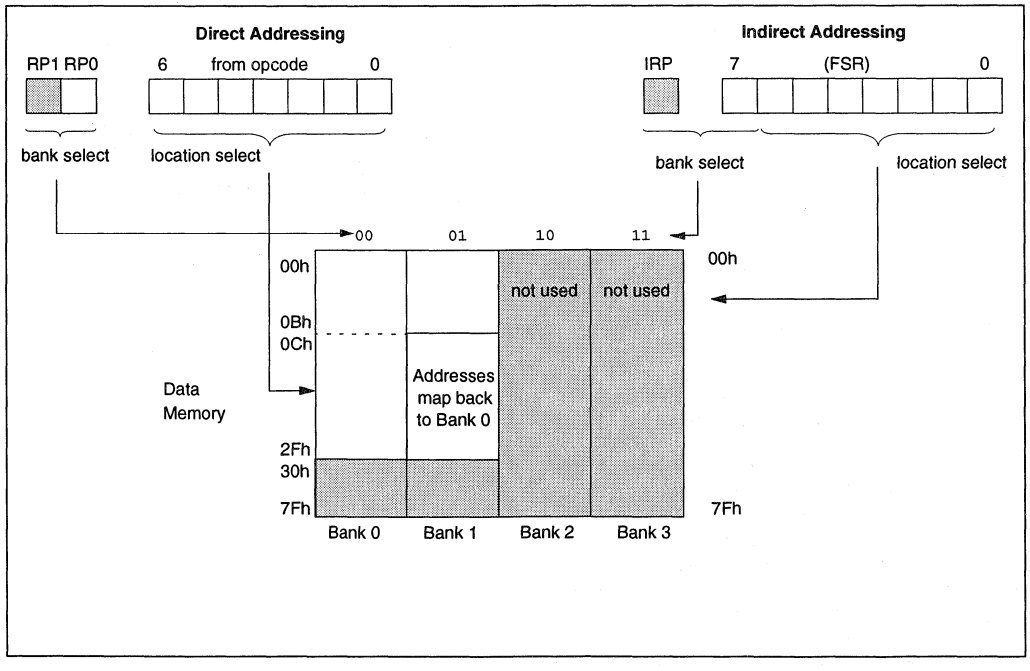
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x20  ;initialize pointer
        movwf   FSR   ;  to RAM
NEXT    clrf    INDF  ;clear INDF register
        incf    FSR   ;inc pointer
        btfss   FSR,4 ;all done?
        goto    NEXT  ;NO, clear next
CONTINUE
        :             ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-7. However, IRP is not used in the PIC16C84.

FIGURE 4-7: DIRECT/INDIRECT ADDRESSING



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5.0 I/O PORTS

The PIC16C84 has two ports, PORTA and PORTB. Some port pins are multiplexed with an alternate function for other features on the device.

5.1 PORTA and TRISA Registers

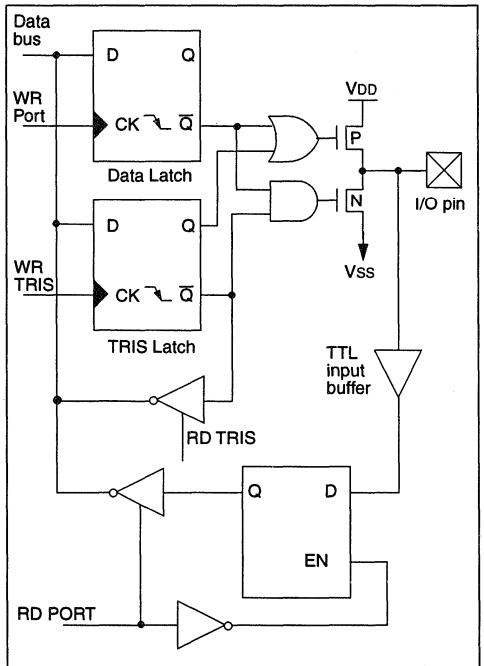
PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedence mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The RA4 pin is multiplexed with the TMR0 clock input.

FIGURE 5-1: BLOCK DIAGRAM OF PINS RA3:RA0

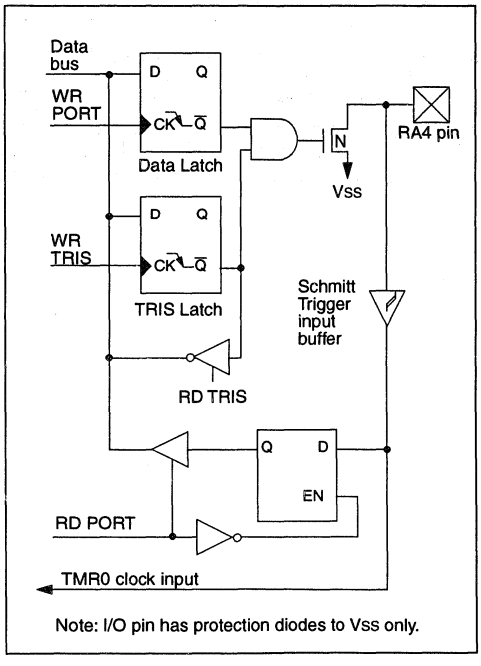


Note: I/O pins have protection diodes to VDD and Vss.

EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF    PORTA       ; Initialize PORTA by
                    ; setting output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0x0F        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISA       ; Set RA<3:0> as inputs
                    ; RA4 as outputs
                    ; TRISA<7:5> are always
                    ; read as '0'.
```

FIGURE 5-2: BLOCK DIAGRAM OF PIN RA4



Note: I/O pin has protection diodes to Vss only.

Note: For crystal oscillator configurations operating below 500 kHz, the device may generate a spurious internal Q-clock when PORTA<0> switches state. This does not occur with an external clock in RC mode. To avoid this, the RA0 pin should be kept static, i.e. in input/output mode, pin RA0 should not be toggled.

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TABLE 5-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are unimplemented, read as '0'

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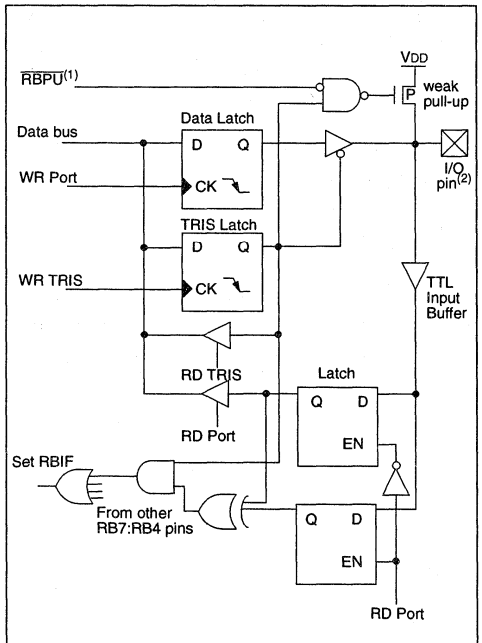
5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. A '1' on any bit in the TRISB register puts the corresponding output driver in a hi-impedance mode. A '0' on any bit in the TRISB register puts the contents of the output latch on the selected pin(s).

Each of the PORTB pins have a weak internal pull-up. A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{RBPU}$ (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The pins value in input mode are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of the pins are OR'ed together to generate the RB port change interrupt.

FIGURE 5-3: BLOCK DIAGRAM OF PINS RB7:RB4



Note 1: TRISB = '1' enables weak pull-up (if $\overline{RBPU}$ = '0' in the OPTION register).
2: I/O pins have diode protection to VDD and VSS.

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Read (or write) PORTB. This will end the mismatch condition.
b) Clear flag bit RBIF.

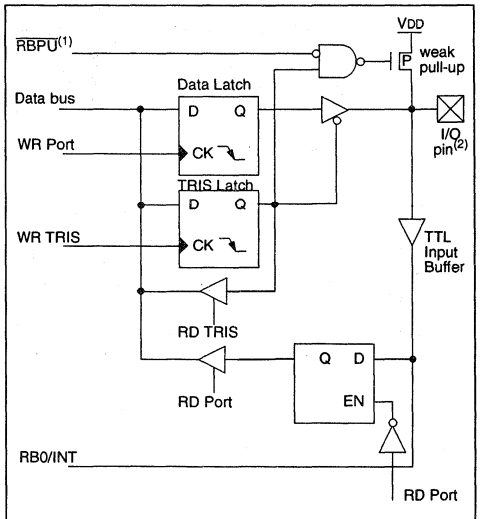
A mismatch condition will continue to set the RBIF bit. Reading PORTB will end the mismatch condition, and allow the RBIF bit to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression (see AN552 in the Embedded Control Handbook).

Note 1: If a change on the I/O pin should occur when a read operation of PORTB is being executed (start of the Q2 cycle), the RBIF interrupt flag bit may not be set.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-4: BLOCK DIAGRAM OF PINS RB3:RB0



Note 1: TRISB = '1' enables weak pull-up (if $\overline{RBPU}$ = '0' in the OPTION register).
2: I/O pins have diode protection to VDD and VSS.

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EXAMPLE 5-2: INITIALIZING PORTB

```
CLRF    PORTB       ; Initialize PORTB by
                    ; setting output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                    ; RB<5:4> as outputs
                    ; RB<7:6> as inputs
```

TABLE 5-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(1)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(1)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.
Note 1: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

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5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (i.e., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch is unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (i.e., BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output current may damage the chip.

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

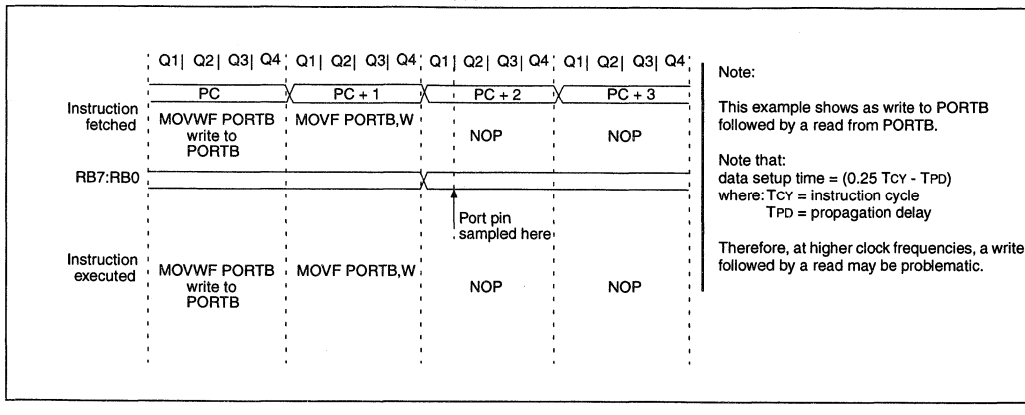
The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such that the pin voltage stabilizes (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

Example 5-3 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

EXAMPLE 5-3: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                       PORT latch  PORT pins
;                       ----------  ---------
  BCF PORTB, 7      ; 01pp ppp    11pp ppp
  BCF PORTB, 6      ; 10pp ppp    11pp ppp
  BSF STATUS, RP0   ;
  BCF TRISB, 7      ; 10pp ppp    11pp ppp
  BCF TRISB, 6      ; 10pp ppp    10pp ppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

FIGURE 5-5: SUCCESSIVE I/O OPERATION



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NOTES:

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6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module (Figure 6-1) will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

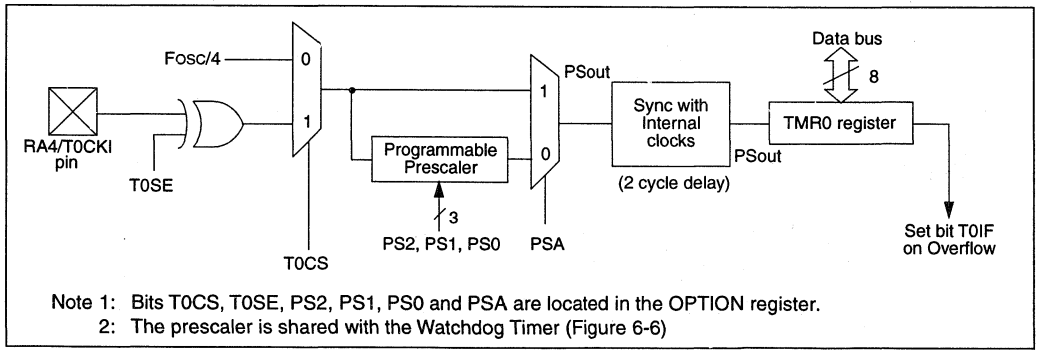
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode TMR0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the T0 source edge select bit, T0SE (OPTION<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 Module and the Watchdog Timer. The prescaler assignment is controlled, in software, by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 Module. The prescaler is not readable or writable. When the prescaler (Section 6.3) is assigned to the Timer0 Module, the prescale value (1:2, 1:4, ..., 1:256) is software selectable.

6.1 TMR0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets the T0IF bit (INTCON<2>). The interrupt can be masked by clearing enable bit T0IE (INTCON<5>). The T0IF bit must be cleared in software by the Timer0 Module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt (Figure 6-4) cannot wake the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 6-1: TMR0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PS2, PS1, PS0 and PSA are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-6)

FIGURE 6-2: TMR0 TIMING: INTERNAL CLOCK/NO PRESCALER

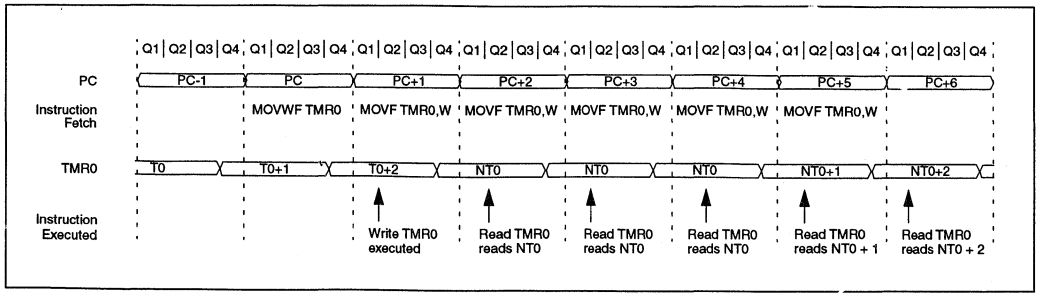


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FIGURE 6-3: TMR0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

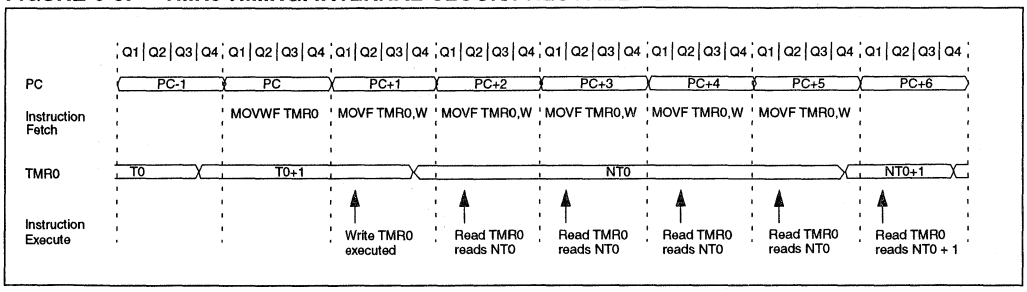
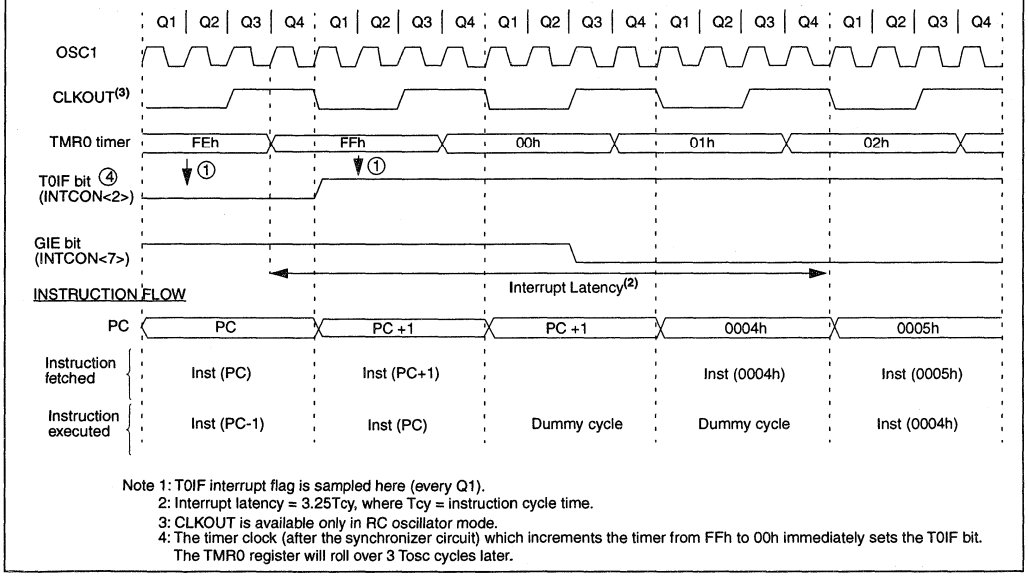


FIGURE 6-4: TMR0 INTERRUPT TIMING



Note 1: T0IF interrupt flag is sampled here (every Q1).
2: Interrupt latency = 3.25Tcy, where Tcy = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.
4: The timer clock (after the synchronizer circuit) which increments the timer from FFh to 00h immediately sets the T0IF bit. The TMR0 register will roll over 3 Tosc cycles later.

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6.2 Using TMR0 with External Clock

When an external clock input is used for TMR0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of the TMR0 register after synchronization.

6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of pin RA4/T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (plus a small RC delay) and low for at least 2Tosc (plus a small RC delay). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by an asynchronous ripple counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (plus a small RC delay) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the AC Electrical Specifications of the desired device.

6.2.2 TMR0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 Module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

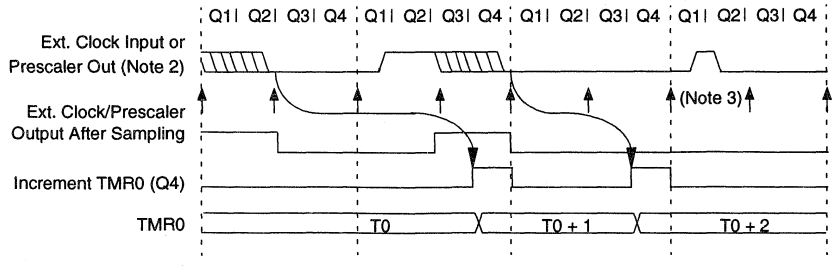
6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 Module, or as a postscaler for the Watchdog Timer (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 Module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 Module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 Module, all instructions writing to the Timer0 Module (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x` ....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to TMR0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on TMR0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows ↑ indicate where sampling occurs. A small clock pulse may be missed by sampling.

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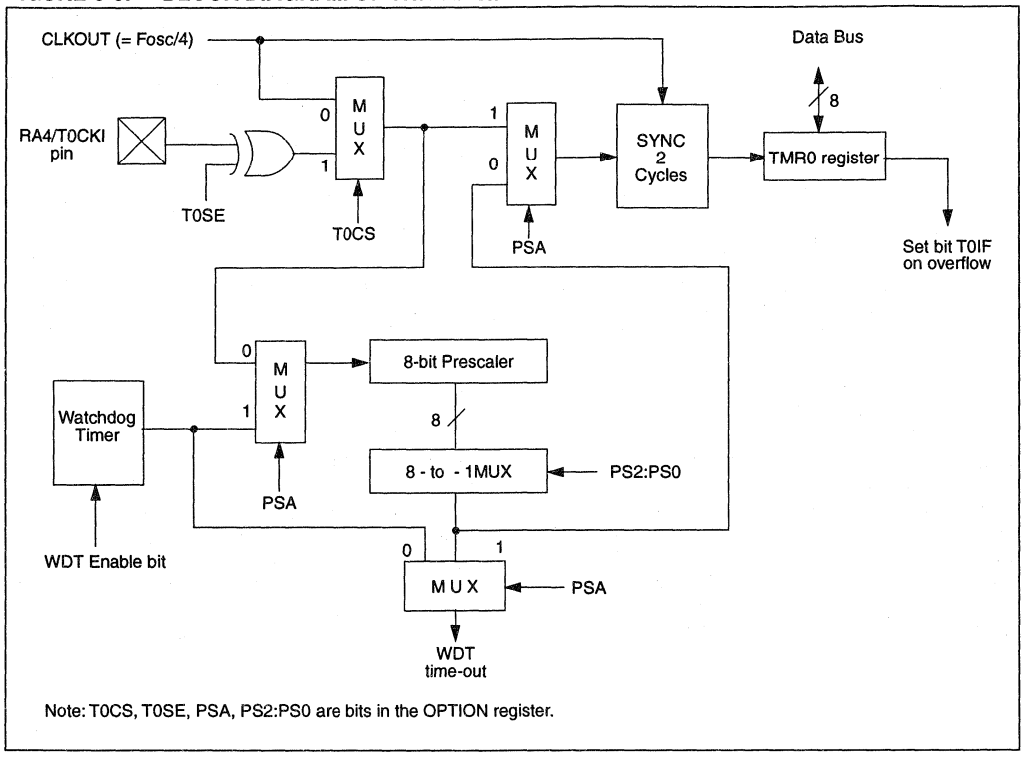
FIGURE 6-6: BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

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6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution).

Note: To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be taken even if the WDT is disabled. To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 6-2.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS, RP0  ;Bank 0
CLRF    TMR0         ;Clear TMR0
                     ; and Prescaler
BSF     STATUS, RP0  ;Bank 1
CLRWDT               ;Clears WDT
MOVLW   b'xxxx1xxx'  ;Select new
MOVWF   OPTION       ; prescale value
BCF     STATUS, RP0  ;Bank 0
```

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT               ;Clear WDT and
                     ; prescaler
BSF     STATUS, RP0  ;Bank 1
MOVLW   b'xxxx0xxx'  ;Select TMR0, new
                     ; prescale value
                     ' and clock source
MOVWF   OPTION       ;
BCF     STATUS, RP0  ;Bank 0
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 0000
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not associated with Timer0.

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NOTES:

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7.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16C84 devices have 64 bytes of data EEPROM with an address range from 0h to 3Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

7.1 EEADR

The EEADR register can address up to a maximum of 256 bytes of data EEPROM. Only the first 64 bytes of data EEPROM are implemented.

The upper two bits are address decoded. This means that these two bits must always be '0' to ensure that the address is in the 64 byte memory space.

FIGURE 7-1: EECON1 REGISTER (ADDRESS 88h)

U	U	U	R/W-0	R/W-x	R/W-0	R/S-0	R/S-x
—	—	—	EEIF	WRERR	WREN	WR	RD
bit7							bit0

R = Readable bit
W = Writable bit
S = Settable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7:5 **Unimplemented:** Read as '0'

bit 4 **EEIF**: EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 **WRERR**: EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any $\overline{MCLR}$ reset or any WDT reset during normal operation)
0 = The write operation completed

bit 2 **WREN**: EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 **WR**: Write Control bit
1 = initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
0 = Write cycle to the data EEPROM is complete

bit 0 **RD**: Read Control bit
1 = Initiates an EEPROM read (read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software).
0 = Does not initiate an EEPROM read

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7.2 EECON1 and EECON2 Registers

EECON1 is the control register with five low order bits physically implemented. The upper-three bits are non-existent and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ reset or a WDT time-out reset during normal operation. In these situations, following reset, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDATA and EEADR registers.

Interrupt flag bit EEIF is set when write is complete. It must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the Data EEPROM write sequence.

7.3 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 7-1: DATA EEPROM READ

```
BCF     STATUS, RP0  ; Bank 0
MOVLW   CONFIG_ADDR  ;
MOVWF   EEADR        ; Address to read
BSF     STATUS, RP0  ; Bank 1
BSF     EECON1, RD   ; EE Read
BCF     STATUS, RP0  ; Bank 0
MOVF    EEDATA, W    ; W = EEDATA
```

7.4 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

EXAMPLE 7-2: DATA EEPROM WRITE

```
        BSF     STATUS, RP0  ; Bank 1
        BCF     INTCON, GIE  ; Disable INTs.
        BSF     EECON1, WREN ; Enable Write
Required
Sequence
        MOVLW   55h          ;
        MOVWF   EECON2       ; Write 55h
        MOVLW   AAh          ;
        MOVWF   EECON2       ; Write AAh
        BSF     EECON1,WR    ; Set WR bit
                             ;   begin write
        BSF     INTCON, GIE  ; Enable INTs.
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

Note: The data EEPROM memory E/W cycle time may occasionally exceed the 10 ms specification (typical). To ensure that the write cycle is complete, use the EE interrupt or poll the WR bit (EECON1<1>). Both these events signify the completion of the write cycle.

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7.5 Write Verify

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (Example 7-3) to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit. The Total Endurance disk will help determine your comfort level.

Generally the EEPROM write failure will be a bit which was written as a '1', but reads back as a '0' (due to leakage off the bit).

EXAMPLE 7-3: WRITE VERIFY

```
    BCF   STATUS, RP0 ; Bank 0
    :                 ; Any code can go here
    :                 ;
    MOVF  EEDATA, W   ; Must be in Bank 0
    BSF   STATUS, RP0 ; Bank 1
READ
    BSF   EECON1, RD  ; YES, Read the
                      ;   value written
    BCF   STATUS, RP0 ; Bank 0
;
; Is the value written (in W reg) and
;   read (in EEDATA) the same?
;
    SUBWF EEDATA, W   ;
    BTFSS STATUS, Z   ; Is difference 0?
    GOTO  WRITE_ERR   ; NO, Write error
    :                 ; YES, Good write
    :                 ; Continue program
```

7.6 Protection Against Spurious Writes

There are conditions when the device may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch, or software malfunction.

7.7 Data EEPROM Operation during Code Protect

When the device is code protected, the CPU is able to read and write unscrambled data to the Data EEPROM.

For ROM devices, there are two code protection bits (Section 8.1). One for the ROM program memory and one for the Data EEPROM memory.

7.8 Power Consumption Considerations

Note: It is recommended that the EEADR<7:6> bits be cleared. When either of these bits is set, the maximum I_{DD} for the device is higher than when both are cleared. The specification is 400 µA. With EEADR<7:6> cleared, the maximum is approximately 150 µA.

TABLE 7-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by Data EEPROM.

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NOTES:

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8.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16C84 has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- OSC selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16C84 has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

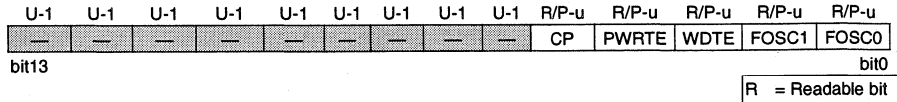
SLEEP mode offers a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

8.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming.

FIGURE 8-1: CONFIGURATION WORD



R = Readable bit
P = Programmable bit
U = Unimplemented bit, read as '1'
- n = Value at POR reset
u = unchanged

bit 13:5 **Unimplemented:** Read as '1'

bit 4 **CP**: Code Protection bit
1 = Code protection off
0 = All memory is code protected

bit 3 **PWRTE**: Power-up Timer Enable bit
1 = Power-up timer is enabled
0 = Power-up timer is disabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1:0 **FOSC1:FOSC0**: Oscillator Selection bits
11 =RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

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8.2 Oscillator Configurations

8.2.1 OSCILLATOR TYPES

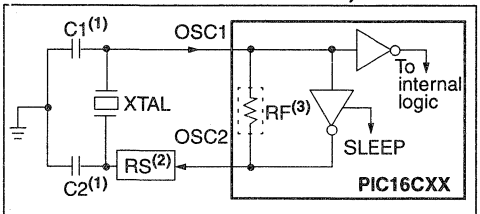
The PIC16C84 can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 8-2).

FIGURE 8-2: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note1: See Table 8-1 and Table 8-2 for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen.

The PIC16C84 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 8-3).

FIGURE 8-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

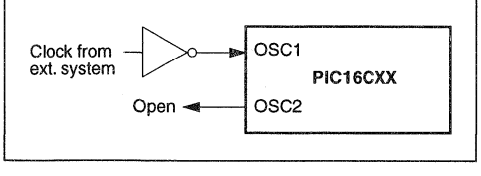


TABLE 8-1: PIC16C84 CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Tested:			
Mode	**Freq**	**OSC1/C1**	**OSC2/C2**
XT	455 kHz	47 - 100 pF	47 - 100 pF
	2.0 MHz	15 - 33 pF	15 - 33 pF
	4.0 MHz	15 - 33 pF	15 - 33 pF
HS	8.0 MHz	15 - 33 pF	15 - 33 pF
	10.0 MHz	15 - 33 pF	15 - 33 pF

Note: Recommended values of C1 and C2 are identical to the ranges tested table.
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for the appropriate values of external components.

Resonators Tested:		
455 kHz	Panasonic EFO-A455K04B	± 0.3%
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%
10.0 MHz	Murata Erie CSA10.00MTZ	± 0.5%

None of the resonators had built-in capacitors.

TABLE 8-2: PIC16C84 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	10 MHz	15 - 33 pF	15 - 33 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.

Crystals Tested:		
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM
200 kHz	STD XTL 200.000 KHz	± 20 PPM
1.0 MHz	ECS ECS-10-13-2	± 50 PPM
2.0 MHz	ECS ECS-20-S-2	± 50 PPM
4.0 MHz	ECS ECS-40-S-4	± 50 PPM
10.0 MHz	ECS ECS-100-S-4	± 50 PPM

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8.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits are available; one with series resonance, and one with parallel resonance.

Figure 8-4 shows a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 8-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

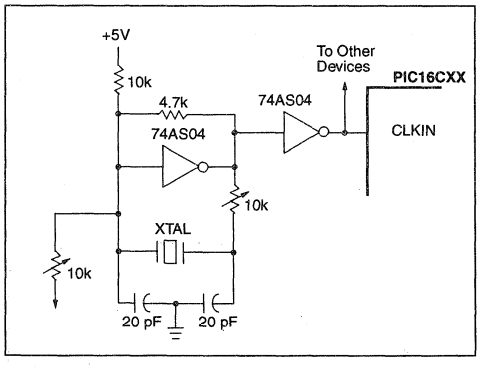
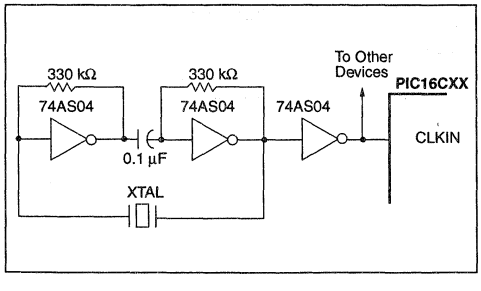


Figure 8-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 8-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



8.2.4 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) values, capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low Cext values. The user needs to take into account variation due to tolerance of the external R and C components. Figure 8-6 shows how an R/C combination is connected to the PIC16C84. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

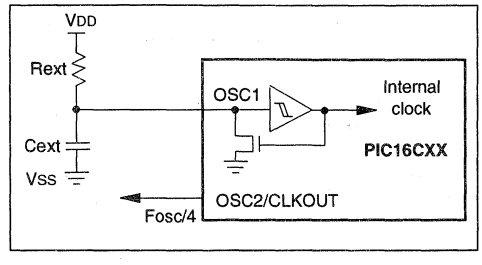
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With little or no external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See the electrical specification section for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance has a greater affect on RC frequency).

See the electrical specification section for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-2 for waveform).

FIGURE 8-6: RC OSCILLATOR MODE



Note: When the device oscillator is in RC mode, do not drive the OSC1 pin with an external clock or you may damage the device.

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8.3 Reset

The PIC16C84 differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{MCLR}$ reset during normal operation
- $\overline{MCLR}$ reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

Figure 8-7 shows a simplified block diagram of the on-chip reset circuit. The electrical specifications state the pulse width requirements for the $\overline{MCLR}$ pin.

Some registers are not affected in any reset condition; their status is unknown on a POR reset and unchanged in any other reset. Most other registers are reset to a "reset state" on POR, $\overline{MCLR}$ or WDT reset during normal operation and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation.

Table 8-3 gives a description of reset conditions for the program counter (PC) and the STATUS register. Table 8-4 gives a full description of reset states for all registers.

The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations (Section 8.7). These bits are used in software to determine the nature of the reset.

FIGURE 8-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

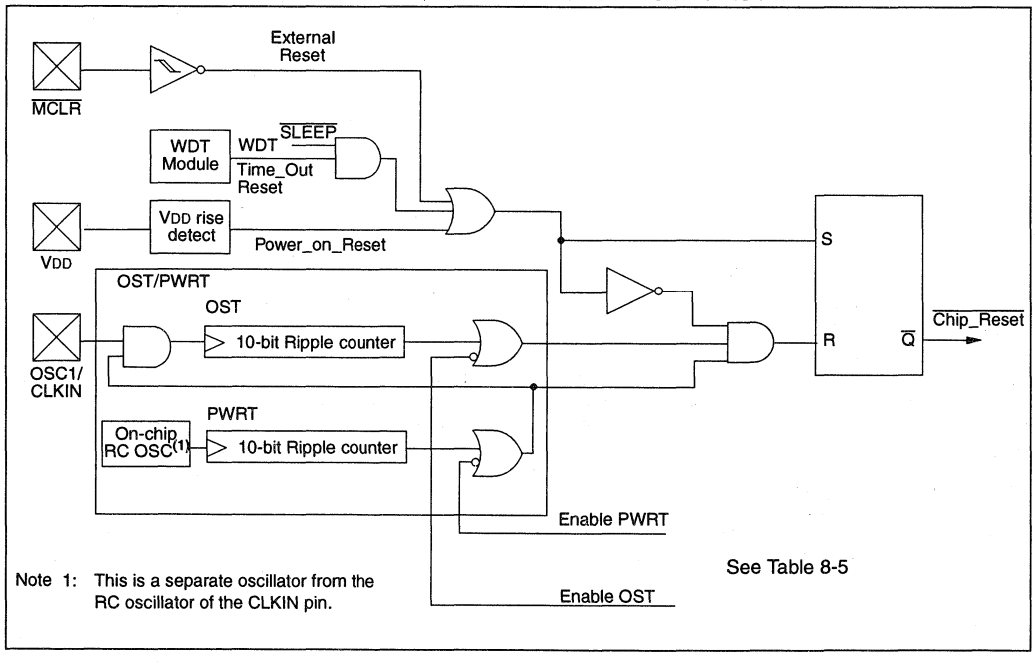

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TABLE 8-3: RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1 (1)	uuu1 0uuu

Legend: u = unchanged, x = unknown.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 8-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	$\overline{MCLR}$ Reset during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1 (2)
STATUS	03h	0001 1xxx	000q quuu (3)	uuuq quuu (3)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---x xxxx	---u uuuu	---u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu (1)
INDF	80h	---- ----	---- ----	---- ----
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000q quuu (3)	uuuq quuu (3)
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu (1)

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.
Note 1: One or more bits in INTCON will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: Table 8-3 lists the reset value for each specific condition.

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8.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting.*"

The POR circuit does not produce an internal reset when VDD declines.

8.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out (TPWRT) from POR (Figure 8-9, Figure 8-10, Figure 8-11 and Figure 8-12). The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level (Possible exception shown in Figure 8-12).

A configuration bit, PWRTE, can enable/disable the PWRT (Figure 8-1).

The power-up time delay TPWRT will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

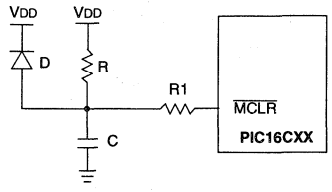
8.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 8-9, Figure 8-10, Figure 8-11 and Figure 8-12). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this case (Figure 8-12), an external power-on reset circuit may be necessary (Figure 8-8).

FIGURE 8-8: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if VDD power-up rate is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{MCLR}$ pin is 5 μA). A larger voltage drop will degrade VIH level on the $\overline{MCLR}$ pin.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of an $\overline{MCLR}$ pin breakdown due to ESD or EOS.

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FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): CASE 1

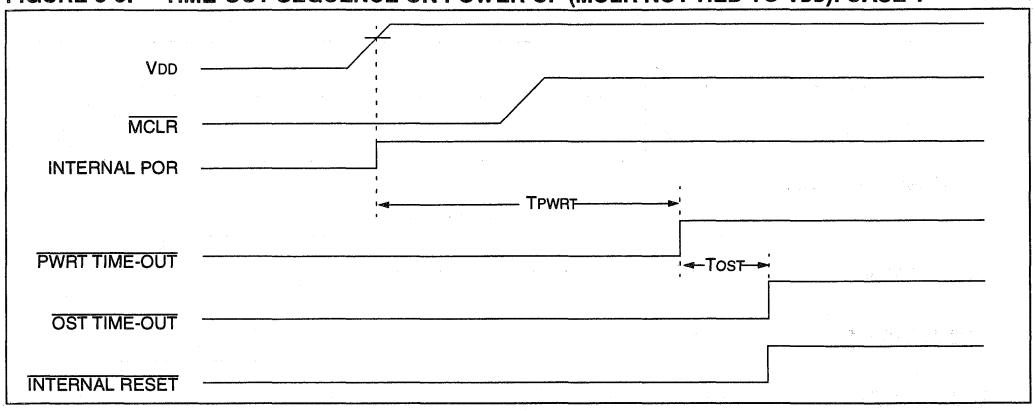

FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): CASE 2

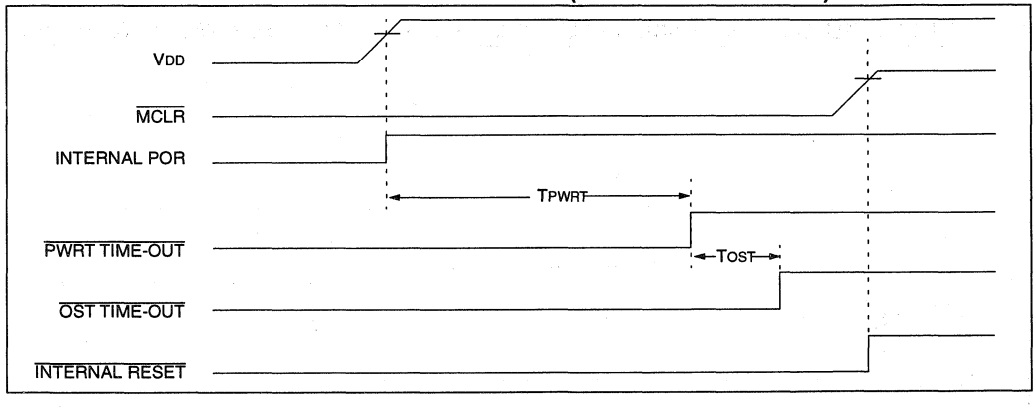

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FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME

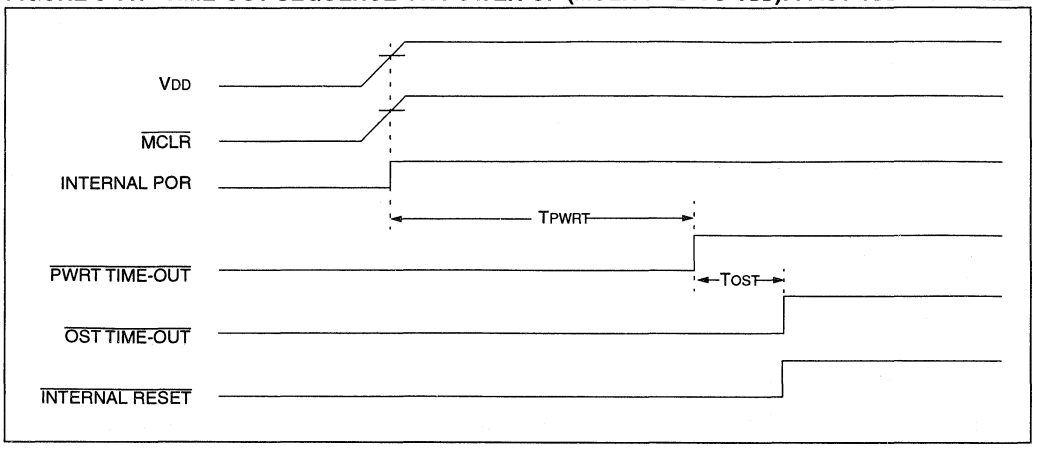
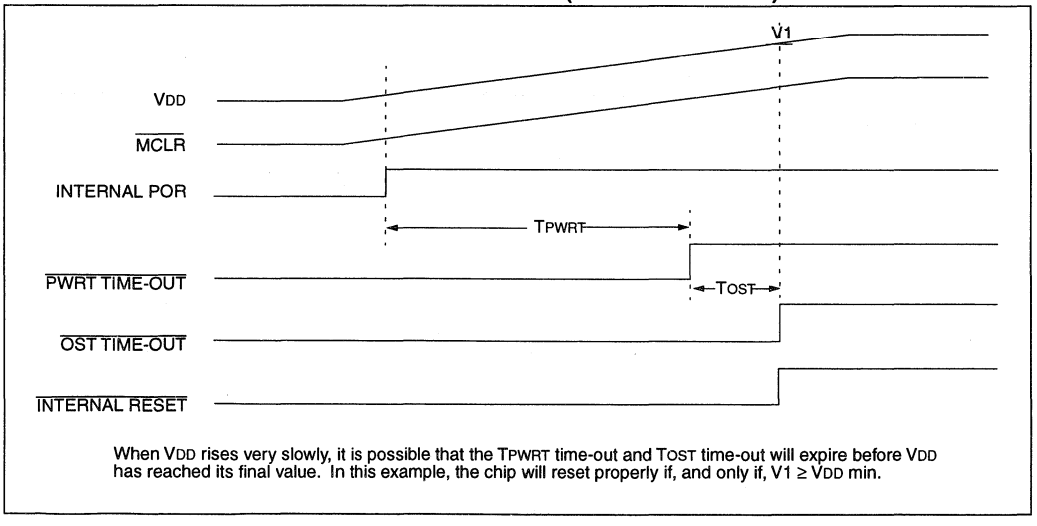


FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME



When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ VDD min.

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8.7 Time-out Sequence and Power Down Status Bits (TO/PD)

On power-up (Figure 8-9, Figure 8-10, Figure 8-11 and Figure 8-12) the time-out sequence is as follows: First PWRT time-out is invoked after a POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and PWRTE configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

TABLE 8-5: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	PWRT Disabled	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	1024Tosc
RC	72 ms	—	—

Since the time-outs occur from the POR reset pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high, execution will begin immediately (Figure 8-9). This is useful for testing purposes or to synchronize more than one PIC16CXX device when operating in parallel.

Table 8-6 shows the significance of the $\overline{TO}$ and $\overline{PD}$ bits. Table 8-3 lists the reset conditions for some special registers, while Table 8-4 lists the reset conditions for all the registers.

TABLE 8-6: STATUS BITS AND THEIR SIGNIFICANCE

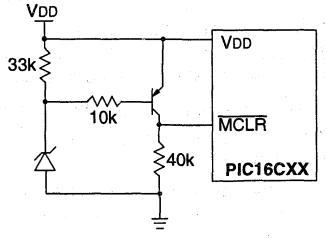
$\overline{TO}$	$\overline{PD}$	Condition
1	1	Power-on Reset
0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	$\overline{MCLR}$ Reset during normal operation
1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

8.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

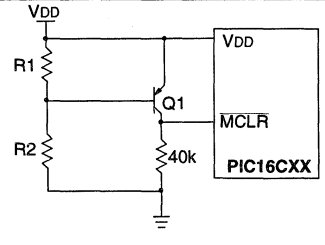
To reset PIC16C84 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-13 and Figure 8-14.

FIGURE 8-13: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

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8.9 Interrupts

The PIC16C84 has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits.

The global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on reset.

The "return from interrupt" instruction, `RETFIE`, exits interrupt routine as well as sets the GIE bit, which re-enable interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to; the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 8-16). The latency is the same for both one and two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note 2: If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the `RETFIE` instruction). The events that would cause this to occur are:

1. An instruction clears the GIE bit while an interrupt is acknowledged
2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the `RETFIE` instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GIE bit is cleared by the instruction, as shown in the following code:

```
LOOP   BCF    INTCON,GIE   ;Disable All
                            ;  Interrupts
       BTFSC  INTCON,GIE   ;All Interrupts
                            ;  Disabled?
       GOTO   LOOP          ;NO, try again
                            ;  Yes, continue
                            ;  with program
                            ;  flow
```


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FIGURE 8-15: INTERRUPT LOGIC

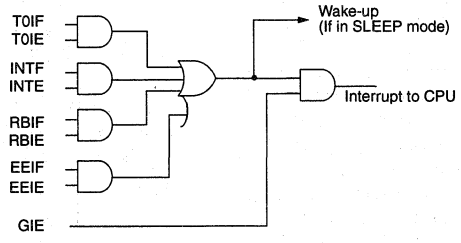
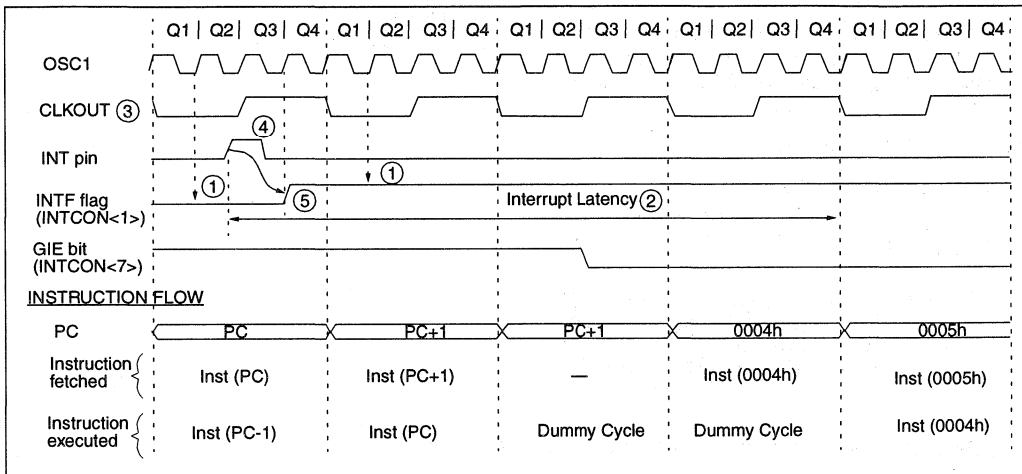


FIGURE 8-16: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4Tcy where Tcy = instruction cycle time.
Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

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8.9.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP (Section 8.12) only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

8.9.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in TMR0 will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 6.0).

8.9.3 PORT RB INTERRUPT

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) (Section 5.2).

Note 1: If a change on an I/O pin should occur when a read operation of PORTB is being executed (start of the Q2 cycle), the RBIF interrupt flag bit may not get set.

8.10 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software.

Example 8-1 stores and restores the STATUS and W register's values. The User defined registers, W_TEMP and STATUS_TEMP are the temporary storage locations for the W and STATUS registers values.

Example 8-1 does the following:

a) Stores the W register.
b) Stores the STATUS register in STATUS_TEMP.
c) Executes the Interrupt Service Routine code.
d) Restores the STATUS (and bank select bit) register.
e) Restores the W register.

EXAMPLE 8-1: SAVING STATUS AND W REGISTERS IN RAM

```
PUSH    MOVWF   W_TEMP          ; Copy W to TEMP register,
        SWAPF   STATUS, W       ; Swap status to be saved into W
        MOVWF   STATUS_TEMP     ; Save status to STATUS_TEMP register
ISR     :                       :
        :                       ; Interrupt Service Routine
        :                       ;  should configure Bank as required
        :                       ;
POP     SWAPF   STATUS_TEMP, W  ; Swap nibbles in STATUS_TEMP register
                                ; and place result into W
        MOVWF   STATUS          ; Move W into STATUS register
                                ;   (sets bank to original state)
        SWAPF   W_TEMP, F       ; Swap nibbles in W_TEMP and place result in W_TEMP
        SWAPF   W_TEMP, W       ; Swap nibbles in W_TEMP and place result into W
```


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8.11 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT Wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit WDTE as a '0' (Section 8.1).

8.11.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

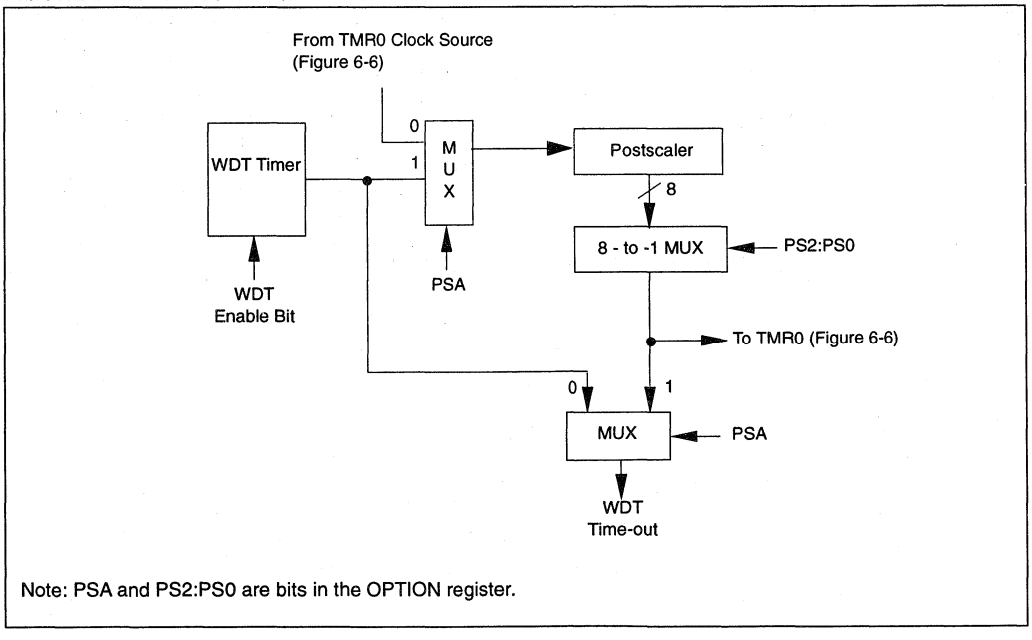
The CLRWDT and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a WDT time-out.

8.11.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 8-17: WATCHDOG TIMER BLOCK DIAGRAM



Note: PSA and PS2:PS0 are bits in the OPTION register.

TABLE 8-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
2007h	Config. bits	—	—	—	CP	PWRTE	WDTE	FOSC1	FOSC0		
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.

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8.12 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

8.12.1 SLEEP

The Power-down mode is entered by executing the SLEEP instruction.

If enabled, the Watchdog Timer is cleared (but keeps running), the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ bit (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For the lowest current consumption in SLEEP mode, place all I/O pins at either at VDD or VSS, with no external circuitry drawing current from the I/O pins, and disable external clocks. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

8.12.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

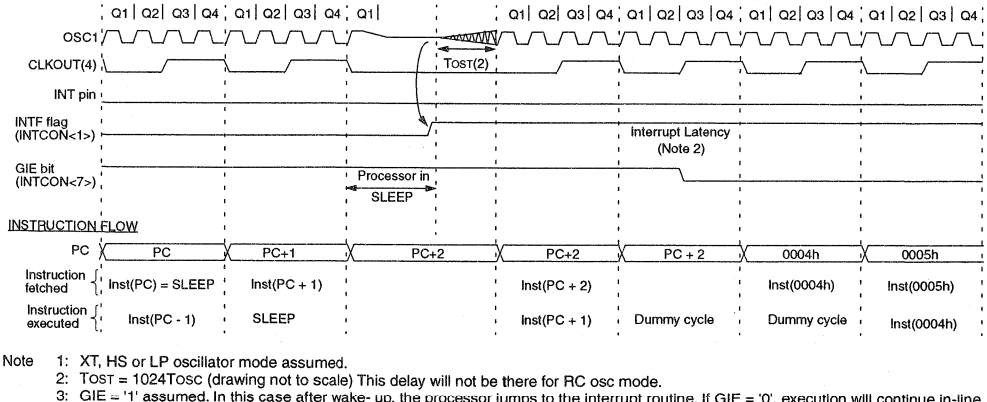
1. External reset input on $\overline{MCLR}$ pin.
2. WDT Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or data EEPROM write complete.

Peripherals cannot generate interrupts during SLEEP, since no on-chip Q clocks are present.

The first event ($\overline{MCLR}$ reset) will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of a device reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

While the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

FIGURE 8-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

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8.12.3 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep . The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

8.13 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices..

8.14 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations to store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable only during program/verify. Only the 4 least significant bits of ID location are usable.

For ROM devices, these values are submitted along with the ROM code.

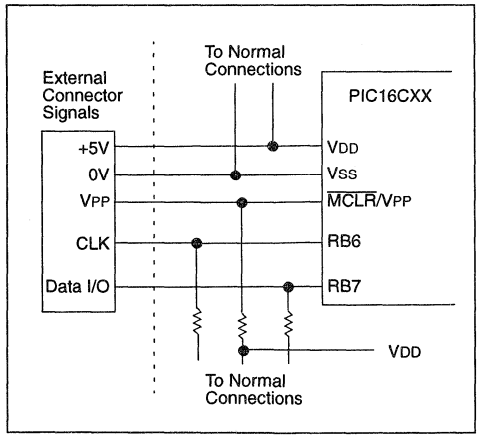
8.15 In-Circuit Serial Programming

PIC16C84 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. Customers can manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product, allowing the most recent firmware or custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low, while raising the $\overline{MCLR}$ pin from V_{IL} to V_{IHH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) points to location 00h. A 6-bit command is then supplied to the device, 14-bits of program data is then supplied to or from the device, using load or read-type instructions. For complete details of serial programming, please refer to the PIC16CXX Programming Specifications (Literature #DS30189).

FIGURE 8-19: TYPICAL IN-SYSTEM SERIAL PROGRAMMING CONNECTION



For ROM devices, both the program memory and Data EEPROM memory may be read, but only the Data EEPROM memory may be programmed.

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NOTES:

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9.0 ELECTRICAL CHARACTERISTICS FOR PIC16C84

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS}(2) ..... -0.3 to +14V
Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)
Total power dissipation(1) ..... 800 mW
Maximum current out of V_{SS} pin ..... 150 mA
Maximum current into V_{DD} pin ..... 100 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 20 mA
Maximum current sunk by PORTA ..... 80 mA
Maximum current sourced by PORTA ..... 50 mA
Maximum current sunk by PORTB ..... 150 mA
Maximum current sourced by PORTB ..... 100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 9-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C84-04	PIC16C84-10	PIC16LC84-04
RC	V_{DD}: 4.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 100 µA max. at 4.0V WDT dis Freq: 4.0 MHz max.	V_{DD}: 4.5V to 5.5V I_{DD}: 1.8 mA typ. at 5.5V I_{PD}: 40.0 µA typ. at 4.5V WDT dis Freq: 4.0 MHz max.	V_{DD}: 2.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 100 µA max. at 4V WDT dis Freq: 2.0 MHz max.
XT	V_{DD}: 4.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 100 µA max. at 4.0V WDT dis Freq: 4.0 MHz max.	V_{DD}: 4.5V to 5.5V I_{DD}: 1.8 mA typ. at 5.5V I_{PD}: 40.0 µA typ. at 4.5V WDT dis Freq: 4.0 MHz max.	V_{DD}: 2.0V to 6.0V I_{DD}: 4.5 mA max. at 5.5V I_{PD}: 100 µA max. at 4V WDT dis Freq: 2.0 MHz max.
HS	V_{DD}: 4.5V to 5.5V I_{DD}: 4.5 mA typ. at 5.5V I_{PD}: 40.0 µA typ. at 4.5V WDT dis Freq: 4.0 MHz max.	V_{DD}: 4.5V to 5.5V I_{DD}: 10 mA max. at 5.5V typ. I_{PD}: 40.0 µA typ. at 4.5V WDT dis Freq: 10 MHz max.	Do not use in HS mode
LP	V_{DD}: 4.0V to 6.0V I_{DD}: 60 µA typ. at 32 kHz, 2.0V I_{PD}: 26 µA typ. at 2.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	V_{DD}: 2.0V to 6.0V I_{DD}: 400 µA max. at 32 kHz, 2.0V I_{PD}: 100 µA max. at 4.0V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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9.1 DC CHARACTERISTICS: PIC16C84-04 (Commercial, Industrial) PIC16C84-10 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	4.0	—	6.0	V	XT, RC and LP osc configuration
D001A			4.5	—	5.5	V	HS osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current (2)					RC and XT osc configuration(4)
D010			—	1.8	4.5	mA	FOSC = 4 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 4 MHz, VDD = 5.5V (During EEPROM programming)
D013			—	5.0	10	mA	HS osc configuration (PIC16C84-10) FOSC = 10 MHz, VDD = 5.5V
D020	IPD	Power-down Current(3)	—	40	100	µA	VDD = 4.0V, WDT enabled, industrial
D021			—	38	100	µA	VDD = 4.0V, WDT disabled, commercial
D021A			—	38	100	µA	VDD = 4.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

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9.2 DC CHARACTERISTICS: PIC16LC84-04 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.0	—	6.0	V	XT, RC, and LP osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current(2)					RC and XT osc configuration(4)
D010			—	1	4	mA	FOSC = 2 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 2 MHz, VDD = 5.5V (During EEPROM programming)
							LP osc configuration
D014			—	60	400	µA	FOSC = 32 kHz, VDD = 2.0V WDT disabled
D020	IPD	Power-down Current(3)	—	26	100	µA	VDD = 2.0V, WDT enabled, industrial
D021			—	26	100	µA	VDD = 2.0V, WDT disabled, commercial
D021A			—	26	100	µA	VDD = 2.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

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9.3 DC CHARACTERISTICS: PIC16C84-04 (Commercial, Industrial)
PIC16C84-10 (Commercial, Industrial)
PIC16LC84-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 9-1 and Section 9.2.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage** I/O ports					
D030		with TTL buffer	VSS	—	0.8	V	4.5 ≤ VDD ≤ 5.5V
D030A			VSS	—	0.16VDD	V	entire range(4)
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	entire range
D032		MCLR, RA4/T0CKI, OSC1 (RC mode)	Vss	—	0.2VDD	V	
D033		OSC1 (XT, HS and LP modes)(1)	Vss	—	0.3VDD	V	
	VIH	**Input High Voltage** I/O ports					
D040		with TTL buffer	0.36VDD	—	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.48VDD				entire range(4)
D041		with Schmitt Trigger buffer	0.45VDD	—	VDD		entire range
D042		MCLR, RA4/T0CKI, OSC1 (RC mode)	0.85VDD	—	VDD	V	
D043		OSC1 (XT, HS and LP modes)(1)	0.7VDD	—	VDD	V	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	TBD	—	—	V	
D070	IPURB	PORTB weak pull-up current	50*	250*	400*	µA	VDD = 5V, VPIN = VSS
	IIL	**Input Leakage Current(2,3)** I/O ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		MCLR, RA4/T0CKI	—	—	±5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1/CLKIN	—	—	±5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
D083		OSC2/CLKOUT (RC osc configuration)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V
	VOH	**Output High Voltage**					
D090		I/O ports(3)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D093		OSC2/CLKOUT (RC osc configuration)	VDD - 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C84 be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may use better of the two specs.

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9.4 DC CHARACTERISTICS: PIC16C84-04 (Commercial, Industrial) PIC16C84-10 (Commercial, Industrial) PIC16LC84-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 9-1 and Section 9.2.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2/CLKOUT pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
		Data EEPROM Memory					
D120	ED	Endurance	1M	10M	—	E/W	25°C at 5V
D121	VDRW	VDD for read/write	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time(1)	—	—	10	ms	
		Program EEPROM Memory					
D130	EP	Endurance	100	1000	—	E/W	
D131	VPR	VDD for read	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for erase/write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time(1)	—	10	—	ms	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The user should use interrupts or poll the EEIF or WR bits to ensure the write cycle has completed.

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TABLE 9-2: TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

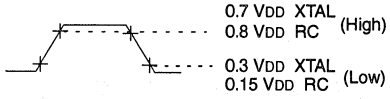
Lowercase symbols (pp) and their meanings:

pp			
2	to	os,osc	OSC1
ck	CLKOUT	ost	oscillator start-up timer
cy	cycle time	pwrt	power-up timer
io	I/O port	rbt	RBx pins
inp	INT pin	t0	T0CKI
mc	$\overline{MCLR}$	wdt	watchdog timer

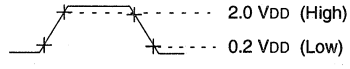
Uppercase symbols and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 9-1: PARAMETER MEASUREMENT INFORMATION



OSC1 Measurement Points

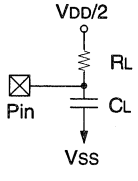


I/O Port Measurement Points

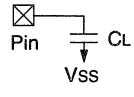
All timings are measured between high and low measurement points as indicated in the figure.

FIGURE 9-2: LOAD CONDITIONS

Load Condition 1



Load Condition 2



RL = 464Ω

CL = 50 pF for all pins except OSC2.

15 pF for OSC2 output.

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9.5 Timing Diagrams and Specifications

FIGURE 9-3: EXTERNAL CLOCK TIMING

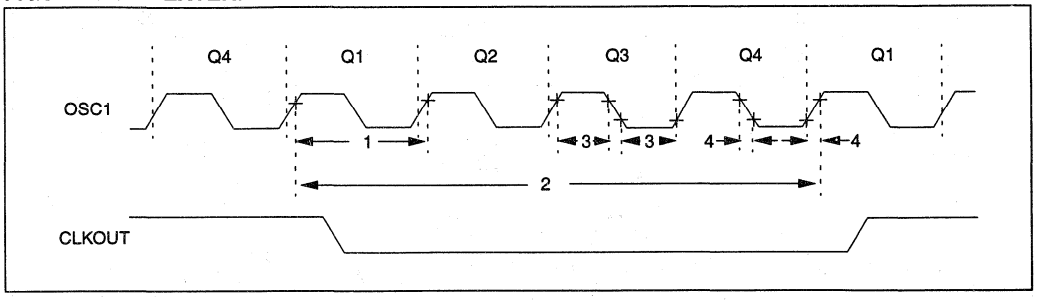

TABLE 9-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
	FOSC	**External CLKIN Frequency(1)**	DC	—	2	MHz	XT, RC osc	PIC16LC84-04
			DC	—	4	MHz	XT, RC osc	PIC16C84-04
			DC	—	10	MHz	HS osc	PIC16C84-10
			DC	—	200	kHz	LP osc	PIC16LC84-04
		Oscillator Frequency(1)	DC	—	2	MHz	RC osc	PIC16LC84-04
			DC	—	4	MHz	RC osc	PIC16C84-04
			0.1	—	2	MHz	XT osc	PIC16LC84-04
			0.1	—	4	MHz	XT osc	PIC16C84-04
			1	—	10	MHz	HS osc	PIC16C84-10
			DC	—	200	kHz	LP osc	PIC16LC84-04
1	TOSC	**External CLKIN Period(1)**	500	—	—	ns	XT, RC osc	PIC16LC84-04
			250	—	—	ns	XT, RC osc	PIC16C84-04
			100	—	—	ns	HS osc	PIC16C84-10
			5	—	—	µs	LP osc	PIC16LC84-04
		Oscillator Period(1)	500	—	—	ns	RC osc	PIC16LC84-04
			250	—	—	ns	RC osc	PIC16C84-04
			500	—	10,000	ns	XT osc	PIC16LC84-04
			250	—	10,000	ns	XT osc	PIC16C84-04
			100	—	1,000	ns	HS osc	PIC16C84-10
			5	—	—	µs	LP osc	PIC16LC84-04
2	TCY	**Instruction Cycle Time(1)**	0.4	4/Fosc	DC	µs		
3	TosL, TosH	**Clock in (OSC1) High or Low Time**	60 *	—	—	ns	XT osc	PIC16LC84-04
			50 *	—	—	ns	XT osc	PIC16C84-04
			2 *	—	—	µs	LP osc	PIC16LC84-04
			35 *	—	—	ns	HS osc	PIC16C84-10
4	TosR, TosF	**Clock in (OSC1) Rise or Fall Time**	25 *	—	—	ns	XT osc	PIC16C84-04
			50 *	—	—	ns	LP osc	PIC16LC84-04
			15 *	—	—	ns	HS osc	PIC16C84-10

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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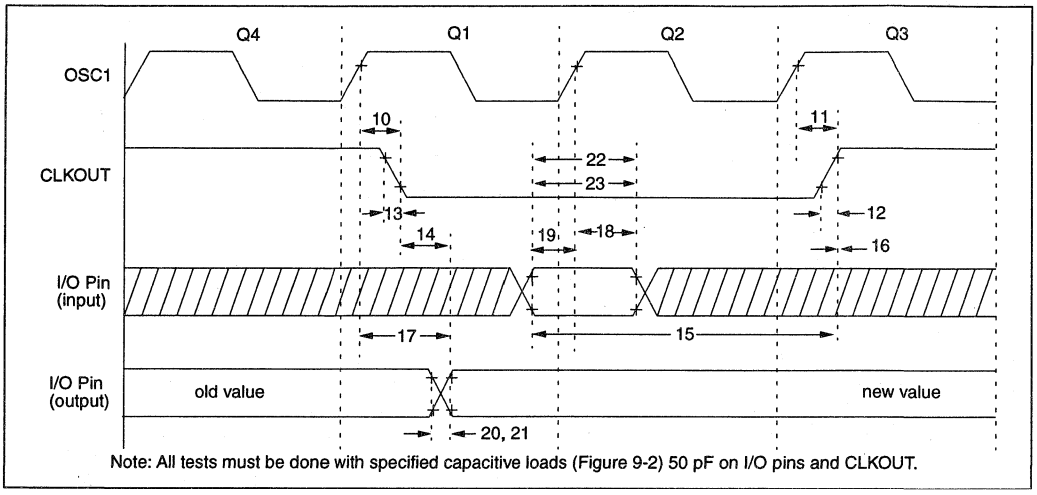
FIGURE 9-4: CLKOUT AND I/O TIMING



Note: All tests must be done with specified capacitive loads (Figure 9-2) 50 pF on I/O pins and CLKOUT.

TABLE 9-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	PIC16C84	—	15	30 *	ns	Note 1
10A			PIC16LC84	—	15	120 *	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	PIC16C84	—	15	30 *	ns	Note 1
11A			PIC16LC84	—	15	120 *	ns	Note 1
12	TckR	CLKOUT rise time	PIC16C84	—	15	30 *	ns	Note 1
12A			PIC16LC84	—	15	100 *	ns	Note 1
13	TckF	CLKOUT fall time	PIC16C84	—	15	30 *	ns	Note 1
13A			PIC16LC84	—	15	100 *	ns	Note 1
14	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY +20 *	ns	Note 1
15	TioV2ckH	Port in valid before	PIC16C84	0.30TCY + 30 *	—	—	ns	Note 1
		CLKOUT ↑	PIC16LC84	0.30TCY + 80 *	—	—	ns	Note 1
16	TckH2iol	Port in hold after CLKOUT ↑		0 *	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to	PIC16C84	—	—	125 *	ns	
		Port out valid	PIC16LC84	—	—	250 *	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		TBD	—	—	ns	
20	TioR	Port output rise time	PIC16C84	—	10	25 *	ns	
20A			PIC16LC84	—	10	60 *	ns	
21	TioF	Port output fall time	PIC16C84	—	10	25 *	ns	
21A			PIC16LC84	—	10	60 *	ns	
22	Tinp	INT pin high	PIC16C84	20 *	—	—	ns	
22A		or low time	PIC16LC84	55 *	—	—	ns	
23	Trbp	RB7:RB4 change INT	PIC16C84	20 *	—	—	ns	
23A		high or low time	PIC16LC84	55 *	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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FIGURE 9-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

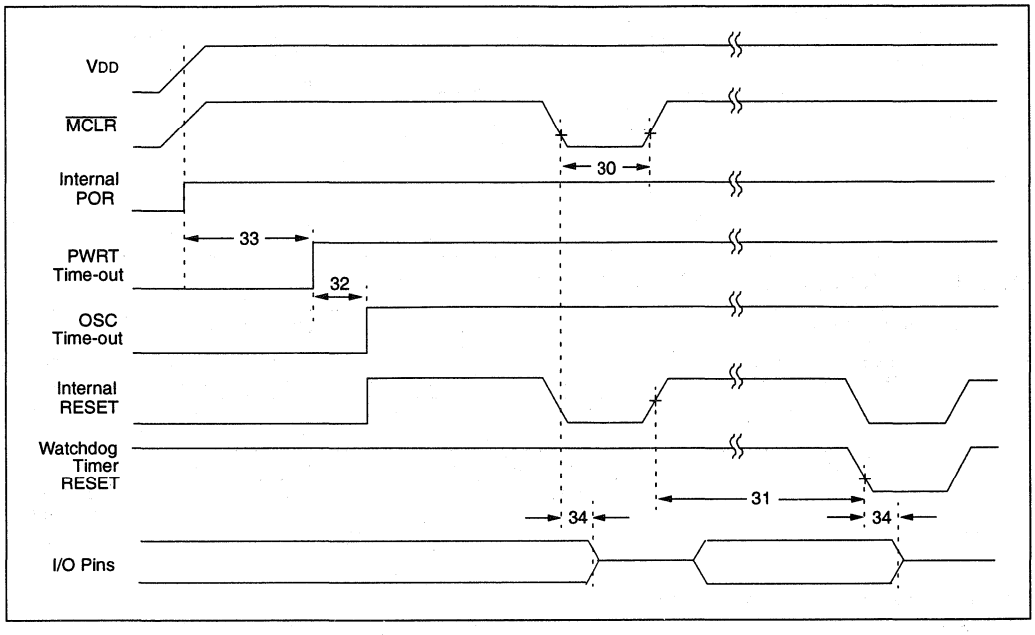

TABLE 9-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	350 * 150 *	— —	— —	ns ns	2.0V ≤ VDD ≤ 3.0V 3.0V ≤ VDD ≤ 6.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5V
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	ms	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or reset	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 9-6: TIMER0 CLOCK TIMINGS

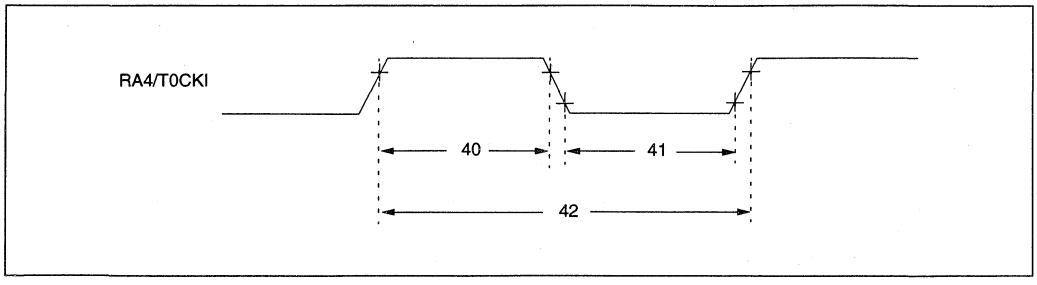

TABLE 9-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20 *	—	—	ns	
			With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				30 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20 *	—	—	ns	
			With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				20 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
42	Tt0P	T0CKI Period		TCY + 40 * / N	—	—	ns	N = prescale value (2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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10.0 DC & AC CHARACTERISTICS GRAPHS/TABLES FOR PIC16C84

The data graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while 'max' or 'Min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 10-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

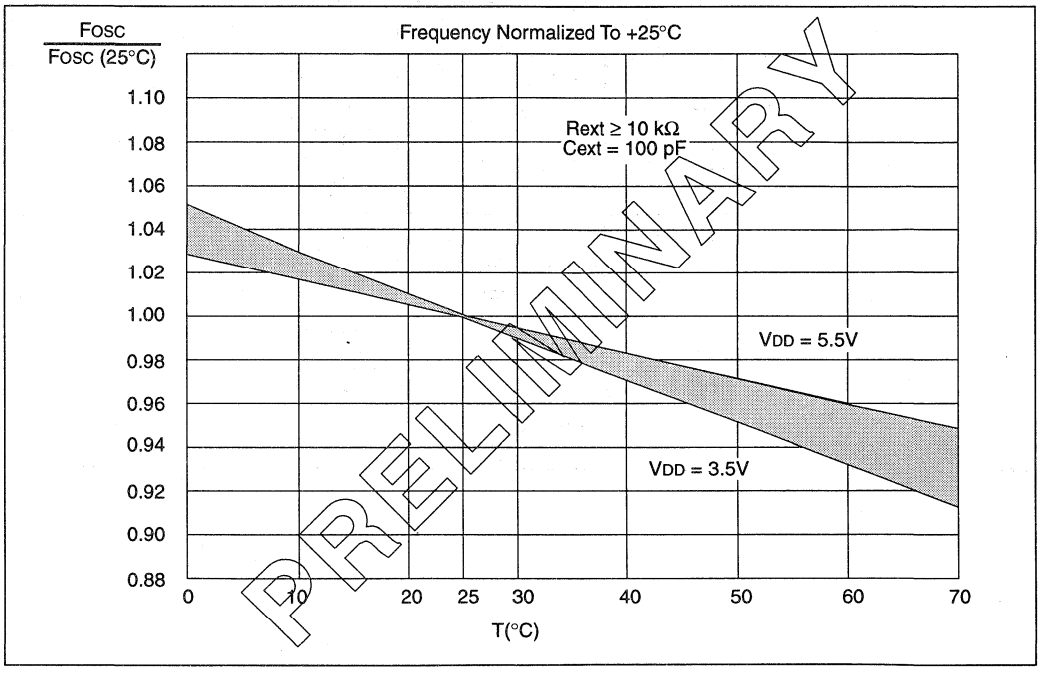

TABLE 10-1: RC OSCILLATOR FREQUENCIES *

Cext	Rext	Average Fosc @ 5V, 25°C	
20 pF	3.3k	4.68 MHz	± 27%
	5.1k	3.94 MHz	± 25%
	10k	2.34 MHz	± 29%
	100k	250.16 kHz	± 33%
100 pF	3.3k	1.49 MHz	± 25%
	5.1k	1.12 MHz	± 25%
	10k	620.31 kHz	± 30%
	100k	90.25 kHz	± 26%
300 pF	3.3k	524.24 kHz	± 28%
	5.1k	415.52 kHz	± 30%
	10k	270.33 kHz	± 26%
	100k	25.37 kHz	± 25%

*Measured in PDIP Packages.The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value.

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FIGURE 10-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD (Cext = 20 pF)

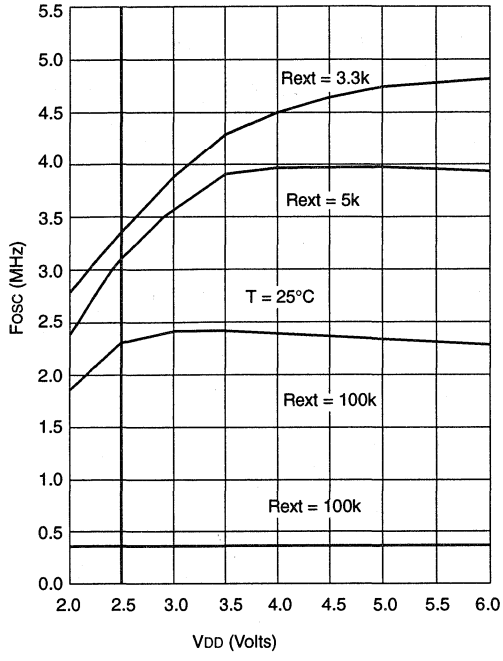

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FIGURE 10-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD (Cext = 100 pF)

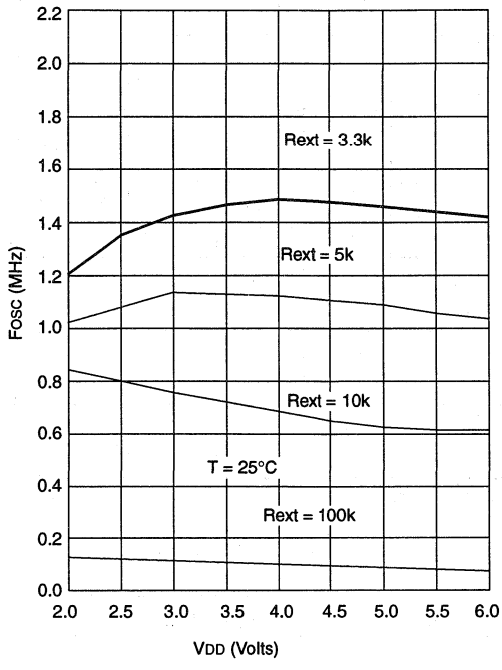

FIGURE 10-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD (Cext = 300 pF)

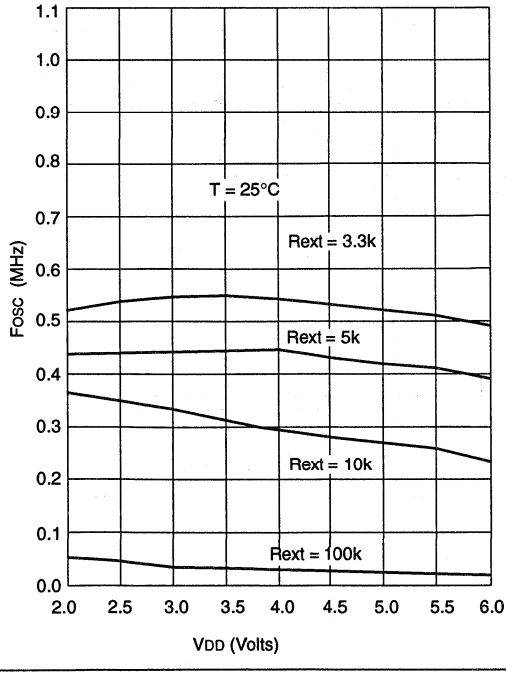

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FIGURE 10-5: TYPICAL I_{PD} vs. V_{DD} WATCHDOG DISABLED (25°C)

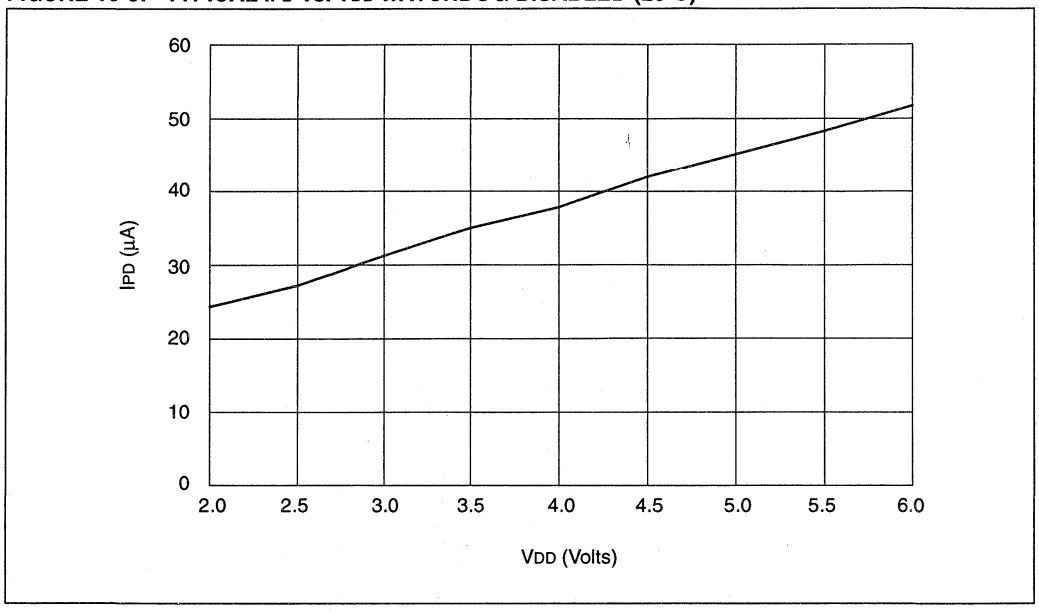

FIGURE 10-6: TYPICAL I_{PD} vs. V_{DD} WATCHDOG ENABLED (25°C)

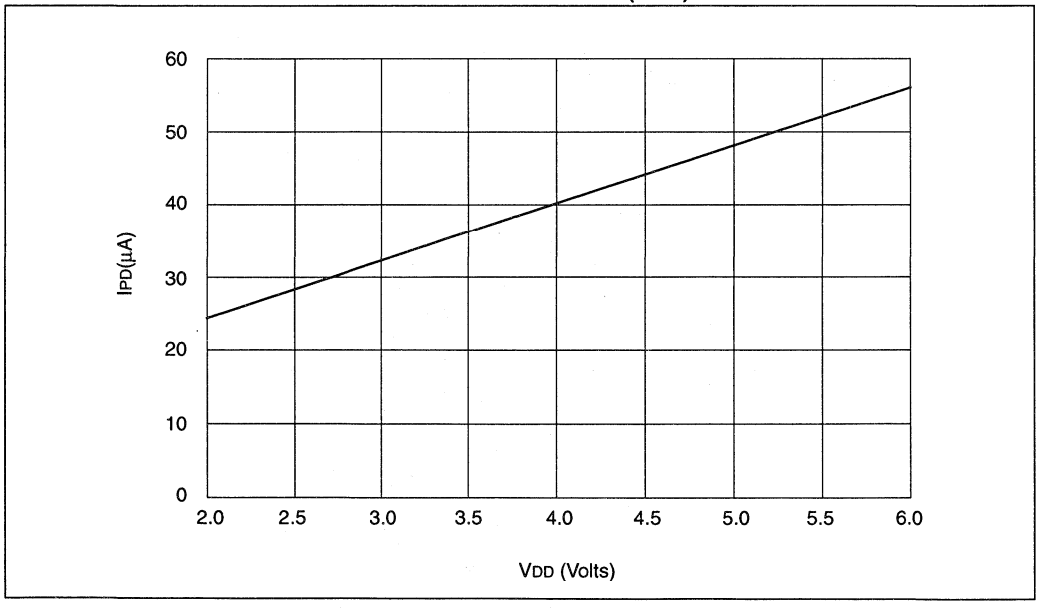

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FIGURE 10-7: MAXIMUM IPD vs. VDD WATCHDOG DISABLED

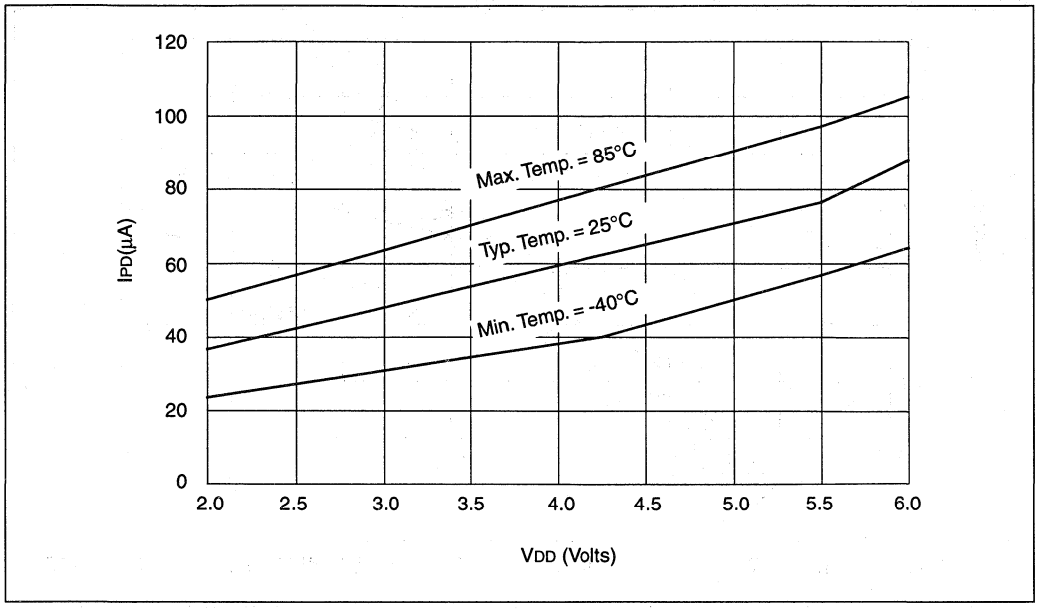
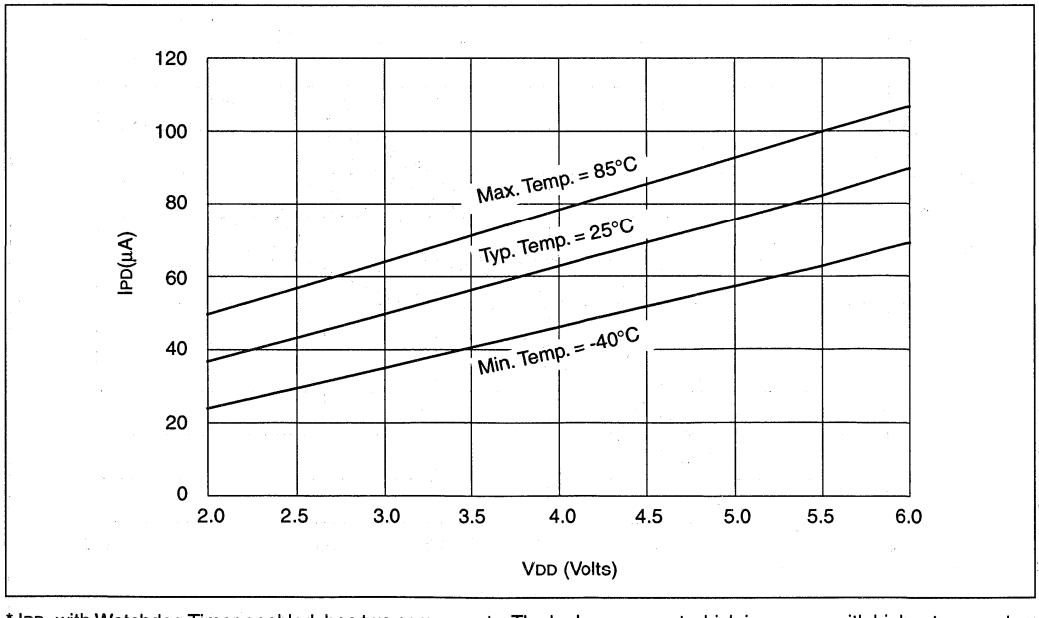


FIGURE 10-8: MAXIMUM IPD vs. VDD WATCHDOG ENABLED*



* IPD, with Watchdog Timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the Watchdog Timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

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FIGURE 10-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

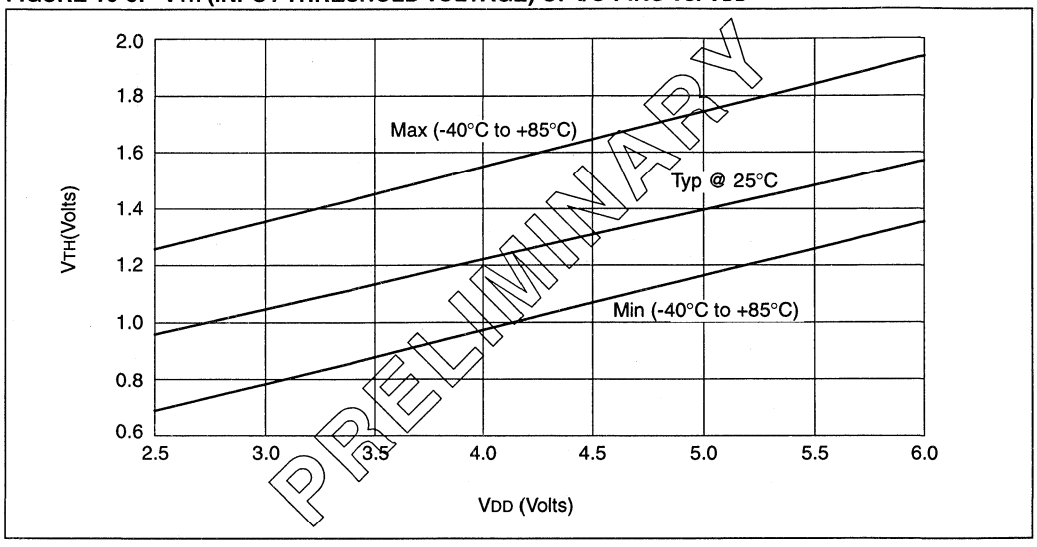

FIGURE 10-10: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD

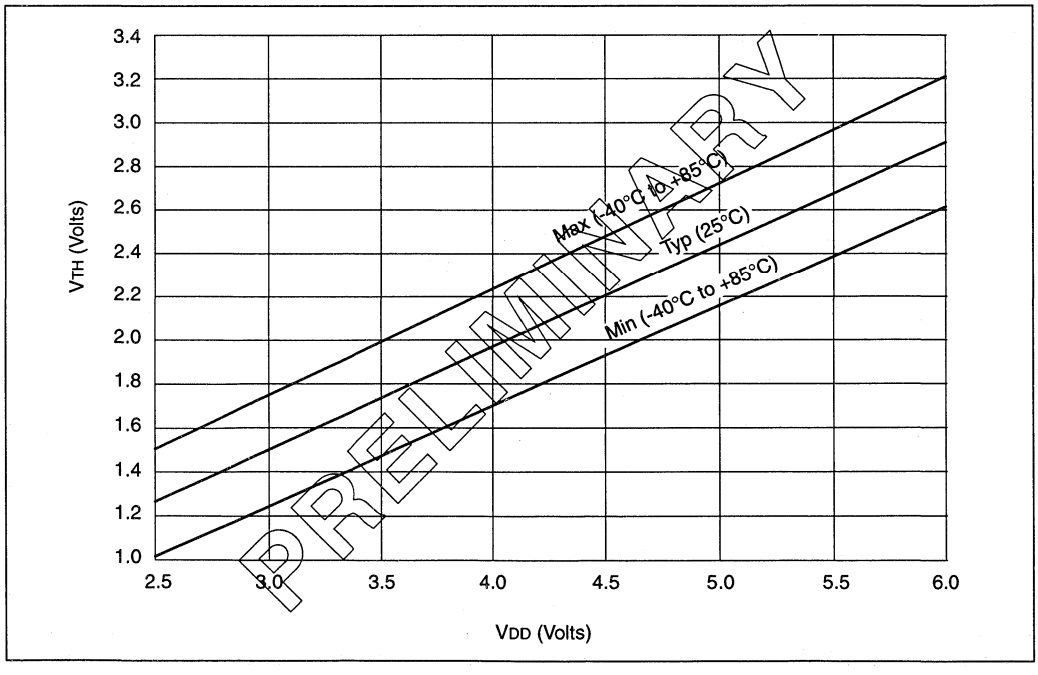

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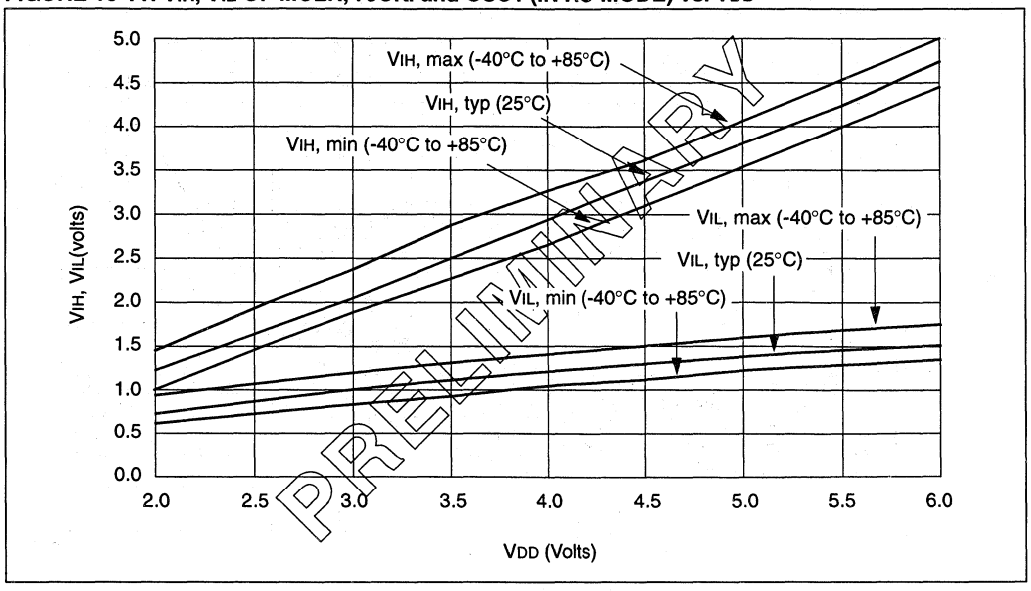
FIGURE 10-11: VIH, VIL OF $\overline{MCLR}$, T0CKI and OSC1 (IN RC MODE) vs. VDD



PRELIMINARY

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FIGURE 10-12: TYPICAL IDD vs. FREQ (EXT CLOCK, 25°C)

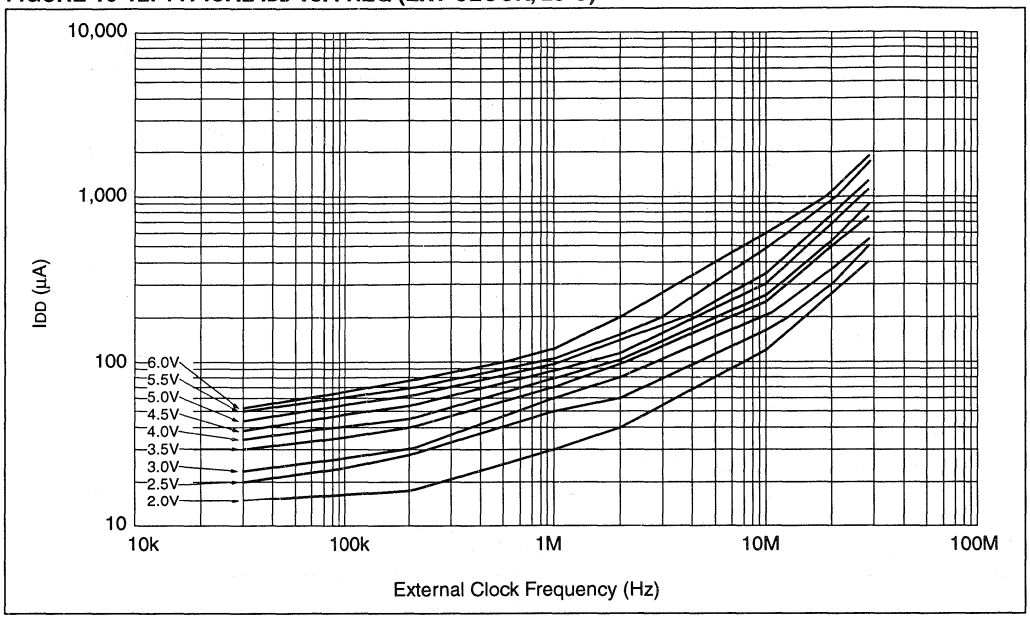

FIGURE 10-13: MAXIMUM IDD vs. FREQ (EXT CLOCK, -40° TO +85°C)

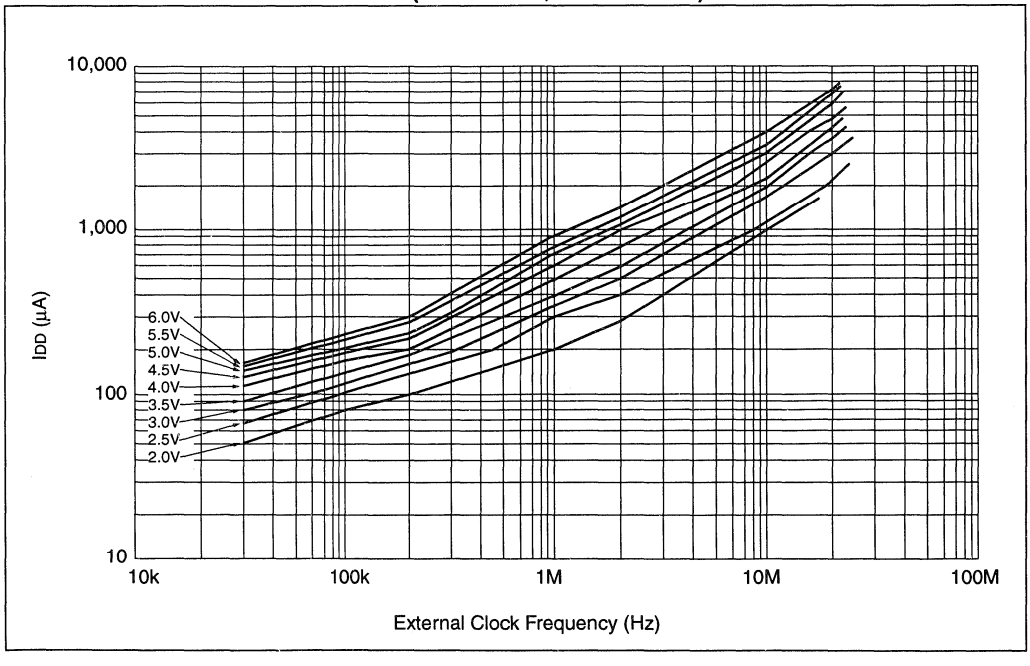

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FIGURE 10-14: WDT TIME-OUT PERIOD vs. VDD

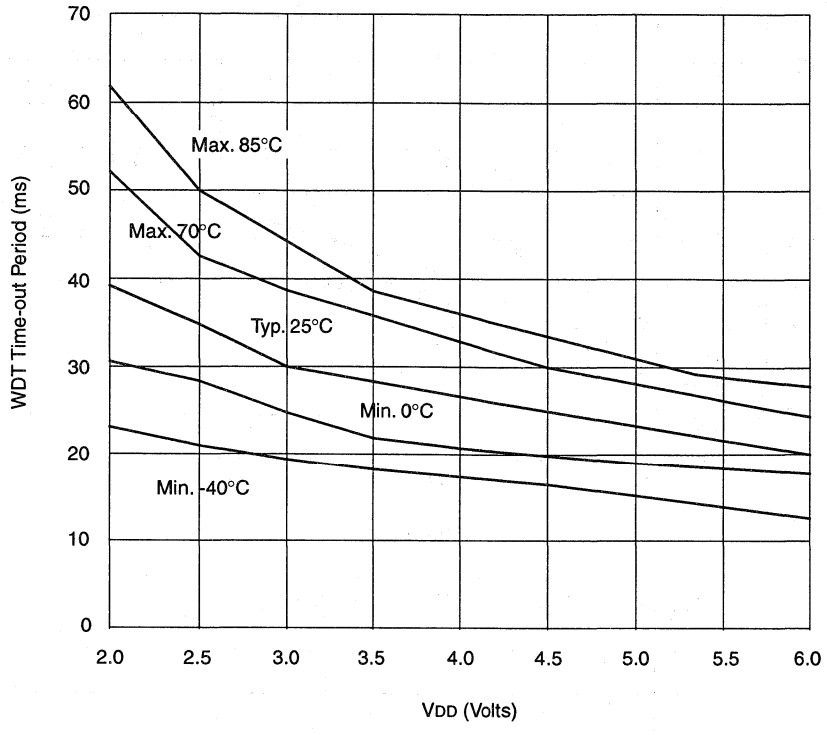

FIGURE 10-15: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

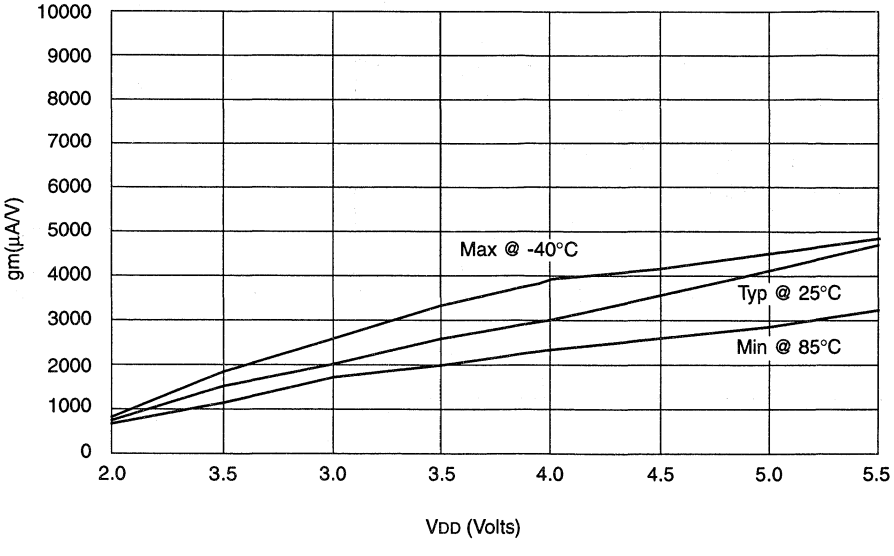

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FIGURE 10-16: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

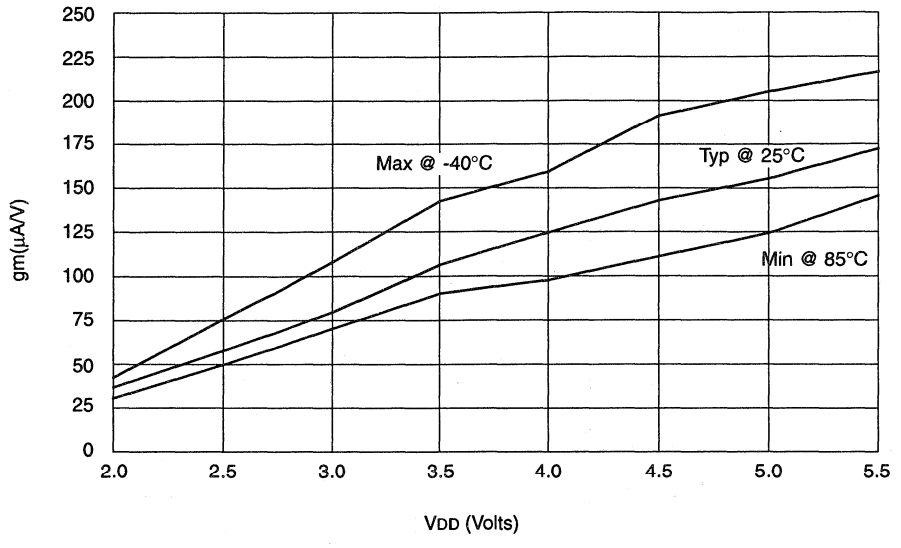

FIGURE 10-17: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

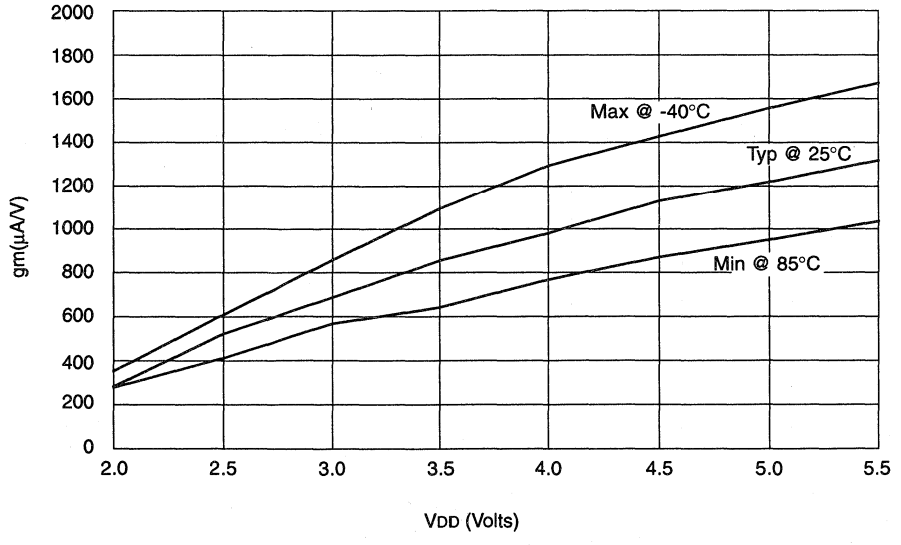

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FIGURE 10-18: IOH vs. VOH, VDD = 3V

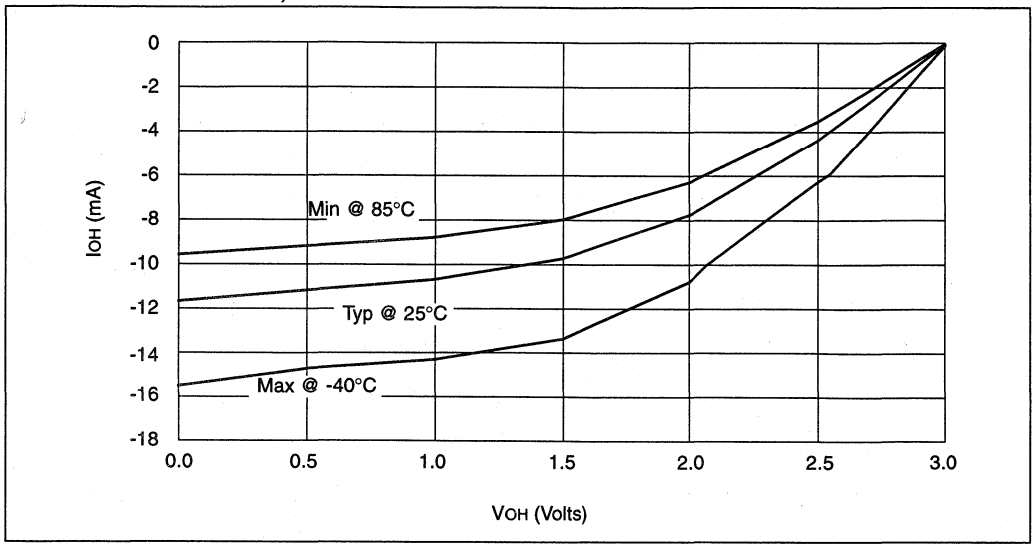

FIGURE 10-19: IOH vs. VOH, VDD = 5V

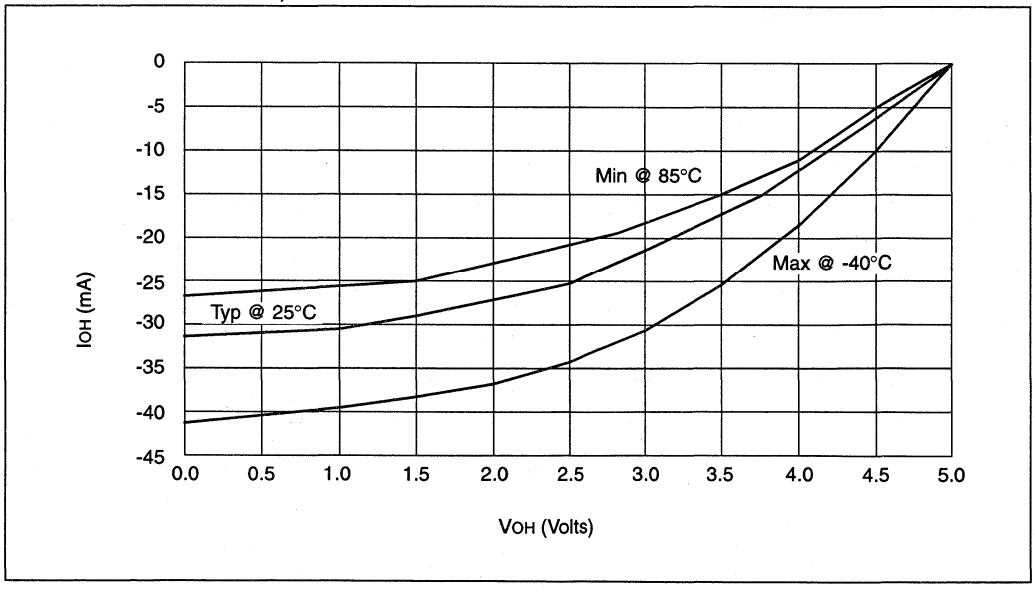

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FIGURE 10-20: IOL vs. VOL, VDD = 3V

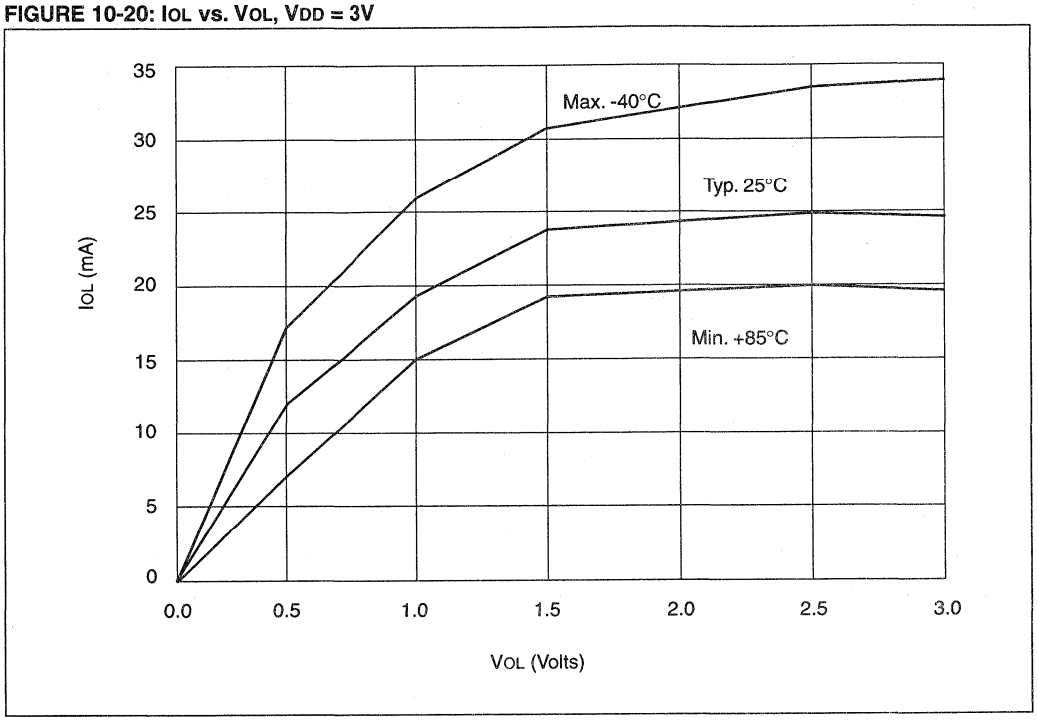

FIGURE 10-21: IOL vs. VOL, VDD = 5V

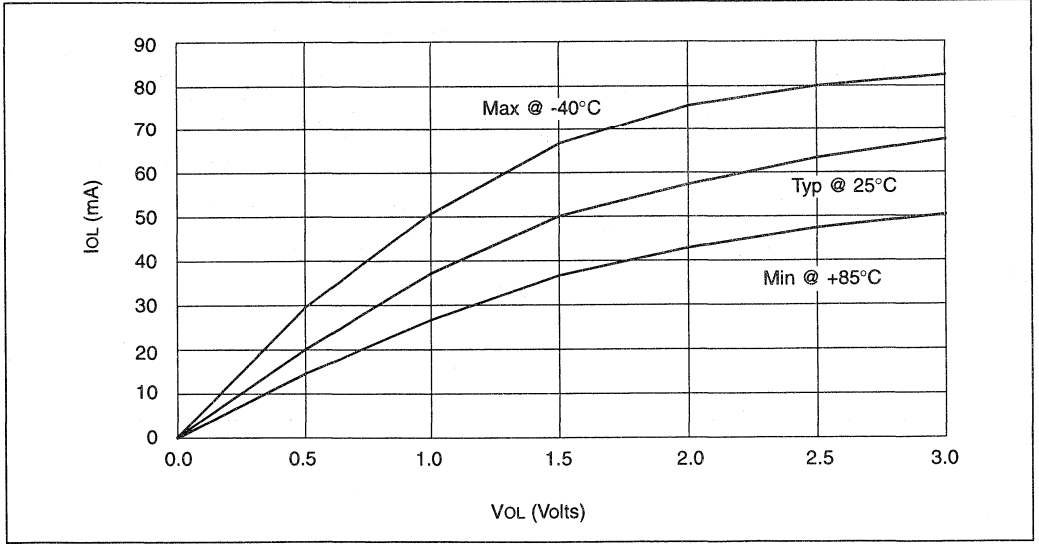

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TABLE 10-2: INPUT CAPACITANCE*

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
PORTA	5.0	4.3
PORTB	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1/CLKIN	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

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NOTES:

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APPENDIX A: FEATURE IMPROVEMENTS

The following is the list of feature improvements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and the register file (128 bytes now versus 32 bytes before).
2. A PC latch register (PCLATH) is added to handle program memory paging. PA2, PA1 and PA0 bits are removed from the status register and placed in the option register.
3. Data memory paging is redefined slightly. The STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions, TRIS and OPTION, are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, the Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change features.
13. T0CKI pin is also a port pin (RA4/T0CKI).
14. FSR is a full 8-bit register.
15. "In system programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16C84, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables for reallocation.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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APPENDIX C: WHAT'S NEW

No new information has been added to this data sheet.

For information on upgrade devices from the PIC16C84, please refer to the PIC16F8X data sheet.

APPENDIX D: WHAT'S CHANGED

Here's what's changed in this data sheet:

1. Some sections have been rearranged for clarity and consistency.
2. Time-out Sequence on Power-up figures in the Special Features of the CPU section have been updated.

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APPENDIX E: PIC16C84 TO PIC16F83/F84/CR83/ CR84 CONVERSION CONSIDERATIONS

This appendix discusses some of the issues that you may encounter as you convert your design from a PIC16C84 to any of the newly introduced devices. These new devices are:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84

Some of the issues that may be encountered are:

1. The polarity of the PWRTE configuration bit has been reversed. Ensure that the programmer has this bit correctly set before programming.
2. The PIC16F84 and PIC16CR84 have larger RAM sizes. Ensure that this does not cause an issue with your program.
3. The $\overline{\text{MCLR}}$ pin now has an on-chip filter. The input signal on the MCLR pin will require a longer low pulse to generate an interrupt.
4. Many electrical specifications have been improved. Compare the electrical specifications of the two devices to ensure that this will not cause a compatibility issue.

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NOTES:

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PIC16C84 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Frequency Range	Temperature Range	Package	Pattern

Device	PIC16C84[2], PIC16C84T[3] PIC16LC84[2], PIC16LC84T[3]	
Frequency Range	04 10	= 4 MHz = 10 MHz
Temperature Range	b[1] I	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial)
Package	P SO	= PDIP = SOIC (Gull Wing, 300 mil body)
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)	

Examples:

a) PIC16C84 -04/P 301 = Commercial temp., PDIP package, 4MHz, normal VDD limitis, QTP pattern #301.

b) PIC16LC84 - 04I/SO = Industrial temp., SOIC package, 200kHz, Extended VDD limits.

Note 1: b = blank
2: C = Standard VDD range
LC = Extended VDD range
3: T = in tape and reel - SOIC, SSOP packages only.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see last page)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Development Tools

For the latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302. The latest version of Development Tools software can be downloaded from either our Bulletin Board or Worldwide Web Site. (Information on how to connect to our BBS or WWW site can be found in the On-Line Support section of this data sheet.)

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MICROCHIP

PIC16F8X

8-Bit CMOS Flash/EEPROM Microcontrollers

Devices Included in this Data Sheet:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84
- Extended voltage range devices available (PIC16**LF**8X, PIC16**LCR**8X)

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single cycle (400 ns @ 10 MHz) except for program branches which are two-cycle
- Operating speed: DC - 10 MHz clock input
  DC - 400 ns instruction cycle

Device	Memory			Freq Max.
	Flash	Data RAM	Data EEPROM	
PIC16F83	512 words	36	64	10 MHz
PIC16CR83	512 words	36	64	10 MHz
PIC16F84	1 K-words	68	64	10 MHz
PIC16CR84	1 K-words	68	64	10 MHz

F = Flash; CR = ROM

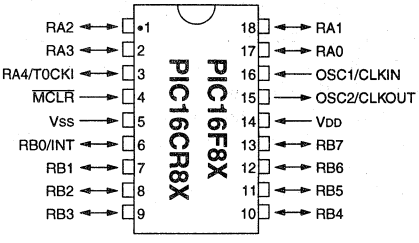
- 14-bit wide instructions
- 8-bit wide data path
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt on change
  - Data EEPROM write complete
- 1,000,000 data memory EEPROM ERASE/WRITE cycles
- EEPROM Data Retention > 40 years

Peripheral Features:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 20 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Pin Diagram

PDIP, SOIC



Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial In-System Programming - via two pins (ROM devices support only Data EEPROM programming)

CMOS Technology:

- Low-power, high-speed CMOS Flash/EEPROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 6.0V
  - Industrial: 2.0V to 6.0V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 1 µA typical standby current @ 2V

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1.0 GENERAL DESCRIPTION

The PIC16F8X is a group in the PIC16CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers. This group contains the following devices:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84

All PIC16/17 microcontrollers employ an advanced RISC architecture. PIC16CXX devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with a separate 8-bit wide data bus. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set is used to achieve a very high performance level.

PIC16F8X microcontrollers typically achieve a 2:1 code compression and up to a 2:1 speed improvement (at 10 MHz) over other 8-bit microcontrollers in their class.

The PIC16F8X has up to 68 bytes of RAM, 64 bytes of Data EEPROM memory, and 13 I/O pins. A timer/counter is also available.

The PIC16CXX family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake the chip from sleep through several external and internal interrupts and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

The devices with Flash program memory allow the same device package to be used for prototyping and production. In-circuit reprogrammability allows the code to be updated without the device being removed from the end application. This is useful in the development of many applications where the device may not be easily accessible, but the prototypes may require code updates. This is also useful for remote applications where the code may need to be updated (such as rate information).

Table 1-1 lists the features of the PIC16F8X, and Appendix D: list the features of all of the Microchip microcontrollers.

A simplified block diagram of the PIC16F8X is shown in Figure 3-1.

The PIC16F8X fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, electronic locks, security devices and smart cards. The Flash/EEPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, security codes, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16F8X very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, serial communication, capture and compare, PWM functions and co-processor applications).

The serial in-system programming feature (via two pins) offers flexibility of customizing the product after complete assembly and testing. This feature can be used to serialize a product, store calibration data, or program the device with the current firmware before shipping.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A: for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to the PIC16F8X (Appendix B:).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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TABLE 1-1: PIC16F8X FAMILY OF DEVICES

	Clock	Memory					Peripherals			Features	
	Maximum Frequency of Operation (MHz)	Program Memory Flash	Program Memory EEPROM	Program Memory ROM	Data Memory (bytes)	Data EEPROM (bytes)	Timer Module(s)	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Packages
PIC16C84	10	—	1K	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F84(1)	10	1K	—	—	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR84(1)	10	—	—	1K	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F83(1)	10	512	—	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR83(1)	10	—	—	512	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16C8X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

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2.0 PIC16F8X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in this section. When placing orders, please use the "PIC16F8X Product Identification System" at the back of this data sheet to specify the correct part number.

There are four device "types" as indicated in the device number.

1. **F**, as in PIC16**F**84. These devices have Flash program memory and operate over the standard voltage range.
2. **LF**, as in PIC16**LF**84. These devices have Flash program memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**83. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**84. These devices have ROM program memory and operate over an extended voltage range.

When discussing memory maps and other architectural features, the use of **F** and **CR** also implies the **LF** and **LCR** versions.

2.1 Electrically Erasable Devices

These devices are offered in the lower cost plastic package, even though the device can be erased and reprogrammed. This allows the same device to be used for prototype development and pilot programs as well as production.

A further advantage of the electrically erasable version is that they can be erased and reprogrammed in-circuit, or by device programmers, such as Microchip's PICSTART® Plus or PRO MATE™ II programmers.

2.2 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices have all Flash locations and configuration options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available.

For information on submitting a QTP code, please contact your Microchip Regional Sales Office.

2.3 Serialized Quick-Turnaround-Production (SQTP^{SM}) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

For information on submitting a SQTP code, please contact your Microchip Regional Sales Office.

2.4 ROM Devices

Some of Microchip's devices have a corresponding device where the program memory is a ROM. These devices give a cost savings over Microchip's traditional user programmed devices (EPROM, EEPROM).

ROM devices (PIC16CR8X) do not allow serialization information in the program memory space. The user may program this information into the Data EEPROM.

For information on submitting a ROM code, please contact your Microchip Regional Sales Office.

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC16CXX opcodes are 14-bits wide, enabling single word instructions. The full 14-bit wide program memory bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle (400 ns @ 10 MHz) except for program branches.

The PIC16F83 and PIC16CR83 address 512 x 14 of program memory, and the PIC16F84 and PIC16CR84 address 1K x 14 program memory. All program memory is internal.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. An orthogonal (symmetrical) instruction set makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), and the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram for the PIC16F8X is shown in Figure 3-1, its corresponding pin description is shown in Table 3-1.

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FIGURE 3-1: PIC16F8X BLOCK DIAGRAM

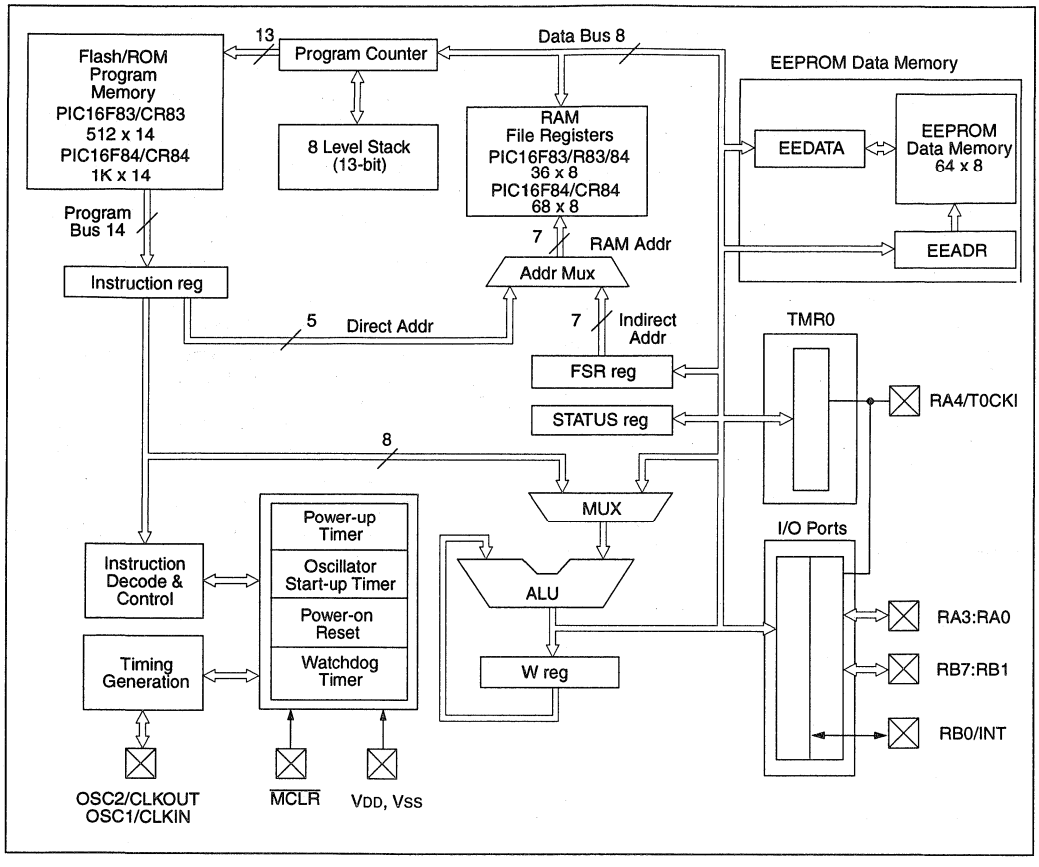

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TABLE 3-1: PIC16F8X PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS (3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST (1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = output I/O = Input/Output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

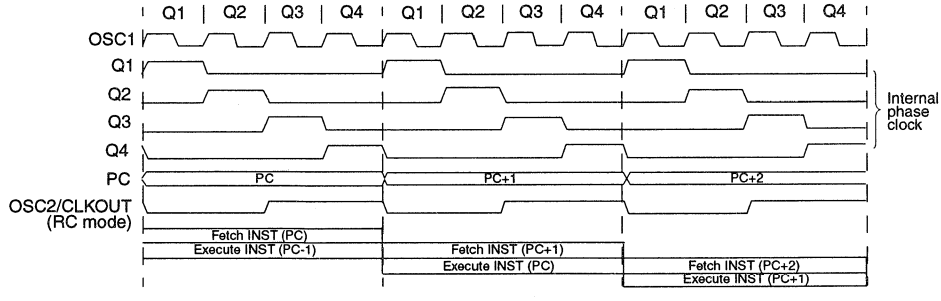
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

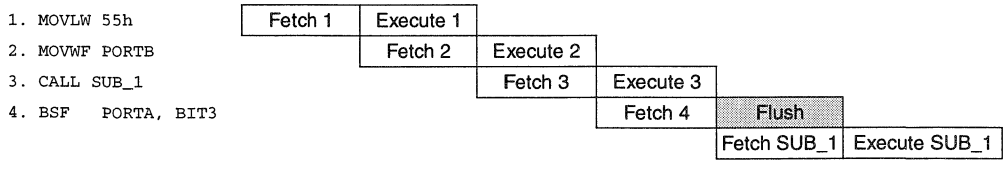
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F8X. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 7.0.

4.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F83 and PIC16CR83, the first 512 x 14 (0000h-01FFh) are physically implemented (Figure 4-1). For the PIC16F84 and PIC16CR84, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 4-2). Accessing a location above the physically implemented address will cause a wrap-around. For example, for the PIC16F84 locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK - PIC16F83/CR83

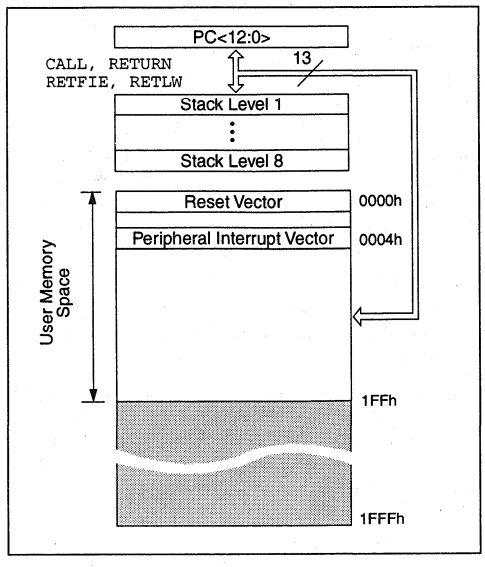
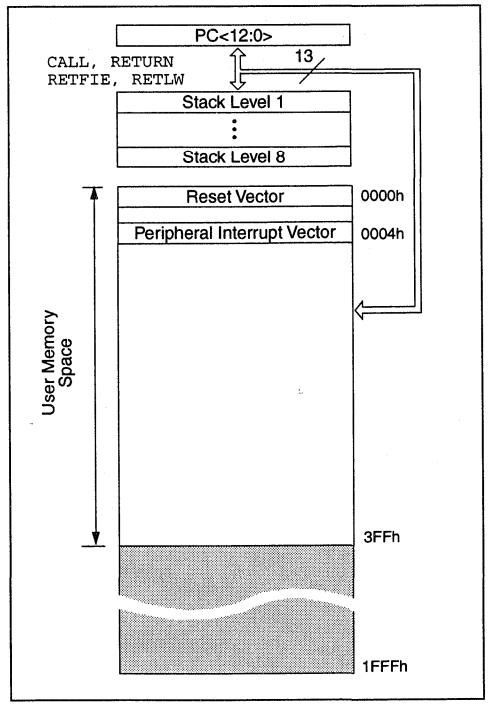


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK - PIC16F84/CR84



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4.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 4-3 and Figure 4-4 show the data memory map organization.

Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 4.5). Indirect addressing uses the present value of the RP1:RP0 bits for access into the banked areas of data memory.

Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

4.2.1 GENERAL PURPOSE REGISTER FILE

All devices have some amount of General Purpose Register (GPR) area. Each GPR is 8 bits wide and is accessed either directly or indirectly through the FSR (Section 4.5).

The GPR addresses in bank 1 are mapped to addresses in bank 0. As an example, addressing location 0Ch or 08h will access the same GPR.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (Figure 4-3, Figure 4-4 and Table 4-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

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FIGURE 4-3: REGISTER FILE MAP - PIC16F83/CR83

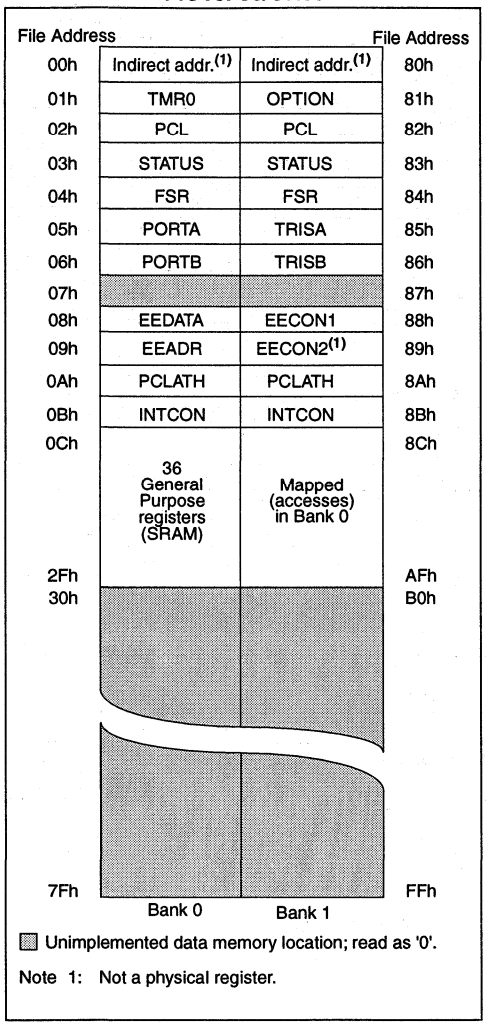

FIGURE 4-4: REGISTER FILE MAP - PIC16F84/CR84

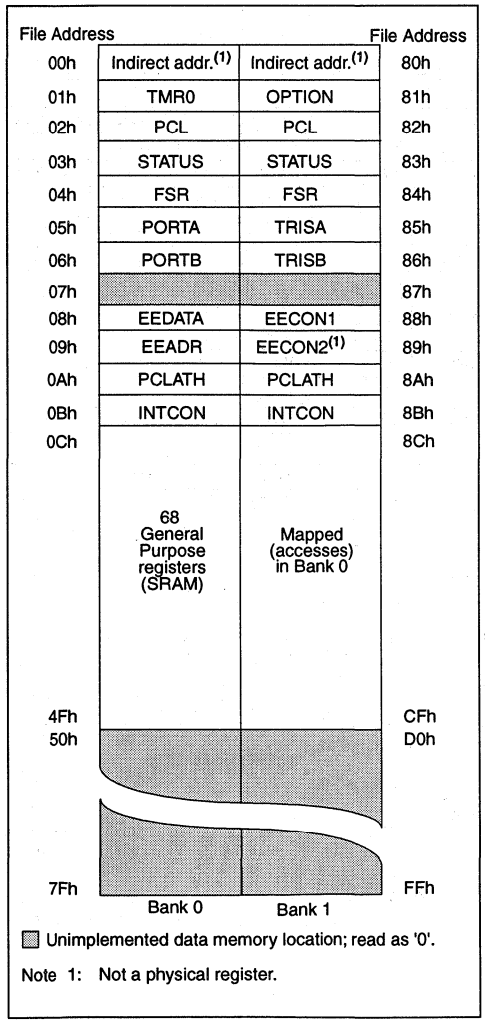

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TABLE 4-1: REGISTER FILE SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note3)
Bank 0											
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h	PCL	Low order 8 bits of the Program Counter (PC)								0000 0000	0000 0000
03h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
07h		Unimplemented location, read as '0'								---- ----	---- ----
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC (1)					---0 0000	---0 0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	0000 0000
83h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA data direction register					---1 1111	---1 1111
86h	TRISB	PORTB data direction register								1111 1111	1111 1111
87h		Unimplemented location, read as '0'								---- ----	---- ----
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2 (not a physical register)								---- ----	---- ----
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC (1)					---0 0000	---0 0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on condition.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> is never transferred to PCLATH.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a $\overline{MCLR}$ reset.

3: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

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4.2.2.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

Only the `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions should be used to alter the STATUS register (Table 9-2) because these instructions do not affect any status bit.

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F8X and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{borrow}$ and digit borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

Note 3: When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

FIGURE 4-5: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
0 = Bank 0, 1 (00h - FFh)
1 = Bank 2, 3 (100h - 1FFh)
The IRP bit is not used by the PIC16F8X. IRP should be maintained clear.

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
10 = Bank 2 (100h - 17Fh)
11 = Bank 3 (180h - 1FFh)
Each bank is 128 bytes. Only bit RP0 is used by the PIC16F8X. RP1 should be maintained clear.

bit 4: $\overline{TO}$: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: $\overline{PD}$: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `ADDLW` instructions) (For $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF` and `ADDLW` instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

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4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

FIGURE 4-6: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled (by individual port latch values)

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to TMR0

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable bits for all interrupt sources.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-7: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

Note: For the operation of the interrupt structure, please refer to Section 8.5.

bit 6: **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT Interrupt Enable bit
1 = Enables the RB0/INT interrupt
0 = Disables the RB0/INT interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 overflow interrupt flag bit
1 = TMR0 has overflowed (must be cleared in software)
0 = TMR0 did not overflow

bit 1: **INTF:** RB0/INT Interrupt Flag bit
1 = The RB0/INT interrupt occurred
0 = The RB0/INT interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

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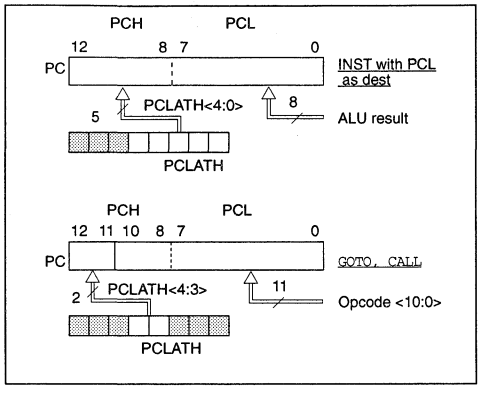
4.3 Program Counter: PCL and PCLATH

The Program Counter (PC) is 13-bits wide. The low byte is the PCL register, which is a readable and writable register. The high byte of the PC (PC<12:8>) is not directly readable nor writable and comes from the PCLATH register. The PCLATH (PC latch high) register is a holding register for PC<12:8>. The contents of PCLATH are transferred to the upper byte of the program counter when the PC is loaded with a new value. This occurs during a CALL, GOTO or a write to PCL. The high bits of PC are loaded from PCLATH as shown in Figure 4-8.

FIGURE 4-8: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 word block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 PROGRAM MEMORY PAGING

The PIC16F83 and PIC16CR83 have 512 words of program memory. The PIC16F84 and PIC16CR84 have 1K of program memory. The CALL and GOTO instructions have an 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. For future PIC16F8X program memory expansion, there must be another two bits to specify the program memory page. These paging bits come from the PCLATH<4:3> bits (Figure 4-8). When doing a CALL or a GOTO instruction, the user must ensure that these page bits (PCLATH<4:3>) are programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is "pushed" onto the stack (see next section). Therefore, manipulation of the PCLATH<4:3> is not required for the return instructions (which "pops" the PC from the stack).

Note: The PIC16F8X ignores the PCLATH<4:3> bits, which are used for program memory pages 1, 2 and 3 (0800h - 1FFFh). The use of PCLATH<4:3> as general purpose R/W bits is not recommended since this may affect upward compatibility with future products.

4.4 Stack

The PIC16FXX has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable.

The entire 13-bit PC is "pushed" onto the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is "popped" in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a push or a pop operation.

Note: There are no instruction mnemonics called push or pop. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

The stack operates as a circular buffer. That is, after the stack has been pushed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

If the stack is effectively popped nine times, the PC value is the same as the value from the first pop.

Note: There are no status bits to indicate stack overflow or stack underflow conditions.

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4.5 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

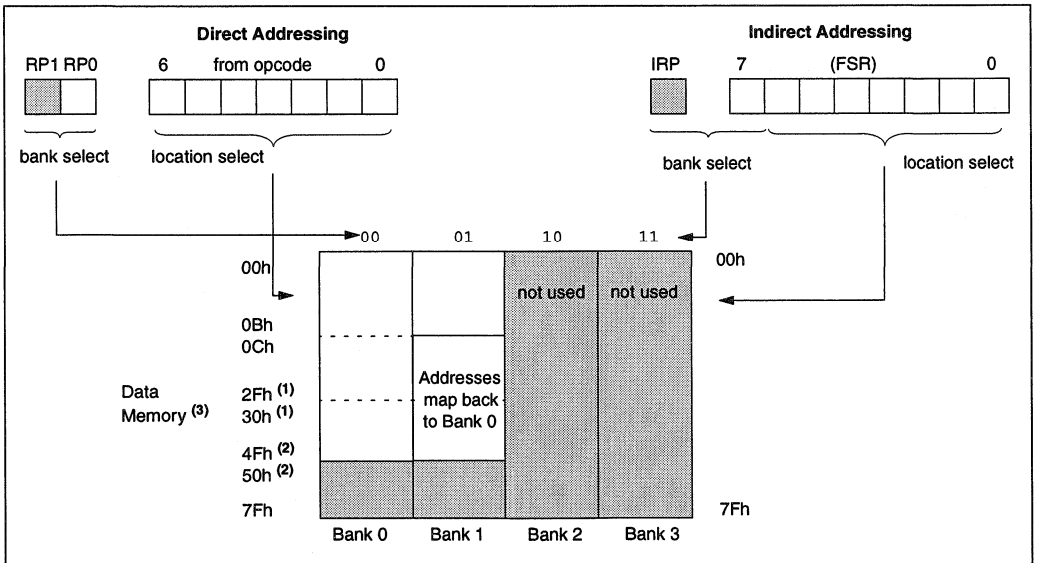
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x20  ;initialize pointer
        movwf   FSR   ;  to RAM
NEXT    clrf    INDF  ;clear INDF register
        incf    FSR   ;inc pointer
        btfss   FSR,4 ;all done?
        goto    NEXT  ;NO, clear next
CONTINUE
        :             ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-9. However, IRP is not used in the PIC16F8X.

FIGURE 4-9: DIRECT/INDIRECT ADDRESSING



Note 1: PIC16F83 and PIC16CR83 devices.
2: PIC16F84 and PIC16CR84 devices
3: For memory map detail see Figure 4-1.

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NOTES:

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5.0 I/O PORTS

The PIC16F8X has two ports, PORTA and PORTB. Some port pins are multiplexed with an alternate function for other features on the device.

5.1 PORTA and TRISA Registers

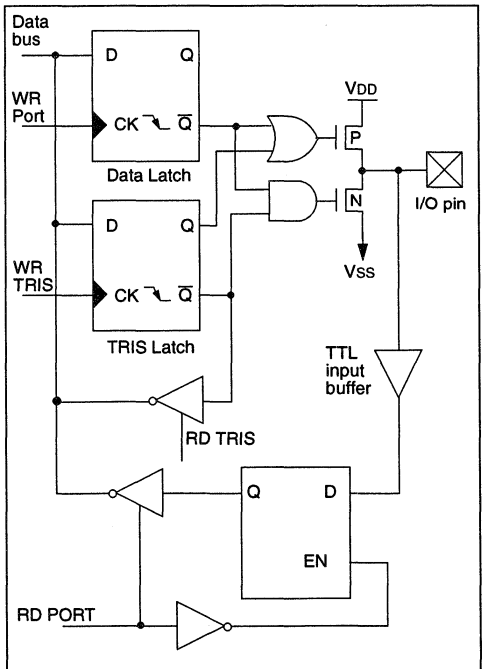
PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedence mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The RA4 pin is multiplexed with the TMR0 clock input.

FIGURE 5-1: BLOCK DIAGRAM OF PINS RA3:RA0

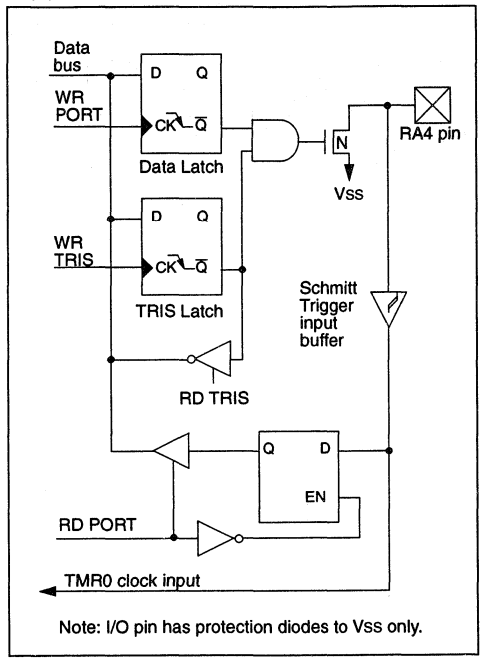


Note: I/O pins have protection diodes to VDD and VSS.

EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF    PORTA       ; Initialize PORTA by
                    ; setting output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0x0F        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISA       ; Set RA<3:0> as inputs
                    ; RA4 as outputs
                    ; TRISA<7:5> are always
                    ; read as '0'.
```

FIGURE 5-2: BLOCK DIAGRAM OF PIN RA4



Note: I/O pin has protection diodes to VSS only.

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TABLE 5-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are unimplemented, read as '0'

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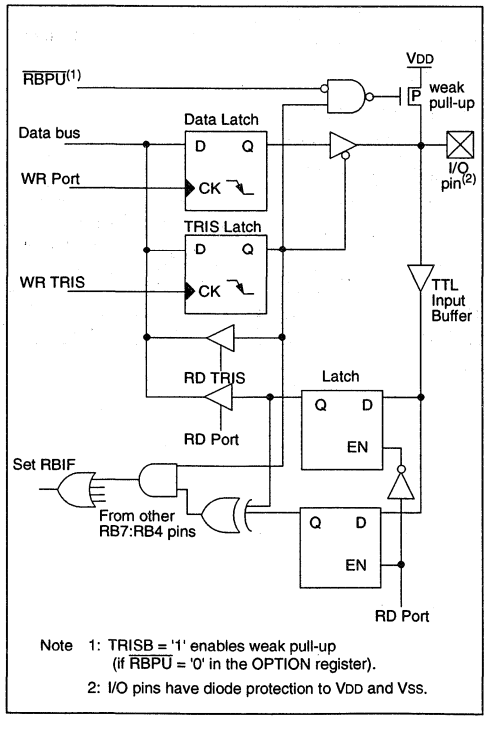
5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. A '1' on any bit in the TRISB register puts the corresponding output driver in a hi-impedance mode. A '0' on any bit in the TRISB register puts the contents of the output latch on the selected pin(s).

Each of the PORTB pins have a weak internal pull-up. A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBPU}}$ (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The pins value in input mode are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of the pins are OR'ed together to generate the RB port change interrupt.

FIGURE 5-3: BLOCK DIAGRAM OF PINS RB7:RB4



Note 1: TRISB = '1' enables weak pull-up (if $\overline{\text{RBPU}}$ = '0' in the OPTION register).
2: I/O pins have diode protection to VDD and VSS.

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Read (or write) PORTB. This will end the mismatch condition.
b) Clear flag bit RBIF.

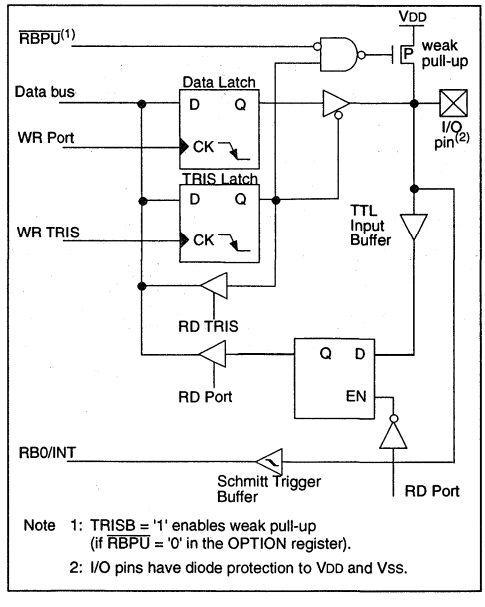
A mismatch condition will continue to set the RBIF bit. Reading PORTB will end the mismatch condition, and allow the RBIF bit to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression (see AN552 in the Embedded Control Handbook).

Note 1: For a change on the I/O pin to be recognized, the pulse width must be at least TCY wide.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-4: BLOCK DIAGRAM OF PINS RB3:RB0



Note 1: TRISB = '1' enables weak pull-up (if $\overline{\text{RBPU}}$ = '0' in the OPTION register).
2: I/O pins have diode protection to VDD and VSS.

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EXAMPLE 5-2: INITIALIZING PORTB

```
CLRF    PORTB       ; Initialize PORTB by
                    ; setting output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                    ; RB<5:4> as outputs
                    ; RB<7:6> as inputs
```

TABLE 5-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

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5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (i.e., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch is unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (i.e., BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output current may damage the chip.

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

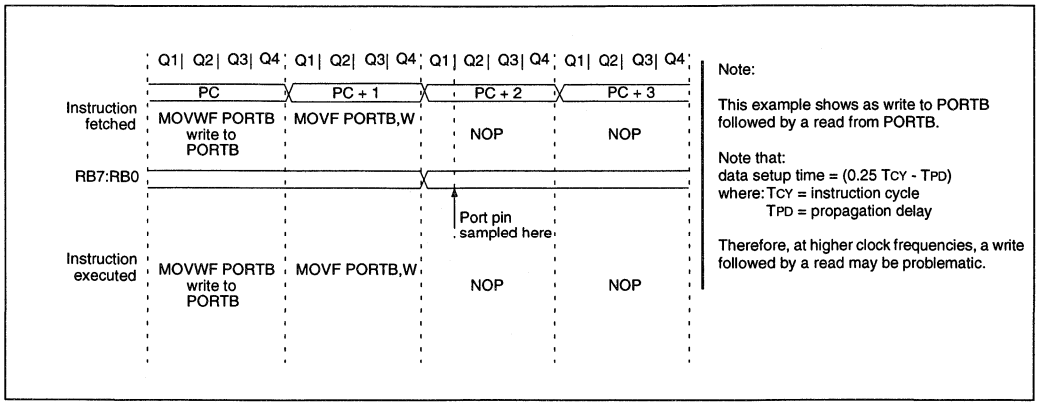
The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such that the pin voltage stabilizes (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

Example 5-3 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

EXAMPLE 5-3: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                       PORT latch  PORT pins
;                       ----------  ---------
  BCF PORTB, 7      ; 01pp ppp    11pp ppp
  BCF PORTB, 6      ; 10pp ppp    11pp ppp
  BSF STATUS, RP0   ;
  BCF TRISB, 7      ; 10pp ppp    11pp ppp
  BCF TRISB, 6      ; 10pp ppp    10pp ppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

FIGURE 5-5: SUCCESSIVE I/O OPERATION



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NOTES:

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6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module (Figure 6-1) will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

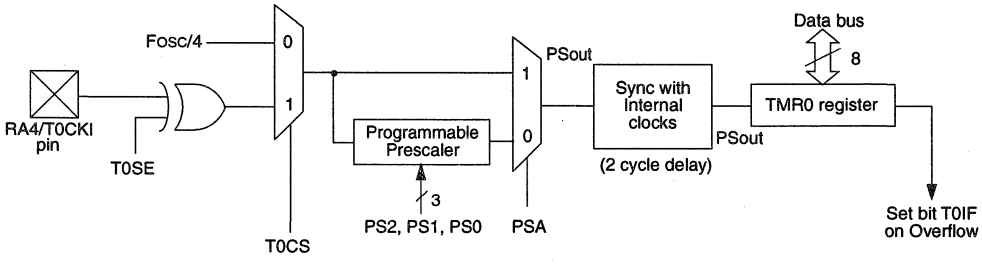
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode TMR0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the T0 source edge select bit, T0SE (OPTION<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 Module and the Watchdog Timer. The prescaler assignment is controlled, in software, by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 Module. The prescaler is not readable or writable. When the prescaler (Section 6.3) is assigned to the Timer0 Module, the prescale value (1:2, 1:4, ..., 1:256) is software selectable.

6.1 TMR0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets the T0IF bit (INTCON<2>). The interrupt can be masked by clearing enable bit T0IE (INTCON<5>). The T0IF bit must be cleared in software by the Timer0 Module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt (Figure 6-4) cannot wake the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 6-1: TMR0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PS2, PS1, PS0 and PSA are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-6)

FIGURE 6-2: TMR0 TIMING: INTERNAL CLOCK/NO PRESCALER

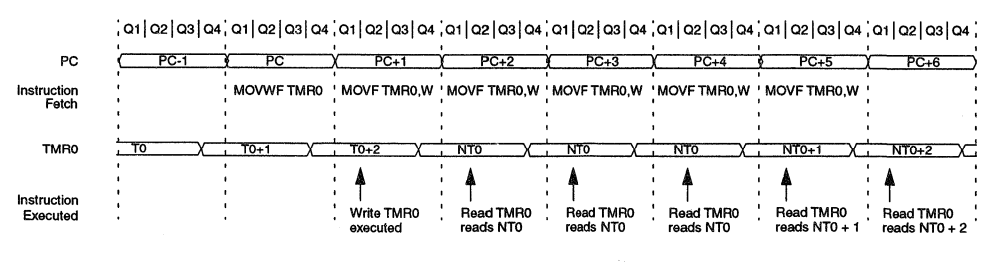


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FIGURE 6-3: TMR0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

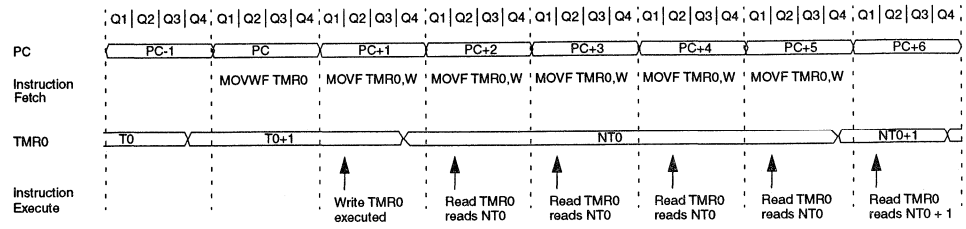
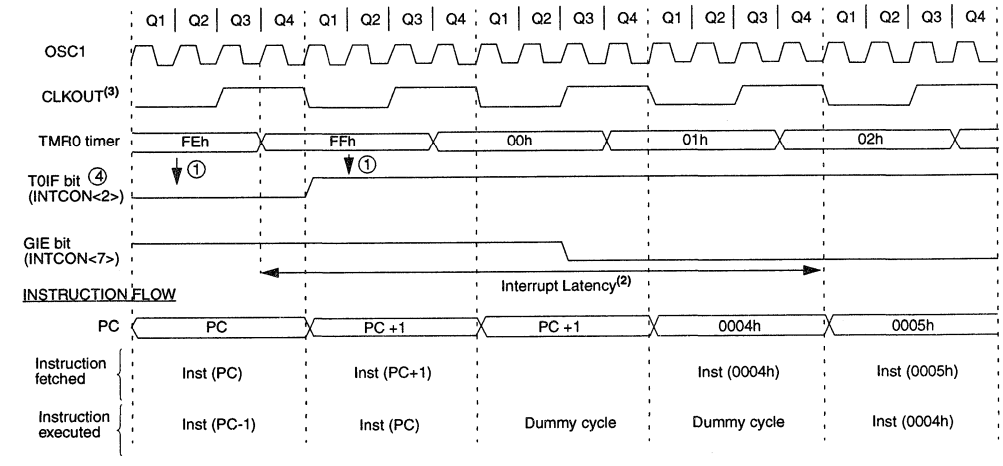


FIGURE 6-4: TMR0 INTERRUPT TIMING



Note 1: T0IF interrupt flag is sampled here (every Q1).
2: Interrupt latency = 3.25Tcy, where Tcy = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.
4: The timer clock (after the synchronizer circuit) which increments the timer from FFh to 00h immediately sets the T0IF bit. The TMR0 register will roll over 3 Tosc cycles later.

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6.2 Using TMR0 with External Clock

When an external clock input is used for TMR0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of the TMR0 register after synchronization.

6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of pin RA4/T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (plus a small RC delay) and low for at least 2Tosc (plus a small RC delay). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by an asynchronous ripple counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (plus a small RC delay) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the AC Electrical Specifications of the desired device.

6.2.2 TMR0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 Module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

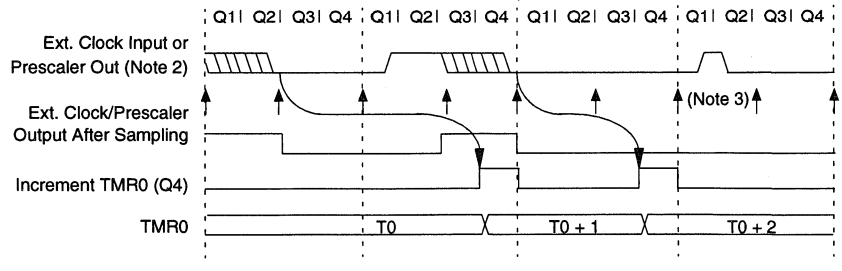
6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 Module, or as a postscaler for the Watchdog Timer (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 Module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 Module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 Module, all instructions writing to the Timer0 Module (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x` ....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to TMR0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on TMR0 input = ± 4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows ↑ indicate where sampling occurs. A small clock pulse may be missed by sampling.

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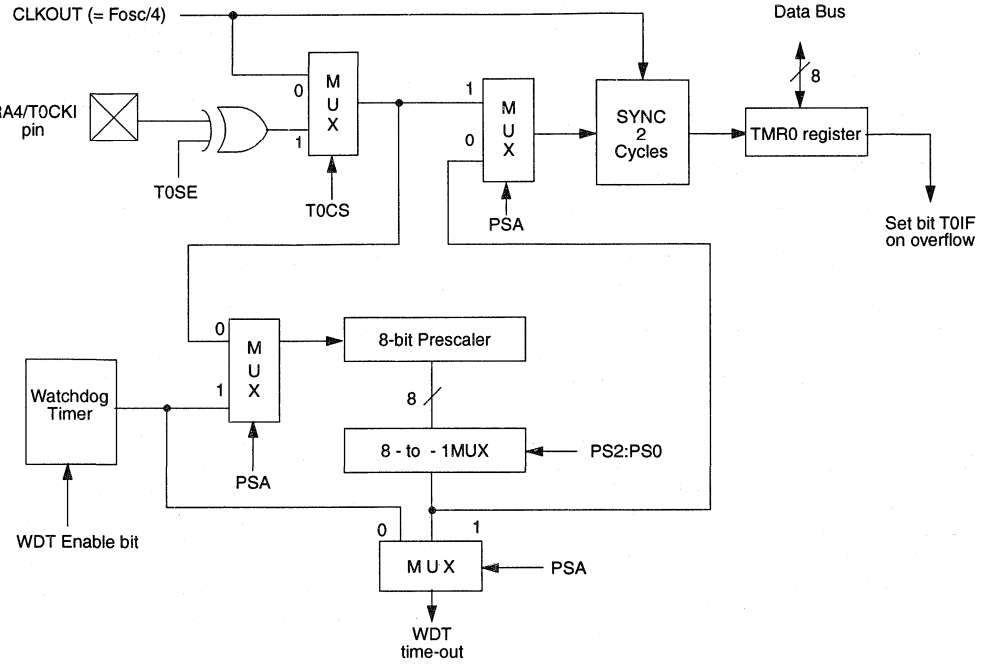
FIGURE 6-6: BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

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6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution).

Note: To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be taken even if the WDT is disabled. To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 6-2.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS, RP0  ;Bank 0
CLRF    TMR0         ;Clear TMR0
                     ; and Prescaler
BSF     STATUS, RP0  ;Bank 1
CLRWDT               ;Clears WDT
MOVLW   b'xxxx1xxx'  ;Select new
MOVWF   OPTION       ; prescale value
BCF     STATUS, RP0  ;Bank 0
```

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT               ;Clear WDT and
                     ; prescaler
BSF     STATUS, RP0  ;Bank 1
MOVLW   b'xxxx0xxx'  ;Select TMR0, new
                     ; prescale value
                     ' and clock source
MOVWF   OPTION       ;
BCF     STATUS, RP0  ;Bank 0
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 0000
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not associated with Timer0.

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7.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F8X devices have 64 bytes of data EEPROM with an address range from 0h to 3Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

7.1 EEADR

The EEADR register can address up to a maximum of 256 bytes of data EEPROM. Only the first 64 bytes of data EEPROM are implemented.

The upper two bits are address decoded. This means that these two bits must always be '0' to ensure that the address is in the 64 byte memory space.

FIGURE 7-1: EECON1 REGISTER (ADDRESS 88h)

U	U	U	R/W-0	R/W-x	R/W-0	R/S-0	R/S-x
—	—	—	EEIF	WRERR	WREN	WR	RD
bit7							bit0

R = Readable bit
W = Writable bit
S = Settable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7:5 **Unimplemented:** Read as '0'

bit 4 **EEIF**: EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 **WRERR**: EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any $\overline{MCLR}$ reset or any WDT reset during normal operation)
0 = The write operation completed

bit 2 **WREN**: EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 **WR**: Write Control bit
1 = initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
0 = Write cycle to the data EEPROM is complete

bit 0 **RD**: Read Control bit
1 = Initiates an EEPROM read (read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software).
0 = Does not initiate an EEPROM read

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7.2 EECON1 and EECON2 Registers

EECON1 is the control register with five low order bits physically implemented. The upper-three bits are non-existent and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{MCLR}$ reset or a WDT time-out reset during normal operation. In these situations, following reset, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDATA and EEADR registers.

Interrupt flag bit EEIF is set when write is complete. It must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the Data EEPROM write sequence.

7.3 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 7-1: DATA EEPROM READ

```
BCF     STATUS, RP0  ; Bank 0
MOVLW   CONFIG_ADDR  ;
MOVWF   EEADR        ; Address to read
BSF     STATUS, RP0  ; Bank 1
BSF     EECON1, RD   ; EE Read
BCF     STATUS, RP0  ; Bank 0
MOVF    EEDATA, W    ; W = EEDATA
```

7.4 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

EXAMPLE 7-2: DATA EEPROM WRITE

```
        BSF     STATUS, RP0  ; Bank 1
        BCF     INTCON, GIE  ; Disable INTs.
        BSF     EECON1, WREN ; Enable Write
Required
Sequence
        MOVLW   55h          ;
        MOVWF   EECON2       ; Write 55h
        MOVLW   AAh          ;
        MOVWF   EECON2       ; Write AAh
        BSF     EECON1,WR    ; Set WR bit
                             ;   begin write
        BSF     INTCON, GIE  ; Enable INTs.
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

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7.5 Write Verify

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (Example 7-3) to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit. The Total Endurance disk will help determine your comfort level.

Generally the EEPROM write failure will be a bit which was written as a '1', but reads back as a '0' (due to leakage off the bit).

EXAMPLE 7-3: WRITE VERIFY

```
    BCF   STATUS, RP0 ; Bank 0
    :                 ; Any code can go here
    :                 ;
    MOVF  EEDATA, W   ; Must be in Bank 0
    BSF   STATUS, RP0 ; Bank 1
READ
    BSF   EECON1, RD  ; YES, Read the
                      ;   value written
    BCF   STATUS, RP0 ; Bank 0
;
; Is the value written (in W reg) and
;   read (in EEDATA) the same?
;
    SUBWF EEDATA, W   ;
    BTFSS STATUS, Z   ; Is difference 0?
    GOTO  WRITE_ERR   ; NO, Write error
    :                 ; YES, Good write
    :                 ; Continue program
```

7.6 Protection Against Spurious Writes

There are conditions when the device may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch, or software malfunction.

7.7 Data EEPROM Operation during Code Protect

When the device is code protected, the CPU is able to read and write unscrambled data to the Data EEPROM.

For ROM devices, there are two code protection bits (Section 8.1). One for the ROM program memory and one for the Data EEPROM memory.

TABLE 7-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by Data EEPROM.

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NOTES:

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8.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16F8X has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- OSC Selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16F8X has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode offers a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

8.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming.

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FIGURE 8-1: CONFIGURATION WORD - PIC16CR83 AND PIC16CR84

R-u	R-u	R-u	R-u	R-u	R-u	R/P-u	R-u	R-u	R-u	R-u	R-u	R-u	R-u
CP	CP	CP	CP	CP	CP	DP	CP	CP	CP	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0

bit13 bit0

R = Readable bit
P = Programmable bit
- n = Value at POR reset
u = unchanged

bit 13:8 **CP**: Program Memory Code Protection bit
1 = Code protection off
0 = Program memory is code protected

bit 7 **DP**: Data Memory Code Protection bit
1 = Code protection off
0 = Data memory is code protected

bit 6:4 **CP**: Program Memory Code Protection bit
1 = Code protection off
0 = Program memory is code protected

bit 3 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = Power-up timer is disabled
0 = Power-up timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1:0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

FIGURE 8-2: CONFIGURATION WORD - PIC16F83 AND PIC16F84

R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0

bit13 bit0

R = Readable bit
P = Programmable bit
- n = Value at POR reset
u = unchanged

bit 13:4 **CP**: Code Protection bit
1 = Code protection off
0 = All memory is code protected

bit 3 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = Power-up timer is disabled
0 = Power-up timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1:0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

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8.2 Oscillator Configurations

8.2.1 OSCILLATOR TYPES

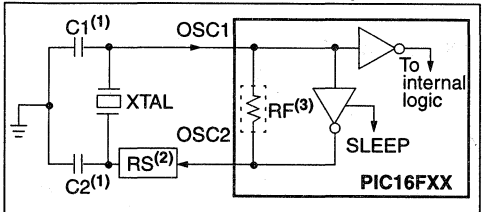
The PIC16F8X can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 8-3).

FIGURE 8-3: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note1: See Table 8-1 for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen.

The PIC16F8X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 8-4).

FIGURE 8-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

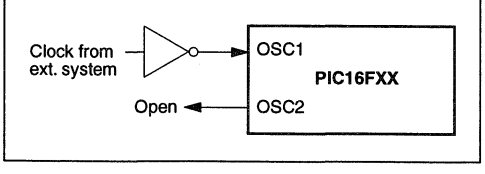


TABLE 8-1: PIC16F83/CR83/F84/CR84 CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Tested:			
Mode	**Freq**	**OSC1/C1**	**OSC2/C2**
XT	455 kHz	47 - 100 pF	47 - 100 pF
	2.0 MHz	15 - 33 pF	15 - 33 pF
	4.0 MHz	15 - 33 pF	15 - 33 pF
HS	8.0 MHz	15 - 33 pF	15 - 33 pF
	10.0 MHz	15 - 33 pF	15 - 33 pF

Note: Recommended values of C1 and C2 are identical to the ranges tested table.
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for the appropriate values of external components.

Resonators Tested:		
455 kHz	Panasonic EFO-A455K04B	± 0.3%
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%
10.0 MHz	Murata Erie CSA10.00MTZ	± 0.5%
None of the resonators had built-in capacitors.		

PRELIMINARY

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TABLE 8-2: PIC16F83/CR83/F84/CR84 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	10 MHz	15 - 33 pF	15 - 33 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

Crystals Tested:		
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM
200 kHz	STD XTL 200.000 KHz	± 20 PPM
1.0 MHz	ECS ECS-10-13-2	± 50 PPM
2.0 MHz	ECS ECS-20-S-2	± 50 PPM
4.0 MHz	ECS ECS-40-S-4	± 50 PPM
10.0 MHz	ECS ECS-100-S-4	± 50 PPM

8.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits are available; one with series resonance, and one with parallel resonance.

Figure 8-5 shows a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 8-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

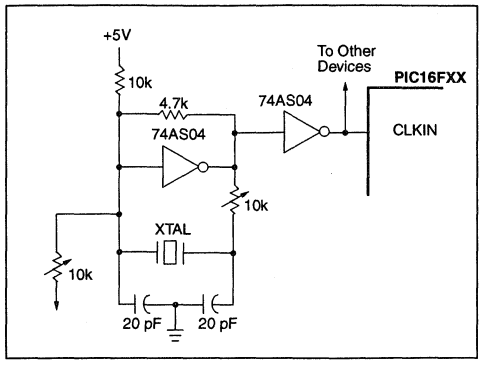
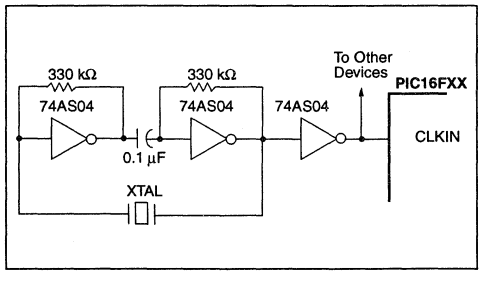


Figure 8-6 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 8-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



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8.2.4 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) values, capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low Cext values. The user needs to take into account variation due to tolerance of the external R and C components. Figure 8-7 shows how an R/C combination is connected to the PIC16F8X. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 5 kΩ and 100 kΩ.

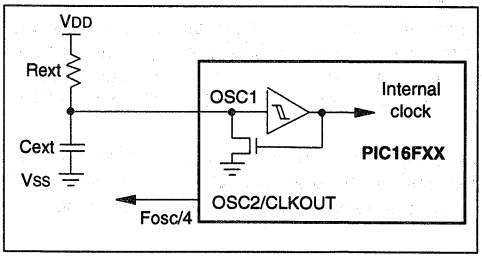
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With little or no external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See the electrical specification section for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance has a greater affect on RC frequency).

See the electrical specification section for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-2 for waveform).

FIGURE 8-7: RC OSCILLATOR MODE



Note: When the device oscillator is in RC mode, do not drive the OSC1 pin with an external clock or you may damage the device.

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8.3 Reset

The PIC16F8X differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{MCLR}$ reset during normal operation
- $\overline{MCLR}$ reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

Figure 8-8 shows a simplified block diagram of the on-chip reset circuit. The $\overline{MCLR}$ reset path has a noise filter to ignore small pulses. The electrical specifications state the pulse width requirements for the $\overline{MCLR}$ pin.

Some registers are not affected in any reset condition; their status is unknown on a POR reset and unchanged in any other reset. Most other registers are reset to a "reset state" on POR, $\overline{MCLR}$ or WDT reset during normal operation and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation.

Table 8-3 gives a description of reset conditions for the program counter (PC) and the STATUS register. Table 8-4 gives a full description of reset states for all registers.

The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations (Section 8.7). These bits are used in software to determine the nature of the reset.

FIGURE 8-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

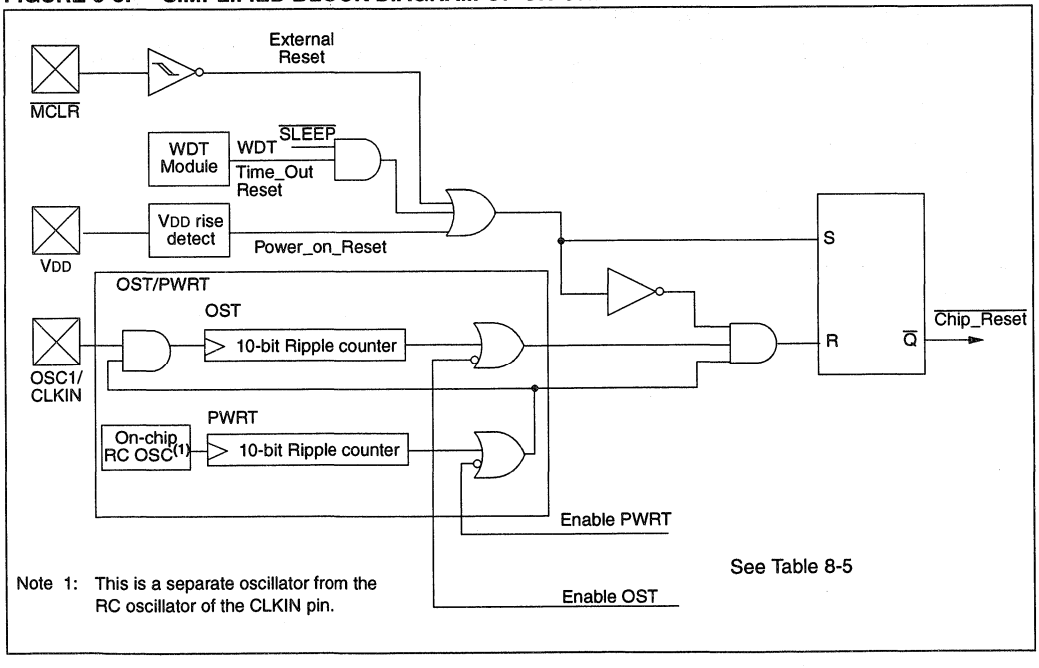

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TABLE 8-3: RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1 (1)	uuu1 0uuu

Legend: u = unchanged, x = unknown.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 8-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	$\overline{MCLR}$ Reset during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1 (2)
STATUS	03h	0001 1xxx	000q quuu (3)	uuuq quuu (3)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---x xxxx	---u uuuu	---u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu (1)
INDF	80h	---- ----	---- ----	---- ----
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000q quuu (3)	uuuq quuu (3)
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu (1)

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.
Note 1: One or more bits in INTCON will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: Table 8-3 lists the reset value for each specific condition.

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8.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting.*"

The POR circuit does not produce an internal reset when VDD declines.

8.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out (TPWRT) from POR (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13). The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level (Possible exception shown in Figure 8-13).

A configuration bit, PWRTE, can enable/disable the PWRT. See either Figure 8-1 or Figure 8-2 for the operation of the PWRTE bit for a particular device.

The power-up time delay TPWRT will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

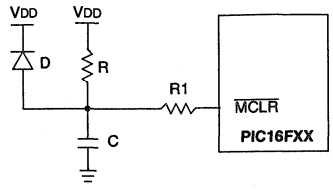
8.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this case (Figure 8-13), an external power-on reset circuit may be necessary (Figure 8-9).

FIGURE 8-9: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if VDD power-up rate is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{MCLR}$ pin is 5 μA). A larger voltage drop will degrade VIH level on the $\overline{MCLR}$ pin.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of an $\overline{MCLR}$ pin breakdown due to ESD or EOS.

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FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): CASE 1

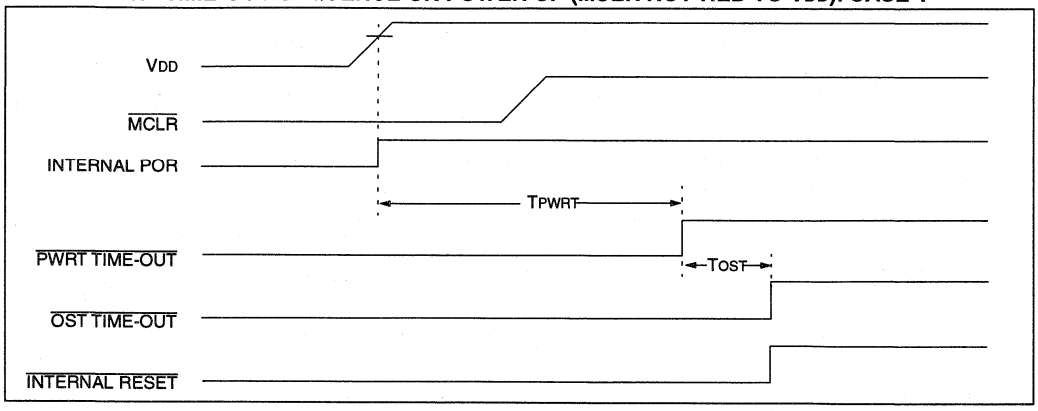

FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): CASE 2

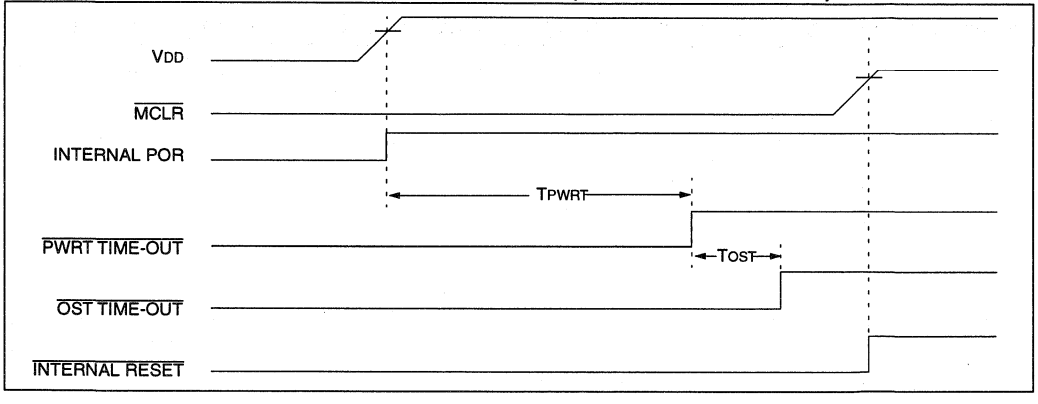

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FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME

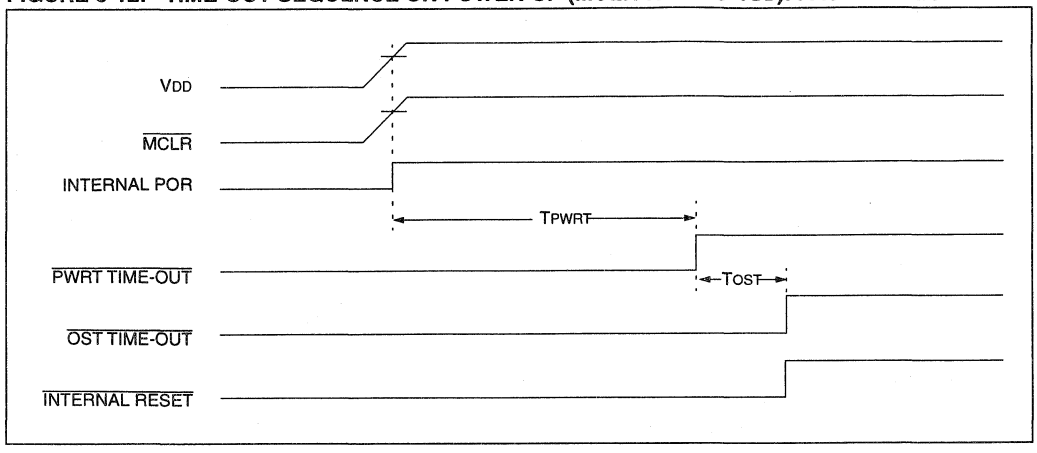
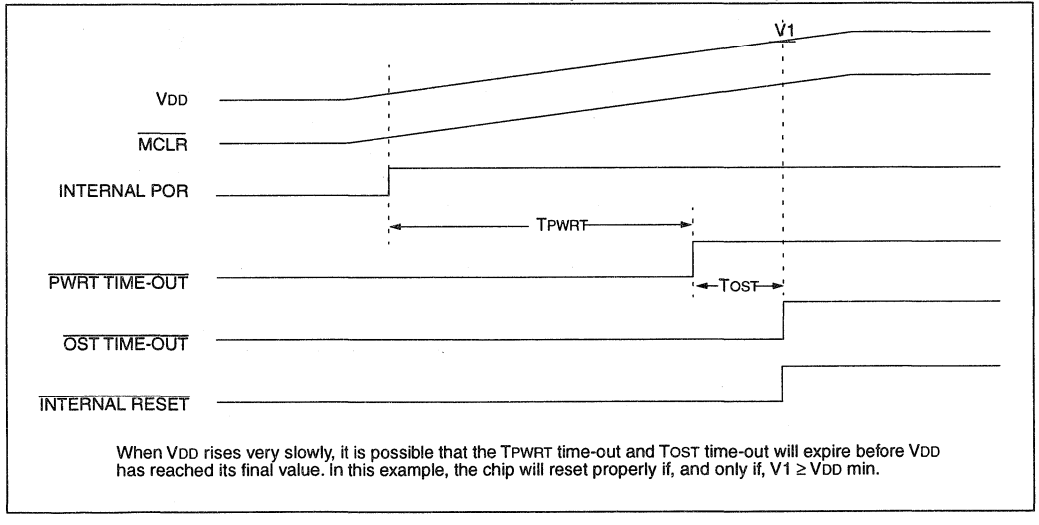


FIGURE 8-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



When V_{DD} rises very slowly, it is possible that the T_{PWRT} time-out and T_{OST} time-out will expire before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ V_{DD} min.

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8.7 Time-out Sequence and Power-down Status Bits (TO/PD)

On power-up (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13) the time-out sequence is as follows: First PWRT time-out is invoked after a POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and PWRTE configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

TABLE 8-5: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	PWRT Disabled	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	1024Tosc
RC	72 ms	—	—

Since the time-outs occur from the POR reset pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high, execution will begin immediately (Figure 8-10). This is useful for testing purposes or to synchronize more than one PIC16F8X device when operating in parallel.

Table 8-6 shows the significance of the $\overline{TO}$ and $\overline{PD}$ bits. Table 8-3 lists the reset conditions for some special registers, while Table 8-4 lists the reset conditions for all the registers.

TABLE 8-6: STATUS BITS AND THEIR SIGNIFICANCE

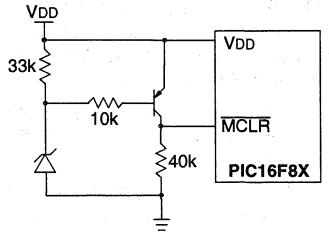
$\overline{TO}$	$\overline{PD}$	Condition
1	1	Power-on Reset
0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	$\overline{MCLR}$ Reset during normal operation
1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

8.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

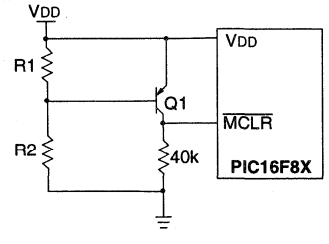
To reset a PIC16F8X device when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-14 and Figure 8-15.

FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

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8.9 Interrupts

The PIC16F8X has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- Data EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits.

The global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on reset.

The "return from interrupt" instruction, `RETFIE`, exits interrupt routine as well as sets the GIE bit, which re-enable interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to; the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 8-17). The latency is the same for both one and two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

FIGURE 8-16: INTERRUPT LOGIC

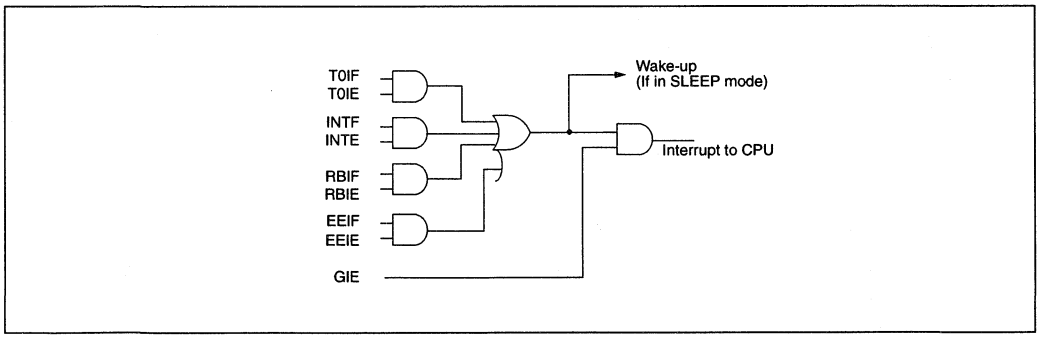

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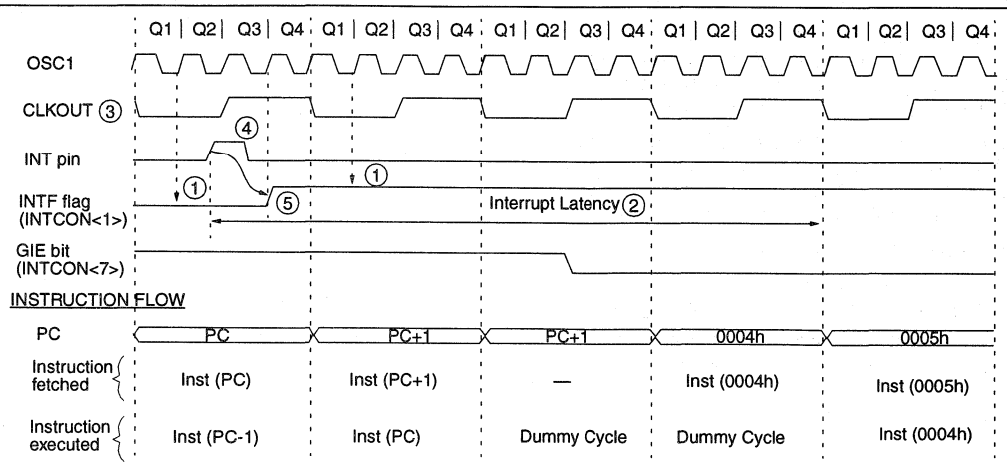
FIGURE 8-17: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4Tcy where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

8.9.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP (Section 8.12) only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

8.9.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in TMR0 will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 6.0).

8.9.3 PORT RB INTERRUPT

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) (Section 5.2).

Note 1: For a change on the I/O pin to be recognized, the pulse width must be at least TCY wide.

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8.10 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software.

Example 8-1 stores and restores the STATUS and W register's values. The User defined registers, W_TEMP and STATUS_TEMP are the temporary storage locations for the W and STATUS registers values.

Example 8-1 does the following:

a) Stores the W register.
b) Stores the STATUS register in STATUS_TEMP.
c) Executes the Interrupt Service Routine code.
d) Restores the STATUS (and bank select bit) register.
e) Restores the W register.

EXAMPLE 8-1: SAVING STATUS AND W REGISTERS IN RAM

```
PUSH    MOVWF   W_TEMP          ; Copy W to TEMP register,
        SWAPF   STATUS, W       ; Swap status to be saved into W
        MOVWF   STATUS_TEMP     ; Save status to STATUS_TEMP register
ISR     :                       :
        :                       ; Interrupt Service Routine
        :                       ;  should configure Bank as required
        :                       ;
POP     SWAPF   STATUS_TEMP, W  ; Swap nibbles in STATUS_TEMP register
                                ; and place result into W
        MOVWF   STATUS          ; Move W into STATUS register
                                ;   (sets bank to original state)
        SWAPF   W_TEMP, F       ; Swap nibbles in W_TEMP and place result in W_TEMP
        SWAPF   W_TEMP, W       ; Swap nibbles in W_TEMP and place result into W
```


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8.11 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT Wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit WDTE as a '0' (Section 8.1).

8.11.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

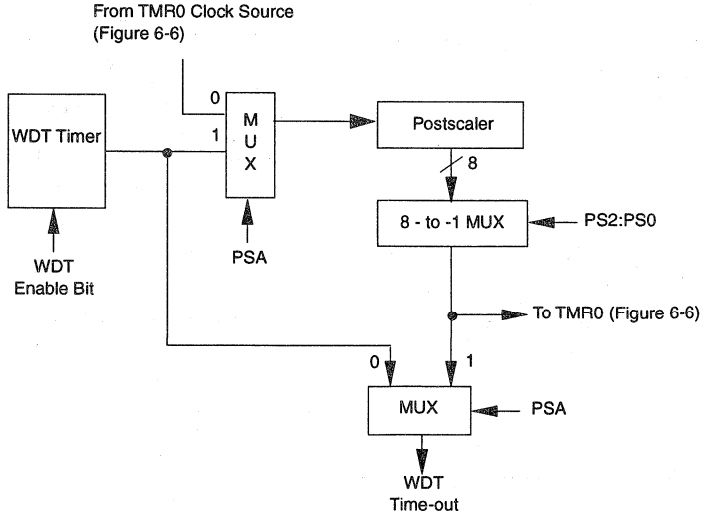
The CLRWDT and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a WDT time-out.

8.11.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 8-18: WATCHDOG TIMER BLOCK DIAGRAM



Note: PSA and PS2:PS0 are bits in the OPTION register.

TABLE 8-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
2007h	Config. bits	(2)	(2)	(2)	(2)	PWRTE(1)	WDTE	FOSC1	FOSC0	(2)	
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.
Note 1: See Figure 8-1 and Figure 8-2 for operation of the PWRTE bit.
2: See Figure 8-1, Figure 8-2 and Section 8.13 for operation of the Code and Data protection bits.

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8.12 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

8.12.1 SLEEP

The Power-down mode is entered by executing the SLEEP instruction.

If enabled, the Watchdog Timer is cleared (but keeps running), the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ bit (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For the lowest current consumption in SLEEP mode, place all I/O pins at either at VDD or VSS, with no external circuitry drawing current from the I/O pins, and disable external clocks. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

8.12.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

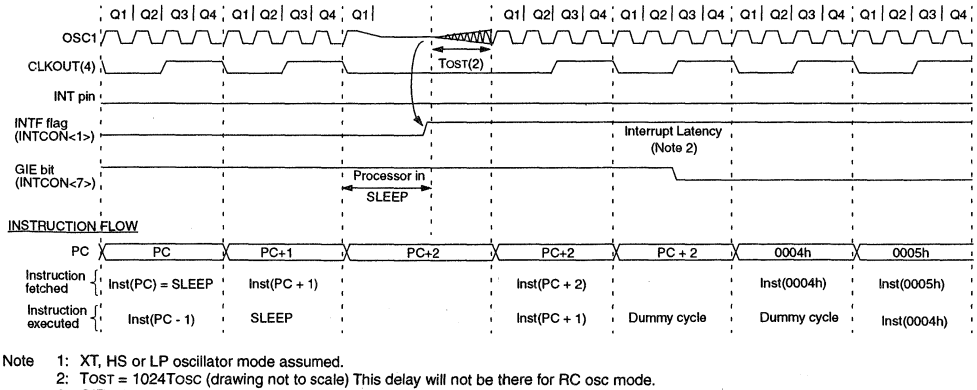
1. External reset input on $\overline{MCLR}$ pin.
2. WDT Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or data EEPROM write complete.

Peripherals cannot generate interrupts during SLEEP, since no on-chip Q clocks are present.

The first event ($\overline{MCLR}$ reset) will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of a device reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

While the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

FIGURE 8-19: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

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8.12.3 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

8.13 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting widowed devices.

8.14 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations to store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable only during program/verify. Only the 4 least significant bits of ID location are usable.

For ROM devices, these values are submitted along with the ROM code.

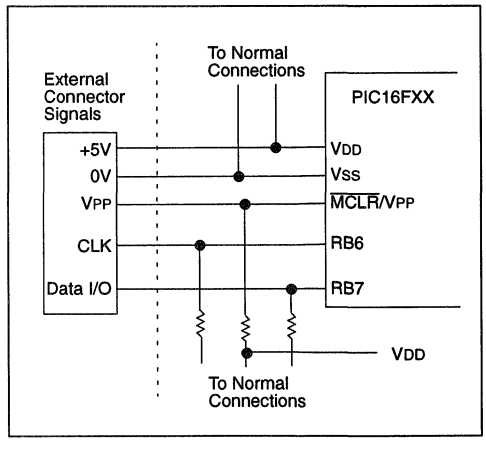
8.15 In-Circuit Serial Programming

PIC16F8X microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. Customers can manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product, allowing the most recent firmware or custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low, while raising the $\overline{MCLR}$ pin from VIL to VIHH (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) points to location 00h. A 6-bit command is then supplied to the device, 14-bits of program data is then supplied to or from the device, using load or read-type instructions. For complete details of serial programming, please refer to the PIC16CXX Programming Specifications (Literature #DS30189).

FIGURE 8-20: TYPICAL IN-SYSTEM SERIAL PROGRAMMING CONNECTION



For ROM devices, both the program memory and Data EEPROM memory may be read, but only the Data EEPROM memory may be programmed.

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NOTES:

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Applicable Devices	F83	CR83	F84	CR84

9.0 ELECTRICAL CHARACTERISTICS FOR PIC16F83 AND PIC16F84

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... -0.3 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... -0.3 to +14V

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.6V to (V_{DD} + 0.6V)

Total power dissipation (1) ..... 800 mW

Maximum current out of V_{SS} pin ..... 150 mA

Maximum current into V_{DD} pin ..... 100 mA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 20 mA

Maximum current sunk by PORTA ..... 80 mA

Maximum current sourced by PORTA ..... 50 mA

Maximum current sunk by PORTB ..... 150 mA

Maximum current sourced by PORTB ..... 100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

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Applicable Devices | F83 | CR83 | F84 | CR84

TABLE 9-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16F84-04 PIC16F83-04	PIC16F84-10 PIC16F83-10	PIC16LF84-04 PIC16LF83-04
RC	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 µA max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 5.5V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 7.0 µA max. at 2V WDT dis Freq: 2.0 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 µA max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 5.5V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 7.0 µA max. at 2V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 4.5 mA typ. at 5.5V IPD: 1.0 µA typ. at 4.5V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V typ. IPD: 1.0 µA typ. at 4.5V WDT dis Freq: 10 MHz max.	Do not use in HS mode
LP	VDD: 4.0V to 6.0V IDD: 35 µA typ. at 32 kHz, 3.0V IPD: 0.6 µA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	VDD: 2.0V to 6.0V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 7 µA max. at 2.0V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

PRELIMINARY

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Applicable Devices F83 CR83 F84 CR84

9.1 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	4.0	—	6.0	V	XT, RC and LP osc configuration
D001A			4.5	—	5.5	V	HS osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current(2)					RC and XT osc configuration(4)
D010			—	1.8	4.5	mA	FOSC = 4.0 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 4.0 MHz, VDD = 5.5V (During Flash programming)
							HS OSC CONFIGURATION (PIC16F84-10)
D013			—	5	10	mA	FOSC = 10 MHz, VDD = 5.5V
D020	IPD	Power-down Current(3)	—	7.0	28	µA	VDD = 4.0V, WDT enabled, industrial
D021			—	1.0	14	µA	VDD = 4.0V, WDT disabled, commercial
D021A			—	1.0	16	µA	VDD = 4.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

PRELIMINARY

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Applicable Devices F83 CR83 F84 CR84

9.2 DC CHARACTERISTICS: PIC16LF84, PIC16LF83 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.0	—	6.0	V	XT, RC, and LP osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current(2)					RC and XT osc configuration(4)
D010			—	1	4	mA	FOSC = 2.0 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 2.0 MHz, VDD = 5.5V (During Flash programming)
							LP osc configuration
D014			—	15	32	µA	FOSC = 32 kHz, VDD = 2.0V, WDT disabled
D020	IPD	Power-down Current(3)	—	3.0	16	µA	VDD = 2.0V, WDT enabled, industrial
D021			—	0.4	7.0	µA	VDD = 2.0V, WDT disabled, commercial
D021A			—	0.4	9.0	µA	VDD = 2.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

PRELIMINARY

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Applicable Devices | F83 | CR83 | F84 | CR84

9.3 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial) PIC16LF84, PIC16LF83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 9.1 and Section 9.2.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports					
D030		with TTL buffer	VSS	—	0.8	V	4.5 V ≤ VDD ≤ 5.5 V
D030A			VSS	—	0.16VDD	V	entire range(4)
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	entire range
D032		MCLR, RA4/T0CKI	Vss	—	0.2VDD	V	
D033		OSC1 (XT, HS and LP modes)(1)	Vss	—	0.3VDD	V	
D034		OSC1 (RC mode)	Vss	—	0.1VDD	V	
		Input High Voltage					
	VIH	I/O ports		—			
D040		with TTL buffer	2.4	—	VDD	V	4.5 V ≤ VDD ≤ 5.5V
D040A			0.48VDD	—	VDD	V	entire range(4)
D041		with Schmitt Trigger buffer	0.45VDD	—	VDD		entire range
D042		MCLR, RA4/T0CKI, OSC1 (RC mode)	0.85 VDD	—	VDD	V	
D043		OSC1 (XT, HS and LP modes)(1)	0.7 VDD	—	VDD	V	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	TBD	—	—	V	
D070	IPURB	PORTB weak pull-up current	50*	250*	400*	µA	VDD = 5.0V, VPIN = VSS
		Input Leakage Current(2,3)					
D060	IIL	I/O ports	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		MCLR, RA4/T0CKI	—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
		Output Low Voltage					
D080	VOL	I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
D083		OSC2/CLKOUT	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(3)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D092		OSC2/CLKOUT	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F8X with an external clock while the device is in RC mode, otherwise chip damage may result.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may use better of the two specs.

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Applicable Devices	F83	CR83	F84	CR84

9.4 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial) PIC16LF84, PIC16F83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 9.1 and Section 9.2.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
		Data EEPROM Memory					
D120	ED	Endurance	1M	10M	—	E/W	25°C at 5V
D121	VDRW	VDD for read/write	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	—	10	ms	
		Program Flash Memory					
D130	EP	Endurance	100	1000	—	E/W	
D131	VPR	VDD for read	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for erase/write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	10	—	ms	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 9-2: TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase symbols (pp) and their meanings:

pp			
2	to	os,osc	OSC1
ck	CLKOUT	ost	oscillator start-up timer
cy	cycle time	pwrt	power-up timer
io	I/O port	rbt	RBx pins
inp	INT pin	t0	T0CKI
mc	$\overline{MCLR}$	wdt	watchdog timer

Uppercase symbols and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	High Impedance

FIGURE 9-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.

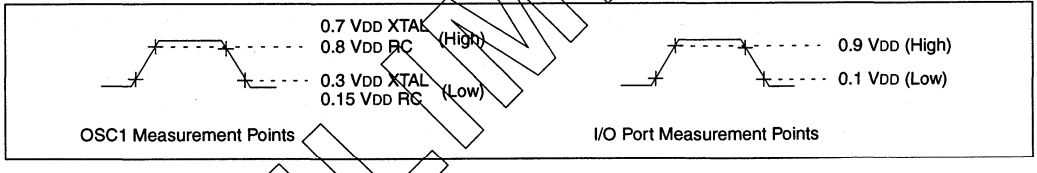
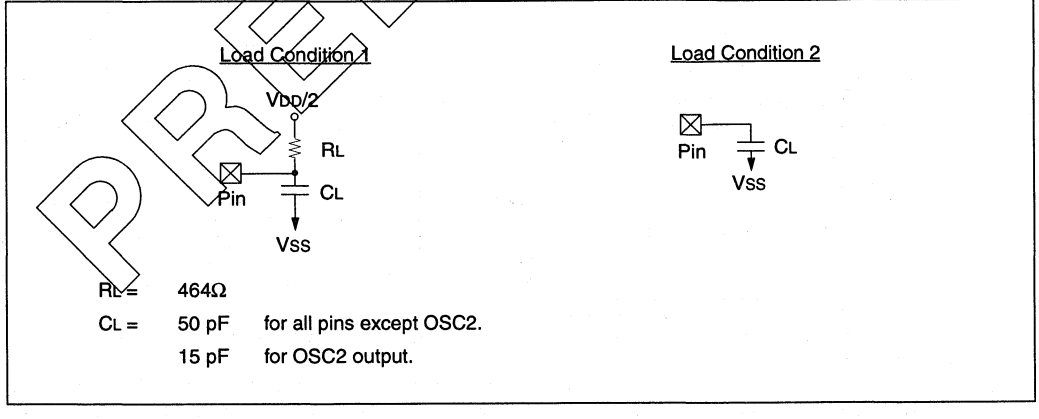


FIGURE 9-2: LOAD CONDITIONS



RL = 464Ω

CL = 50 pF for all pins except OSC2.

15 pF for OSC2 output.

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Applicable Devices F83 CR83 F84 CR84

9.5 Timing Diagrams and Specifications

FIGURE 9-3: EXTERNAL CLOCK TIMING

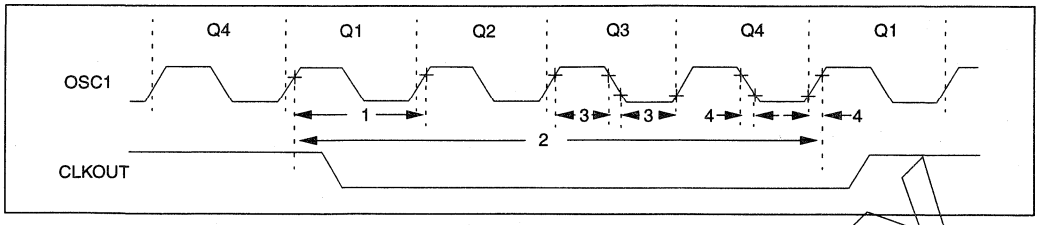

TABLE 9-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
	Fosc	**External CLKIN Frequency(1)**	DC	—	2	MHz	XT, RC osc	PIC16LF8X-04
			DC	—	4	MHz	XT, RC osc	PIC16F8X-04
			DC	—	10	MHz	HS osc	PIC16F8X-10
			DC	—	200	kHz	LP osc	PIC16LF8X-04
		Oscillator Frequency(1)	DC	—	2	MHz	RC osc	PIC16LF8X-04
			DC	—	4	MHz	RC osc	PIC16F8X-04
			0.1	—	2	MHz	XT osc	PIC16LF8X-04
			0.1	—	4	MHz	XT osc	PIC16F8X-04
			1.0	—	10	MHz	HS osc	PIC16F8X-10
			DC	—	200	kHz	LP osc	PIC16LF8X-04
1	Tosc	**External CLKIN Period(1)**	500	—	—	ns	XT, RC osc	PIC16LF8X-04
			250	—	—	ns	XT, RC osc	PIC16F8X-04
			100	—	—	ns	HS osc	PIC16F8X-10
			5.0	—	—	µs	LP osc	PIC16LF8X-04
		Oscillator Period(1)	500	—	—	ns	RC osc	PIC16LF8X-04
			250	—	—	ns	RC osc	PIC16F8X-04
			500	—	10,000	ns	XT osc	PIC16LF8X-04
			250	—	10,000	ns	XT osc	PIC16F8X-04
			100	—	1,000	ns	HS osc	PIC16F8X-10
			5.0	—	—	µs	LP osc	PIC16LF8X-04
2	Tcy	**Instruction Cycle Time(1)**	0.4	4/Fosc	DC	µs		
3	TosL, TosH	**Clock in (OSC1) High or Low Time**	60 *	—	—	ns	XT osc	PIC16LF8X-04
			50 *	—	—	ns	XT osc	PIC16F8X-04
			2.0 *	—	—	µs	LP osc	PIC16LF8X-04
			35 *	—	—	ns	HS osc	PIC16F8X-10
4	TosR, TosF	**Clock in (OSC1) Rise or Fall Time**	25 *	—	—	ns	XT osc	PIC16F8X-04
			50 *	—	—	ns	LP osc	PIC16LF8X-04
			15 *	—	—	ns	HS osc	PIC16F8X-10

* These parameters are characterized but no tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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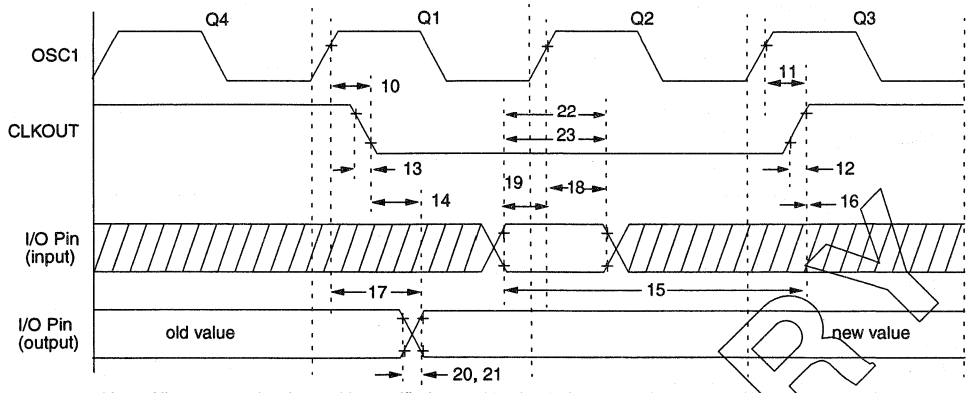
FIGURE 9-4: CLKOUT AND I/O TIMING



Note: All tests must be done with specified capacitive loads (Figure 9-2) 50 pF on I/O pins and CLKOUT.

TABLE 9-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	PIC16F8X	—	15	30 *	ns	Note 1
10A			PIC16LF8X	—	15	120 *	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	PIC16F8X	—	15	30 *	ns	Note 1
11A			PIC16LF8X	—	15	120 *	ns	Note 1
12	TckR	CLKOUT rise time	PIC16F8X	—	15	30 *	ns	Note 1
12A			PIC16LF8X	—	15	100 *	ns	Note 1
13	TckF	CLKOUT fall time	PIC16F8X	—	15	30 *	ns	Note 1
13A			PIC16LF8X	—	15	100 *	ns	Note 1
14	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY +20 *	ns	Note 1
15	TioV2ckH	Port in valid before	PIC16F8X	0.30TCY + 30 *	—	—	ns	Note 1
		CLKOUT↑	PIC16LF8X	0.30TCY + 80 *	—	—	ns	Note 1
16	TckH2iol	Port in hold after CLKOUT ↑		0 *	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to	PIC16F8X	—	—	125 *	ns	
		Port out valid	PIC16LF8X	—	—	250 *	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		TBD	—	—	ns	
20	TioR	Port output rise time	PIC16F8X	—	10	25 *	ns	
20A			PIC16LF8X	—	10	60 *	ns	
21	TioF	Port output fall time	PIC16F8X	—	10	25 *	ns	
21A			PIC16LF8X	—	10	60 *	ns	
22	Tinp	INT pin high	PIC16F8X	20 *	—	—	ns	
22A		or low time	PIC16LF8X	55 *	—	—	ns	
23	Trbp	RB7:RB4 change INT	PIC16F8X	TOSC §	—	—	ns	
23A		high or low time	PIC16LF8X	TOSC §	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

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Applicable Devices	F83	CR83	F84	CR84

FIGURE 9-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

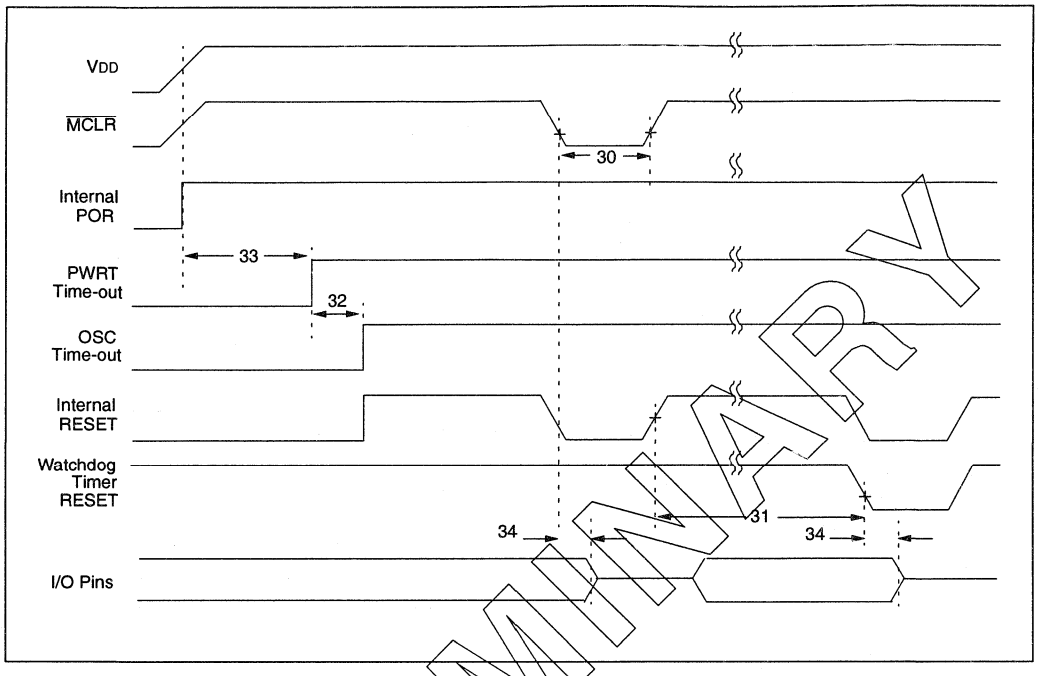

TABLE 9-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000 *	—	—	ns	2.0V ≤ VDD ≤ 6.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5.0V
32	Tost	Oscillation Start-up Timer Period		1024TOSC		ms	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V
34	TIOZ	I/O Hi-impedance from MCLR Low or reset	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Applicable Devices | F83 | CR83 | F84 | CR84

FIGURE 9-6: TIMER0 CLOCK TIMINGS

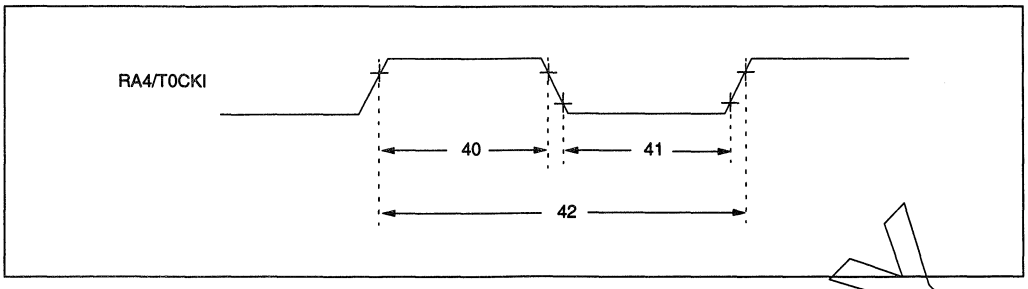

TABLE 9-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20 *	—	—	ns	
			With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				30 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20 *	—	—	ns	
			With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				20 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
42	Tt0P	T0CKI Period		TCY + 40 * N	—	—	ns	N = prescale value (2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Applicable Devices	F83	CR83	F84	CR84

NOTES:

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Applicable Devices	F83	CR83	F84	CR84

10.0 DC & AC CHARACTERISTICS GRAPHS/TABLES FOR PIC16F83 AND PIC16F84

NOT AVAILABLE AT THIS TIME.

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Applicable Devices	F83	CR83	F84	CR84

NOTES:

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Applicable Devices | F83 | CR83 | F84 | CR84

11.0 ELECTRICAL CHARACTERISTICS FOR PIC16CR83 AND PIC16CR84

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... -0.3 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... -0.3 to +14V

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.6V to (V_{DD} + 0.6V)

Total power dissipation (1) ..... 800 mW

Maximum current out of V_{SS} pin ..... 150 mA

Maximum current into V_{DD} pin ..... 100 mA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 20 mA

Maximum current sunk by PORTA ..... 80 mA

Maximum current sourced by PORTA ..... 50 mA

Maximum current sunk by PORTB ..... 150 mA

Maximum current sourced by PORTB ..... 100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Applicable Devices | F83 | CR83 | F84 | CR84

TABLE 11-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR84-04 PIC16CR83-04	PIC16CR84-10 PIC16CR83-10	PIC16LCR84-04 PIC16LCR83-04
RC	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 µA max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 5.5V WDT dis Freq: 4..0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 6.0 µA max. at 2V WDT dis Freq: 2.0 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 µA max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 µA typ. at 5.5V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 6.0 µA max. at 2V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 4.5 mA typ. at 5.5V IPD: 1.0 µA typ. at 4.5V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V typ. IPD: 1.0 µA typ. at 4.5V WDT dis Freq: 10 MHz max.	Do not use in HS mode
LP	VDD: 4.0V to 6.0V IDD: 35 µA typ. at 32 kHz, 3.0V IPD: 0.6 µA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	VDD: 2.0V to 6.0V IDD: 32 µA max. at 32 kHz, 3.0V IPD: 6.0 µA max. at 2V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices | F83 | CR83 | F84 | CR84

11.1 DC CHARACTERISTICS: PIC16CR84, PIC16CR83 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	4.0	—	6.0	V	XT, RC and LP osc configuration
D001A			4.5	—	5.5	V	HS osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current(2)					RC and XT osc configuration(4)
D010			—	1.8	4.5	mA	FOSC = 4.0 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 4.0 MHz, VDD = 5.5V (During EEPROM programming)
							HS OSC CONFIGURATION (PIC16CR84-10)
D013			—	5	10	mA	FOSC = 10 MHz, VDD = 5.5V
D020	IPD	Power-down Current(3)	—	7.0	28	µA	VDD = 4.0V, WDT enabled, industrial
D021			—	1.0	14	µA	VDD = 4.0V, WDT disabled, commercial
D021A			—	1.0	16	µA	VDD = 4.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

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Applicable Devices F83 CR83 F84 CR84

11.2 DC CHARACTERISTICS: PIC16LCR84, PIC16LCR83 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.0	—	6.0	V	XT, RC, and LP osc configuration
D002	VDR	RAM Data Retention Voltage(1)	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	IDD	Supply Current(2)					RC and XT osc configuration(4)
D010			—	1	4	mA	FOSC = 2.0 MHz, VDD = 5.5V
D010A			—	7.3	10	mA	FOSC = 2.0 MHz, VDD = 5.5V (During EEPROM programming)
							LP osc configuration
D014			—	15	32	µA	FOSC = 32 kHz, VDD = 2.0V, WDT disabled
D020	IPD	Power-down Current(3)	—	3.0	16	µA	VDD = 2.0V, WDT enabled, industrial
D021			—	0.4	5.0	µA	VDD = 2.0V, WDT disabled, commercial
D021A			—	0.4	6.0	µA	VDD = 2.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

PRELIMINARY

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Applicable Devices | F83 | CR83 | F84 | CR84

11.3 DC CHARACTERISTICS: PIC16CR84A, PIC16CR83 (Commercial, Industrial) PIC16LCR84, PIC16LCR83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage** I/O ports					
D030		with TTL buffer	VSS	—	0.8	V	4.5 V ≤ VDD ≤ 5.5 V
D030A			VSS	—	0.16VDD	V	entire range(4)
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	entire range
D032		MCLR, RA4/T0CKI	VSS	—	0.2VDD	V	
D033		OSC1 (XT, HS and LP modes)(1)	VSS	—	0.3VDD	V	
D034		OSC1 (RC mode)	VSS	—	0.1VDD	V	
	VIH	**Input High Voltage** I/O ports		—			
D040		with TTL buffer	2.4	—	VDD	V	4.5 V ≤ VDD ≤ 5.5V
D040A			0.48VDD	—	VDD	V	entire range(4)
D041		with Schmitt Trigger buffer	0.45VDD	—	VDD		entire range
D042		MCLR, RA4/T0CKI, OSC1 (RC mode)	0.85 VDD	—	VDD	V	
D043		OSC1 (XT, HS and LP modes)(1)	0.7 VDD	—	VDD	V	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	TBD	—	—	V	
D070	IPURB	PORTB weak pull-up current	50*	250*	400*	µA	VDD = 5.0V, VPIN = VSS
		Input Leakage Current(2,3)					
D060	IIL	I/O ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		MCLR, RA4/T0CKI	—	—	±5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
		Output Low Voltage					
D080	VOL	I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
D083		OSC2/CLKOUT	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(3)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D092		OSC2/CLKOUT	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16CR8X with an external clock while the device is in RC mode, otherwise chip damage may result.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may use better of the two specs.

PRELIMINARY

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Applicable Devices | F83 | CR83 | F84 | CR84

11.4 DC CHARACTERISTICS: PIC16CR84A, PIC16CR83 (Commercial, Industrial) PIC16LCR84A, PIC16LCR83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
		Data EEPROM Memory					
D120	ED	Endurance	1M	10M	—	E/W	25°C at 5V
D121	VDRW	VDD for read/write	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	—	10	ms	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Applicable Devices	F83	CR83	F84	CR84

TABLE 11-2: TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase symbols (pp) and their meanings:

pp			
2	to	os,osc	OSC1
ck	CLKOUT	ost	oscillator start-up timer
cy	cycle time	pwrt	power-up timer
io	I/O port	rbt	RBx pins
inp	INT pin	t0	T0CKI
mc	$\overline{\text{MCLR}}$	wdt	watchdog timer

Uppercase symbols and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	High Impedance

FIGURE 11-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.

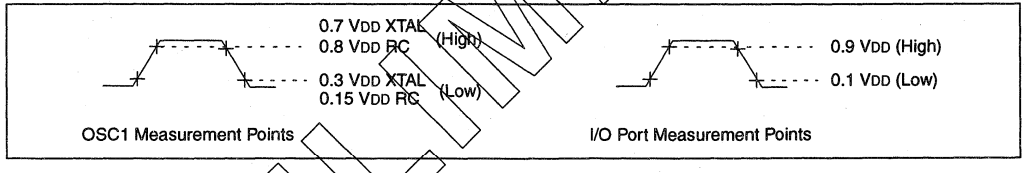
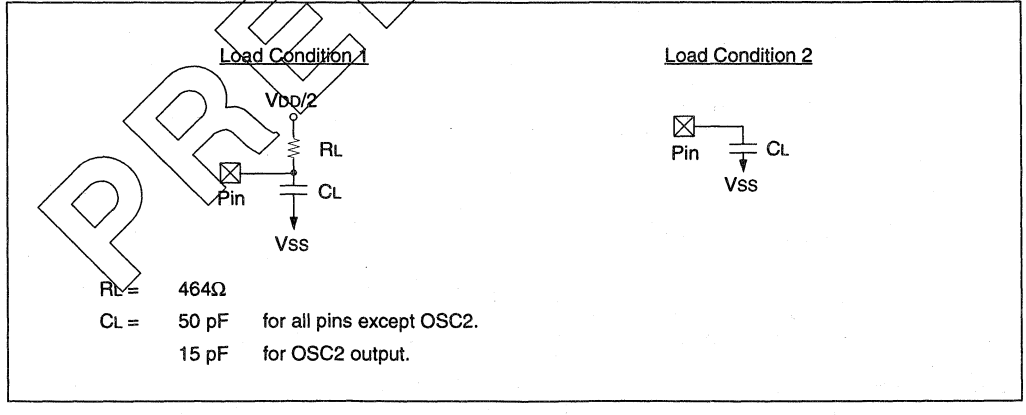


FIGURE 11-2: LOAD CONDITIONS



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Applicable Devices | F83 | CR83 | F84 | CR84

11.5 Timing Diagrams and Specifications

FIGURE 11-3: EXTERNAL CLOCK TIMING

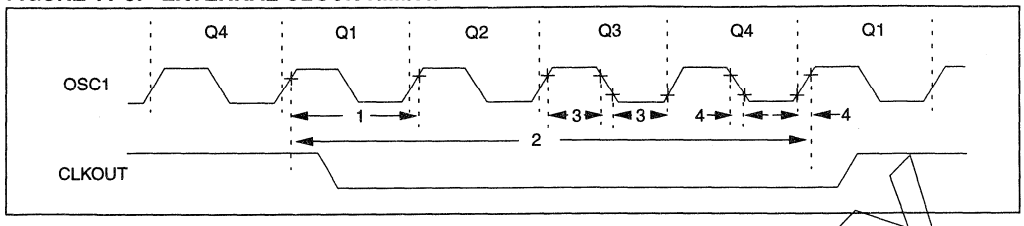

TABLE 11-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
	FOSC	**External CLKIN Frequency(1)**	DC	—	2	MHz	XT, RC osc	PIC16LCR8X-04
			DC	—	4	MHz	XT, RC osc	PIC16CR8X-04
			DC	—	10	MHz	HS osc	PIC16CR8X-10
			DC	—	200	kHz	LP osc	PIC16LCR8X-04
		Oscillator Frequency(1)	DC	—	2	MHz	RC osc	PIC16LCR8X-04
			DC	—	4	MHz	RC osc	PIC16CR8X-04
			0.1	—	2	MHz	XT osc	PIC16LCR8X-04
			0.1	—	4	MHz	XT osc	PIC16CR8X-04
			1.0	—	10	MHz	HS osc	PIC16CR8X-10
			DC	—	200	kHz	LP osc	PIC16LCR8X-04
1	TOSC	**External CLKIN Period(1)**	500	—	—	ns	XT, RC osc	PIC16LCR8X-04
			250	—	—	ns	XT, RC osc	PIC16CR8X-04
			100	—	—	ns	HS osc	PIC16CR8X-10
			5.0	—	—	µs	LP osc	PIC16LCR8X-04
		Oscillator Period(1)	500	—	—	ns	RC osc	PIC16LCR8X-04
			250	—	—	ns	RC osc	PIC16CR8X-04
			500	—	10,000	ns	XT osc	PIC16LCR8X-04
			250	—	10,000	ns	XT osc	PIC16CR8X-04
			100	—	1,000	ns	HS osc	PIC16CR8X-10
			5.0	—	—	µs	LP osc	PIC16LCR8X-04
2	TCY	**Instruction Cycle Time(1)**	0.4	4/Fosc	DC	µs		
3	TOSL, TOSH	**Clock in (OSC1) High or Low Time**	60 *	—	—	ns	XT osc	PIC16LCR8X-04
			50 *	—	—	ns	XT osc	PIC16CR8X-04
			2.0 *	—	—	µs	LP osc	PIC16LCR8X-04
			35 *	—	—	ns	HS osc	PIC16CR8X-10
4	TOSR, TOSF	**Clock in (OSC1) Rise or Fall Time**	25 *	—	—	ns	XT osc	PIC16CR8X-04
			50 *	—	—	ns	LP osc	PIC16LCR8X-04
			15 *	—	—	ns	HS osc	PIC16CR8X-10

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

PRELIMINARY

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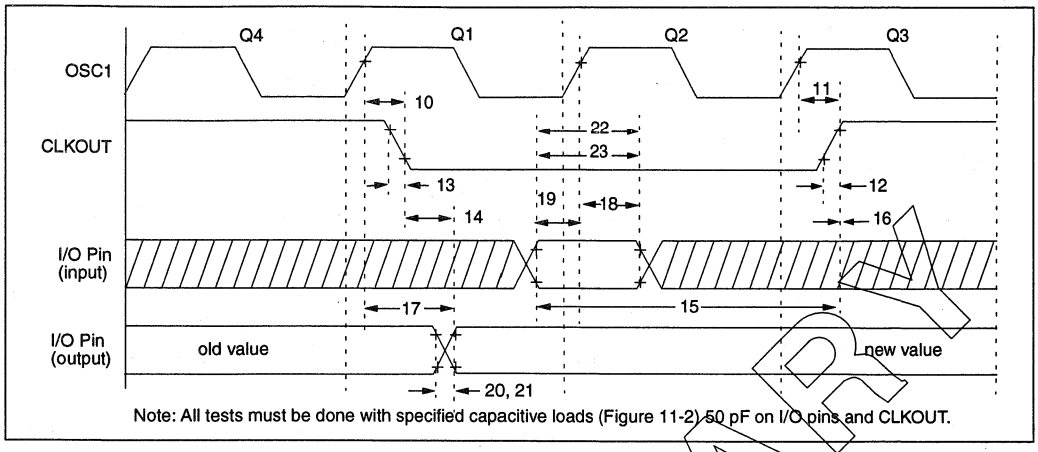
FIGURE 11-4: CLKOUT AND I/O TIMING



Note: All tests must be done with specified capacitive loads (Figure 11-2) 50 pF on I/O pins and CLKOUT.

TABLE 11-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	PIC16CR8X	—	15	30 *	ns	Note 1
10A			PIC16LCR8X	—	15	120 *	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	PIC16CR8X	—	15	30 *	ns	Note 1
11A			PIC16LCR8X	—	15	120 *	ns	Note 1
12	TckR	CLKOUT rise time	PIC16CR8X	—	15	30 *	ns	Note 1
12A			PIC16LCR8X	—	15	100 *	ns	Note 1
13	TckF	CLKOUT fall time	PIC16CR8X	—	15	30 *	ns	Note 1
13A			PIC16LCR8X	—	15	100 *	ns	Note 1
14	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY +20 *	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	PIC16CR8X	0.30TCY + 30 *	—	—	ns	Note 1
			PIC16LCR8X	0.30TCY + 80 *	—	—	ns	Note 1
16	TckH2iol	Port in hold after CLKOUT ↑		0 *	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	PIC16CR8X	—	—	125 *	ns	
			PIC16LCR8X	—	—	250 *	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		TBD	—	—	ns	
20	TioR	Port output rise time	PIC16CR8X	—	10	25 *	ns	
20A			PIC16LCR8X	—	10	60 *	ns	
21	TioF	Port output fall time	PIC16CR8X	—	10	25 *	ns	
21A			PIC16LCR8X	—	10	60 *	ns	
22	Tinp	INT pin high or low time	PIC16CR8X	20 *	—	—	ns	
22A			PIC16LCR8X	55 *	—	—	ns	
23	Trbp	RB7:RB4 change INT high or low time	PIC16CR8X	TOSC §	—	—	ns	
23A			PIC16LCR8X	TOSC §	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

PRELIMINARY

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Applicable Devices F83 | CR83 | F84 | CR84

FIGURE 11-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

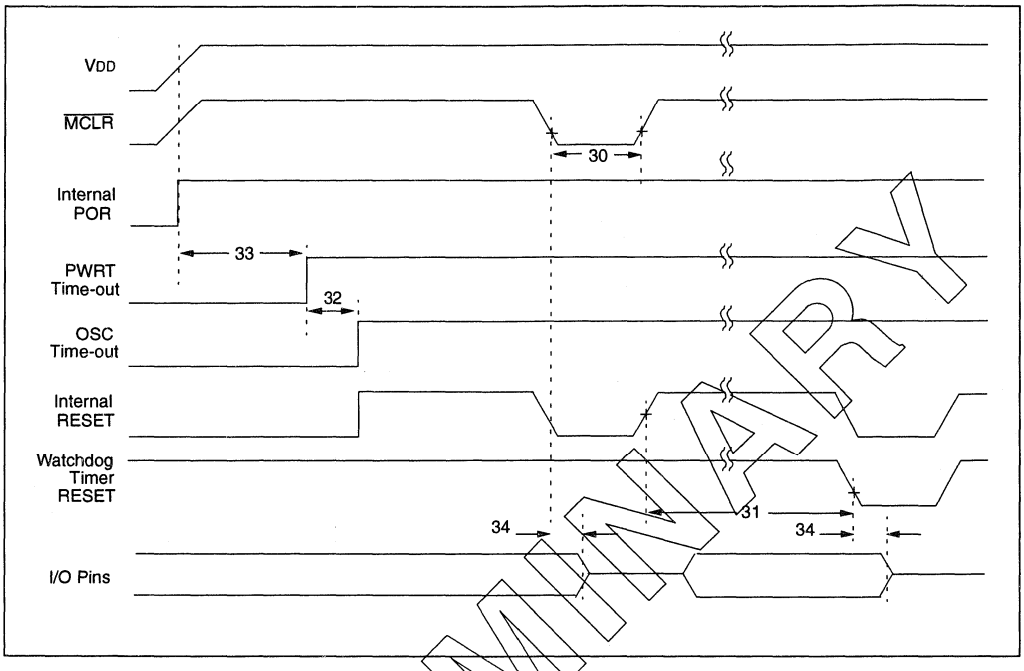

TABLE 11-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000 *	—	—	ns	2.0V ≤ VDD ≤ 6.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5.0V
32	Tost	Oscillation Start-up Timer Period		1024Tosc		ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V
34	TIOZ	I/O Hi-impedance from MCLR Low or reset	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PRELIMINARY

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FIGURE 11-6: TIMER0 CLOCK TIMINGS

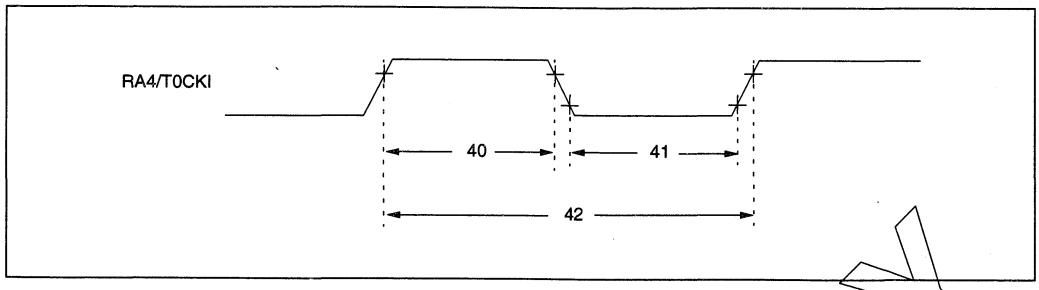

TABLE 11-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20 *	—	—	ns	
			With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				30 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20 *	—	—	ns	
			With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				20 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
42	Tt0P	T0CKI Period		TCY + 40 * N	—	—	ns	N = prescale value (2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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Applicable Devices	F83	CR83	F84	CR84

NOTES:

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12.0 DC & AC CHARACTERISTICS GRAPHS/TABLES FOR PIC16CR83 AND PIC16CR84

NOT AVAILABLE AT THIS TIME.

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Applicable Devices	F83	CR83	F84	CR84

NOTES:

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APPENDIX A: FEATURE IMPROVEMENTS

The following is the list of feature improvements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and the register file (128 bytes now versus 32 bytes before).
2. A PC latch register (PCLATH) is added to handle program memory paging. PA2, PA1 and PA0 bits are removed from the status register and placed in the option register.
3. Data memory paging is redefined slightly. The STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions, TRIS and OPTION, are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, the Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change features.
13. T0CKI pin is also a port pin (RA4/T0CKI).
14. FSR is a full 8-bit register.
15. "In system programming" is made possible. The user can program PIC16FXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16F8X, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables for reallocation.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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APPENDIX C: WHAT'S NEW

Not applicable - new document.

APPENDIX D: WHAT'S CHANGES

Not applicable - new document.

APPENDIX E: PIC16C84 TO PIC16F83/CR83 AND PIC16F84/CR84 CONVERSION CONSIDERATIONS

This appendix discusses some of the issues that you may encounter as you convert your design from a PIC16C84 to a PIC16F83 or PIC16F84 device. These new devices are:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84

Some of the issues that may be encountered are:

1. The polarity of the PWRTE configuration bit has been reversed. Ensure that the programmer has this bit correctly set before programming.
2. The PIC16F84 and PIC16CR84 have larger RAM sizes. Ensure that this does not cause an issue with your program.
3. The $\overline{MCLR}$ pin now has an on-chip filter. The input signal on the $\overline{MCLR}$ pin will require a longer low pulse to generate an interrupt.
4. Many electrical specifications have been improved. Compare the electrical specifications of the two devices to ensure that this will not cause a compatibility issue.

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PIC16F8X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Frequency Range	Temperature Range	Package	Pattern

Device	PIC16F8X[2], PIC16F8XT[3] PIC16LF8X[2], PIC16LF8XT[3] PIC16CR8X[2], PIC16CR8XT[3] PIC16LCR8X[2], PIC16LCR8XT[3]	
Frequency Range	04 10	= 4 MHz = 10 MHz
Temperature Range	b[1] I	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial)
Package	P SO	= PDIP = SOIC (Gull Wing, 300 mil body)
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)	

Examples:

a) PIC16F84 -04/P 301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern #301.

b) PIC16LF84 - 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended VDD limits.

c) PIC16CR84 - 10I/P = ROM program memory, Industrial temp., PDIP package, 10MHz, normal VDD limits.

Note 1: b = blank
2: F = Standard VDD range
LF = Extended VDD range
CR = ROM Version, Standard VDD range
LCR = ROM Version, Extended VDD range
3: T = in tape and reel - SOIC, SSOP packages only.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see last page)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Development Tools

For the latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302. The latest version of Development Tools software can be downloaded from either our Bulletin Board or Worldwide Web Site. (Information on how to connect to our BBS or WWW site can be found in the On-Line Support section of this data sheet.)

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PIC16C822

EPROM/EEPROM 8-Bit Microcontroller Product Brief

High Performance RISC CPU Features:

- Simple instruction set - 35 total
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle
- 14-bit program word
- 8-bit data word
- ★ 2048 words program memory
- ★ **64 bytes EEPROM data memory**
- 128 bytes RAM data memory
- Interrupt capability
- 18 special function hardware registers
- Eight levels of hardware stack
- Direct, Indirect and Relative addressing modes

Peripheral Features:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- ★ Analog comparator module with:
  - 2 analog comparators
  - Programmable on-chip voltage reference (V_{REF}) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs can be output signals
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

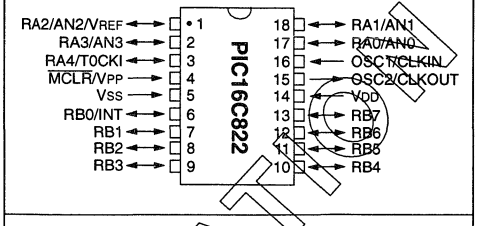
- ★ **64 bytes data EEPROM**
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Four user programmable ID locations

CMOS Technology:

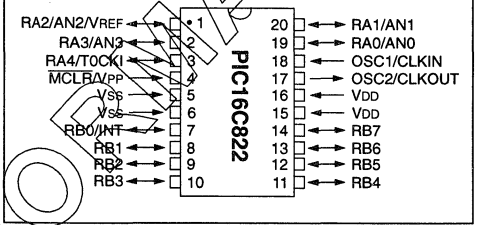
- ★ Low-power, high-speed CMOS **EPROM/EEPROM** technology
- Fully static design
- Wide operating voltage range
  - 2.5V to 6.0V

Pin Diagram

PDIP, SOIC, Windowed CERDIP



★ **SSOP**



- Commercial, industrial and automotive temperature ranges
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - ★ < 1.0 µA typical standby current @ 3.0V

Applications:

- Remote Keyless Entry (RKE)
- Smart Sensors / Smart Cards
- Automobile Immobilizer
- Home Security
- RF Tags
- Settop converter boxes
- Instrumentation
- Garage door opener receiver

PRELIMINARY
DEVICE INFORMATION

11

NOTES:

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PIC16CR8XA

ROM/EEPROM 8-Bit Microcontroller Product Brief

Devices included:

- PIC16CR83A
- PIC16CR84A

High Performance RISC CPU:

- Simple instruction set - 35 total
- All single-cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle

Device	ROM Program	EEPROM Data	RAM Data
PIC16CR83A	512*	64	36
PIC16CR84A	1K*	64	68

- PIC16CXX MCU core
- 14-bit program word
- 8-bit data word
- Interrupt capability
- 18 special function hardware registers
- Eight levels of hardware stack
- Direct, Indirect and Relative addressing modes

Peripheral Features:

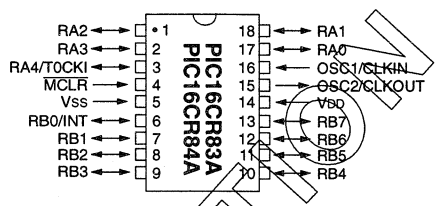
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

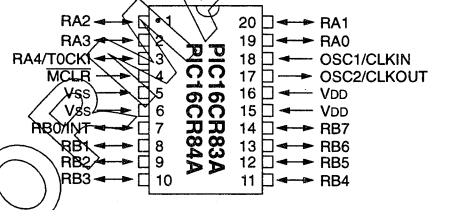
- ★ 64 bytes data EEPROM
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options

Pin Diagram

PDIP, SOIC



★ SSOP



CMOS Technology:

- ★ Low-power, high-speed CMOS ROM/EEPROM technology
- Fully static design
- Wide operating voltage range
  - 2.5V to 6.0V
- Commercial, industrial and automotive temperature ranges
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - ★ < 1.0 µA typical standby current @ 3.0V

Applications:

- Remote Keyless Entry (RKE)
- Smart Sensors / Smart Cards
- Automobile Immobilizer
- Home Security
- RF Tags
- Settop converter boxes
- Instrumentation
- Garage door opener receiver

ADVANCE INFORMATION

*See PIC16C822 for 2K word EPROM program memory.

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NOTES:

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SECTION 12
PIC16C9XX MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC16C9XX 8-Bit CMOS Microcontroller with LCD Driver 12-1

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PIC16C9XX

8-Bit CMOS Microcontroller with LCD Driver

Devices included in this data sheet:

- PIC16C923
- PIC16C924

Microcontroller Core Features:

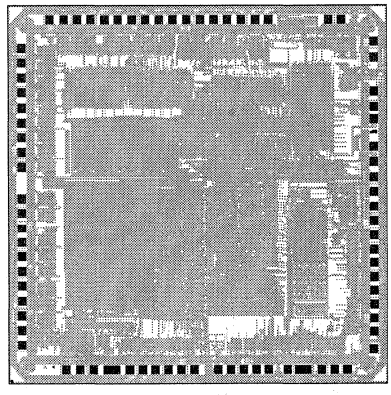
- High performance RISC CPU
- Only 35 single word instructions to learn
- 4K x 14 on-chip EPROM program memory
- 176 x 8 general purpose registers (SRAM)
- All single cycle instructions (500 ns) except for program branches which are two-cycle
- Operating speed: DC - 8 MHz clock input
  DC - 500 ns instruction cycle
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes

Peripheral Features:

- 25 I/O pins with individual direction control
- 25-27 input only pins
- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- One pin that can be configured a capture input, PWM output, or compare output
  - Capture is 16-bit, max. resolution 31.25 ns
  - Compare is 16-bit, max. resolution 500 ns
  - PWM resolution is 1- to 10-bits. Maximum PWM frequency @ 8-bit resolution = 32 kHz, @ 10-bit resolution = 8 kHz
- Programmable LCD timing module
  - Multiple LCD timing sources available
  - Can drive LCD panel while in Sleep mode
  - Static, 1/2, 1/3, 1/4 multiplex
  - Static drive and 1/3 bias capability
  - 16 bytes of dedicated LCD RAM
  - Up to 32 segments, up to 4 commons

Common	Segment	Pixels
1	32	32
2	31	62
3	30	90
4	29	116

Available in Die Form



- Synchronous Serial Port (SSP) with SPI™ and I²C™
- 8-bit multichannel Analog to Digital converter (PIC16C924 only)

Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-system programming (via two pins)

CMOS Technology

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range: 3.0V to 6.0V
- Commercial and Industrial temperature ranges
- Low-power consumption:
  - < 2 mA @ 5.5V, 4 MHz
  - 22.5 µA typical @ 4V, 32 kHz
  - < 1 µA typical standby current @ 3.0V

I²C is a trademark of Philips Corporation. SPI is a trademark of Motorola Corporation.

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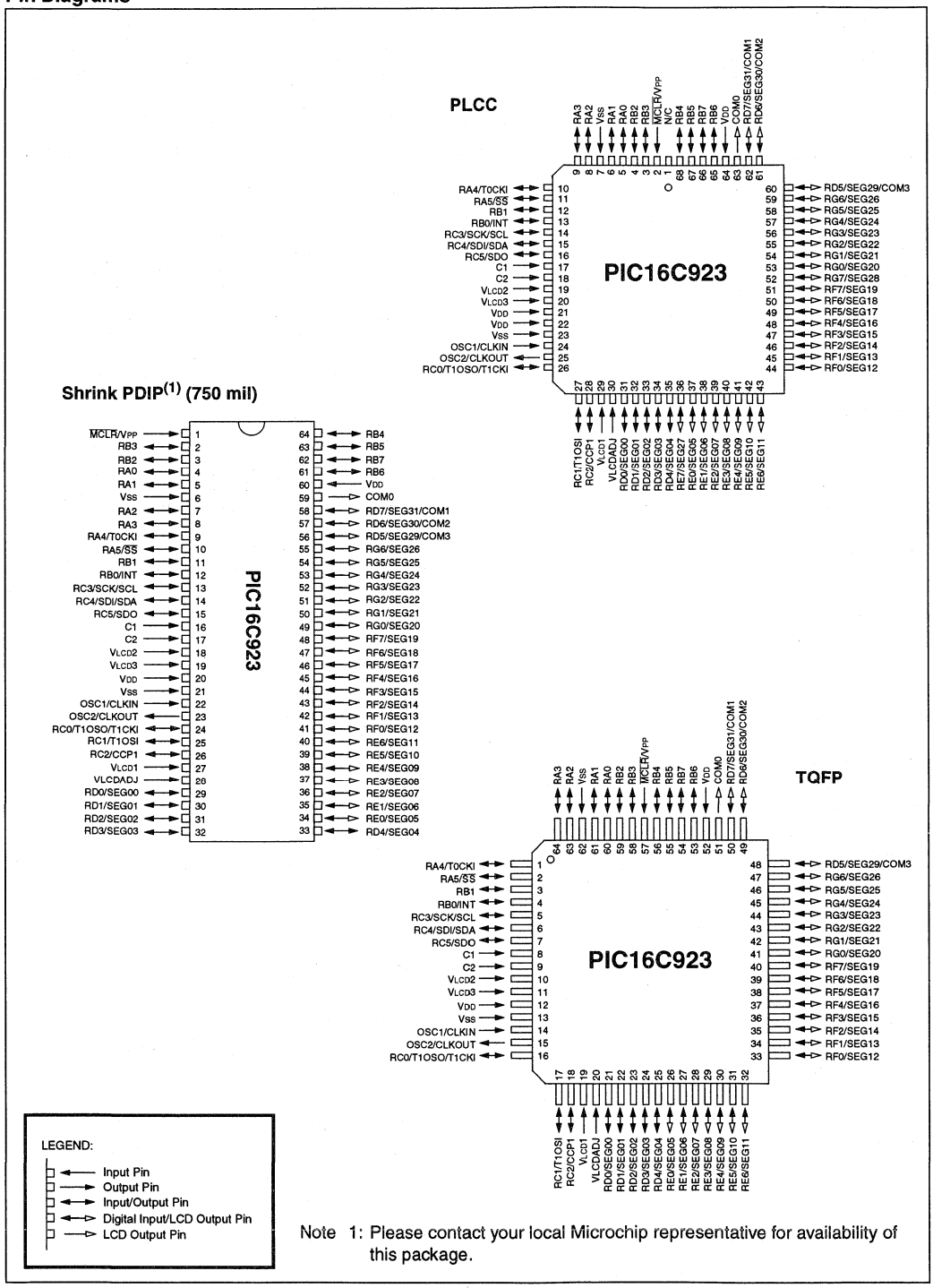
Pin Diagrams



Note 1: Please contact your local Microchip representative for availability of this package.

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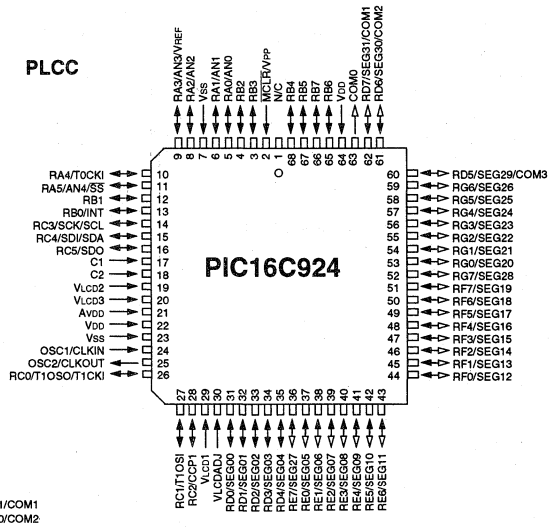
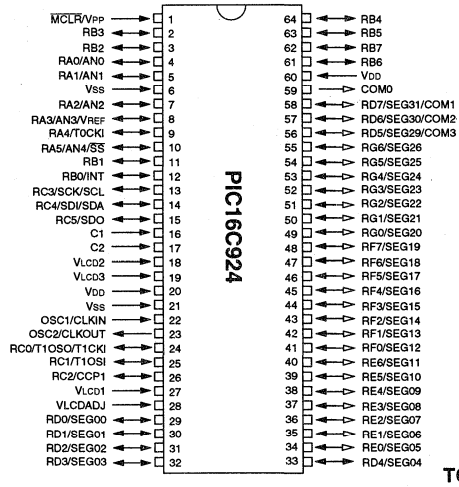
Pin Diagrams (Cont.'d)

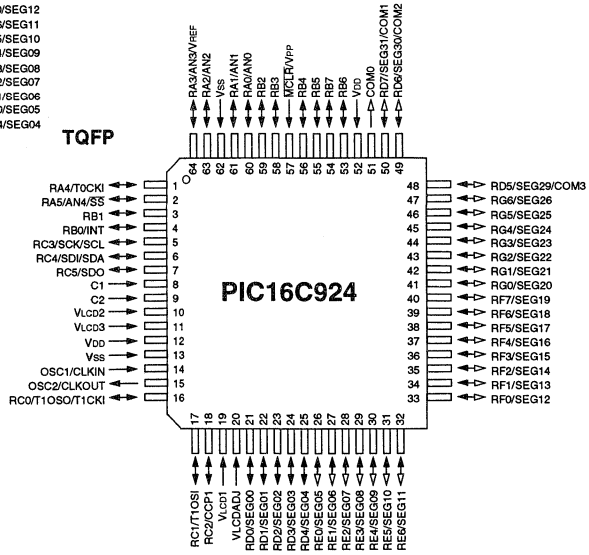
PLCC



Shrink PDIP(1) (750 mil)



TQFP



LEGEND:

- Input Pin
- Output Pin
- Input/Output Pin
- Digital Input/LCD Output Pin
- LCD Output Pin

Note 1: Please contact your local Microchip representative for availability of this package.

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To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

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1.0 GENERAL DESCRIPTION

The PIC16C9XX is a family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers with an integrated LCD Driver module, in the PIC16CXX mid-range family.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16CXX microcontroller family has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The **PIC16C923** devices have 176 bytes of RAM and 25 I/O pins. In addition several peripheral features are available including: three timer/counters, one Capture/Compare/PWM module, one serial port and one LCD module. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The LCD module features programmable multiplex mode (static, 1/2, 1/3 and 1/4) and drive bias (static and 1/3). It is capable of driving up to 32 segments and up to 4 commons. It can also drive the LCD panel while in SLEEP mode.

The **PIC16C924** devices have 176 bytes of RAM and 25 I/O pins. In addition several peripheral features are available including: three timer/counters, one Capture/Compare/PWM module, one serial port and one LCD module. The Synchronous Serial Port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Integrated Circuit (I^2C) bus. The LCD module features programmable multiplex mode (static, 1/2, 1/3 and 1/4) and drive bias (static and 1/3). It is capable of driving up to 32 segments and up to 4 commons. It can also drive the LCD panel while in SLEEP mode. The PIC16C924 also has an 5-channel high-speed 8-bit A/D. The 8-bit resolution is ideally suited for applications requiring low-cost analog interface, e.g. thermostat control, pressure sensing, and meters.

The PIC16C9XX family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) feature provides a power saving mode. The user can wake up the chip from SLEEP through several external and internal interrupts and reset(s).

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides recovery in the event of a software lock-up.

A UV erasable CERQUAD (compatible with PLCC) packaged version is ideal for code development while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC16C9XX family fits perfectly in applications ranging from handheld meters, thermostats, to home security products. The EPROM technology makes customization of application programs (LCD panels, calibration constants, sensor interfaces, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16C9XX very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, capture and compare, PWM functions and coprocessor applications).

1.1 Family and Upward Compatibility

Users familiar with the PIC16C5X microcontroller family will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for the PIC16C5X can be easily ported to the PIC16CXX family of devices (Appendix B).

1.2 Development Support

The PIC16C9XX family will be supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also in development.

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TABLE 1-1: PIC16C9XX FAMILY OF DEVICES

	Clock	Memory			Peripherals					Features					
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (words)	Data Memory (bytes)	Timer Module(s)	Capture/Compare/PWM Module(s)	Serial Port(s) (SPI/I²C, USART)	Parallel Slave Port	A/D Converter (8-bit) Channels	LCD Module	Interrupt Sources	I/O Pins	Input Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Brown-out Reset	Packages
PIC16C923	8	4K	176	TMR0, TMR1, TMR2	1	SPI/I²C	—	—	4 Com 32 Seg	8	25	27	3.0-6.0	Yes	—	64-pin SDIP[1], TQFP, 68-pin PLCC, DIE
PIC16C924	8	4K	176	TMR0, TMR1, TMR2	1	SPI/I²C	—	5	4 Com 32 Seg	9	25	27	3.0-6.0	Yes	—	64-pin SDIP[1], TQFP, 68-pin PLCC, DIE

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.
All PIC16CXX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip representative for availability of this package.

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2.0 PIC16C9XX DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C9XX Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C9XX family, there are two device "types" as indicated in the device number:

1. **C**, as in PIC16**C**924. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**924. These devices have EPROM type memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERQUAD package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes. Microchip's PICSTART® Plus and PRO MATE™ II programmers both support the PIC16C9XX. Third party programmers also are available; refer to the *Microchip Third Party Guide* for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle (500 ns @ 8 MHz) except for program branches.

The PIC16C923 and PIC16C924 both address 4K x 14 of program memory and 176 x 8 of data memory.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient, thus significantly reducing the learning curve.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ bit and a $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 3-1: PIC16C923 BLOCK DIAGRAM

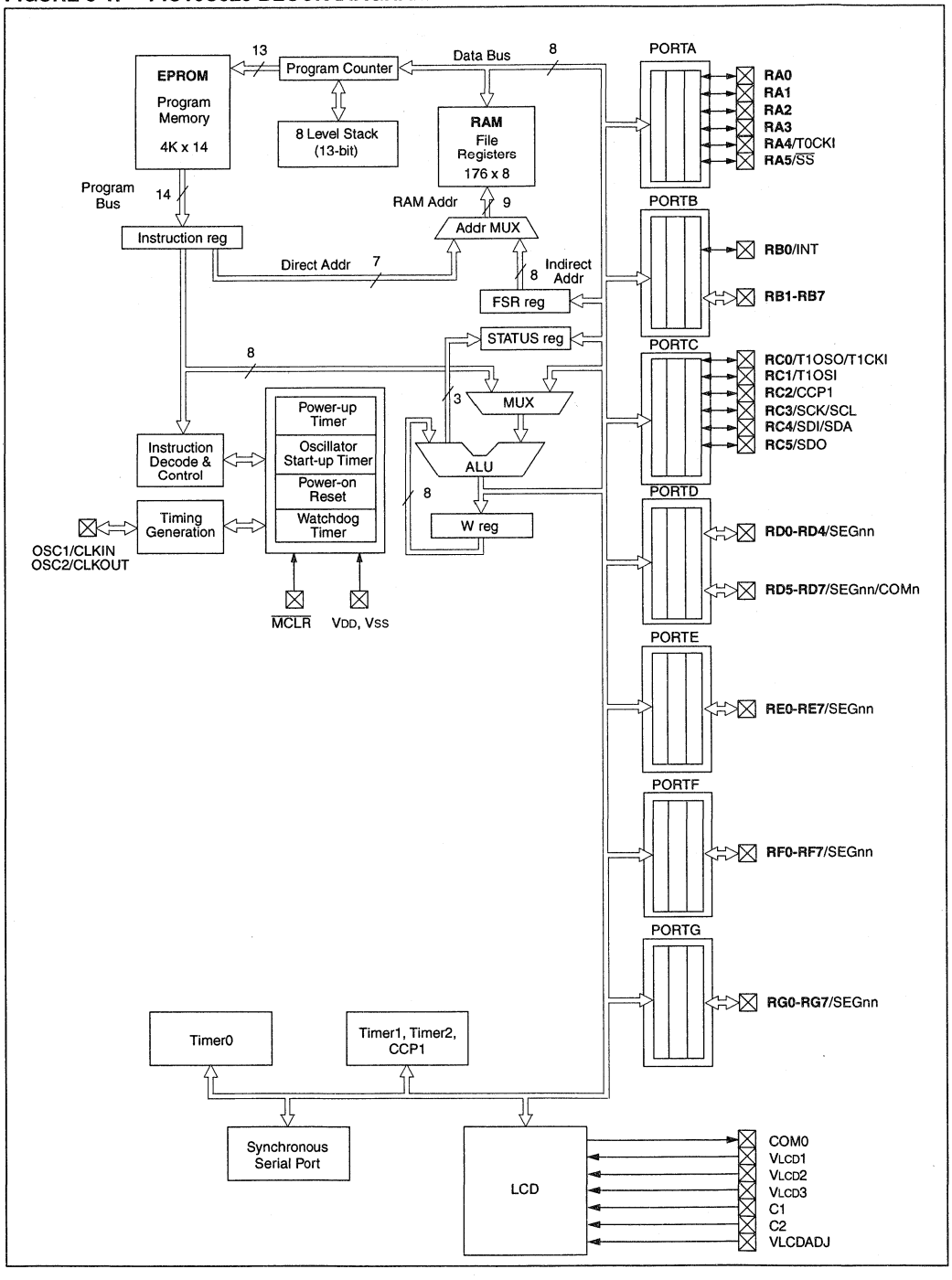

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FIGURE 3-2: PIC16C924 BLOCK DIAGRAM

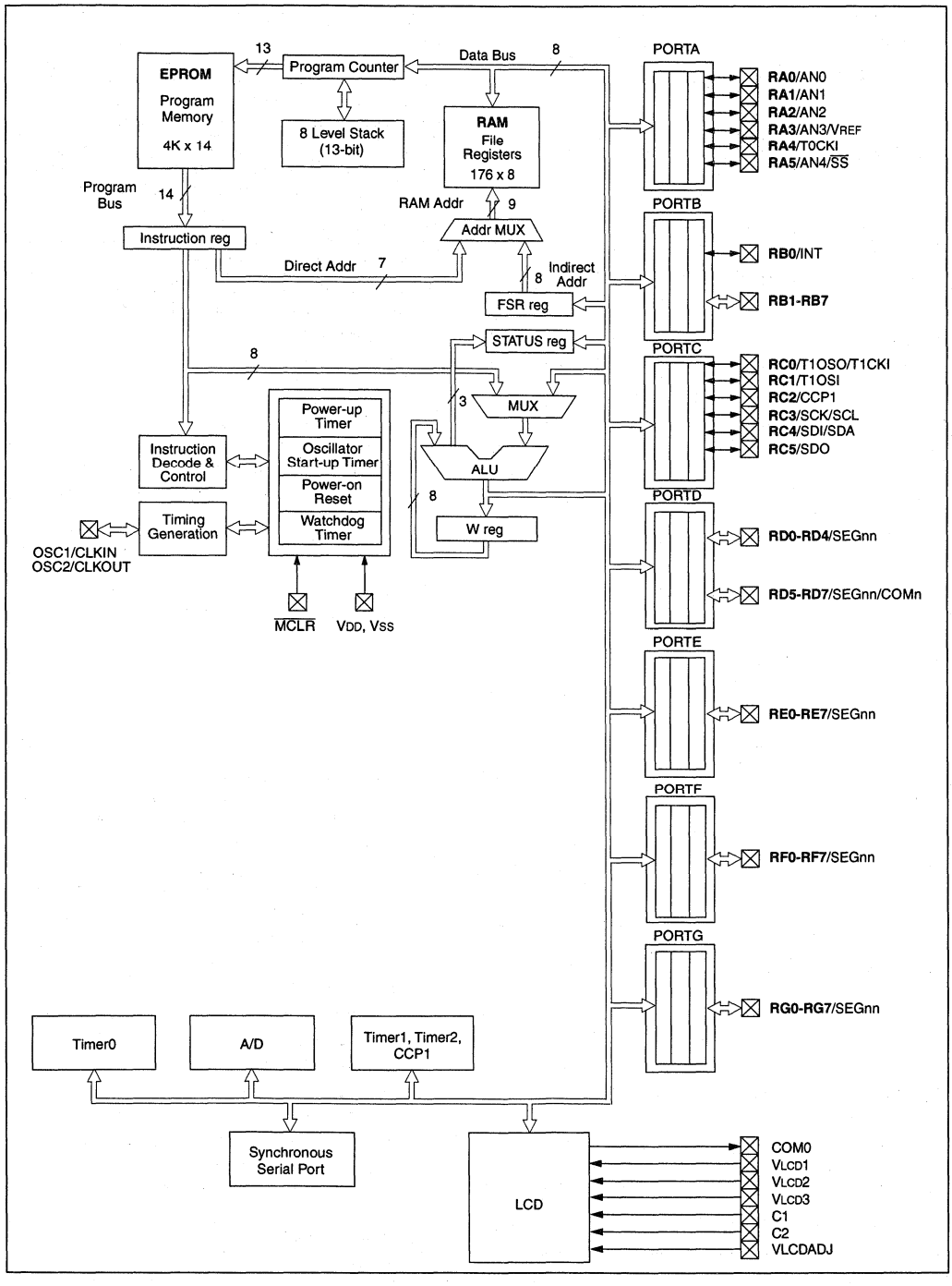

TABLE 3-1: PIC16C9XX PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	TQFP Pin#	Pin Type	Buffer Type	Description
OSC1/CLKIN	22	24	14	I	ST/CMOS	Oscillator crystal input/external clock source input. This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
OSC2/CLKOUT	23	25	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	57	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port. The AN and VREF multiplexed functions are used by the PIC16C924 only.
RA0/AN0	4	5	60	I/O	TTL	Analog input0
RA1/AN1	5	6	61	I/O	TTL	Analog input1
RA2/AN2	7	8	63	I/O	TTL	Analog input2
RA3/AN3/VREF	8	9	64	I/O	TTL	Analog input3/A/D Voltage Reference
RA4/T0CKI	9	10	1	I/O	ST	RA4 can also be selected to be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/AN4/$\overline{SS}$	10	11	2	I/O	TTL	RA5 can also be the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT	12	13	4	I/O	TTL/ST	RB0 can also be selected as an external interrupt pin. This buffer is a Schmitt Trigger input when configured as an external interrupt.
RB1	11	12	3	I/O	TTL	
RB2	3	4	59	I/O	TTL	
RB3	2	3	58	I/O	TTL	
RB4	64	68	56	I/O	TTL	Interrupt on change pin.
RB5	63	67	55	I/O	TTL	Interrupt on change pin.
RB6	61	65	53	I/O	TTL/ST	Interrupt on change pin. Serial programming clock. This buffer is a Schmitt Trigger input when used in serial programming mode.
RB7	62	66	54	I/O	TTL/ST	Interrupt on change pin. Serial programming data. This buffer is a Schmitt Trigger input when used in serial programming mode.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	24	26	16	I/O	ST	RC0 can also be selected as a Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI	25	27	17	I/O	ST	RC1 can also be selected as a Timer1 oscillator input.
RC2/CCP1	26	28	18	I/O	ST	RC2 can also be selected as a Capture input/Compare output/PWM output.
RC3/SCK/SCL	13	14	5	I/O	ST	RC3 can also be selected as the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	14	15	6	I/O	ST	RC4 can also be selected as the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	15	16	7	I/O	ST	RC5 can also be selected as the SPI Data Out (SPI mode).
C1	16	17	8	P		LCD Voltage Generation
C2	17	18	9	P		LCD Voltage Generation

Legend: I = input O = output P = power L = LCD Driver
— = Not used TTL = TTL input ST = Schmitt Trigger input

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TABLE 3-1: PIC16C9XX PINOUT DESCRIPTION (Cont.'d)

Pin Name	DIP Pin#	PLCC Pin#	TQFP Pin#	Pin Type	Buffer Type	Description
COM0	59	63	51	L		Common Driver0
						PORTD is a digital input/output port. These pins are also used as LCD Segment and/or Common Drivers.
RD0/SEG00	29	31	21	I/O/L	ST	Segment Driver00/Digital Input/Output
RD1/SEG01	30	32	22	I/O/L	ST	Segment Driver01/Digital Input/Output
RD2/SEG02	31	33	23	I/O/L	ST	Segment Driver02/Digital Input/Output
RD3/SEG03	32	34	24	I/O/L	ST	Segment Driver03/Digital Input/Output
RD4/SEG04	33	35	25	I/O/L	ST	Segment Driver04/Digital Input/Output
RD5/SEG29/COM3	56	60	48	I/L	ST	Segment Driver29/Common Driver3/Digital Input
RD6/SEG30/COM2	57	61	49	I/L	ST	Segment Driver30/Common Driver2/Digital Input
RD7/SEG31/COM1	58	62	50	I/L	ST	Segment Driver31/Common Driver1/Digital Input
						PORTE is a digital input or LCD Segment Driver port.
RE0/SEG05	34	37	26	I/L	ST	Segment Driver05
RE1/SEG06	35	38	27	I/L	ST	Segment Driver06
RE2/SEG07	36	39	28	I/L	ST	Segment Driver07
RE3/SEG08	37	40	29	I/L	ST	Segment Driver08
RE4/SEG09	38	41	30	I/L	ST	Segment Driver09
RE5/SEG10	39	42	31	I/L	ST	Segment Driver10
RE6/SEG11	40	43	32	I/L	ST	Segment Driver11
RE7/SEG27	-	36	-	I/L	ST	Segment Driver27 (Not available on 64-pin devices)
						PORTF is a digital input or LCD Segment Driver port.
RF0/SEG12	41	44	33	I/L	ST	Segment Driver12
RF1/SEG13	42	45	34	I/L	ST	Segment Driver13
RF2/SEG14	43	46	35	I/L	ST	Segment Driver14
RF3/SEG15	44	47	36	I/L	ST	Segment Driver15
RF4/SEG16	45	48	37	I/L	ST	Segment Driver16
RF5/SEG17	46	49	38	I/L	ST	Segment Driver17
RF6/SEG18	47	50	39	I/L	ST	Segment Driver18
RF7/SEG19	48	51	40	I/L	ST	Segment Driver19
						PORTG is a digital input or LCD Segment Driver port.
RG0/SEG20	49	53	41	I/L	ST	Segment Driver20
RG1/SEG21	50	54	42	I/L	ST	Segment Driver21
RG2/SEG22	51	55	43	I/L	ST	Segment Driver22
RG3/SEG23	52	56	44	I/L	ST	Segment Driver23
RG4/SEG24	53	57	45	I/L	ST	Segment Driver24
RG5/SEG25	54	58	46	I/L	ST	Segment Driver25
RG6/SEG26	55	59	47	I/L	ST	Segment Driver26
RG7/SEG28	—	52	—	I/L	ST	Segment Driver28 (Not available on 64-pin devices)
VLCDADJ	28	30	20	P		LCD Voltage Generation
AVDD	—	21	—	P		Analog Power (PIC16C924 only)
VDD	—	21	—	P		Power (PIC16C923 only)
VLCD1	27	29	19	P		LCD Voltage
VLCD2	18	19	10	P	—	LCD Voltage

Legend: I = input O = output P = power L = LCD Driver
— = Not used TTL = TTL input ST = Schmitt Trigger input

TABLE 3-1: PIC16C9XX PINOUT DESCRIPTION (Cont'd)

Pin Name	DIP Pin#	PLCC Pin#	TQFP Pin#	Pin Type	Buffer Type	Description
VLCD3	19	20	11	P	—	LCD Voltage
VDD	20, 60	22, 64	12, 52	P	—	Digital power
VSS	6, 21	7, 23	13, 62	P	—	Ground reference
NC	—	1	—	—	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output P = power L = LCD Driver
— = Not used TTL = TTL input ST = Schmitt Trigger input

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-3.

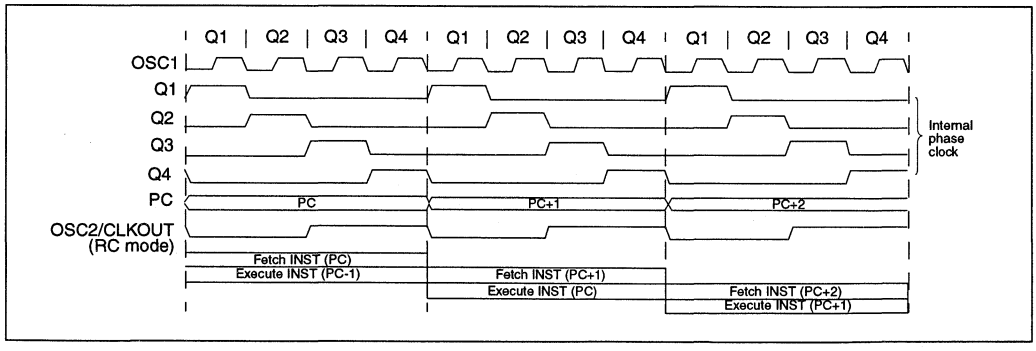
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

	Tcy0	Tcy1	Tcy2	Tcy3	Tcy4	Tcy5
1. MOVLW 55h	Fetch 1	Execute 1				
2. MOVWF PORTB		Fetch 2	Execute 2			
3. CALL SUB_1			Fetch 3	Execute 3		
4. BSF PORTA, BIT3 (Forced NOP)				Fetch 4	Flush	
5. Instruction @ address SUB_1					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

NOTES:

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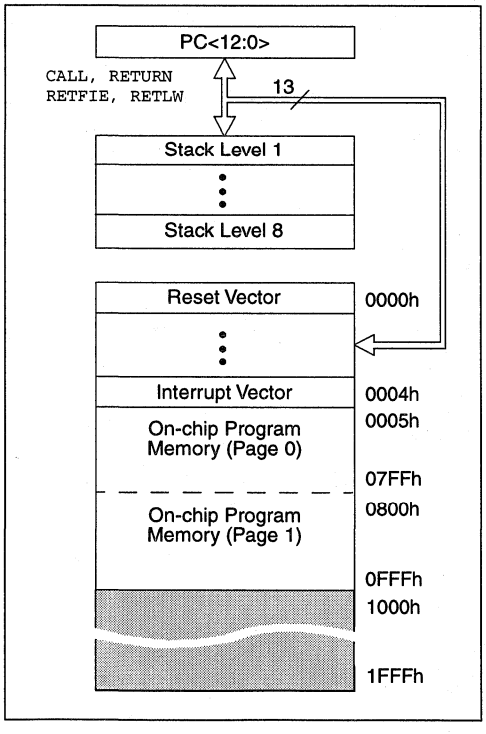
4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C9XX family has a 13-bit program counter capable of addressing an 8K x 14 program memory space.

Only the first 4K x 14 (0000h-0FFFh) is physically implemented. Accessing a location above the physically implemented addresses will cause a wraparound. The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

The data memory is partitioned into four Banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1:RP0 (STATUS<6:5>)

11 = Bank 3 (180h-1FFh)

10 = Bank 2 (100h-17Fh)

01 = Bank 1 (80h-FFh)

00 = Bank 0 (00h-7Fh)

The lower locations of each Bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers implemented as static RAM. All four banks contain special function registers. Some "high use" special function registers are mirrored in other banks for code reduction and quicker access.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

The following General Purpose Registers are not physically implemented:

- F0h-FFh of Bank 1
- 170h-17Fh of Bank 2
- 1F0h-1FFh of Bank 3

These locations are used for common access across banks.

FIGURE 4-2: REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h	Indirect addr.(1)	100h	Indirect addr.(1)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	PORTF	107h	TRISF	187h
PORTD	08h	TRISD	88h	PORTG	108h	TRISG	188h
PORTE	09h	TRISE	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh	LCDSE	10Dh		18Dh
TMR1L	0Eh	PCON	8Eh	LCDPS	10Eh		18Eh
TMR1H	0Fh		8Fh	LCDCON	10Fh		18Fh
T1CON	10h		90h	LCDD00	110h		190h
TMR2	11h		91h	LCDD01	111h		191h
T2CON	12h	PR2	92h	LCDD02	112h		192h
SSPBUF	13h	SSPADD	93h	LCDD03	113h		193h
SSPCON	14h	SSPSTAT	94h	LCDD04	114h		194h
CCPR1L	15h		95h	LCDD05	115h		195h
CCPR1H	16h		96h	LCDD06	116h		196h
CCP1CON	17h		97h	LCDD07	117h		197h
	18h		98h	LCDD08	118h		198h
	19h		99h	LCDD09	119h		199h
	1Ah		9Ah	LCDD10	11Ah		19Ah
	1Bh		9Bh	LCDD11	11Bh		19Bh
	1Ch		9Ch	LCDD12	11Ch		19Ch
	1Dh		9Dh	LCDD13	11Dh		19Dh
ADRES(2)	1Eh		9Eh	LCDD14	11Eh		19Eh
ADCON0(2)	1Fh	ADCON1(2)	9Fh	LCDD15	11Fh		19Fh
General Purpose Register	20h	General Purpose Register	A0h		120h		1A0h
	7Fh		EFh		16F		1EFh
		Mapped in Bank 0 70h-7Fh	F0h	Mapped in Bank 0 70h-7Fh	170	Mapped in Bank 0 70h-7Fh	1F0h
			FFh		17F		1FFh

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: These registers are not implemented on the PIC16C923.

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4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). Those registers associated with the "core" functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						(4)	(4)
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	—	—	PORTC Data Latch when written: PORTC pins when read						--xx xxxx	--uu uuuu
08h	PORTD	PORTD Data Latch when written: PORTD pins when read								0000 0000	0000 0000
09h	PORTE	PORTE pins when read								0000 0000	0000 0000
0Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(2)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh(1)	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh(1)	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', shaded locations are unimplemented, read as '0'.

Note 1: Registers ADRES, ADCON0, and ADCON1 are not implemented in the PIC16C923, read as '0'.
2: These bits are reserved on the PIC16C923, always maintain these bits clear.
3: These pixels do not display, but can be used as general purpose RAM.
4: PIC16C923 reset values for PORTA: --xx xxxx for a POR, and --uu uuuu for all other resets,
PIC16C924 reset values for PORTA: --0x 0000 for a POR, and --0u 0000 for all other resets.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	—	—	PORTC Data Direction Register						--11 1111	--11 1111
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	PORTE Data Direction Register								1111 1111	1111 1111
8Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC					---0 0000	---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	LCDIE	ADIE(2)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	—	---- --0-	---- --u-
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	—	Unimplemented								—	—
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh(1)	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', shaded locations are unimplemented, read as '0'.

Note 1: Registers ADRES, ADCON0, and ADCON1 are not implemented in the PIC16C923, read as '0'.
2: These bits are reserved on the PIC16C923, always maintain these bits clear.
3: These pixels do not display, but can be used as general purpose RAM.
4: PIC16C923 reset values for PORTA: --xx xxxx for a POR, and --uu uuuu for all other resets, PIC16C924 reset values for PORTA: --0x 0000 for a POR, and --0u 0000 for all other resets.

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TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY (Cont'd)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
Bank 2											
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
101h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
104h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
107h	PORTF	PORTF pins when read								0000 0000	0000 0000
108h	PORTG	PORTG pins when read								0000 0000	0000 0000
109h	—	Unimplemented								—	—
10Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC					---0 0000	---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
10Ch	—	Unimplemented								—	—
10Dh	LCDSE	SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0	1111 1111	1111 1111
10Eh	LCDPS	—	—	—	—	LP3	LP2	LP1	LP0	---- 0000	---- 0000
10Fh	LCDCON	LCDEN	SLPEN	—	VGEN	CS1	CS0	LMUX1	LMUX0	00-0 0000	00-0 0000
110h	LCDD00	SEG07 COM0	SEG06 COM0	SEG05 COM0	SEG04 COM0	SEG03 COM0	SEG02 COM0	SEG01 COM0	SEG00 COM0	xxxx xxxx	uuuu uuuu
111h	LCDD01	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG09 COM0	SEG08 COM0	xxxx xxxx	uuuu uuuu
112h	LCDD02	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0	xxxx xxxx	uuuu uuuu
113h	LCDD03	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0	xxxx xxxx	uuuu uuuu
114h	LCDD04	SEG07 COM1	SEG06 COM1	SEG05 COM1	SEG04 COM1	SEG03 COM1	SEG02 COM1	SEG01 COM1	SEG00 COM1	xxxx xxxx	uuuu uuuu
115h	LCDD05	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG09 COM1	SEG08 COM1	xxxx xxxx	uuuu uuuu
116h	LCDD06	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1	xxxx xxxx	uuuu uuuu
117h	LCDD07	SEG31 COM1(3)	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1	xxxx xxxx	uuuu uuuu
118h	LCDD08	SEG07 COM2	SEG06 COM2	SEG05 COM2	SEG04 COM2	SEG03 COM2	SEG02 COM2	SEG01 COM2	SEG00 COM2	xxxx xxxx	uuuu uuuu
119h	LCDD09	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG09 COM2	SEG08 COM2	xxxx xxxx	uuuu uuuu
11Ah	LCDD10	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	xxxx xxxx	uuuu uuuu
11Bh	LCDD11	SEG31 COM2(3)	SEG30 COM2(3)	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2	xxxx xxxx	uuuu uuuu
11Ch	LCDD12	SEG07 COM3	SEG06 COM3	SEG05 COM3	SEG04 COM3	SEG03 COM3	SEG02 COM3	SEG01 COM3	SEG00 COM3	xxxx xxxx	uuuu uuuu
11Dh	LCDD13	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG09 COM3	SEG08 COM3	xxxx xxxx	uuuu uuuu
11Eh	LCDD14	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	xxxx xxxx	uuuu uuuu
11Fh	LCDD15	SEG31 COM3(3)	SEG30 COM3(3)	SEG29 COM3(3)	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', shaded locations are unimplemented, read as '0'.

Note 1: Registers ADRES, ADCON0, and ADCON1 are not implemented in the PIC16C923, read as '0'.
2: These bits are reserved on the PIC16C923, always maintain these bits clear.
3: These pixels do not display, but can be used as general purpose RAM.
4: PIC16C923 reset values for PORTA: --xx xxxx for a POR, and --uu uuuu for all other resets, PIC16C924 reset values for PORTA: --0x 0000 for a POR, and --0u 0000 for all other resets.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
Bank 3											
180h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
181h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
183h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
184h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
187h	TRISF	PORTF Data Direction Register								1111 1111	1111 1111
188h	TRISG	PORTG Data Direction Register								1111 1111	1111 1111
189h	—	Unimplemented								—	—
18Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC					---0 0000	---0 0000
18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
18Ch	—	Unimplemented								—	—
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	—	Unimplemented								—	—
192h	—	Unimplemented								—	—
193h	—	Unimplemented								—	—
194h	—	Unimplemented								—	—
195h	—	Unimplemented								—	—
196h	—	Unimplemented								—	—
197h	—	Unimplemented								—	—
198h	—	Unimplemented								—	—
199h	—	Unimplemented								—	—
19Ah	—	Unimplemented								—	—
19Bh	—	Unimplemented								—	—
19Ch	—	Unimplemented								—	—
19Dh	—	Unimplemented								—	—
19Eh	—	Unimplemented								—	—
19Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', shaded locations are unimplemented, read as '0'.

Note 1: Registers ADRES, ADCON0, and ADCON1 are not implemented in the PIC16C923, read as '0'.
2: These bits are reserved on the PIC16C923, always maintain these bits clear.
3: These pixels do not display, but can be used as general purpose RAM.
4: PIC16C923 reset values for PORTA: --xx xxxx for a POR, and --uu uuuu for all other resets, PIC16C924 reset values for PORTA: --0x 0000 for a POR, and --0u 0000 for all other resets.

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4.2.2.1 STATUS REGISTER

The STATUS register, shown in Figure 4-3, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

Note 1: The C and DC bits operate as a $\overline{borrow}$ and $\overline{digit\ borrow}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 4-3: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h - 1FFh)
`10` = Bank 2 (100h - 17Fh)
`01` = Bank 1 (80h - FFh)
`00` = Bank 0 (00h - 7Fh)

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT pin interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

FIGURE 4-4: OPTION REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, RB Port change and external RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-5: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (see Section 5.2 to clear interrupt)
0 = None of the RB7:RB4 pins have changed state

4.2.2.4 PIE1 REGISTER

This register contains the individual enable bits for the peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

FIGURE 4-6: PIE1 REGISTER (ADDRESS 8Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **LCDIE:** LCD Interrupt Enable bit
1 = Enables the LCD interrupt
0 = Disables the LCD interrupt

bit 6: **ADIE:** A/D Converter Interrupt Enable bit(1)
1 = Enables the A/D interrupt
0 = Disables the A/D interrupt

bit 5-4: **Unimplemented:** Read as '0'

bit 3: **SSPIE:** Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2: **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1: **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0: **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Note 1: Bit ADIE is reserved on the PIC16C923, always maintain this bit clear.

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4.2.2.5 PIR1 REGISTER

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-7: PIR1 REGISTER (ADDRESS 0Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **LCDIF:** LCD Interrupt Flag bit
1 = LCD interrupt occurred (must be cleared in software)
0 = LCD interrupt did not occur

bit 6: **ADIF**: A/D Converter Interrupt Flag bit(1)
1 = An A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

bit 5-4: **Unimplemented**: Read as '0'

bit 3: **SSPIF**: Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 2: **CCP1IF**: CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

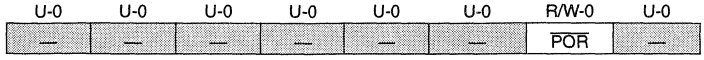
Note 1: Bit ADIF is reserved on the PIC16C923, always maintain this bit clear.

4.2.2.6 PCON REGISTER

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external $\overline{MCLR}$ Reset or WDT Reset.

For various reset conditions see Table 14-4 and Table 14-5.

FIGURE 4-8: PCON REGISTER (ADDRESS 8Eh)



R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1: **$\overline{POR}$**: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0: **Unimplemented:** Read as '0'

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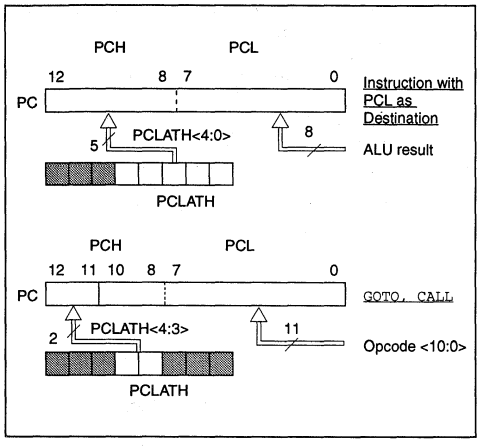
4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-9 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-9: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16CXX family has an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

4.4 Program Memory Paging

The PIC16C9XX has 4K of program memory, but the CALL and GOTO instructions only have a 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 4K program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (Figure 4-9). When doing a CALL or GOTO instruction, the user must ensure that this page bit (PCLATH<3>) is programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is PUSHed onto the stack. Therefore, manipulation of the PCLATH<3> is not required for the return instructions (which POPs the address from the stack).

Note 1: The PIC16C9XX ignores paging bit (PCLATH<4>), which is used to access program memory pages 2 and 3 (1000h - 1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

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Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0x500
BSF     PCLATH,3   ;Select page 1 (800h-FFFh)
CALL    SUB1_P1    ;Call subroutine in
        :          ;page 1 (800h-FFFh)
        :
        :
ORG 0x900
SUB1_P1:           ;called subroutine
        :          ;page 1 (800h-FFFh)
        :
RETURN             ;return to Call subroutine
                   ;in page 0 (000h-7FFh)
```

4.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

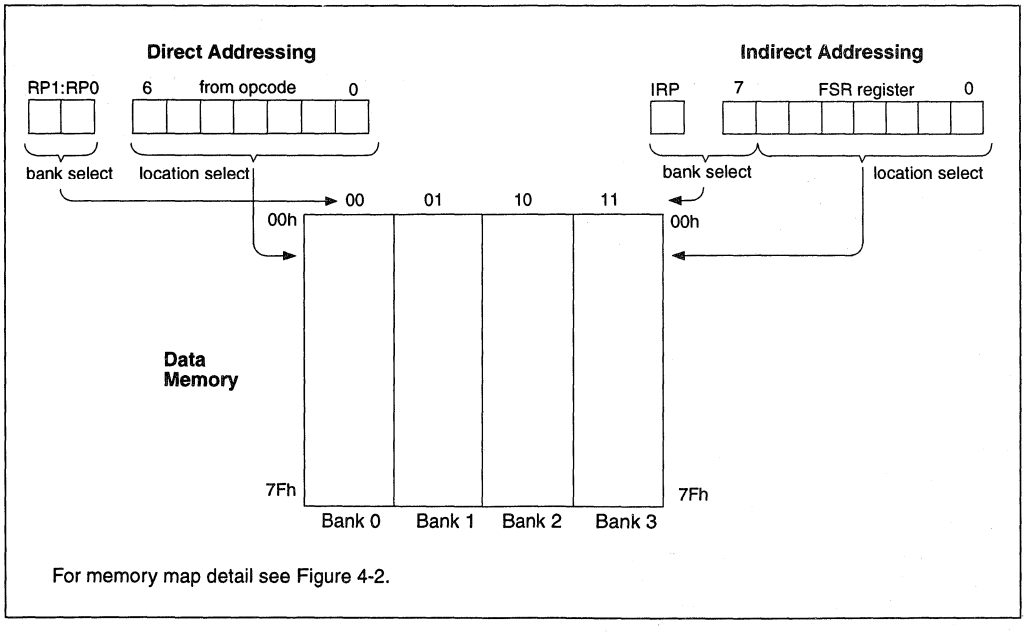
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register (FSR). Reading the INDF register itself indirectly (FSR = '0') will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-10.

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR,F   ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;no clear next
CONTINUE
        :               ;yes continue
```

FIGURE 4-10: DIRECT/INDIRECT ADDRESSING



For memory map detail see Figure 4-2.

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5.0 PORTS

Some pins for these ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used in its normal pin function.

5.1 PORTA and TRISA Register

The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All RA pins have data direction bits (TRISA register) which can configure these pins as output or input.

Setting a bit in the TRISA register puts the corresponding output driver in a hi-impedance mode. Clearing a bit in the TRISA register puts the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin.

For the PIC16C924 only, other PORTA pins are multiplexed with analog inputs and the analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

Note: On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

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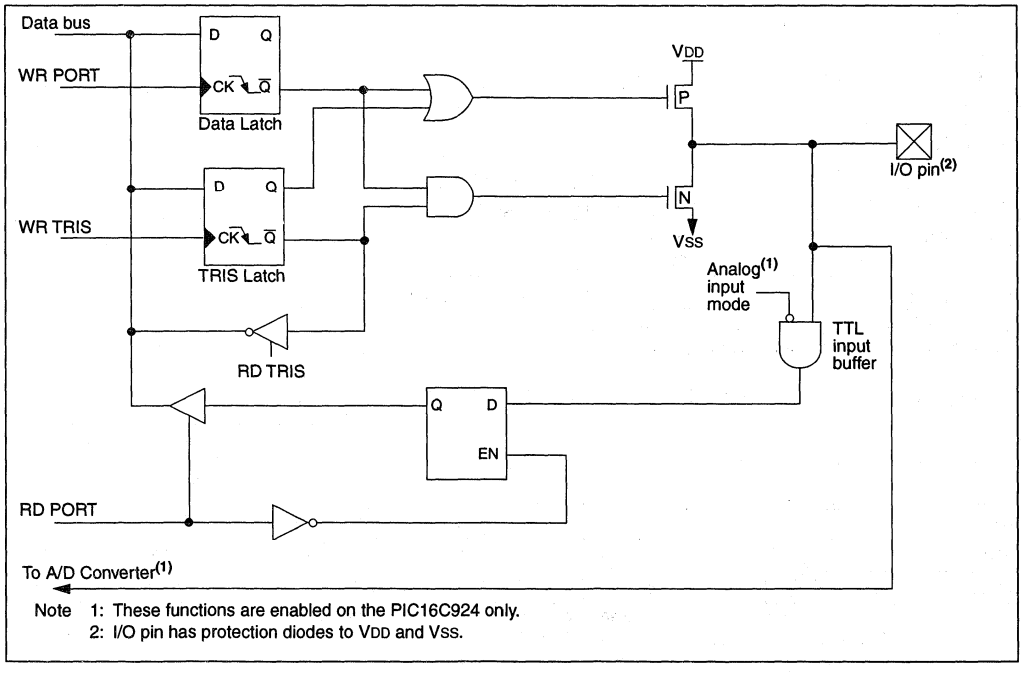
EXAMPLE 5-1: INITIALIZING PORTA

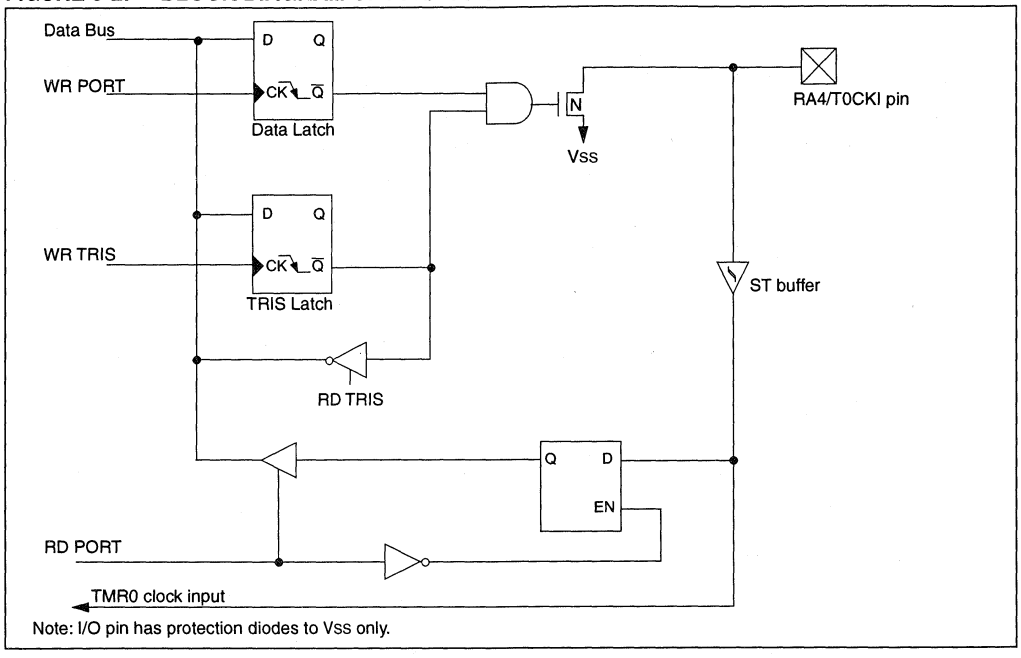
```
CLRF    PORTA         ; Initialize PORTA
BCF     STATUS, RP1   ; Select Bank 1
BSF     STATUS, RP0   ;
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISA         ; Set RA<3:0> as inputs
                      ; RA<5:4> as outputs
                      ; RA<7:6> are always
                      ; read as '0'.
```

FIGURE 5-1: BLOCK DIAGRAM OF PINS RA3:RA0 AND RA5



Note 1: These functions are enabled on the PIC16C924 only.
2: I/O pin has protection diodes to VDD and VSS.

FIGURE 5-2: BLOCK DIAGRAM OF RA4/T0CKI PIN



Note: I/O pin has protection diodes to Vss only.

TABLE 5-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0(1)	bit0	TTL	Input/output or analog input
RA1/AN1(1)	bit1	TTL	Input/output or analog input
RA2/AN2(1)	bit2	TTL	Input/output or analog input
RA3/AN3/VREF(1)	bit3	TTL	Input/output or analog input/VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/AN4/$\overline{SS}$ (1)	bit5	TTL	Input/output or slave select input for synchronous serial port, or analog input

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: The AN and VREF functions are for the A/D module and are only implemented on the PIC16C924.

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	(2)	(2)
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
9Fh(1)	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: The ADCON1 register is implemented on the PIC16C924 only.

2: PIC16C923 reset values for PORTA: --xx xxxx for a POR, and --uu uuuu for all other resets,
PIC16C924 reset values for PORTA: --0x 0000 for a POR, and --0u 0000 for all other resets.

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5.2 PORTB and TRISB Register

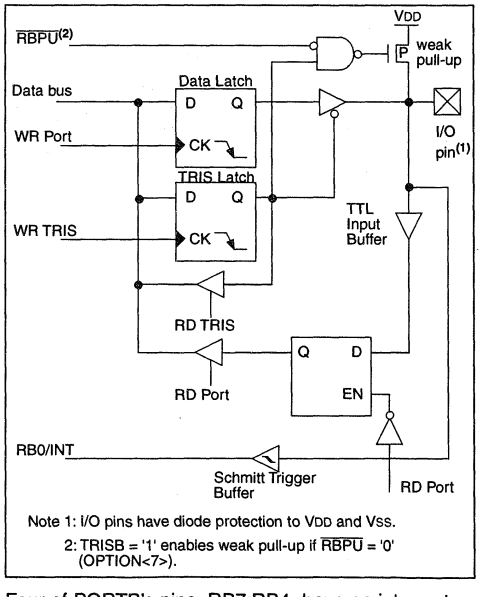
PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a bit in the TRISB register puts the corresponding output driver in a hi-impedance input mode. Clearing a bit in the TRISB register puts the contents of the output latch on the selected pin(s).

EXAMPLE 5-2: INITIALIZING PORTB

```
CLRF    PORTB          ; Initialize PORTB
BCF     STATUS, RP1    ; Select Bank 1
BSF     STATUS, RP0    ;
MOVLW   0xCF           ; Value used to
                       ; initialize data
                       ; direction
MOVWF   TRISB          ; Set RB<3:0> as inputs
                       ; RB<5:4> as outputs
                       ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{RBPU}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are also disabled on a Power-on Reset.

FIGURE 5-3: BLOCK DIAGRAM OF RB3:RB0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if $\overline{RBPU}$ = '0' (OPTION<7>).

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

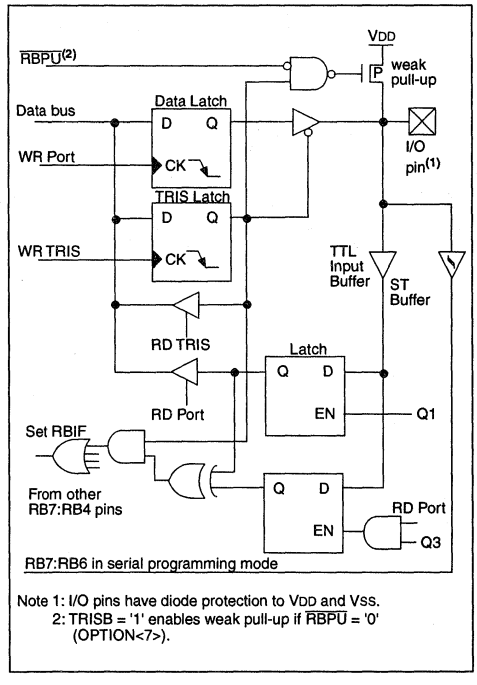
b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a keypad and make it possible for wake-up on key-depression. Refer to the *Embedded Control Handbook, "Implementing Wake-Up on Key Stroke"* (AN552).

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-4: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: I/O pins have diode protection to VDD and VSS.
2: TRISB = '1' enables weak pull-up if $\overline{RBPU}$ = '0' (OPTION<7>).

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TABLE 5-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST	Input/output pin or external interrupt input. Internal software programmable weak pull-up. This buffer is a Schmitt Trigger input when configured as the external interrupt.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock. This buffer is a Schmitt Trigger input when used in serial programming mode.
RB7	bit7	TTL/ST	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data. This buffer is a Schmitt Trigger input when used in serial programming mode.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h, 181h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

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5.3 PORTC and TRISC Register

PORTC is an 6-bit bi-directional port. Each pin is individually configurable as an input or output through the TRISC register. PORTC is multiplexed with several peripheral functions (Table 5-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

EXAMPLE 5-3: INITIALIZING PORTC

```
CLRF    PORTC         ; Initialize PORTC
BCF     STATUS, RP1   ; Select Bank 1
BSF     STATUS, RP0   ;
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISC         ; Set RC<3:0> as inputs
                      ; RC<5:4> as outputs
                      ; RC<7:6> always read 0
```

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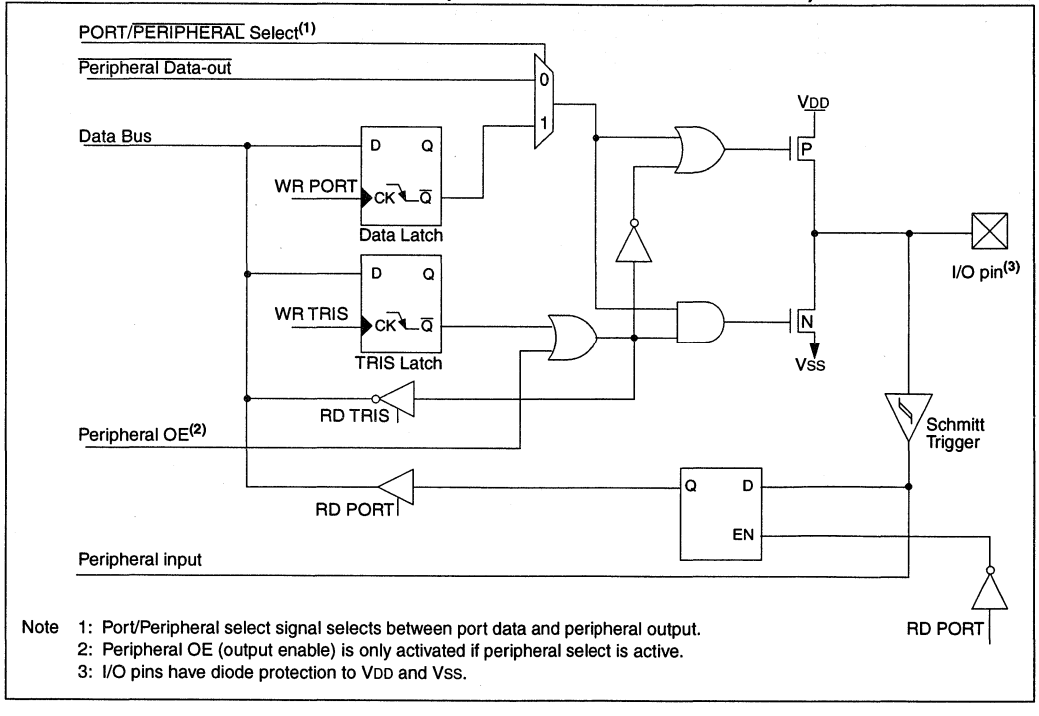
FIGURE 5-5: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only activated if peripheral select is active.
3: I/O pins have diode protection to VDD and VSS.

TABLE 5-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output or Timer1 clock input
RC1/T1OSI	bit1	ST	Input/output port pin or Timer1 oscillator input
RC2/CCP1	bit2	ST	Input/output port pin or Capture input/Compare output/PWM output
RC3/SCK/SCL	bit3	ST	Input/output port pin or the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	Input/output port pin or the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data out

Legend: ST = Schmitt Trigger input

TABLE 5-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTC.

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5.4 PORTD and TRISD Registers

PORTD is an 8-bit port with Schmitt Trigger input buffers. The first five pins are configurable as general purpose I/O pins or LCD segment drivers. Pins RD5, RD6 and RD7 can be digital inputs or LCD segment or common drivers.

TRISD controls the direction of pins RD0 through RD4 when PORTD is configured as a digital port.

Note: On a Power-on Reset these pins are configured as LCD segment drivers.

Note: To configure the pins as a digital port, the corresponding bits in the LCDSE register must be cleared. Any bit set in the LCDSE register overrides any bit settings in the corresponding TRIS register.

EXAMPLE 5-4: INITIALIZING PORTD

```
BCF   STATUS,RP0    ;Select Bank 2
BSF   STATUS,RP1    ;
BCF   LCDSE,SE29    ;Make RD<7:5> digital
BCF   LCDSE,SE0     ;Make RD<4:0> digital
BSF   STATUS,RP0    ;Select Bank 1
BCF   STATUS,RP1    ;
MOVLW 0x07          ;Make RD<4:0> outputs
MOVWF TRISD         ;Make RD<7:5> inputs
```

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FIGURE 5-6: PORTD<4:0> BLOCK DIAGRAM

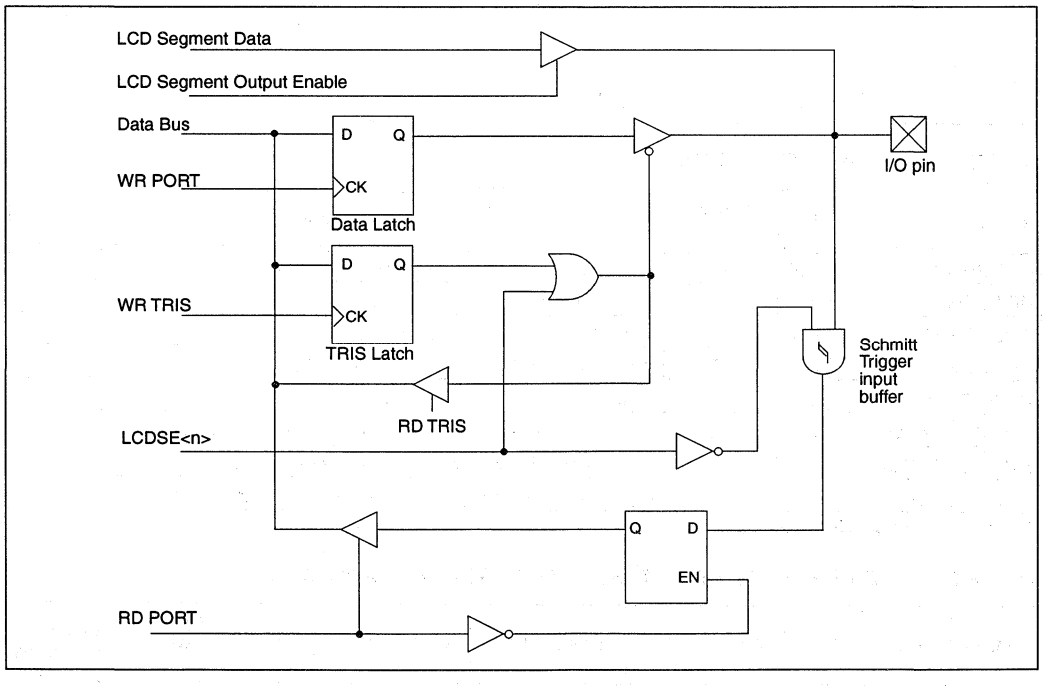

FIGURE 5-7: PORTD<7:5> BLOCK DIAGRAM

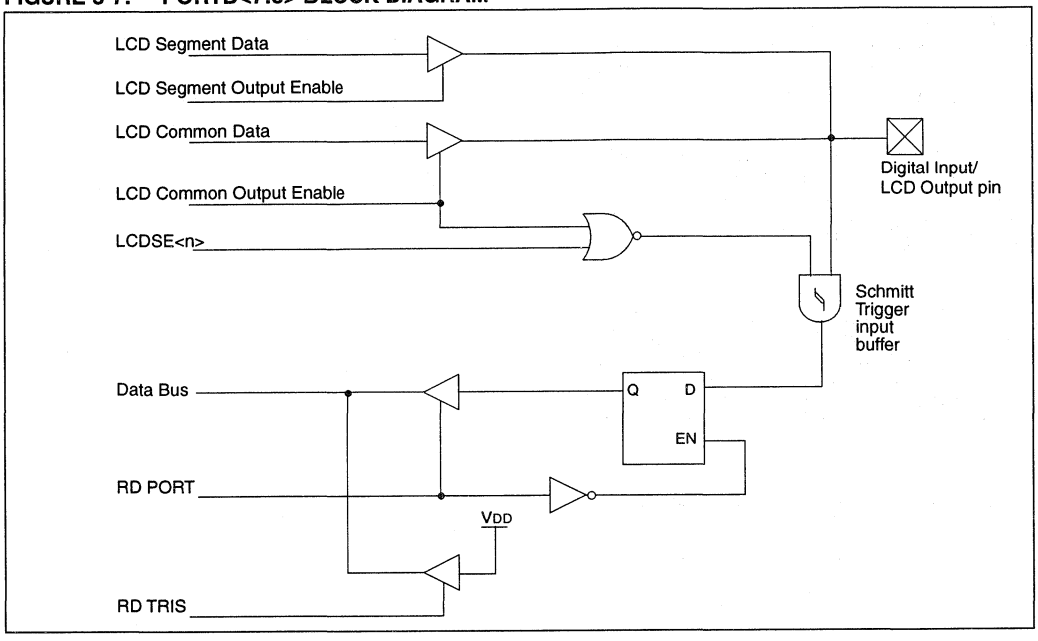

TABLE 5-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/SEG00	bit0	ST	Input/output port pin or Segment Driver00
RD1/SEG01	bit1	ST	Input/output port pin or Segment Driver01
RD2/SEG02	bit2	ST	Input/output port pin or Segment Driver02
RD3/SEG03	bit3	ST	Input/output port pin or Segment Driver03
RD4/SEG04	bit4	ST	Input/output port pin or Segment Driver04
RD5/SEG29/COM3	bit5	ST	Digital input pin or Segment Driver29 or Common Driver3
RD6/SEG30/COM2	bit6	ST	Digital input pin or Segment Driver30 or Common Driver2
RD7/SEG31/COM1	bit7	ST	Digital input pin or Segment Driver31 or Common Driver1

Legend: ST = Schmitt Trigger input

TABLE 5-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	0000 0000	0000 0000
88h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111
10Dh	LCDSE	SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0	1111 1111	1111 1111

Legend: Shaded cells are not used by PORTD.

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5.5 PORTE and TRISE Register

PORTE is an digital input only port. Each pin is multiplexed with an LCD segment driver. These pins have Schmitt Trigger input buffers.

Note 1: On a Power-on Reset these pins are configured as LCD segment drivers.

Note 2: To configure the pins as a digital port, the corresponding bits in the LCDSE register must be cleared. Any bit set in the LCDSE register overrides any bit settings in the corresponding TRIS register.

EXAMPLE 5-5: INITIALIZING PORTE

```
BCF STATUS,RP0     ;Select Bank 2
BSF STATUS,RP1     ;
BCF LCDSE,SE27     ;Make all PORTE
BCF LCDSE,SE5      ;and PORTG<7>
BCF LCDSE,SE9      ;digital inputs
```

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FIGURE 5-8: PORTE BLOCK DIAGRAM

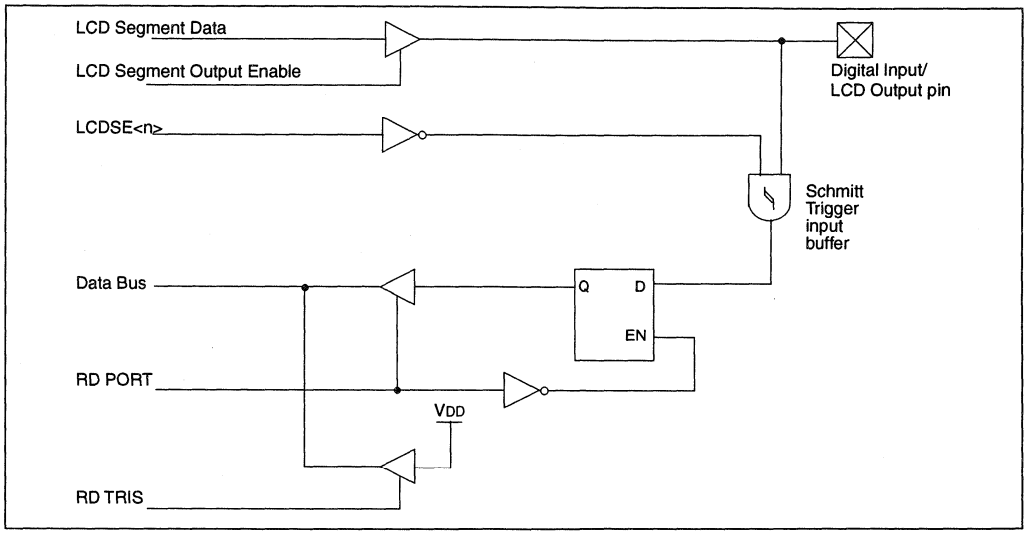

TABLE 5-9: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/SEG05	bit0	ST	Digital input or Segment Driver05
RE1/SEG06	bit1	ST	Digital input or Segment Driver06
RE2/SEG07	bit2	ST	Digital input or Segment Driver07
RE3/SEG08	bit3	ST	Digital input or Segment Driver08
RE4/SEG09	bit4	ST	Digital input or Segment Driver09
RE5/SEG10	bit5	ST	Digital input or Segment Driver10
RE6/SEG11	bit6	ST	Digital input or Segment Driver11
RE7/SEG27	bit7	ST	Digital input or Segment Driver27 (not available on 64-pin devices)

Legend: ST = Schmitt Trigger input

TABLE 5-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
09h	PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	0000 0000	0000 0000
89h	TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	1111 1111	1111 1111
10Dh	LCDSE	SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0	1111 1111	1111 1111

Legend: Shaded cells are not used by PORTE.

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5.6 PORTF and TRISF Register

PORTF is an digital input only port. Each pin is multiplexed with an LCD segment driver. These pins have Schmitt Trigger input buffers.

Note 1: On a Power-on Reset these pins are configured as LCD segment drivers.

Note 2: To configure the pins as a digital port, the corresponding bits in the LCDSE register must be cleared. Any bit set in the LCDSE register overrides any bit settings in the corresponding TRIS register.

EXAMPLE 5-6: INITIALIZING PORTF

```
BCF STATUS,RP0    ;Select Bank 2
BSF STATUS,RP1    ;
BCF LCDSE,SE16    ;Make all PORTF
BCF LCDSE,SE12    ;digital inputs
```

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FIGURE 5-9: PORTF BLOCK DIAGRAM

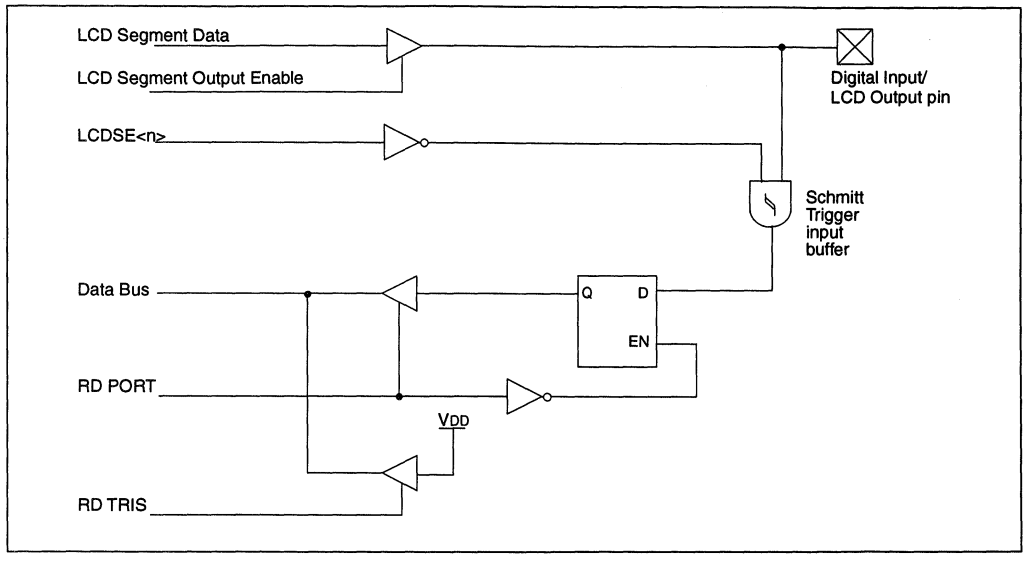

TABLE 5-11: PORTF FUNCTIONS

Name	Bit#	Buffer Type	Function
RF0/SEG12	bit0	ST	Digital input or Segment Driver12
RF1/SEG13	bit1	ST	Digital input or Segment Driver13
RF2/SEG14	bit2	ST	Digital input or Segment Driver14
RF3/SEG15	bit3	ST	Digital input or Segment Driver15
RF4/SEG16	bit4	ST	Digital input or Segment Driver16
RF5/SEG17	bit5	ST	Digital input or Segment Driver17
RF6/SEG18	bit6	ST	Digital input or Segment Driver18
RF7/SEG19	bit7	ST	Digital input or Segment Driver19

Legend: ST = Schmitt Trigger input

TABLE 5-12: SUMMARY OF REGISTERS ASSOCIATED WITH PORTF

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
107h	PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	0000 0000	0000 0000
187h	TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	1111 1111	1111 1111
10Dh	LCDSE	SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0	1111 1111	1111 1111

Legend: Shaded cells are not used by PORTF.

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5.7 PORTG and TRISG Register

PORTG is an digital input only port. Each pin is multiplexed with an LCD segment driver. These pins have Schmitt Trigger input buffers.

Note 1: On a Power-on Reset these pins are configured as LCD segment drivers.

Note 2: To configure the pins as a digital port, the corresponding bits in the LCDSE register must be cleared. Any bit set in the LCDSE register overrides any bit settings in the corresponding TRIS register.

EXAMPLE 5-7: INITIALIZING PORTG

```
BCF STATUS,RP0    ;Select Bank 2
BSF STATUS,RP1    ;
BCF LCDSE,SE27    ;Make all PORTG
BCF LCDSE,SE20    ;and PORTE<7>
                  ;digital inputs
```

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FIGURE 5-10: PORTG BLOCK DIAGRAM

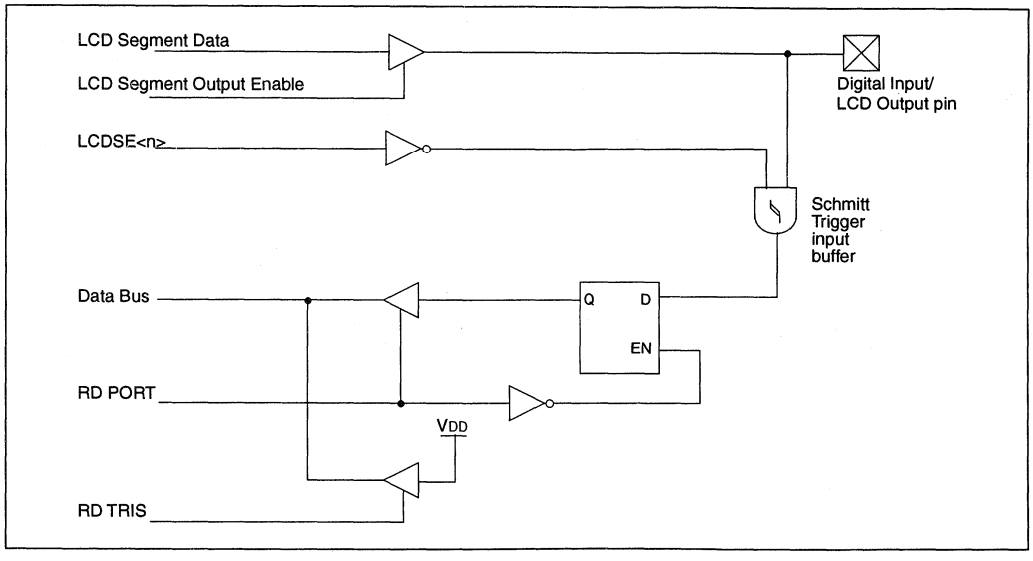

TABLE 5-13: PORTG FUNCTIONS

Name	Bit#	Buffer Type	Function
RG0/SEG20	bit0	ST	Digital input or Segment Driver20
RG1/SEG21	bit1	ST	Digital input or Segment Driver21
RG2/SEG22	bit2	ST	Digital input or Segment Driver22
RG3/SEG23	bit3	ST	Digital input or Segment Driver23
RG4/SEG24	bit4	ST	Digital input or Segment Driver24
RG5/SEG25	bit5	ST	Digital input or Segment Driver25
RG6/SEG26	bit6	ST	Digital input or Segment Driver26
RG7/SEG28	bit7	ST	Digital input or Segment Driver28 (not available on 64-pin devices)

Legend: ST = Schmitt Trigger input

TABLE 5-14: SUMMARY OF REGISTERS ASSOCIATED WITH PORTG

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
108h	PORTG	RG7	RG6	RG5	RG4	RG3	RG2	RG1	RG0	0000 0000	0000 0000
188h	TRISG	TRISG7	TRISG6	TRISG5	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	1111 1111	1111 1111
10Dh	LCDSE	SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0	1111 1111	1111 1111

Legend: Shaded cells are not used by PORTG.

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5.8 I/O Programming Considerations

5.8.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the contents of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-8 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 5-8: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

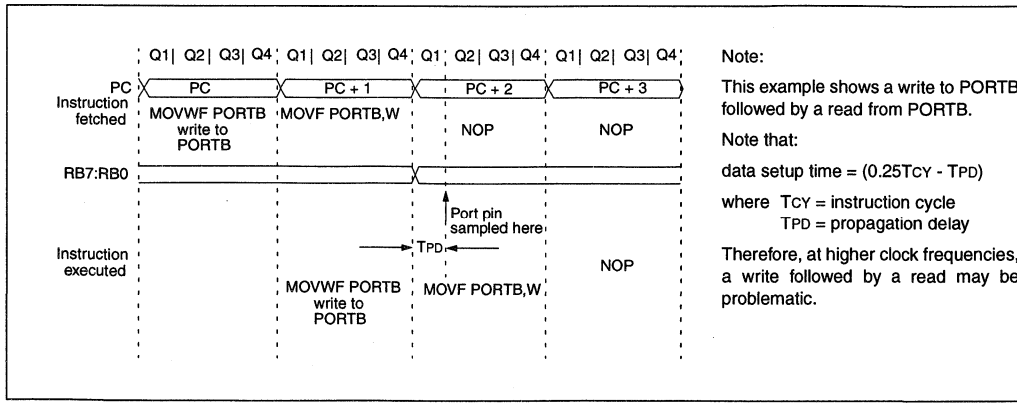
```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                       PORT latch  PORT pins
;                       ----------  ---------
  BCF PORTB, 7     ; 01pp pppp    11pp pppp
  BCF PORTB, 6     ; 10pp pppp    11pp pppp
  BCF STATUS, RP1 ;
  BSF STATUS, RP0 ;
  BCF TRISB, 7     ; 10pp pppp    11pp pppp
  BCF TRISB, 6     ; 10pp pppp    10pp pppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.8.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-11). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-11: SUCCESSIVE I/O OPERATION



NOTES:

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6.0 OVERVIEW OF TIMER MODULES

Each module can generate an interrupt to indicate that an event has occurred (e.g. timer overflow). Each of these modules is explained in full detail in the following sections. The timer modules are:

- Timer0 Module (Section 7.0)
- Timer1 Module (Section 8.0)
- Timer2 Module (Section 9.0)

6.1 Timer0 Overview

The Timer0 module is a simple 8-bit timer/counter. The clock source can be either the internal system clock (Fosc/4) or an external clock. When the clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

The Timer0 module also has a programmable prescaler option. This prescaler can be assigned to either the Timer0 module or the Watchdog Timer. Bit PSA (OPTION<3>) assigns the prescaler, and bits PS2:PS0 (OPTION<2:0>) determine the prescaler value. Timer0 can increment at the following rates: 1:1 when prescaler assigned to Watchdog timer, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

6.2 Timer1 Overview

Timer1 is a 16-bit timer/counter. The clock source can be either the internal system clock (Fosc/4), an external clock, or an external crystal. Timer1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchronously to the device. Asynchronous operation allows Timer1 to operate during sleep, which is useful for applications that require a real-time clock as well as the power savings of SLEEP mode.

Timer1 also has a prescaler option which allows Timer1 to increment at the following rates: 1:1, 1:2, 1:4, and 1:8. Timer1 can be used in conjunction with the Capture/Compare/PWM module. When used with a CCP module, Timer1 is the time-base for 16-bit capture or the 16-bit compare and must be synchronized to the device. Timer1 oscillator is also one of the clock sources for the LCD module.

6.3 Timer2 Overview

Timer2 is an 8-bit timer with a programmable prescaler and postscaler, as well as an 8-bit period register (PR2). Timer2 can be used with the CCP1 module (in PWM mode) as well as the clock source for the Synchronous Serial Port (SSP). The prescaler option allows Timer2 to increment at the following rates: 1:1, 1:4, 1:16.

The postscaler allows the TMR2 register to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP Overview

The CCP module can operate in one of these three modes: 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM).

Capture mode captures the 16-bit value of TMR1 into the CCPR1H:CCPR1L register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or the sixteenth rising edge of the CCP1 pin.

Compare mode compares the TMR1H:TMR1L register pair to the CCPR1H:CCPR1L register pair. When a match occurs an interrupt can be generated, and the output pin CCP1 can be forced to given state (High or Low), TMR1 can be reset and start A/D conversion. This depends on the control bits CCP1M3:CCP1M0.

PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPR1H:CCPR1L<5:4>) as well as to an 8-bit period register (PR2). When the TMR2 register = Duty Cycle register, the CCP1 pin will be forced low. When TMR2 = PR2, TMR2 is cleared to 00h, an interrupt can be generated, and the CCP1 pin (if an output) will be forced high.

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NOTES:

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7.0 TIMER0 MODULE

The Timer0 module has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit T0CS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

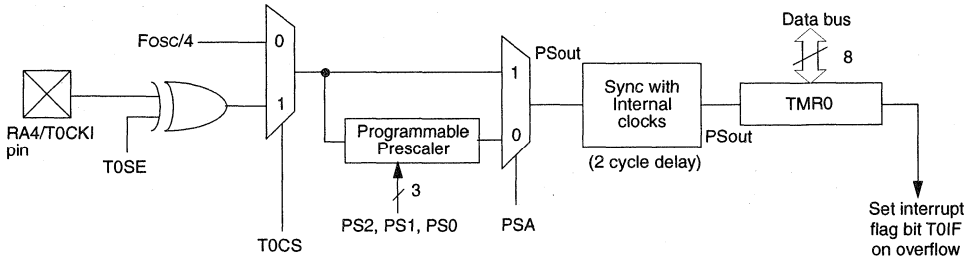
Counter mode is selected by setting bit T0CS (OPTION<5>). In counter mode Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP. Figure 7-4 displays the Timer0 interrupt timing.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS2:PS0 (OPTION<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 7-6 for detailed block diagram).

FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

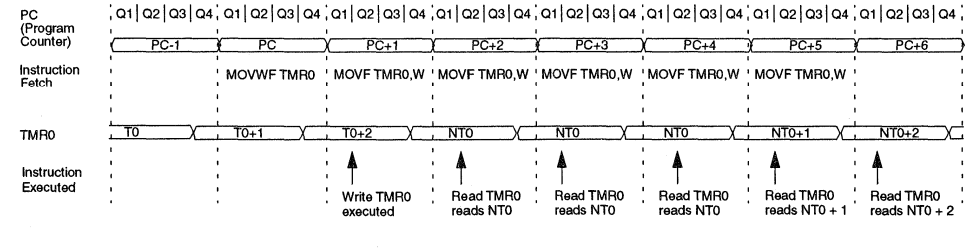


FIGURE 7-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

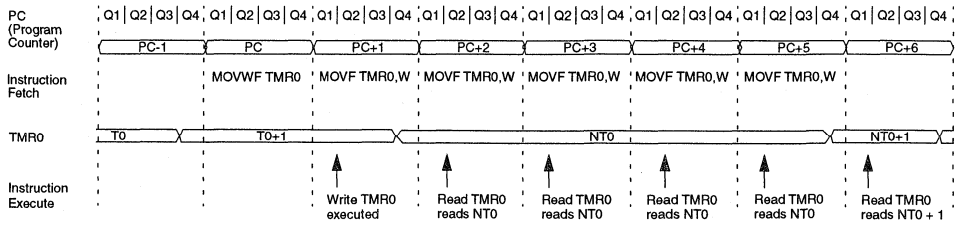
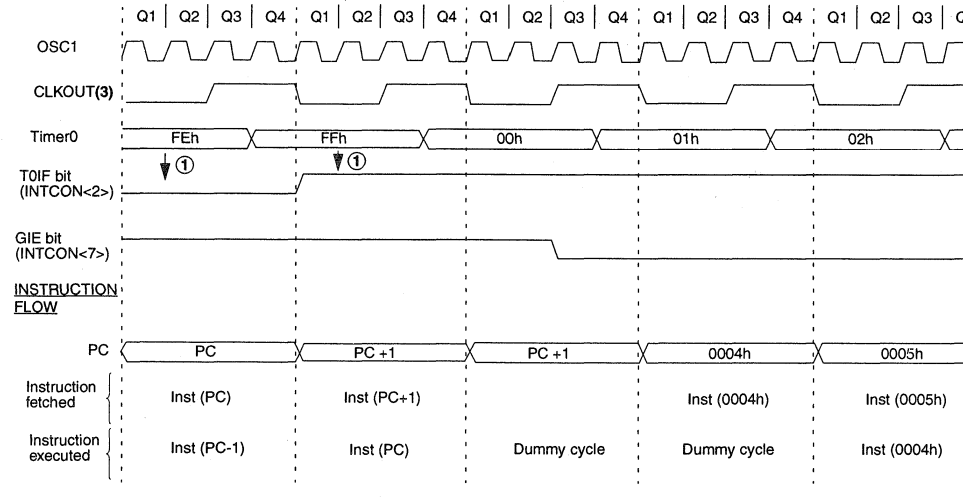


FIGURE 7-4: TIMER0 INTERRUPT TIMING



Note 1: Interrupt flag bit T0IF is sampled here (every Q1).
2: Interrupt latency = 4Tcy where Tcy = instruction cycle time.
3: CLKOUT is available only in RC oscillator mode.

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7.2 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TMR0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

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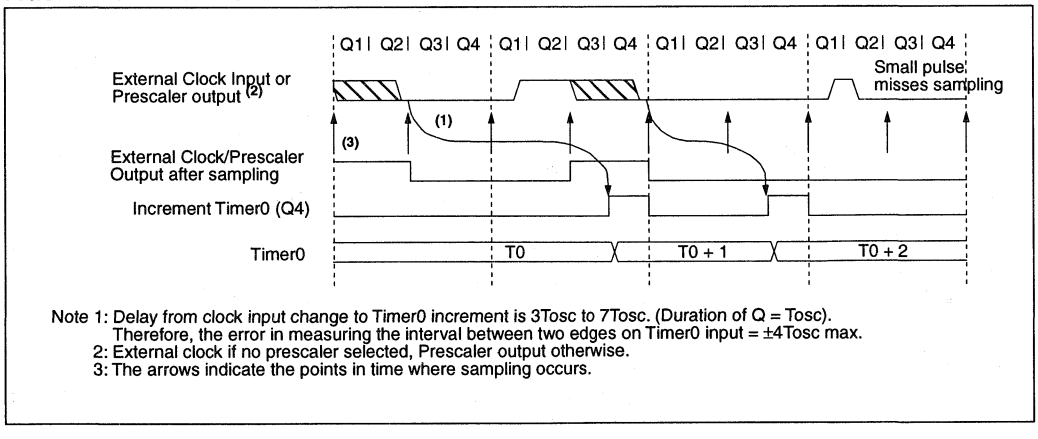
FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

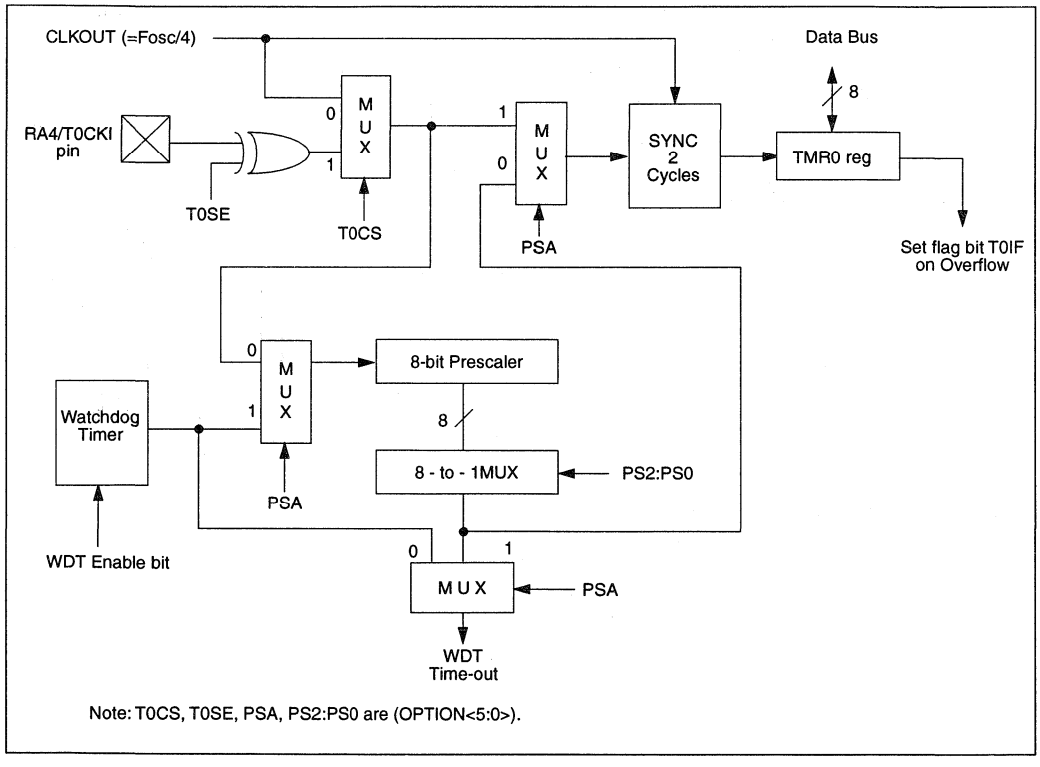
7.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. `CLRF 1, MOVWF 1, BSF 1,x`....etc.) will clear the prescaler count. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler count along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 7-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are (OPTION<5:0>).

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7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution.

Note: To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This precaution must be followed even if the WDT is disabled.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS, RP1  ;Select Bank 0
BCF     STATUS, RP0  ;
CLRF    TMR0         ;Clear TMR0 & Prescaler
BSF     STATUS, RP0  ;Select Bank 1
CLRWDT               ;Clears WDT
MOVLW   b'xxxx1xxx'  ;Select new prescale
MOVWF   OPTION_REG   ;value & WDT
BCF     STATUS, RP0  ;Select Bank 0
```

To change prescaler from the WDT to the Timer0 module use the precaution shown in Example 7-2.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT               ;Clear WDT and
                     ;prescaler
BCF     STATUS, RP1 ;Select Bank 1
BSF     STATUS, RP0 ;
MOVLW   b'xxxx0xxx' ;Select TMR0, new
                     ;prescale value and
MOVWF   OPTION_REG   ;clock source
BCF     STATUS, RP0 ;Select Bank 0
```

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TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
01h, 101h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h, 181h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

NOTES:

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8.0 TIMER1 MODULE

Timer1 is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

Timer1 can be turned on and off using the control bit TMR1ON (T1CON<0>).

Timer1 also has an internal "reset input". This reset can be generated by the CCP module (Section 10.0). Figure 8-1 shows the Timer1 control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs.

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FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off
Note: The oscillator inverter and feedback resistor are turned off to eliminate power drain

bit 2: **$\overline{\text{T1SYNC}}$**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input

TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit
1 = External clock from pin T1CKI (on the rising edge)
0 = Internal clock (Fosc/4)

bit 0: **TMR1ON**: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

8.1 Timer1 Operation in Timer Mode

Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is Fosc/4. The synchronize control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 Timer1 Operation in Synchronized Counter Mode

Counter mode is selected by setting bit TMR1CS. In this mode the timer increments on every rising edge of clock input on pin RC1/T1OSI when bit T1OSCEN is set or pin RC0/T1OSO/T1CKI when bit T1OSCEN is cleared.

If $\overline{\text{T1SYNC}}$ is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler is an asynchronous ripple-counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if the external clock is present, since the synchronization circuit is shut off. The prescaler however will continue to increment.

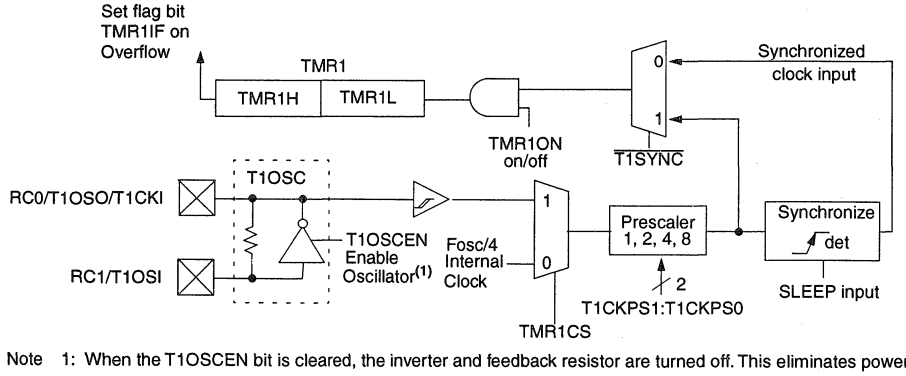
8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

When an external clock input is used for Timer1 in synchronized counter mode, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of TMR1 after synchronization.

When the prescaler is 1:1, the external clock input is the same as the prescaler output. The synchronization of T1CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T1CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the appropriate electrical specifications, parameters 45, 46, and 47.

When a prescaler other than 1:1 is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. In order for the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T1CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T1CKI high and low time is that they do not violate the minimum pulse width requirements of 10 ns). Refer to the appropriate electrical specifications, parameters 40, 42, 45, 46, and 47.

FIGURE 8-2: TIMER1 BLOCK DIAGRAM



Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

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8.3 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow which will wake-up the processor. However, special precautions in software are needed to read-from or write-to the Timer1 register pair (TMR1H:TMR1L) (Section 8.3.2).

In asynchronous counter mode, Timer1 cannot be used as a time-base for capture or compare operations.

8.3.1 EXTERNAL CLOCK INPUT TIMING WITH UNSYNCHRONIZED CLOCK

If control bit $\overline{\text{T1SYNC}}$ is set, the timer will increment completely asynchronously. The input clock must meet certain minimum high time and low time requirements, as specified in timing parameters 45, 46, and 47.

8.3.2 READING AND WRITING TMR1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running, from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

```
; All interrupts are disabled
   MOVF   TMR1H, W  ;Read high byte
   MOVWF  TMPH      ;
   MOVF   TMR1L, W  ;Read low byte
   MOVWF  TMPL      ;
   MOVF   TMR1H, W  ;Read high byte
   SUBWF  TMPH,  W  ;Sub 1st read
                    ; with 2nd read
   BTFSC  STATUS,Z  ;Is result = 0
   GOTO   CONTINUE  ;Good 16-bit read
;
; TMR1L may have rolled over between the read
; of the high and low bytes. Reading the high
; and low bytes now will read a good value.
;
   MOVF   TMR1H, W  ;Read high byte
   MOVWF  TMPH      ;
   MOVF   TMR1L, W  ;Read low byte
   MOVWF  TMPL      ;
; Re-enable the Interrupt (if required)
CONTINUE            ;Continue with your code
```

8.4 Timer1 Oscillator

A crystal oscillator circuit is built in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

TABLE 8-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz(1)	15 pF	15 pF
	100 kHz	15 pF	15 pF
	200 kHz	0 - 15 pF	0 - 15 pF
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.			
Crystals Tested:			
32.768 kHz	Epson C-001R32.768K-A		± 20 PPM
100 kHz	Epson C-2 100.00 KC-P		± 20 PPM
200 kHz	STD XTL 200.000 kHz		± 20 PPM

8.5 Resetting Timer1 using the CCP Trigger Output

If the CCP1 module is configured in compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1.

Note:	The special event trigger from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence.

In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for Timer1.

8.6 Resetting of Timer1 Register Pair (TMR1H:TMR1L)

TMR1H and TMR1L registers are not reset on a POR or any other reset except by the CCP1 special event trigger.

T1CON register is reset to 00h on a Power-on Reset. In any other reset, the register is unaffected.

8.7 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by theTimer1 module.
Note 1: Bits ADIE and ADIF are reserved on the PIC16C923, always maintain these bits clear.

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9.0 TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module. The TMR2 register is readable and writable, and is cleared on any device reset.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4 or 1:16 (selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>)).

The Timer2 module has an 8-bit period register, PR2. TMR2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is set during RESET.

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 9-2 shows the Timer2 control register.

9.1 Timer2 Prescaler and Postscaler

The prescaler and postscaler counters are cleared when any of the following occurs:

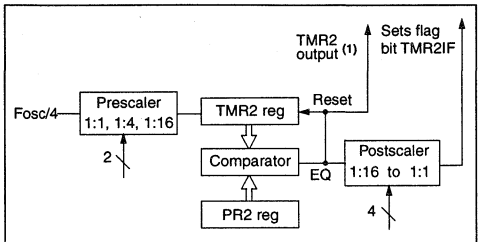
- a write to the TMR2 register
- a write to the T2CON register
- any device reset (Power-on Reset, $\overline{MCLR}$ Reset, or Watchdog Timer Reset)

TMR2 will not clear when T2CON is written, only for a WDT, POR, and $\overline{MCLR}$ reset.

9.2 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

FIGURE 9-1: TIMER2 BLOCK DIAGRAM



Note 1: TMR2 register output can be software selected by the SSP Module as the source clock.

FIGURE 9-2: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0:** Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2: **TMR2ON:** Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0: **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.
Note 1: Bits ADIE and ADIF are reserved on the PIC16C923, always maintain these bits clear.

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10.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register, or as a PWM master/slave duty cycle register. Table 10-1 shows the timer resources used by the CCP module.

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All three are readable and writable.

Figure 10-1 shows the CCP1CON register.

For use of the CCP module, refer to the *Embedded Control Handbook*, "Using the CCP Modules" (AN594).

TABLE 10-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

12

FIGURE 10-1: CCP1CON REGISTER (ADDRESS 17h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCP1X:CCP1Y**: PWM Least Significant bits
Capture Mode
Unused
Compare Mode
Unused
PWM Mode
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0: **CCP1M3:CCP1M0**: CCP1 Mode Select bits
0000 = Capture/Compare/PWM off (resets CCP1 module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (bit CCP1IF is set)
1001 = Compare mode, clear output on match (bit CCP1IF is set)
1010 = Compare mode, generate software interrupt on match (bit CCP1IF is set, CCP1 pin is unaffected)
1011 = Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1)
11xx = PWM mode

10.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1 (Figure 10-2). An event is defined as:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

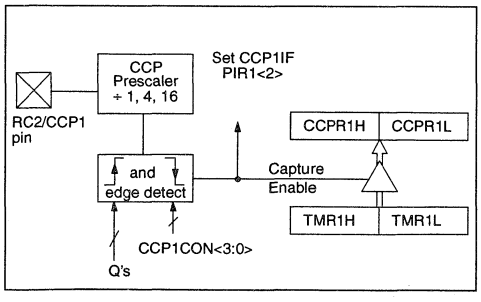
An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

10.1.1 CCP PIN CONFIGURATION

In capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note: If the RC2/CCP1 pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 10-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP module to use the capture feature. In asynchronous counter mode the capture operation may not work.

10.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep enable bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear flag bit CCP1IF following any such change in operating mode.

10.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON     ; Turn CCP module off
MOVLW   NEW_CAPT_PS ; Load the W reg with
                    ; the new prescaler
                    ; mode value and CCP ON
MOVWF   CCP1CON     ; Load CCP1CON with
                    ; this value
```

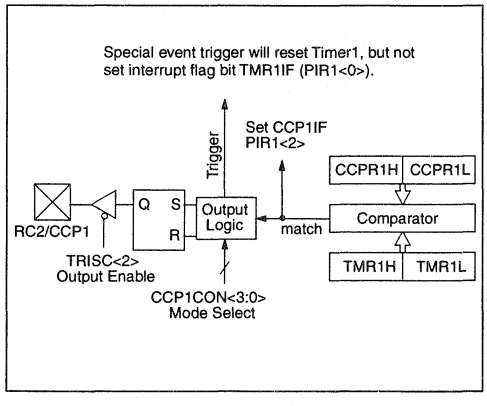
10.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven High
- Driven Low
- Remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, a compare interrupt is also generated.

FIGURE 10-3: COMPARE MODE OPERATION BLOCK DIAGRAM



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10.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note:	Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

10.2.1 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

10.2.2 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

10.2.3 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair and starts an A/D conversion. This allows the CCPR1H:CCPR1L register pair to effectively be a 16-bit programmable period register for Timer1.

Note:	The "special event trigger" from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

10.3 PWM Mode

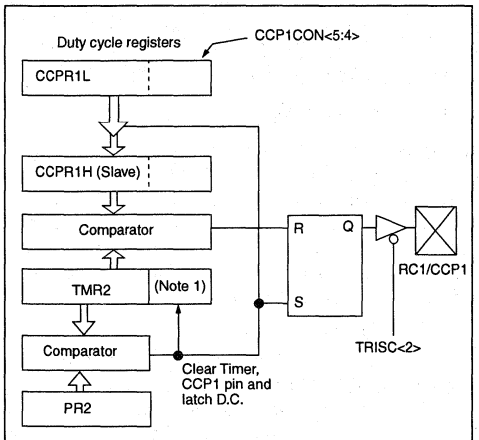
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 10-4 shows a simplified block diagram of the CCP module in PWM mode.

For a step by step procedure on how to set up the CCP module for PWM operation, see Section 10.3.3.

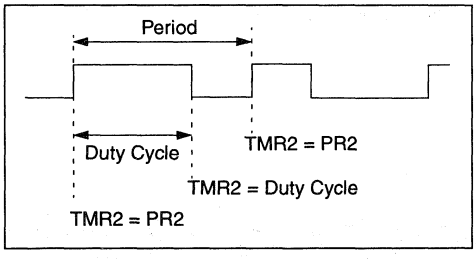
FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base.

A PWM output (Figure 10-5) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 10-5: PWM OUTPUT



10.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

PWM period = [(PR2) + 1] * 4 * Tosc * (TMR2 prescale value)

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (Section 9.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

10.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSbs and CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle:

PWM duty cycle = (CCPR1L:CCP1CON<5:4>) * Tosc * (TMR2 prescale value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period (PWM duty cycle = 100%), the CCP1 pin will not be cleared.

EXAMPLE 10-2: PWM PERIOD AND DUTY CYCLE CALCULATION

Desired PWM frequency is 31.25 kHz,
Fosc = 8 MHz
TMR2 prescale = 1

1/31.25 kHz = [(PR2) + 1] * 4 * 1/8 MHz * 1
32 µs = [(PR2) + 1] * 4 * 125 ns * 1
PR2 = 63

Find the maximum resolution of the duty cycle that can be used with a 31.25 kHz frequency and 8 MHz oscillator:

1/31.25 kHz = $2^{\text{PWM RESOLUTION}}$ * 1/8 MHz * 1
32 µs = $2^{\text{PWM RESOLUTION}}$ * 125 ns * 1
256 = $2^{\text{PWM RESOLUTION}}$
log(256) = (PWM Resolution) * log(2)
8.0 = PWM Resolution

At most, an 8-bit resolution duty cycle can be obtained from a 31.25 kHz frequency and a 8 MHz oscillator, i.e., 0 ≤ CCPR1L:CCP1CON<5:4> ≤ 255. Any value greater than 255 will result in a 100% duty cycle.

In order to achieve higher resolution, the PWM frequency must be decreased. In order to achieve higher PWM frequency, the resolution must be decreased.

Table 10-2 lists example PWM frequencies and resolutions for Fosc = 8 MHz. TMR2 prescaler and PR2 values are also shown.

10.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP module for PWM operation.

TABLE 10-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 8 MHz

PWM Frequency	488 Hz	1.95 kHz	7.81 kHz	31.25 kHz	62.5 kHz	250 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x07
Maximum Resolution (bits)	10	10	10	8	7	5

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TABLE 10-3: REGISTERS ASSOCIATED WITH TIMER1, CAPTURE AND COMPARE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in these modes.
Note 1: Bits ADIE and ADIF reserved on the PIC16C923, always maintain these bits clear.

TABLE 10-4: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's Period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used in this mode.
Note 1: Bits ADIE and ADIF reserved on the PIC16C923, always maintain these bits clear.

NOTES:

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11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

Refer to Application Note AN578, *"Use of the SSP Module in the I^2C Multi-Master Environment."*

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **SMP:** SPI data input sample phase
SPI Master Mode
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave Mode
SMP must be cleared when SPI is used in slave mode

bit 6: **CKE**: SPI Clock Edge Select (Figure 11-5, Figure 11-6, and Figure 11-7)
CKP = 0
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK
CKP = 1
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK

bit 5: **D/$\overline{A}$**: Data/$\overline{Address}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)
0 = Stop bit was not detected last

bit 3: **S**: Start bit (I^2C mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)
0 = Start bit was not detected last

bit 2: **R/$\overline{W}$**: Read/Write bit information (I^2C mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next start bit, stop bit, or $\overline{ACK}$ bit.
1 = Read
0 = Write

bit 1: **UA**: Update Address (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit

Receive (SPI and I^2C modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit (I^2C mode only)
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

FIGURE 11-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **WCOL**: Write Collision Detect bit
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6: **SSPOV**: Receive Overflow Indicator bit

In SPI mode
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In master mode the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
0 = No overflow

In I^2C mode
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in transmit mode. SSPOV must be cleared in software in either mode.
0 = No overflow

bit 5: **SSPEN**: Synchronous Serial Port Enable bit

In SPI mode
1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins
0 = Disables serial port and configures these pins as I/O port pins

In I^2C mode
1 = Enables the serial port and configures the SDA and SCL pins as serial port pins
0 = Disables serial port and configures these pins as I/O port pins
In both modes, when enabled, these pins must be properly configured as input or output.

bit 4: **CKP**: Clock Polarity Select bit
In SPI mode
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
In I^2C mode
SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch) (Used to ensure data setup time)

bit 3-0: **SSPM3:SSPM0**: Synchronous Serial Port Mode Select bits
0000 = SPI master mode, clock = Fosc/4
0001 = SPI master mode, clock = Fosc/16
0010 = SPI master mode, clock = Fosc/64
0011 = SPI master mode, clock = TMR2 output/2
0100 = SPI slave mode, clock = SCK pin. $\overline{SS}$ pin control enabled.
0101 = SPI slave mode, clock = SCK pin. $\overline{SS}$ pin control disabled. $\overline{SS}$ can be used as I/O pin
0110 = I^2C slave mode, 7-bit address
0111 = I^2C slave mode, 10-bit address
1011 = I^2C Firmware controlled master mode (slave idle)
1110 = I^2C slave mode, 7-bit address with start and stop bit interrupts enabled
1111 = I^2C slave mode, 10-bit address with start and stop bit interrupts enabled

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11.1 SPI Mode

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI
- Serial Clock (SCK) RC3/SCK

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select ($\overline{SS}$) RA5/AN4/$\overline{SS}$ (the AN4 function is implemented on the PIC16C924 only)

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select Mode (Slave mode only)

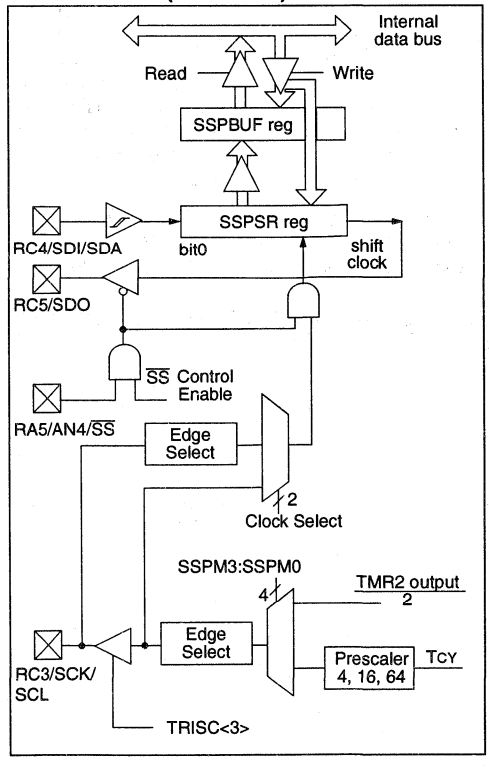
The SSP consists of a transmit/receive Shift Register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit BF (SSPSTAT<0>) and interrupt flag bit SSPIF (PIR1<3>) are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit WCOL (SSPCON<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully. When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit BF (SSPSTAT<0>) indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, bit BF is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-1 shows the loading of the SSPBUF (SSPSR) for data transmission. The shaded instruction is only required if the received data is meaningful.

EXAMPLE 11-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
     BCF   STATUS, RP1    ;Specify Bank 1
     BSF   STATUS, RP0    ;
LOOP BTFSS SSPSTAT, BF    ;Has data been
                          ;received
                          ;(transmit
                          ;complete)?
     GOTO  LOOP           ;No
     BCF   STATUS, RP0    ;Specify Bank 0
     MOVF  SSPBUF, W      ;W reg = contents
                          ; of SSPBUF
     MOVWF RXDATA         ;Save in user RAM
     MOVF  TXDATA, W      ;W reg = contents
                          ; of TXDATA
     MOVWF SSPBUF         ;New data to xmit
```

The block diagram of the SSP module, when in SPI mode (Figure 11-3), shows that the SSPSR is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

FIGURE 11-3: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- $\overline{SS}$ must have TRISA<5> set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and $\overline{SS}$ could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

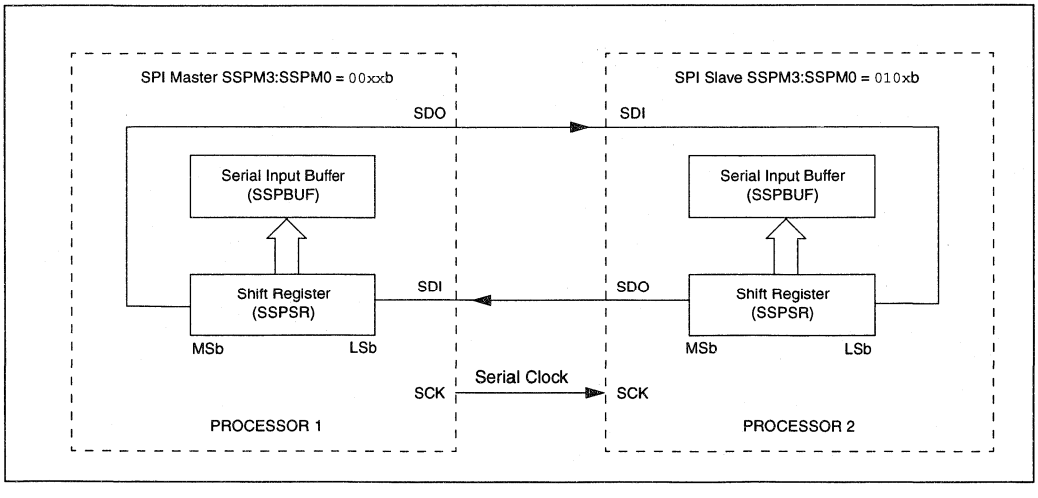
The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-5, Figure 11-6, and Figure 11-7 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 • TCY)
- FOSC/64 (or 16 • TCY)
- Timer2 output/2

This allows a maximum bit clock frequency (at 8 MHz) of 2 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

FIGURE 11-4: SPI MASTER/SLAVE CONNECTION



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The $\overline{SS}$ pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set for the synchronous slave mode to be enabled. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/ pull-down resistors may be desirable, depending on the application.

Note: When the SPI is in Slave Mode with $\overline{SS}$ pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the $\overline{SS}$ pin is set to VDD.

Note: If the SPI is used in Slave Mode with CKE = '1', then the $\overline{SS}$ pin control must be enabled.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

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FIGURE 11-5: SPI MODE TIMING, MASTER MODE

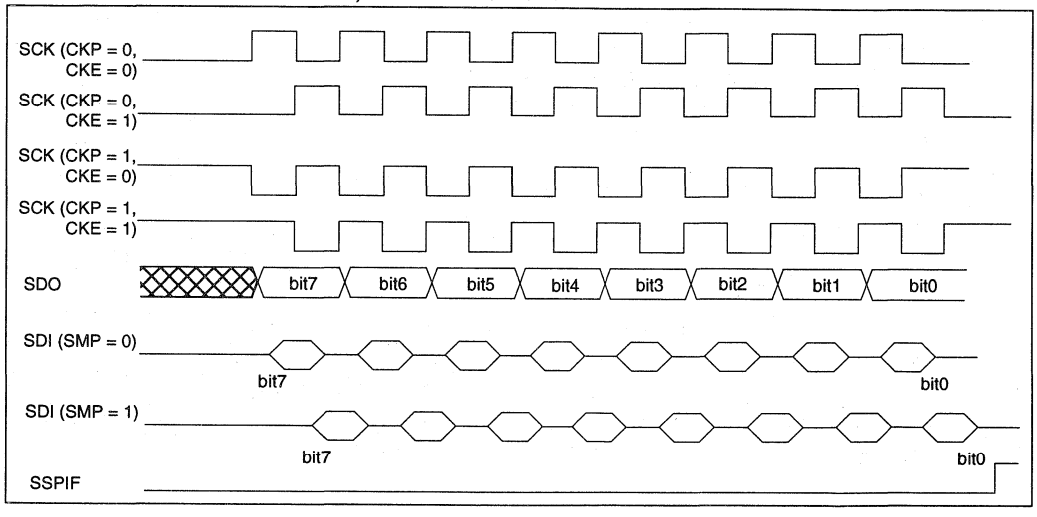

FIGURE 11-6: SPI MODE TIMING (SLAVE MODE WITH CKE = 0)

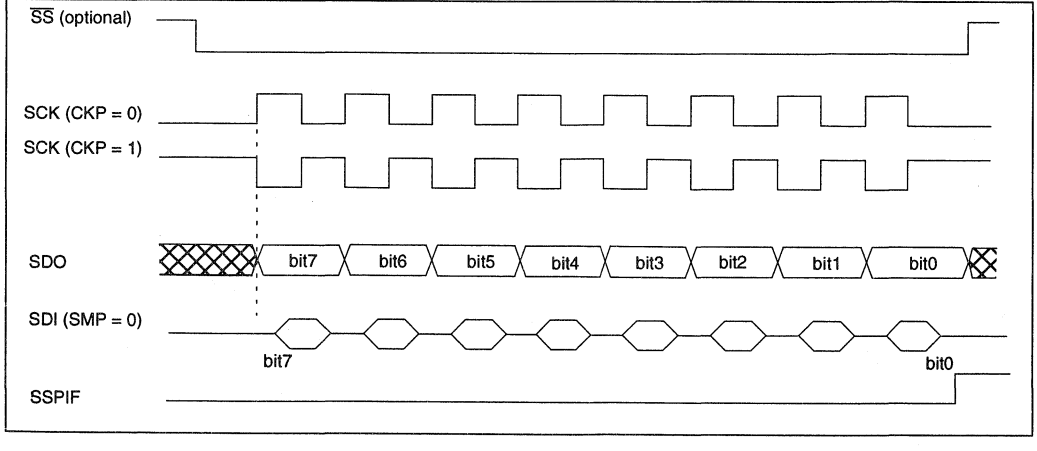

FIGURE 11-7: SPI MODE TIMING (SLAVE MODE WITH CKE = 1)

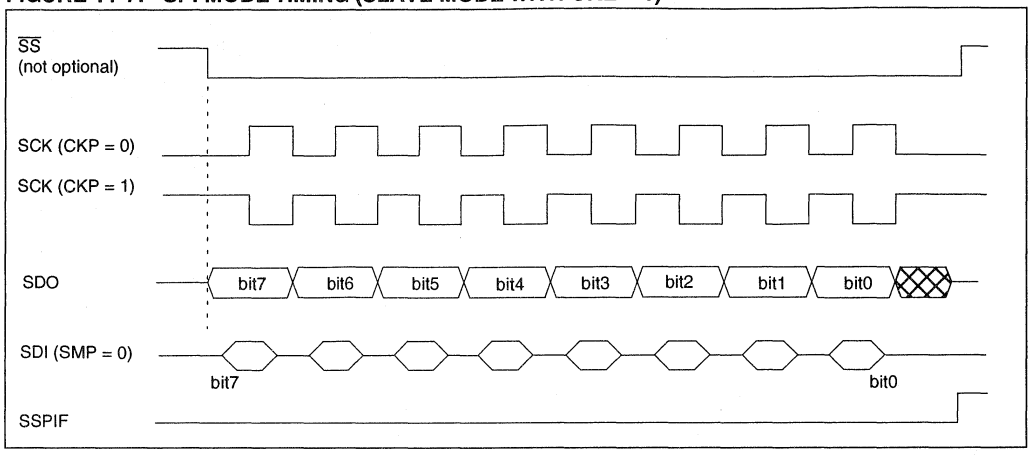

TABLE 11-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the SSP in SPI mode.
Note 1: Bits ADIE and ADIF are reserved on the PIC16C923, always maintain these bits clear.

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11.2 I²C™ Overview

This section provides an overview of the Inter-Integrated Circuit (I^2C) bus, with Section 11.3 discussing the operation of the SSP module in I^2C mode.

The I^2C bus is a two-wire serial interface developed by the Philips Corporation. The original specification, or standard mode, was for data transfers of up to 100 Kbps. An enhanced specification, or fast mode is not supported. This device will communicate with fast mode devices if attached to the same bus.

The I^2C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master" which initiates transfer on the bus and generates the clock signals to permit that transfer, while the other device(s) acts as the "slave." All portions of the slave protocol are implemented in the SSP module's hardware, except general call support, while portions of the master protocol need to be addressed in the PIC16CXX software. Table 11-2 defines some of the I^2C bus terminology. For additional information on the I^2C interface specification, refer to the Philips document "*The I^2C bus and how to use it.*"#939839340011, which can be obtained from the Philips Corporation.

In the I^2C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to "talk" to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read-from/write-to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of as operating in either of these two relations:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level when no device is pulling the line down. The number of devices that may be attached to the I^2C bus is limited only by the maximum bus loading specification of 400 pF.

11.2.1 INITIATING AND TERMINATING DATA TRANSFER

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure 11-8 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

FIGURE 11-8: START AND STOP CONDITIONS

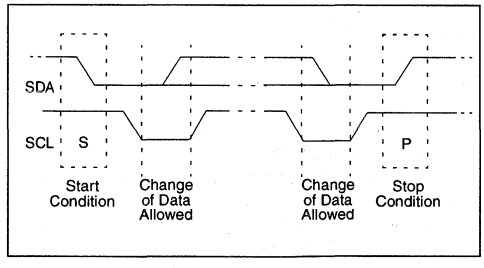


TABLE 11-2: I^2C BUS TERMINOLOGY

Term	Description
Transmitter	The device that sends the data to the bus.
Receiver	The device that receives the data from the bus.
Master	The device which initiates the transfer, generates the clock and terminates the transfer.
Slave	The device addressed by a master.
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensure that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

11.2.2 ADDRESSING I^2C DEVICES

There are two address formats. The simplest is the 7-bit address format with a R/$\overline{W}$ bit (Figure 11-9). The more complex is the 10-bit address with a R/$\overline{W}$ bit (Figure 11-10). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

FIGURE 11-9: 7-BIT ADDRESS FORMAT

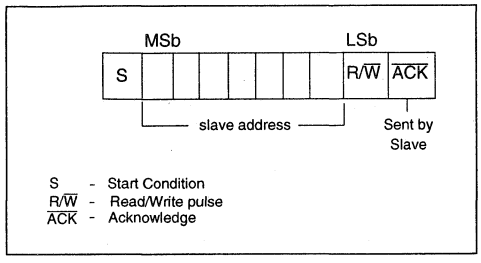
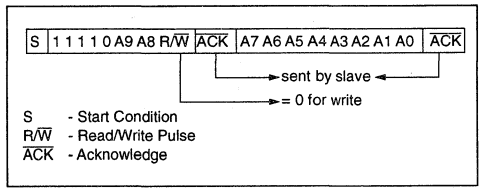


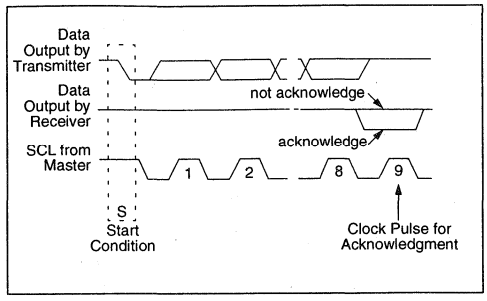
FIGURE 11-10: I^2C 10-BIT ADDRESS FORMAT



11.2.3 TRANSFER ACKNOWLEDGE

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit ($\overline{ACK}$) (Figure 11-11). When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP condition (Figure 11-8).

FIGURE 11-11: SLAVE-RECEIVER ACKNOWLEDGE



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level, Figure 11-12. The slave will inherently stretch the clock, when it is a transmitter, but will not when it is a receiver. The slave will have to clear the SSPCON<4> bit to enable clock stretching when it is a receiver.

FIGURE 11-12: DATA TRANSFER WAIT STATE

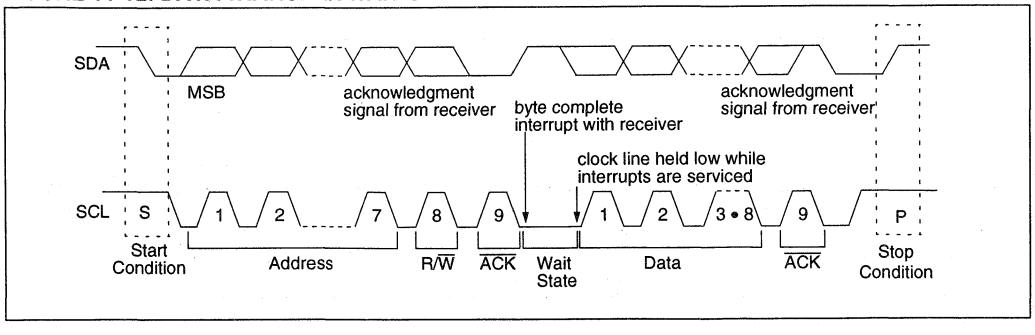


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Figure 11-13 and Figure 11-14 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-15.

FIGURE 11-13: MASTER-TRANSMITTER SEQUENCE

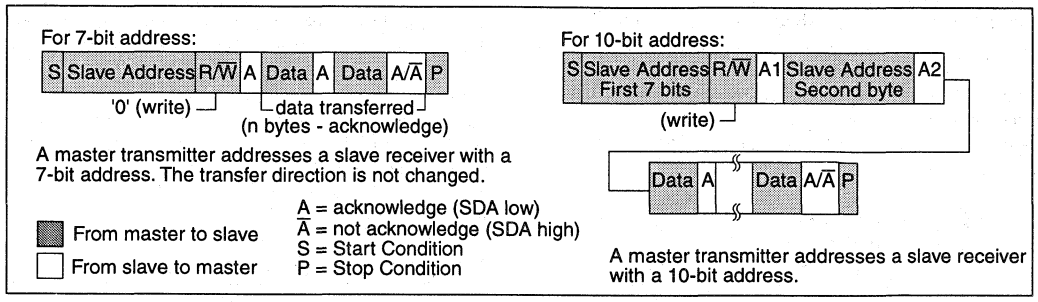


FIGURE 11-14: MASTER-RECEIVER SEQUENCE

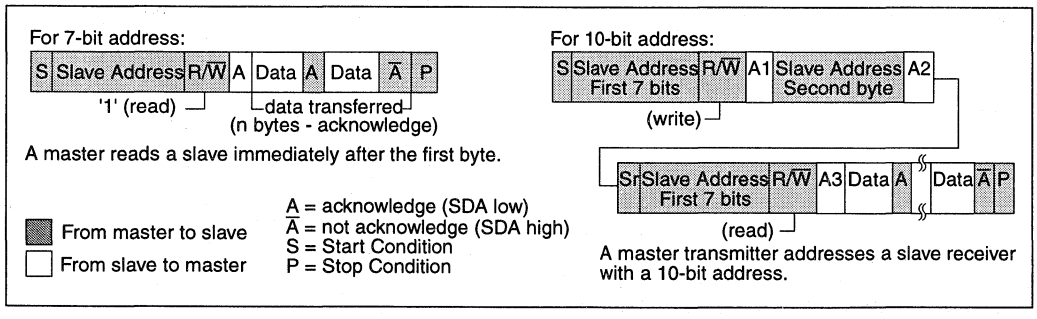
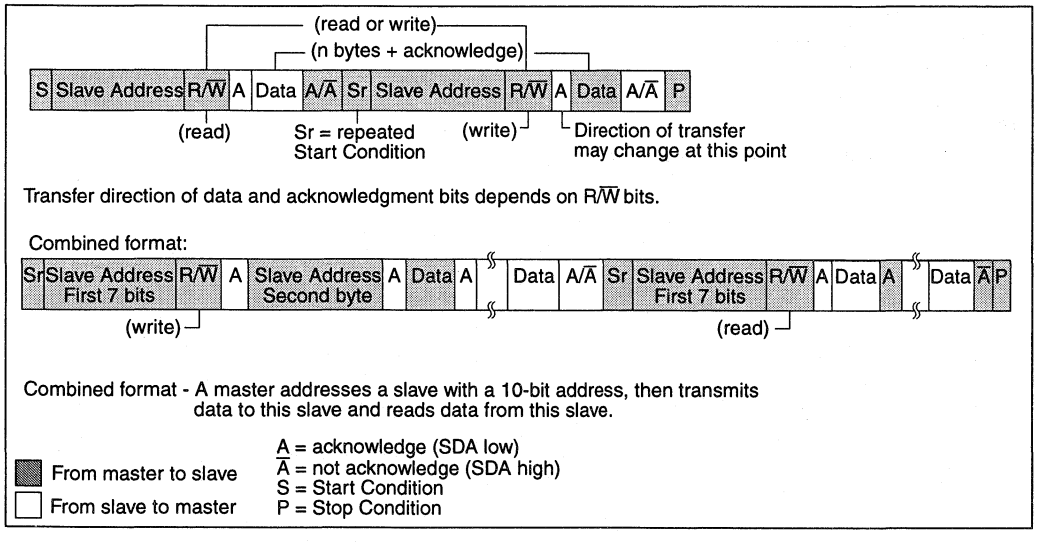


FIGURE 11-15: COMBINED FORMAT



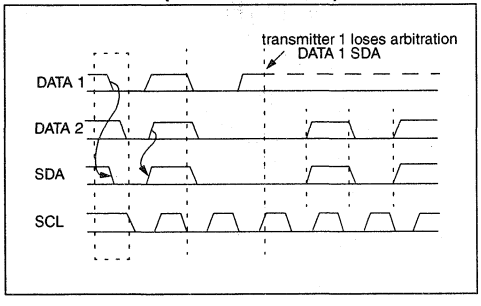
11.2.4 MULTI-MASTER

The I^2C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

11.2.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure 11-16), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

FIGURE 11-16: MULTI-MASTER ARBITRATION (TWO MASTERS)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

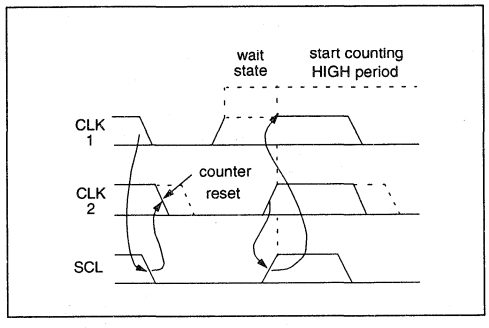
- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

11.2.4.2 Clock Synchronization

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period, Figure 11-17.

FIGURE 11-17: CLOCK SYNCHRONIZATION



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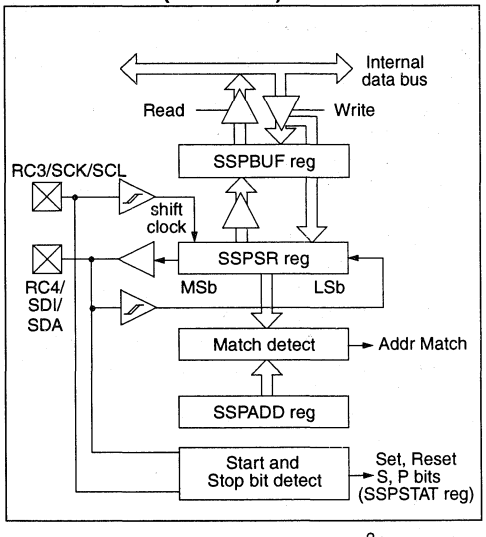
11.3 SSP I²C Operation

The SSP module in I²C mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to facilitate software implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

FIGURE 11-18: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with with start and stop bit interrupts enabled
- I²C Firmware controlled Master Mode, slave is idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

11.3.1 SLAVE MODE

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge ($\overline{ACK}$) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this $\overline{ACK}$ pulse. These are if either (or both):

a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.

b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 11-3 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I^2C specification as well as the requirement of the SSP module is shown in timing parameter #100 and parameter #101.

11.3.1.1 ADDRESSING

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

a) The SSPSR register value is loaded into the SSPBUF register.

b) The buffer full bit, BF is set.

c) An $\overline{ACK}$ pulse is generated.

d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave (Figure 11-10). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/$\overline{W}$ (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for a 10-bit address is as follows, with steps 7- 9 for slave-transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
5. Update the SSPADD register with the first (high) byte of Address, if match releases SCL line, this will clear bit UA.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive repeated START condition.
8. Receive first (high) byte of Address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

TABLE 11-3: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received				
BF	**SSPOV**	**SSPSR → SSPBUF**	**Generate $\overline{ACK}$ Pulse**	**Set bit SSPIF (SSP Interrupt occurs if enabled)**
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

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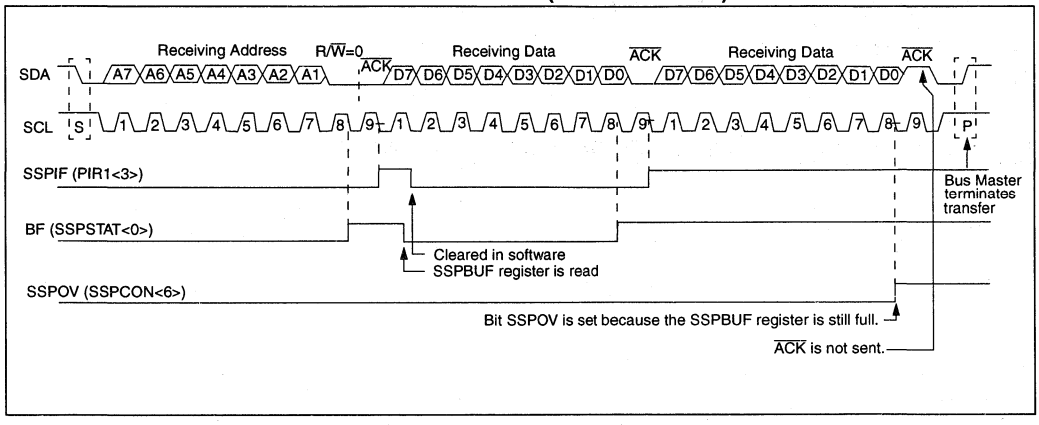
11.3.1.2 RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

FIGURE 11-19: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



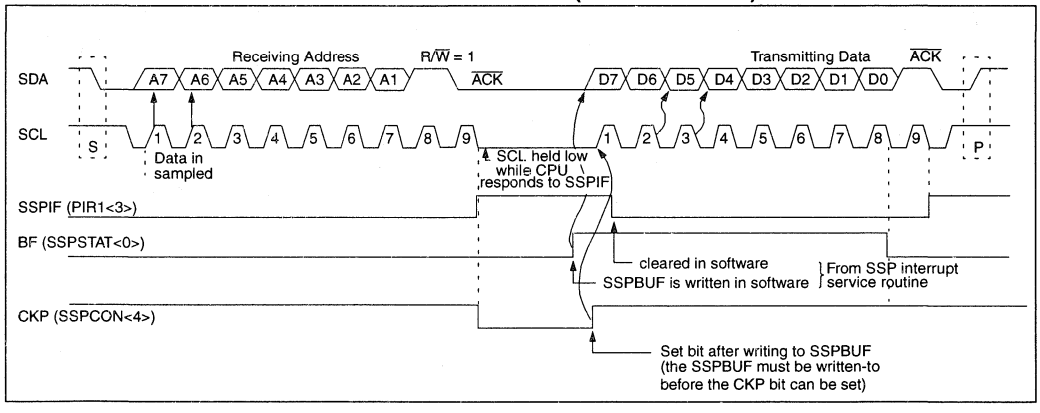
11.3.1.3 TRANSMISSION

When the R/$\overline{W}$ bit of the incoming address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The $\overline{ACK}$ pulse will be sent on the ninth bit, and pin RC3/SCK/SCL is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 11-20).

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. When the $\overline{ACK}$ is latched by the slave, the slave logic is reset and the slave then monitors for another occurrence of the START bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP.

FIGURE 11-20: I^2C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



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11.3.2 MASTER MODE

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is idle with both the S and P bits clear.

In master mode the SCL and SDA lines are manipulated by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

11.3.3 MULTI-MASTER MODE

In multi-master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, they are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed an $\overline{ACK}$ pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

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TABLE 11-4: REGISTERS ASSOCIATED WITH I^2C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by SSP in I^2C mode.
Note 1: Bits ADIE and ADIF are reserved on the PIC16C923, always maintain these bits clear.

FIGURE 11-21: OPERATION OF THE I²C MODULE IN IDLE_MODE, RCV_MODE OR XMIT_MODE

```
IDLE_MODE (7-bit):
if (Addr_match)                 {       Set interrupt;
                                        if (R/W = 1)    {       Send ACK = 0;
                                                                set XMIT_MODE;
                                                        }
                                        else if (R/W = 0) set RCV_MODE;
                                }
RCV_MODE:
if ((SSPBUF=Full) OR (SSPOV = 1))
        {       Set SSPOV;
                Do not acknowledge;
        }
else    {       transfer SSPSR → SSPBUF;
                send ACK = 0;
        }
Receive 8-bits in SSPSR;
Set interrupt;
XMIT_MODE:
While ((SSPBUF = Empty) AND (CKP=0)) Hold SCL Low;
Send byte;
Set interrupt;
if ( ACK Received = 1)          {       End of transmission;
                                        Go back to IDLE_MODE;
                                }
else if ( ACK Received = 0)   Go back to XMIT_MODE;
IDLE_MODE (10-Bit):
If (High_byte_addr_match AND (R/W = 0))
        {       PRIOR_ADDR_MATCH = FALSE;
                Set interrupt;
                if ((SSPBUF = Full) OR  (SSPOV = 1))
                        {       Set SSPOV;
                                Do not acknowledge;
                        }
                else    {       Set UA = 1;
                                Send ACK = 0;
                                While (SSPADD not updated) Hold SCL low;
                                Clear UA = 0;
                                Receive Low_addr_byte;
                                Set interrupt;
                                Set UA = 1;
                                If (Low_byte_addr_match)
                                        {       PRIOR_ADDR_MATCH = TRUE;
                                                Send ACK = 0;
                                                while (SSPADD not updated) Hold SCL low;
                                                Clear UA = 0;
                                                Set RCV_MODE;
                                        }
                        }
        }
else if (High_byte_addr_match AND (R/W = 1)
        {       if (PRIOR_ADDR_MATCH)
                        {       send ACK = 0;
                                set XMIT_MODE;
                        }
        else PRIOR_ADDR_MATCH = FALSE;
        }
```

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12.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

This section applies to the PIC16C924 only.

The analog-to-digital (A/D) converter module has five inputs.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Figure 12-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 12-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

FIGURE 12-1: ADCON0 REGISTER (ADDRESS 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from an RC oscillation)

bit 5-3: **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)

bit 2: **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

If ADON = 1
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **Unimplemented**: Read as '0'

bit 0: **ADON**: A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

FIGURE 12-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-3: **Unimplemented:** Read as '0'

bit 2-0: **PCFG2:PCFG0**: A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA5	RA3	VREF
000	A	A	A	A	A	VDD
001	A	A	A	A	VREF	RA3
010	A	A	A	A	A	VDD
011	A	A	A	A	VREF	RA3
100	A	A	D	D	A	VDD
111	D	D	D	D	D	—

A = Analog input

D = Digital I/O

The ADRES register contains the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 12-3.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine sample time, see Section 12.1. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins / voltage reference / and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

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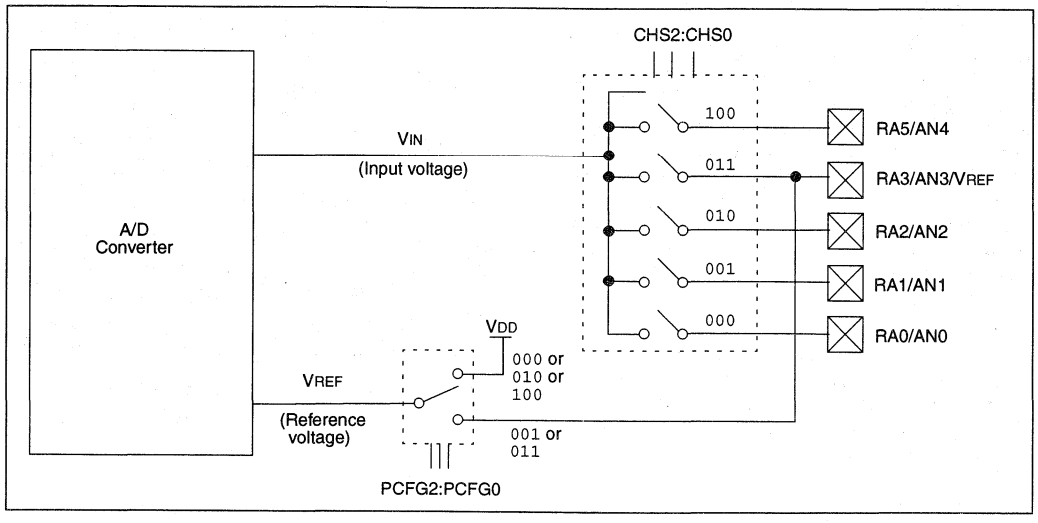
FIGURE 12-3: A/D BLOCK DIAGRAM



12.1 A/D Sampling Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 12-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), (Figure 12-4). **The maximum recommended impedance for analog sources is 10 kΩ.** After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 12-1 may be used. This equation assumes that 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

EQUATION 12-1: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/512)) \bullet (1 - e^{(-Tc/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$

or

$$Tc = -(51.2\ pF)(1\ k\Omega + R_{SS} + R_S)\ \ln(1/511)$$

Example 12-1 shows the calculation of the minimum required acquisition time (TACQ). This calculation is based on the following system assumptions.

RS = 10 kΩ

1/2 LSb error

VDD = 5V → RSS = 7 kΩ

Temp (system max.) = 50°C

VHOLD = 0 @ t = 0

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

Note 3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

Note 4: After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

EXAMPLE 12-1: CALCULATING THE MINIMUM REQUIRED SAMPLE TIME

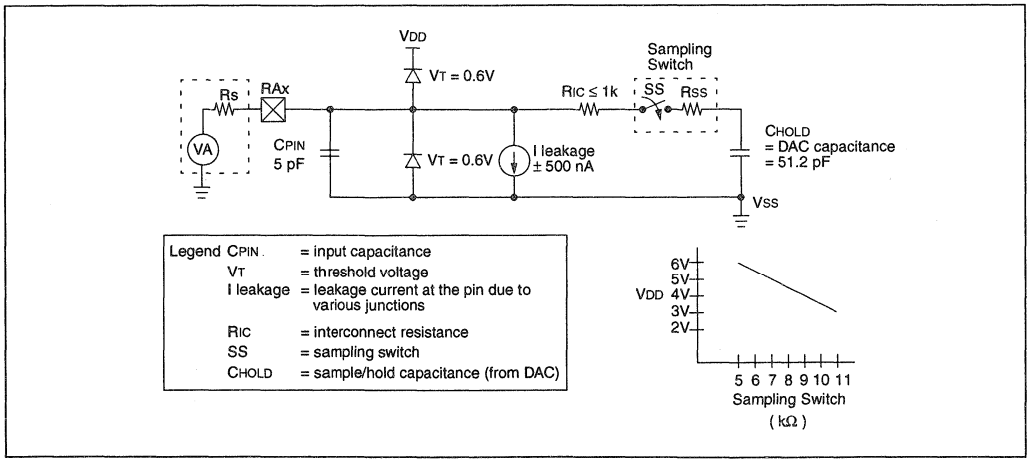
TACQ = Amplifier Settling Time +
Holding Capacitor Charging Time +
Temperature Coefficient

TACQ = 5 µs + Tc + [(Temp - 25°C)(0.05 µs/°C)]

TC = -CHOLD (RIC + RSS + RS) ln(1/512)
-51.2 pF (1 kΩ + 7 kΩ + 10 kΩ) ln(0.0020)
-51.2 pF (18 kΩ) ln(0.0020)
-0.921 µs (-6.2146)
5.724 µs

TACQ = 5 µs + 5.724 µs + [(50°C - 25°C)(0.05 µs/°C)]
10.724 µs + 1.25 µs
11.974 µs

FIGURE 12-4: ANALOG INPUT MODEL



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12.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5 TAD per 8-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for TAD are:

- 2TOSC
- 8TOSC
- 32TOSC
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 µs.

Table 12-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

12.3 Configuring Analog Port Pins

The ADCON1 and TRISA registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, all pins configured as analog inputs will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the AN4:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

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TABLE 12-1: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**8 MHz**	**5 MHz**	**1.25 MHz**	**333.33 kHz**
2TOSC	00	250 ns(2)	400 ns(2)	1.6 µs	6 µs
8TOSC	01	1 µs	1.6 µs	6.4 µs	24 µs(3)
32TOSC	10	4 µs	6.4 µs	25.6 µs(3)	96 µs(3)
RC	11	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1)

Note 1: The RC source has a typical TAD time of 4 µs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: While in RC mode, with device frequency above 1 MHz, conversion accuracy is out of specification.

12.4 A/D Conversions

Example 12-2 show how to perform an A/D conversion. The RA pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the RA0 channel.

Note: The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

EXAMPLE 12-2: DOING AN A/D CONVERSION

```
    BCF     STATUS, RP1         ; Select Bank 1
    BSF     STATUS, RP0         ;
    CLRF    ADCON1              ; Configure A/D inputs
    BSF     PIE1,   ADIE        ; Enable A/D interrupts
    BCF     STATUS, RP0         ; Select Bank 0
    MOVLW   0xC1                ; RC Clock, A/D is on, Channel 0 is selected
    MOVWF   ADCON0              ;
    BCF     PIR1,   ADIF        ; Clear A/D interrupt flag bit
    BSF     INTCON, PEIE        ; Enable peripheral interrupts
    BSF     INTCON, GIE         ; Enable all interrupts
;
;  Ensure that the required acquisition time for the selected input channel has elapsed.
;  Then the conversion may be started.
;
    BSF     ADCON0, GO          ; Start A/D Conversion
      :                         ; The ADIF bit will be set and the GO/DONE bit
      :                         ;  is cleared upon completion of the A/D Conversion.
```

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12.4.1 FASTER CONVERSION - LOWER RESOLUTION TRADE-OFF

Not all applications require a result with 8-bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the A/D module may be switched so that the TAD time violates the minimum specified time (see the applicable electrical specification). Once the TAD time violates the minimum specified time, all the following A/D result bits are not valid (see A/D Conversion Timing in the Electrical Specifications section.) The clock sources may only be switched between the three oscillator versions (cannot be switched from/to RC). The equation to determine the time before the oscillator can be switched is as follows:

Conversion time = $2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$
Where: N = number of bits of resolution required.

Since the TAD is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D oscillator may be changed. Example 12-3 shows a comparison of time required for a conversion with 4-bits of resolution, versus the 8-bit resolution conversion. The example is for devices operating at 8 MHz (The A/D clock is programmed for $32T_{OSC}$), and assumes that immediately after $6T_{AD}$, the A/D clock is programmed for $2T_{OSC}$.

The $2T_{OSC}$ violates the minimum TAD time, therefore the last 4-bits will not be converted to correct values.

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EXAMPLE 12-3: 4-BIT vs. 8-BIT CONVERSION TIMES

	Freq. (MHz)	Resolution	
		4-bit	8-bit
TAD	8	1.6 µs	1.6 µs
TOSC	8	12.5 ns	125 ns
$2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$	8	10.6 µs	16 µs

12.5 A/D Operation During Sleep

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/$\overline{\text{DONE}}$ bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in SLEEP, the GO/$\overline{\text{DONE}}$ bit must be set, followed by the SLEEP instruction.

12.6 A/D Accuracy/Error

The overall accuracy of the A/D is less than ± 1 LSb for V_{DD} = 5V ± 10% and the analog V_{REF} = V_{DD}. This overall accuracy includes offset error, full scale error, and integral error. The A/D converter is guaranteed to be monotonic. The resolution and accuracy may be less when either the analog reference (V_{DD}) is less than 5.0V or when the analog reference (V_{REF}) is less than V_{DD}.

The maximum pin leakage current is ± 5 µA.

In systems where the device frequency is low, use of the A/D internal RC clock is preferred. At moderate to high frequencies, T_{AD} should be derived from the device oscillator. T_{AD} must not violate the minimum and should be ≤ 8 µs for preferred operation. This is because T_{AD}, when derived from T_{OSC}, is kept away from on-chip phase clock transitions. This reduces, to a large extent, the effects of digital switching noise. This is not possible with the RC derived clock. The loss of accuracy due to digital switching noise can be significant if many I/O pins are active.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

12.7 Effects of a RESET

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRES register is not modified for a Power-on Reset. The ADRES register will contain unknown data after a Power-on Reset.

12.8 Use of the CCP Trigger

An A/D conversion can be started by the "special event trigger" of the CCP1 module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as 1011 and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving the ADRES to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the "special event trigger" sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 counter.

12.9 Connection Considerations

If the input voltage exceeds the rail values (V_{SS} or V_{DD}) by greater than 0.2V, then the accuracy of the conversion is out of specification.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 kΩ recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

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12.10 Transfer Function

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) is 1 LSb (or Analog VREF / 256) (Figure 12-5).

FIGURE 12-5: A/D TRANSFER FUNCTION

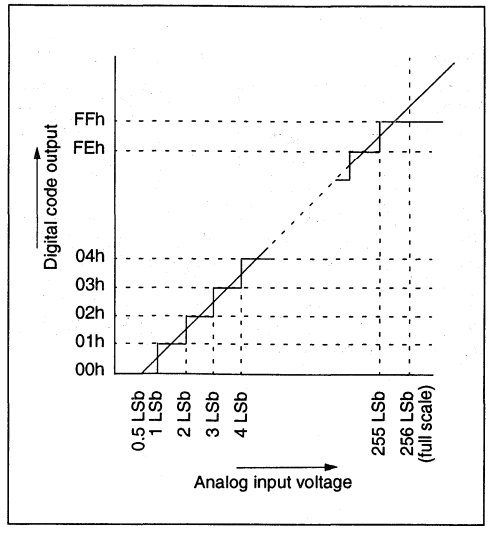

FIGURE 12-6: FLOWCHART OF A/D OPERATION

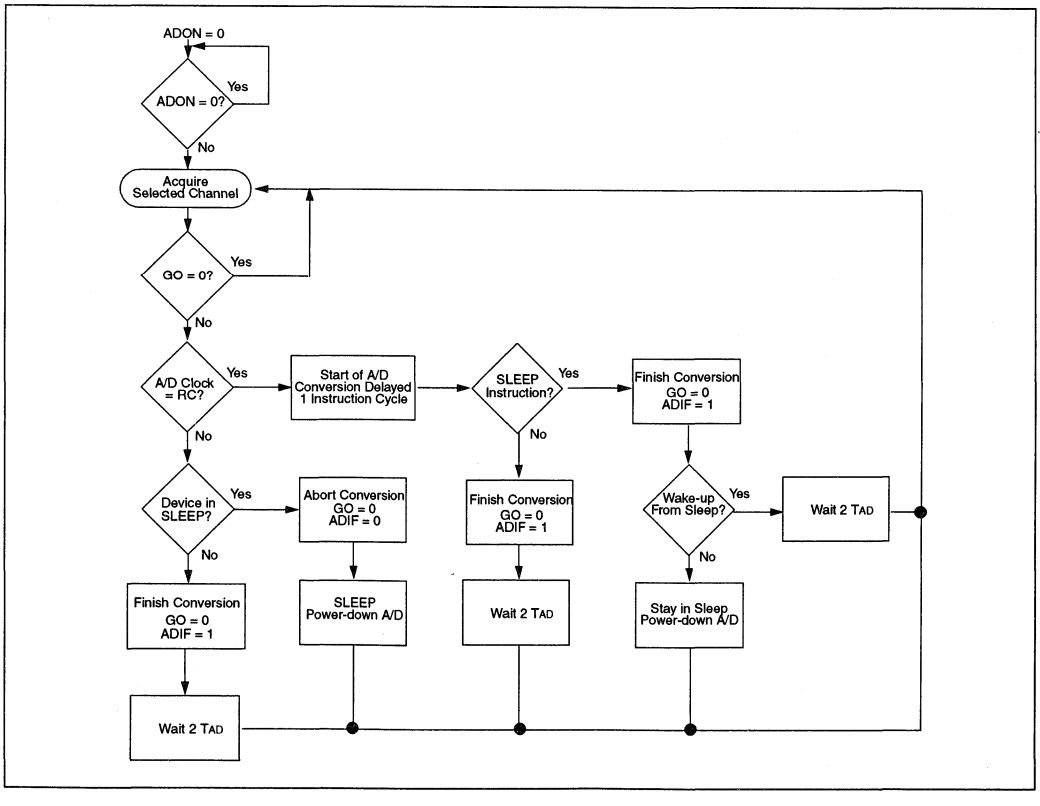

TABLE 12-2: SUMMARY OF A/D REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

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13.0 LCD MODULE

The LCD module generates the timing control to drive a static or multiplexed LCD panel, with support for up to 32 segments multiplexed with up to 4 commons. It also provides control of the LCD pixel data.

The interface to the module consists of 3 control registers (LCDCON, LCDSE, and LCDPS) used to define the timing requirements of the LCD panel and up to 16 LCD data registers (LCD00-LCD15) that represent the array of the pixel data. In normal operation, the control registers are configured to match the LCD panel being used. Primarily, the initialization information consists of selecting the number of commons required by the LCD panel, and then specifying the LCD Frame clock rate to be used by the panel.

Once the module is initialized for the LCD panel, the individual bits of the LCD data registers are cleared/set to represent a clear/dark pixel respectively.

Once the module is configured, the LCDEN (LCDCON<7>) bit is used to enable or disable the LCD module. The LCD panel can also operate during sleep by clearing the SLPEN (LCDCON<6>) bit.

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FIGURE 13-1: LCDCON REGISTER (ADDRESS 10Fh)

R/W-0	R/W-0	U	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDEN	SLPEN	—	VGEN	CS1	CS0	LMUX1	LMUX0
bit7							bit0

R =Readable bit
W =Writable bit
U =Unimplemented bit, Read as '0'
-n =Value at POR reset

bit 7: **LCDEN**: Module drive enable bit
1 = LCD drive enabled
0 = LCD drive disabled

bit 6: **SLPEN**: LCD display sleep enable
1 = LCD module will stop operating during SLEEP
0 = LCD module will continue to display during SLEEP

bit 5: **Unimplemented:** Read as '0'

bit 4: **VGEN**: Voltage Generator Enable
1 = Internal LCD Voltage Generator Enabled, (powered-up)
0 = Internal LCD Voltage Generator powered-down, voltage is expected to be provided externally

bit 3-2: **CS1:CS0**: Clock Source Select bits
00 = Fosc/256
01 = T1CKI (Timer1)
1x = Internal RC oscillator

bit 1-0: **LMUX1:LMUX0**: Common Selection bits
Specifies the number of commons and the bias method

LMUX1:LMUX0	MULTIPLEX	BIAS	Max # of Segments
00	Static (COM0)	Static	32
01	1/2 (COM0, 1)	1/3	31
10	1/3 (COM0, 1, 2)	1/3	30
11	1/4 (COM0, 1, 2, 3)	1/3	29

FIGURE 13-2: LCD MODULE BLOCK DIAGRAM

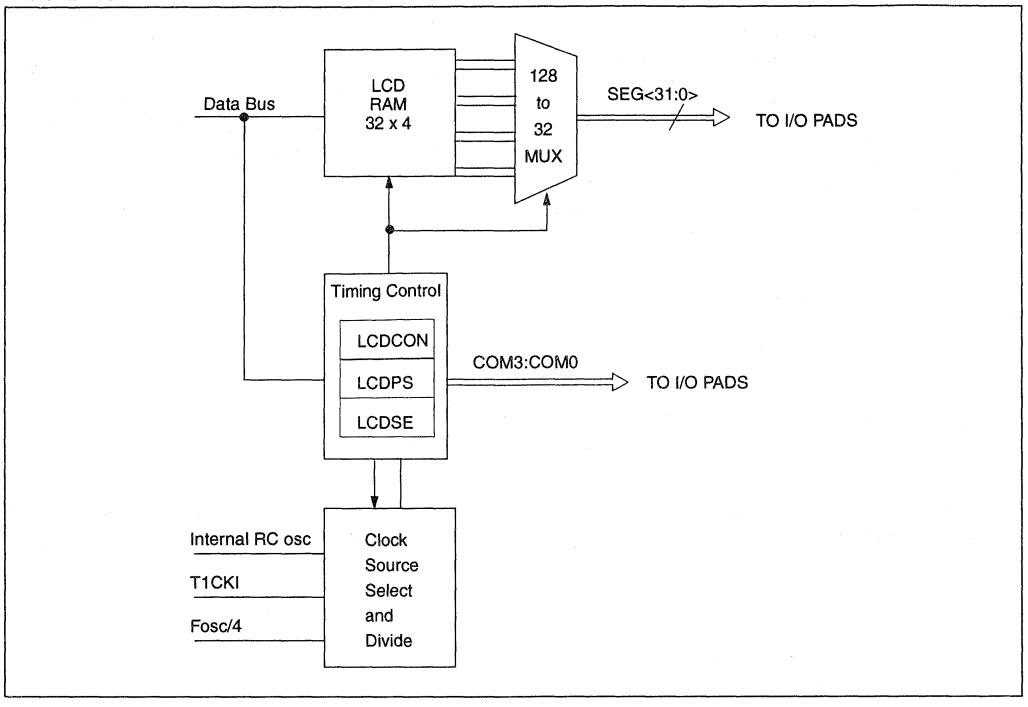

FIGURE 13-3: LCDPS REGISTER (ADDRESS 10Eh)

U	U	U	U	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	LP3	LP2	LP1	LP0
bit7							bit0

R =Readable bit
W =Writable bit
U =Unimplemented bit, Read as '0'
-n =Value at POR reset

bit 7-4: **Unimplemented,** read as '0'

bit 3-0: **LP3:LP0**: Frame Clock Prescale Selection bits

LMUX1:LMUX0	Multiplex	Frame Frequency =
00	Static	Clock source / (128 * (LP3:LP0 + 1))
01	1/2	Clock source / (128 * (LP3:LP0 + 1))
10	1/3	Clock source / (96 * (LP3:LP0 + 1))
11	1/4	Clock source / (128 * (LP3:LP0 + 1))

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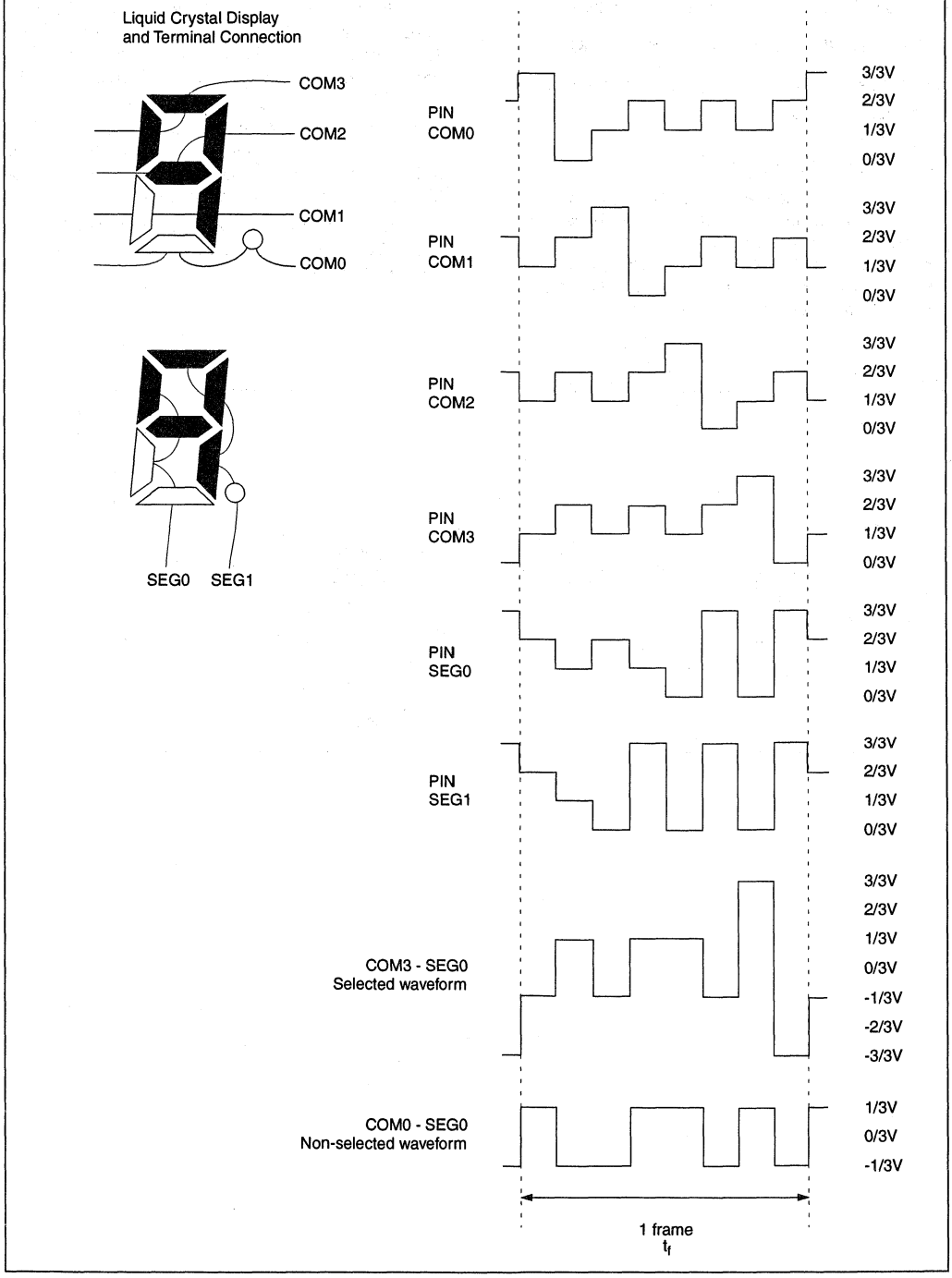
FIGURE 13-4: WAVEFORMS IN 1/4 MUX DRIVE



13.1 LCD Timing

The LCD module has 3 possible clock source inputs and supports static, 1/2, 1/3, and 1/4 multiplexing.

13.1.1 TIMING CLOCK SOURCE SELECTION

The clock sources for the LCD timing generation are:

- Internal RC oscillator
- Timer1 oscillator
- System clock divided by 256

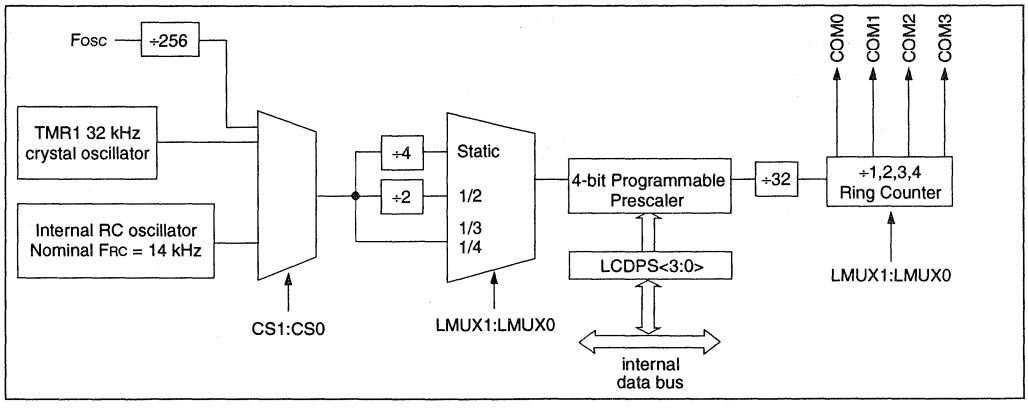
The first timing source is an internal RC oscillator which runs at a nominal frequency of 14 kHz. This oscillator provides a lower speed clock which may be used to continue running the LCD while the processor is in sleep. The RC oscillator will power-down when it is not selected or when the LCD module is disabled.

The second source is the Timer1 external oscillator. This oscillator provides a lower speed clock which may be used to continue running the LCD while the processor is in sleep. It is assumed that the frequency provided on this oscillator will be 32 kHz. To use the Timer1 oscillator as a LCD module clock source, it is only necessary to set the T1OSCEN (T1CON<3>) bit.

The third source is the system clock divided by 256. This divider ratio is chosen to provide about 32 kHz output when the external oscillator is 8 MHz. The divider is not programmable. Instead the LCDPS register is used to set the LCD frame clock rate.

All of the clock sources are selected with bits CS1:CS0 (LCDCON<3:2>). Refer to Figure 13-1 for details of the register programming.

FIGURE 13-5: LCD CLOCK GENERATION



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13.1.2 MULTIPLEX TIMING GENERATION

The timing generation circuitry will generate 1 to 4 common clocks based on the display mode selected. The mode is specified by bits LMUX1:LMUX0 (LCDCON<1:0>). Table 13-1 shows the formulas for calculating the frame frequency.

TABLE 13-1: FRAME FREQUENCY FORMULAS

Multiplex	Frame Frequency =
Static	Clock source / (128 * (LP3:LP0 + 1))
1/2	Clock source / (128 * (LP3:LP0 + 1))
1/3	Clock source / (96 * (LP3:LP0 + 1))
1/4	Clock source / (128 * (LP3:LP0 + 1))

TABLE 13-2: APPROX. FRAME FREQ IN Hz USING TIMER1 @ 32 kHz OR Fosc @ 8 MHz

LP3:LP0	Static	1/2	1/3	1/4
2	85	85	114	85
3	64	64	85	64
4	51	51	68	51
5	43	43	57	43
6	37	37	49	37
7	32	32	43	32

TABLE 13-3: APPROX. FRAME FREQ IN Hz USING INTERNAL RC OSC @ 14 kHz

LP3:LP0	Static	1/2	1/3	1/4
0	109	109	146	109
1	55	55	73	55
2	36	36	49	36
3	27	27	36	27

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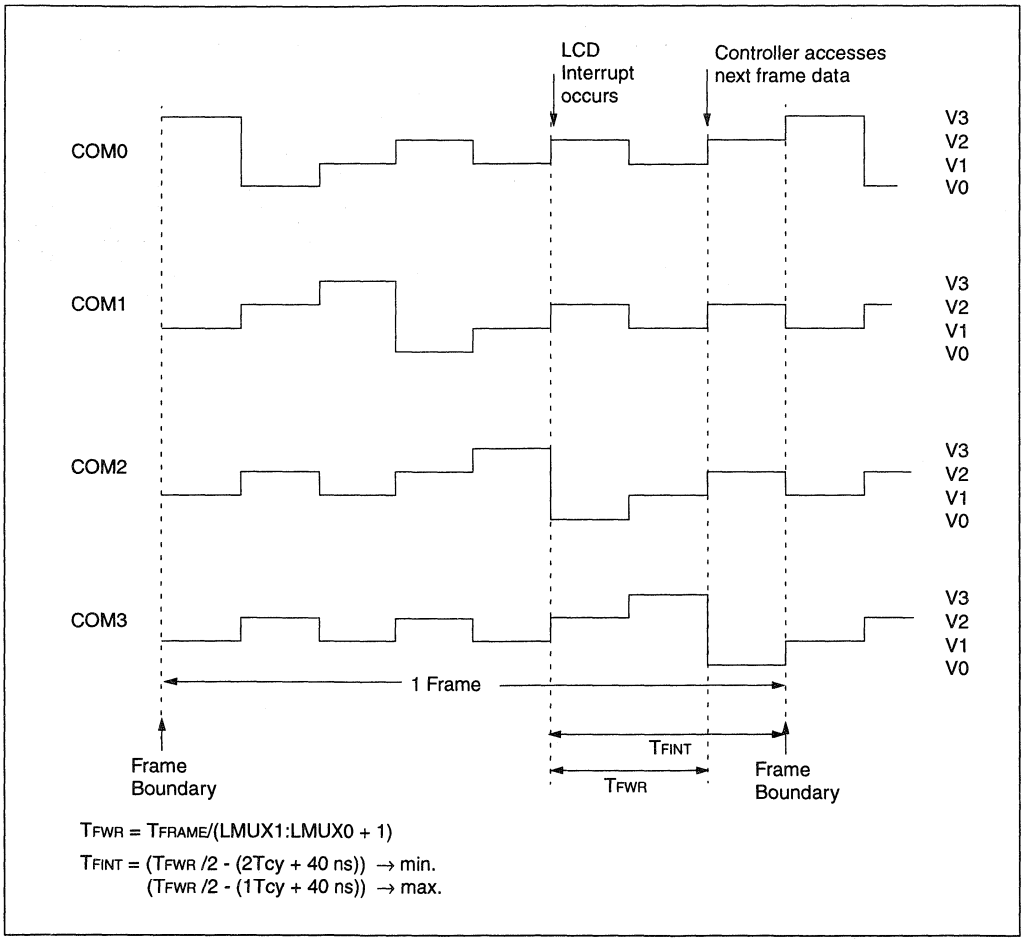
13.2 LCD Interrupts

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame. Writing pixel data at the frame boundary allows a visually crisp transition of the image. This interrupt can also be used to synchronize external events to the LCD. For example, the interface to an external segment driver, such as a Microchip AY0438, can be synchronized for segment data update to the LCD frame.

A new frame is defined to begin at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a certain fixed time before the frame boundary as shown in Figure 13-6. The LCD controller will begin to access data for the next frame within TFWR after the interrupt.

FIGURE 13-6: EXAMPLE WAVEFORMS IN 1/4 MUX DRIVE



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13.3 Pixel Control

13.3.1 LCDD (PIXEL DATA) REGISTERS

The pixel registers contain bits which define the state of each pixel. Each bit defines one unique pixel.

Table 13-4 shows the correlation of each bit in the LCDD registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

FIGURE 13-7: GENERIC LCDD REGISTER LAYOUT

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc
bit7							bit0

R =Readable bit
W =Writable bit
U =Unimplemented bit, Read as '0'
-n =Value at POR reset

bit 7-0: **SEGsCOMc**: Pixel Data Bit for segment s and common c
1 = Pixel on (dark)
0 = Pixel off (clear)

13.4 Operation During Sleep

The LCD module can operate during sleep. The selection is controlled by bit SLPEN (LCDCON<6>). Setting the SLPEN bit allows the LCD module to go to sleep. Clearing the SLPEN bit allows the module to continue to operate during sleep.

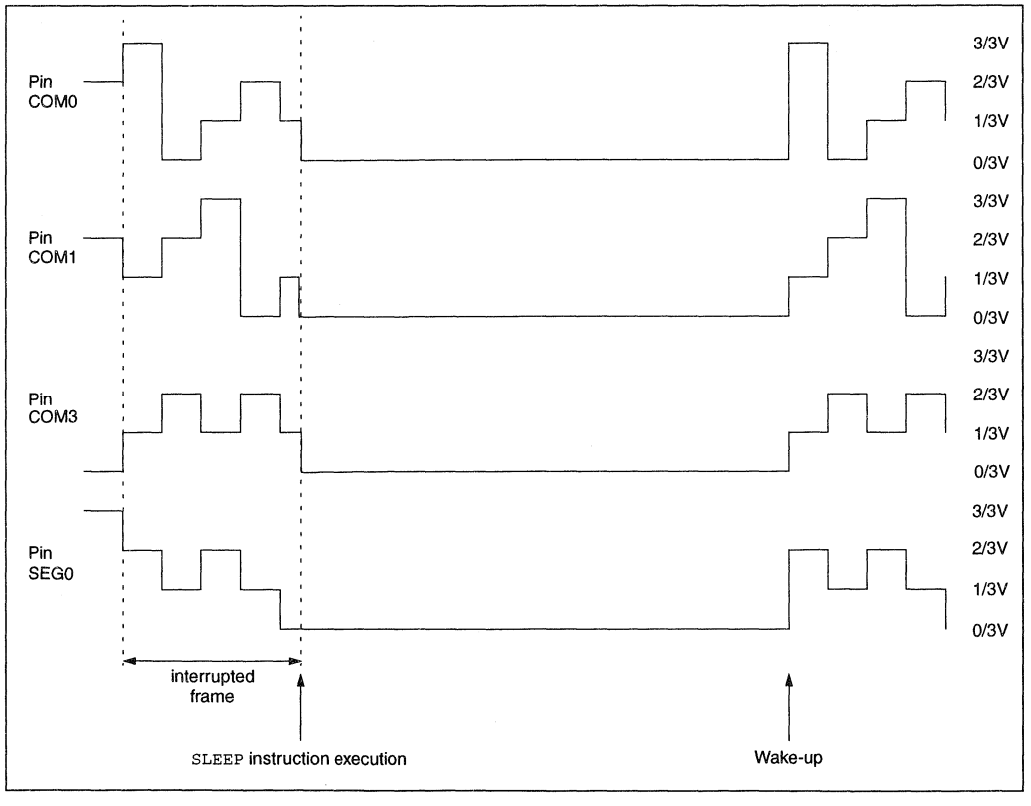
If a SLEEP instruction is executed and SLPEN = '1', the LCD module will cease all functions and go into a very low current consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 13-8 shows this operation. To ensure that the LCD completes the frame, the SLEEP instruction should be executed immediately after a LCD frame boundary.

The LCD interrupt can be used to determine the frame boundary. See Section 13.2 for the formulas to calculate the delay.

If a SLEEP instruction is executed and SLPEN = '0', the module will continue to display the current contents of the LCDD registers. To allow the module to continue operation while in sleep, the clock source must be either the internal RC oscillator or Timer1 external oscillator. While in sleep, the LCD data cannot be changed. The LCD module current consumption will not decrease in this mode, however the overall consumption of the device will be lower due to shutdown of the core and other peripheral functions.

Note:	The internal RC oscillator or external Timer1 oscillator must be used to operate the LCD module during sleep.

FIGURE 13-8: SLEEP ENTRY/EXIT WHEN SLPEN = 1 OR CS1:CS0 = 00



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13.4.1 SEGMENT ENABLES

The LCDSE register is used to select the pin function for groups of pins. The selection allows each group of pins to operate as either LCD drivers or digital only pins. To configure the pins as a digital port, the corresponding bits in the LCDSE register must be cleared.

If the pin is a digital I/O the corresponding TRIS bit controls the data direction. Any bit set in the LCDSE register overrides any bit settings in the corresponding TRIS register.

Note 1: On a Power-on Reset these pins are configured as LCD drivers.

Note 2: The LMUX1:LMUX0 takes precedence over the LCDSE bit settings for pins RD7, RD6 and RD5.

EXAMPLE 13-1: STATIC MUX WITH 32 SEGMENTS

```
BCF   STATUS,RP0    ;Select Bank 2
BSF   STATUS,RP1    ;
BCF   LCDCON,LMUX1 ;Select Static MUX
BCF   LCDCON,LMUX0 ;
MOVLW 0xFF          ;Make PortD,E,F,G
MOVWF LCDSE         ;LCD pins
. . .               ;configure rest of LCD
```

EXAMPLE 13-2: 1/3 MUX WITH 13 SEGMENTS

```
BCF   STATUS,RP0    ;Select Bank 2
BSF   STATUS,RP1    ;
BSF   LCDCON,LMUX1 ;Select 1/3 MUX
BCF   LCDCON,LMUX0 ;
MOVLW 0x87          ;Make PORTD<7:0> &
MOVWF LCDSE         ;PORTE<6:0> LCD pins
. . .               ;configure rest of LCD
```

FIGURE 13-9: LCDSE REGISTER (ADDRESS 10Dh)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0
bit7							bit0

R =Readable bit
W =Writable bit
U =Unimplemented bit, Read as '0'
-n =Value at POR reset

bit 7: **SE29**: Pin function select RD7/COM1/SEG31 - RD5/COM3/SEG29
1 = pins have LCD drive function
0 = pins have digital Input function
The LMUX1:LMUX0 setting takes precedence over the LCDSE register.

bit 6: **SE27**: Pin function select RG7/SEG28 and RE7/SEG27
1 = pins have LCD drive function
0 = pins have digital Input function

bit 5: **SE20**: Pin function select RG6/SEG26 - RG0/SEG20
1 = pins have LCD drive function
0 = pins have digital Input function

bit 4: **SE16**: Pin function select RF7/SEG19 - RF4/SEG16
1 = pins have LCD drive function
0 = pins have digital Input function

bit 3: **SE12**: Pin function select RF3/SEG15 - RF0/SEG12
1 = pins have LCD drive function
0 = pins have digital Input function

bit 2: **SE9**: Pin function select RE6/SEG11 - RE4/SEG09
1 = pins have LCD drive function
0 = pins have digital Input function

bit 1: **SE5**: Pin function select RE3/SEG08 - RE0/SEG05
1 = pins have LCD drive function
0 = pins have digital Input function

bit 0: **SE0**: Pin function select RD4/SEG04 - RD0/SEG00
1 = pins have LCD drive function
0 = pins have digital I/O function

13.5 Voltage Generation

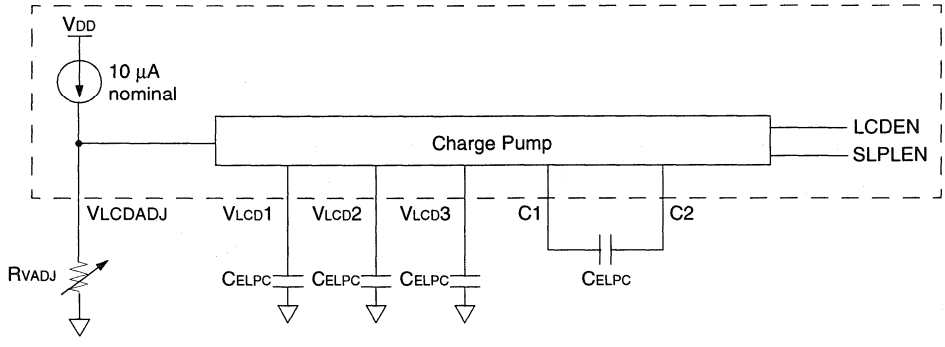
There are two methods for LCD voltage generation, internal charge pump, or external resistor ladder.

13.5.1 CHARGE PUMP

The LCD charge pump is shown in Figure 13-10. The 1.0V - 2.3V regulator will establish a stable base voltage from the varying battery voltage. This regulator is adjustable through the range by connecting a variable external resistor from VLCDADJ to ground. The potentiometer provides contrast adjustment for the LCD. This base voltage is connected to VLCD1 on the charge pump. The charge pump boosts VLCD1 into VLCD2 = 2*VLCD1 and VLCD3 = 3 * VLCD1. When the charge pump is not operating, Vlcd3 will be internally tied to VDD. See the Electrical Specifications section for charge pump capacitor and potentiometer values.

Note:	The LCD charge pump is under development. To minimize risk, designs should accommodate both the charge pump and the external resistor ladder.

FIGURE 13-10: CHARGE PUMP BLOCK DIAGRAM



See Electrical Specifications section for component values (parameter numbers D260 and D271).

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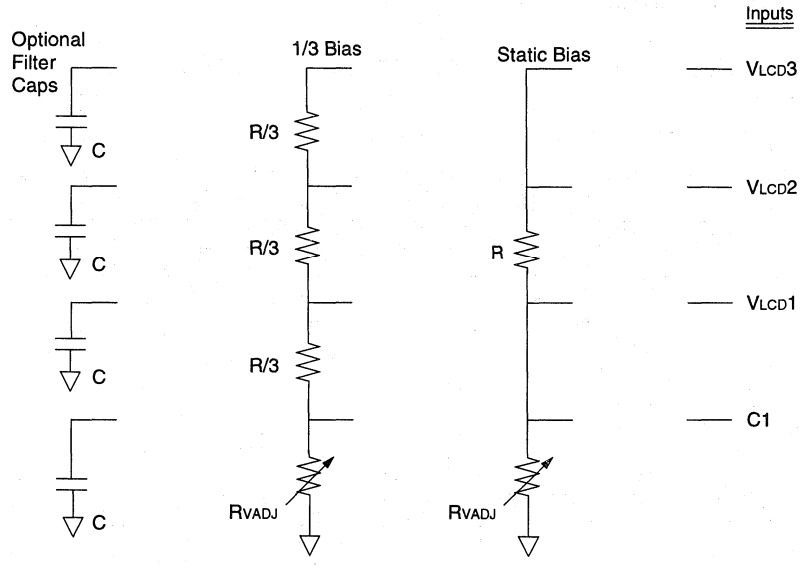
13.5.2 EXTERNAL R-LADDER

The LCD module can also use an external resistor ladder (R-Ladder) to generate the LCD voltages. Figure 13-11 shows external connections for static and 1/3 bias. The VGEN (LCDCON<4>) bit must be cleared to use an external R-Ladder.

FIGURE 13-11: EXTERNAL RESISTOR LADDER CONNECTION



The values for R and C are application dependent.

13.6 Configuring the LCD Module

The following is the sequence of steps to follow to configure the LCD module.

1. Select the frame clock prescale using bits LP3:LP0 (LCDPS<3:0>).
2. Configure the appropriate pins to function as segment drivers using the LCDSE register.
3. Configure the LCD module for the following using the LCDCON register.
   - Multiplex mode and Bias, bits LMUX1:LMUX0
   - Timing source, bits CS1:CS0
   - Voltage generation, bit VGEN
   - Sleep mode, bit SLPEN
4. Write initial values to pixel data registers, LCDD00 through LCDD15.
5. Clear LCD interrupt flag, LCDIF (PIR1<7>), and if desired, enable the interrupt by setting bit LCDIE (PIE1<7>).
6. Enable the LCD module, by setting bit LCDEN (LCDCON<7>).

TABLE 13-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE LCD MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	LCDIF	ADIF(1)	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	00-- 0000	00-- 0000
8Ch	PIE1	LCDIE	ADIE(1)	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	00-- 0000	00-- 0000
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
10Dh	LCDSE	SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0	1111 1111	1111 1111
10Eh	LCDPS	—	—	—	—	LP3	LP2	LP1	LP0	---- 0000	---- 0000
10Fh	LCDCON	LCDEN	SLPEN	—	VGEN	CS1	CS0	LMUX1	LMUX0	00-0 0000	00-0 0000
110h	LCDD00	SEG07 COM0	SEG06 COM0	SEG05 COM0	SEG04 COM0	SEG03 COM0	SEG02 COM0	SEG01 COM0	SEG00 COM0	xxxx xxxx	uuuu uuuu
111h	LCDD01	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG09 COM0	SEG08 COM0	xxxx xxxx	uuuu uuuu
112h	LCDD02	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0	xxxx xxxx	uuuu uuuu
113h	LCDD03	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0	xxxx xxxx	uuuu uuuu
114h	LCDD04	SEG07 COM1	SEG06 COM1	SEG05 COM1	SEG04 COM1	SEG03 COM1	SEG02 COM1	SEG01 COM1	SEG00 COM1	xxxx xxxx	uuuu uuuu
115h	LCDD05	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG09 COM1	SEG08 COM1	xxxx xxxx	uuuu uuuu
116h	LCDD06	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1	xxxx xxxx	uuuu uuuu
117h	LCDD07	SEG31 COM1(2)	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1	xxxx xxxx	uuuu uuuu
118h	LCDD08	SEG07 COM2	SEG06 COM2	SEG05 COM2	SEG04 COM2	SEG03 COM2	SEG02 COM2	SEG01 COM2	SEG00 COM2	xxxx xxxx	uuuu uuuu
119h	LCDD09	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG09 COM2	SEG08 COM2	xxxx xxxx	uuuu uuuu
11Ah	LCDD10	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	xxxx xxxx	uuuu uuuu
11Bh	LCDD11	SEG31 COM2(2)	SEG30 COM2(2)	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2	xxxx xxxx	uuuu uuuu
11Ch	LCDD12	SEG07 COM3	SEG06 COM3	SEG05 COM3	SEG04 COM3	SEG03 COM3	SEG02 COM3	SEG01 COM3	SEG00 COM3	xxxx xxxx	uuuu uuuu
11Dh	LCDD13	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG09 COM3	SEG08 COM3	xxxx xxxx	uuuu uuuu
11Eh	LCDD14	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	xxxx xxxx	uuuu uuuu
11Fh	LCDD15	SEG31 COM3(2)	SEG30 COM3(2)	SEG29 COM3(2)	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the LCD Module.
Note 1: These bits are reserved on the PIC16C923, always maintain these bits clear.
2: These pixels do not display, but can be used as general purpose RAM.

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14.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

14.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 14-1: CONFIGURATION WORD

CP1	CP0	CP1	CP0	CP1	CP0	—	—	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

Register: CONFIG
Address 2007h

bit 13-8 **CP1:CP0** Code protection bits (1)
5-4: 11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4 of program memory code protected
00 = All memory is code protected

bit 6: **Unimplemented**: Read as '1'

bit 3: **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: All of the CP1:CP0 bits have to be given the same value to enable the code protection scheme listed.

14.2 Oscillator Configurations

14.2.1 OSCILLATOR TYPES

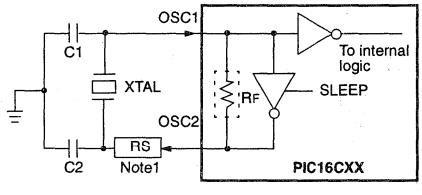
The PIC16CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

14.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 14-2). The PIC16CXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 14-3).

FIGURE 14-2: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



See Table 14-1 and Table 14-2 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.

FIGURE 14-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

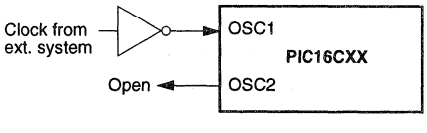


TABLE 14-1: CERAMIC RESONATORS

Ranges Tested:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF
HS	8.0 MHz	10 - 68 pF	10 - 68 pF
Note: Recommended values of C1 and C2 are identical to the ranges tested table. Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.			
Resonators Used:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
All resonators used did not have built-in capacitors.			

TABLE 14-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1	OSC2
LP	32 kHz(1) 200 kHz	15 - 47 pF 15 - 33 pF	15 - 47 pF 15 - 33 pF
XT	100 kHz 500 kHz 1 MHz 2 MHz 4 MHz	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF	47 - 100 pF 20 - 68 pF 15 - 68 pF 15 - 47 pF 15 - 33 pF
HS	8 MHz	15 - 47 pF	15 - 47 pF
Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components. Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.			

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14.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 14-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 14-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

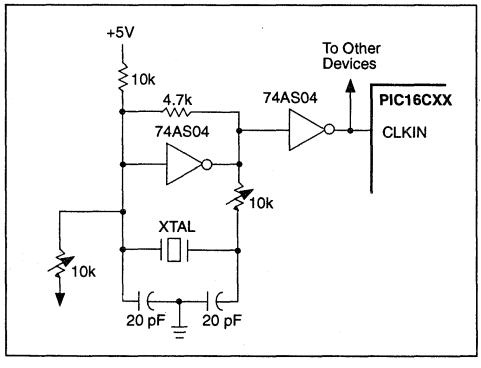
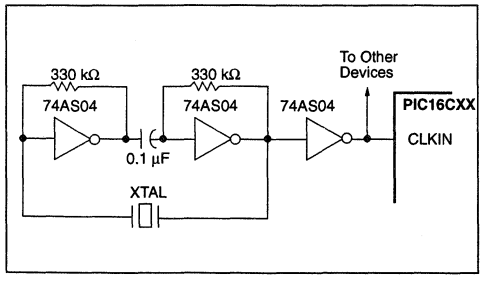


Figure 14-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 14-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



14.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 14-6 shows how the R/C combination is connected to the PIC16CXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kΩ and 100 kΩ.

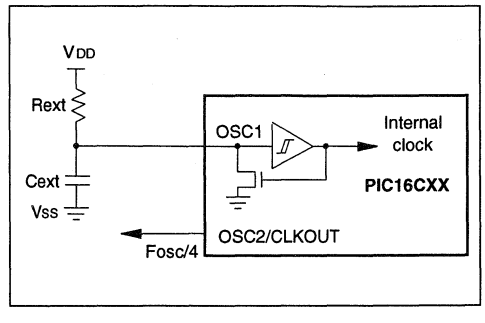
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See characterization data for desired device for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characterization data for desired device for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-3 for waveform).

FIGURE 14-6: RC OSCILLATOR MODE



14.3 Reset

The PIC16CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{MCLR}$ Reset during normal operation
- $\overline{MCLR}$ Reset during SLEEP
- WDT Reset (normal operation)

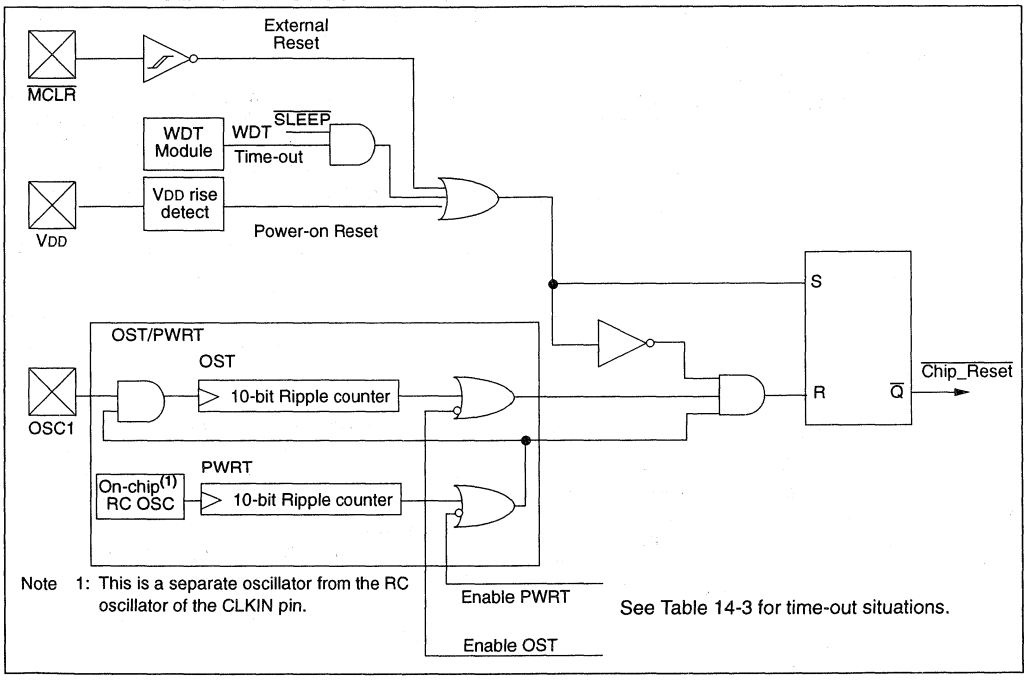
Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on the $\overline{MCLR}$ and WDT Reset, and on $\overline{MCLR}$ Reset during SLEEP. They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 14-4. These bits are used in software to determine the nature of the reset. See Table 14-6 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 14-7.

The devices all have a $\overline{MCLR}$ noise filter in the $\overline{MCLR}$ reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

FIGURE 14-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



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14.4 Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)

14.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting.*"

14.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

14.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

14.4.4 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 14-8, Figure 14-9, and Figure 14-10 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (Figure 14-9). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 14-5 shows the reset conditions for some special function registers, while Table 14-6 shows the reset conditions for all the registers.

14.4.5 POWER CONTROL/STATUS REGISTER (PCON)

Bit1 is Power-on Reset Status bit $\overline{POR}$. It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 14-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	$\overline{PWRTE}$ = 1	$\overline{PWRTE}$ = 0	
XT, HS, LP	1024TOSC	72 ms + 1024TOSC	1024 TOSC
RC	—	72 ms	—

TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{TO}$	$\overline{PD}$	
0	1	1	Power-on Reset
0	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	1	WDT Reset
1	0	0	WDT Wake-up
1	u	u	$\overline{MCLR}$ Reset during normal operation
1	1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

Legend: u = unchanged, x = unknown

TABLE 14-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0-
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- --u-
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---- --u-
WDT Reset	000h	0000 1uuu	---- --u-
WDT Wake-up	PC + 1	uuu0 0uuu	---- --u-
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 14-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset	$\overline{MCLR}$ Resets WDT Reset	Wake-up via WDT or Interrupt
W	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	923	924	N/A	N/A	N/A
TMR0	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	923	924	0000h	0000h	PC + 1(2)
STATUS	923	924	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	923	924	--xx xxxx	--uu uuuu	--uu uuuu
PORTA	923	924	--0x 0000	--0u 0000	--uu uuuu
PORTB	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	923	924	--xx xxxx	--uu uuuu	--uu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition
Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: See Table 14-5 for reset value for specific condition.
4: Bits PIE<6> and PIR<6> are reserved on the PIC16C923, always maintain these bits clear.

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TABLE 14-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Register	Applicable Devices		Power-on Reset	$\overline{\text{MCLR}}$ Resets WDT Reset	Wake-up via WDT or Interrupt
PORTD	923	924	0000 0000	0000 0000	uuuu uuuu
PORTE	923	924	0000 0000	0000 0000	uuuu uuuu
PCLATH	923	924	---0 0000	---0 0000	---u uuuu
INTCON	923	924	0000 000x	0000 000u	uuuu uuuu(1)
PIR1(4)	923	924	00-- 0000	00-- 0000	uu-- uuuu(1)
TMR1L	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	923	924	--00 0000	--uu uuuu	--uu uuuu
TMR2	923	924	0000 0000	0000 0000	uuuu uuuu
T2CON	923	924	-000 0000	-000 0000	-uuu uuuu
SSPBUF	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	923	924	0000 0000	0000 0000	uuuu uuuu
CCPR1L	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	923	924	--00 0000	--00 0000	--uu uuuu
ADRES	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	923	924	0000 00-0	0000 00-0	uuuu uu-u
OPTION	923	924	1111 1111	1111 1111	uuuu uuuu
TRISA	923	924	--11 1111	--11 1111	--uu uuuu
TRISB	923	924	1111 1111	1111 1111	uuuu uuuu
TRISC	923	924	--11 1111	--11 1111	--uu uuuu
TRISD	923	924	1111 1111	1111 1111	uuuu uuuu
TRISE	923	924	1111 1111	1111 1111	uuuu uuuu
PIE1(4)	923	924	00-- 0000	00-- 0000	uu-- uuuu
PCON	923	924	---- --0-	---- --u-	---- --u-
PR2	923	924	1111 1111	1111 1111	1111 1111
SSPADD	923	924	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	923	924	0000 0000	0000 0000	uuuu uuuu
ADCON1	923	924	---- -000	---- -000	---- -uuu
PORTF	923	924	0000 0000	0000 0000	uuuu uuuu
PORTG	923	924	0000 0000	0000 0000	uuuu uuuu
LCDSE	923	924	1111 1111	1111 1111	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 14-5 for reset value for specific condition.

4: Bits PIE<6> and PIR<6> are reserved on the PIC16C923, always maintain these bits clear.

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TABLE 14-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Register	Applicable Devices		Power-on Reset	$\overline{\text{MCLR}}$ Resets WDT Reset	Wake-up via WDT or Interrupt
LCDPS	923	924	---- 0000	---- 0000	---- uuuu
LCDCON	923	924	00-0 0000	00-0 0000	uu-u uuuu
LCDD00 to LCDD15	923	924	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISF	923	924	1111 1111	1111 1111	uuuu uuuu
TRISG	923	924	1111 1111	1111 1111	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 14-5 for reset value for specific condition.

4: Bits PIE<6> and PIR<6> are reserved on the PIC16C923, always maintain these bits clear.

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FIGURE 14-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

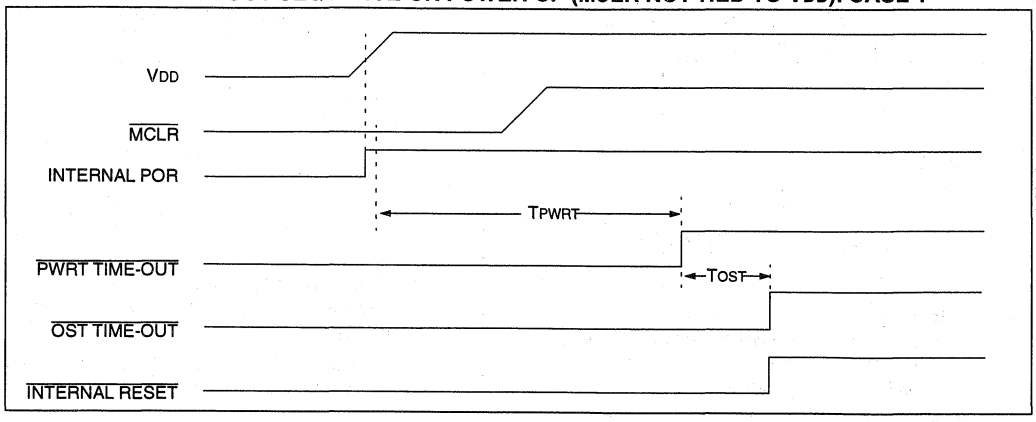


FIGURE 14-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

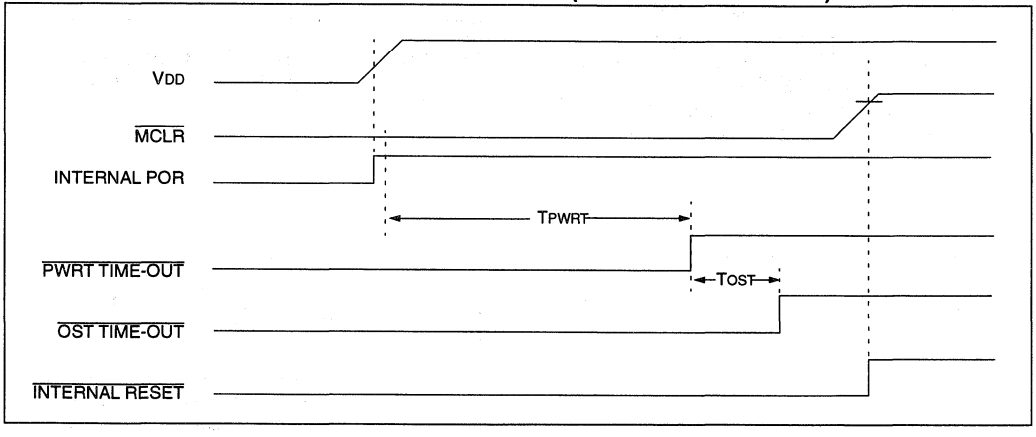


FIGURE 14-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

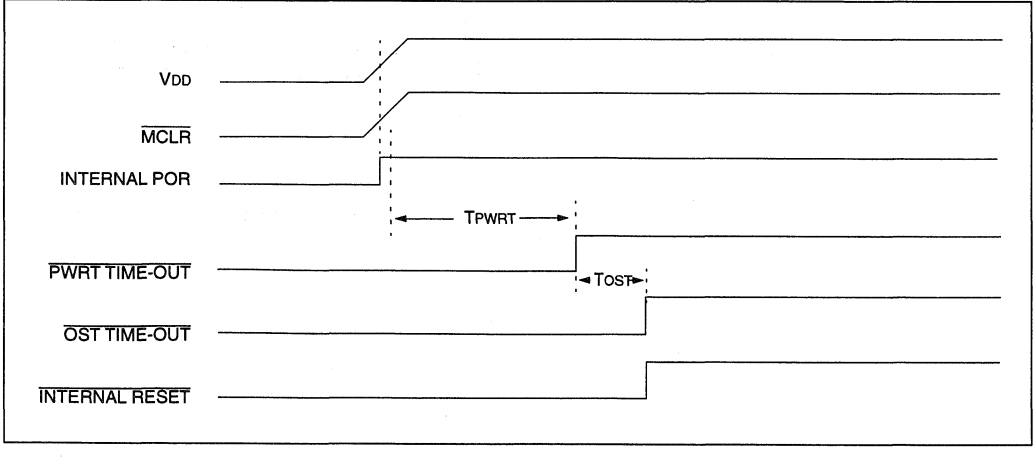
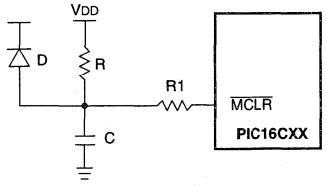


FIGURE 14-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

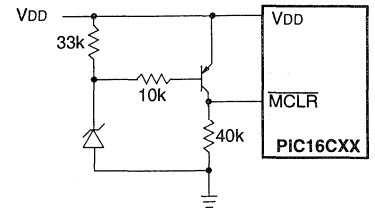


Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

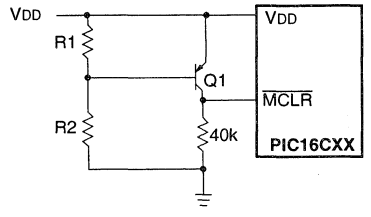
FIGURE 14-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

2: Resistors should be adjusted for the characteristics of the transistors.

FIGURE 14-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Resistors should be adjusted for the characteristics of the transistors.

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14.5 Interrupts

The PIC16C9XX family has up to 9 sources of interrupt:

Interrupt Sources	Applicable Devices	
External interrupt RB0/INT	923	924
TMR0 overflow interrupt	923	924
PORTB change interrupts (pins RB7:RB4)	923	924
A/D Interrupt	923	924
TMR1 overflow interrupt	923	924
TMR2 matches period interrupt	923	924
CCP1 interrupt	923	924
Synchronous serial port interrupt	923	924
LCD Module interrupt	923	924

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set regardless of the status of the GIE bit. The GIE bit is cleared on reset.

The "return from interrupt" instruction, `RETFIE`, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

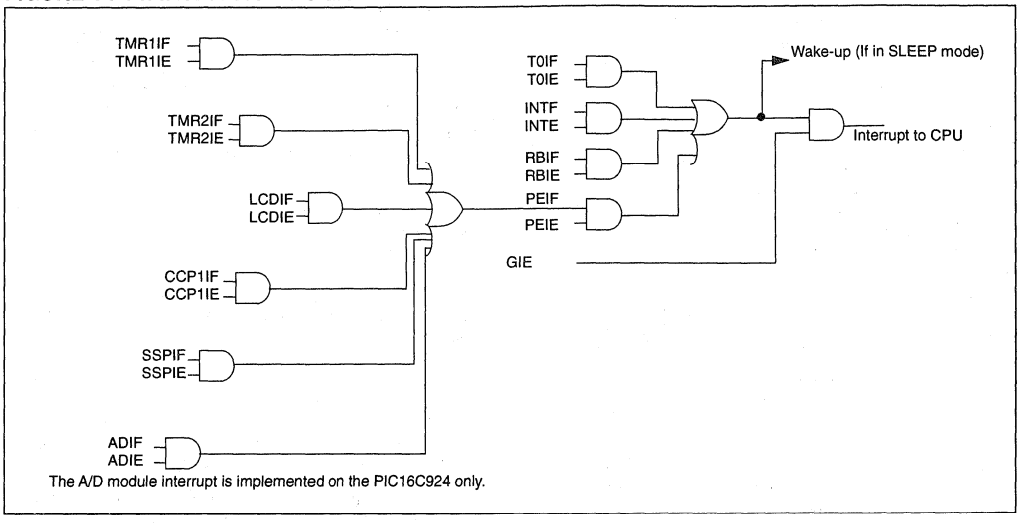
The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function register PIR1. The corresponding interrupt enable bits are contained in special function register PIE1, and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupts, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

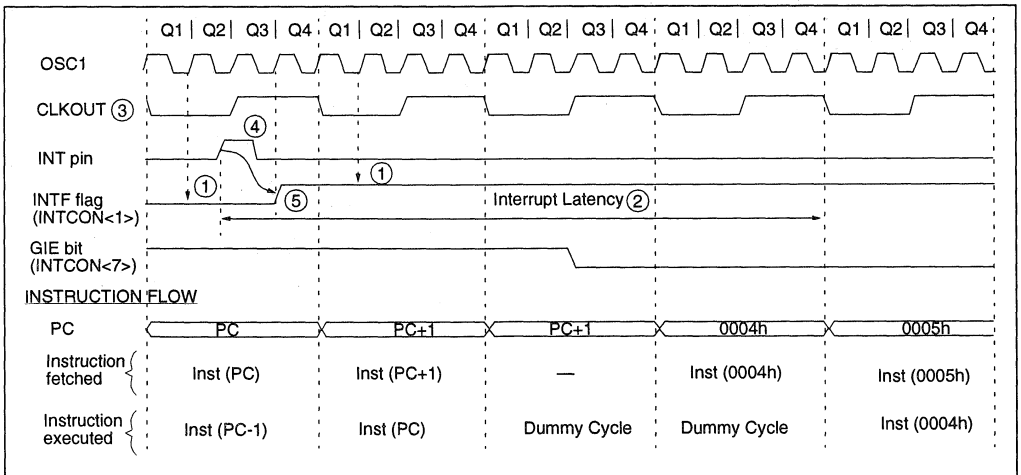
For external interrupt events, such as the RB0/INT pin or RB Port change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 14-15). The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

FIGURE 14-14: INTERRUPT LOGIC



The A/D module interrupt is implemented on the PIC16C924 only.

FIGURE 14-15: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTFcan be set anytime during the Q4-Q1 cycles.

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14.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 14.8 for details on SLEEP mode.

14.5.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 7.0)

14.5.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 5.2)

14.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 14-1 stores and restores the STATUS and W registers. The register, W_TEMP, must be defined in all banks and must be defined at the same offset from the bank base address in the last 16 registers (i.e., if W_TEMP is defined at 0x70 in bank 0, it must also be defined at 0xF0 in bank 1, 0x170 in bank 2, and 0x1F0 in bank 3).

The example:

a) Stores the W register.
b) Stores the STATUS register in bank 0.
c) Executes the ISR code.
d) Restores the STATUS register (and bank select bits).
e) Restores the W register.

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EXAMPLE 14-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP          ;Copy W to TEMP register, could be any bank
SWAPF   STATUS,W        ;Swap status to be saved into W
BCF     STATUS,RP1      ;Change to bank zero, regardless of current bank
BCF     STATUS,RP0      ;
MOVWF   STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF   STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF   STATUS          ;Move W into STATUS register
SWAPF   W_TEMP,F        ;Swap W_TEMP
SWAPF   W_TEMP,W        ;Swap W_TEMP into W
```

14.7 Watchdog Timer (WDT)

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 14.1).

14.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

14.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note:	When the prescaler is assigned to the WDT, always execute a CLRWDT instruction before changing the prescale value. Otherwise a WDT reset may occur.

FIGURE 14-16: WATCHDOG TIMER BLOCK DIAGRAM

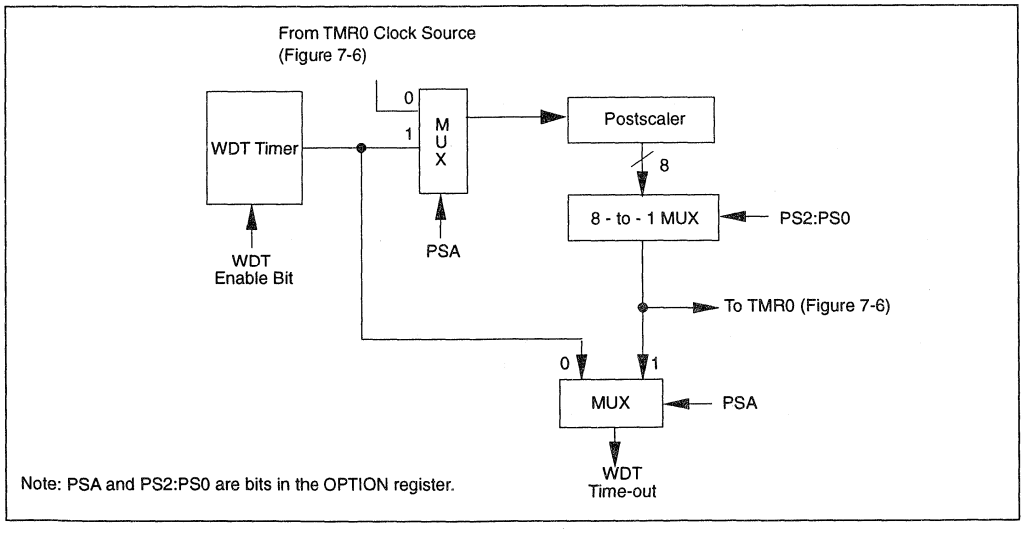

FIGURE 14-17: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	(1)	CP1	CP0	$\overline{PWRTE}$(1)	WDTE	FOSC1	FOSC0
81h, 181h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 14-1 for operation of these bits.

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14.8 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D, disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

14.8.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or some peripheral interrupts.

External $\overline{MCLR}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. SSP (Start/Stop) bit detect interrupt.
3. SSP transmit or receive in slave mode (SPI/I^2C).
4. CCP capture mode interrupt.
5. A/D conversion (when A/D clock source is RC).
6. Special event trigger (Timer1 in asynchronous mode using an external clock).
7. LCD module.

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

14.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep . The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

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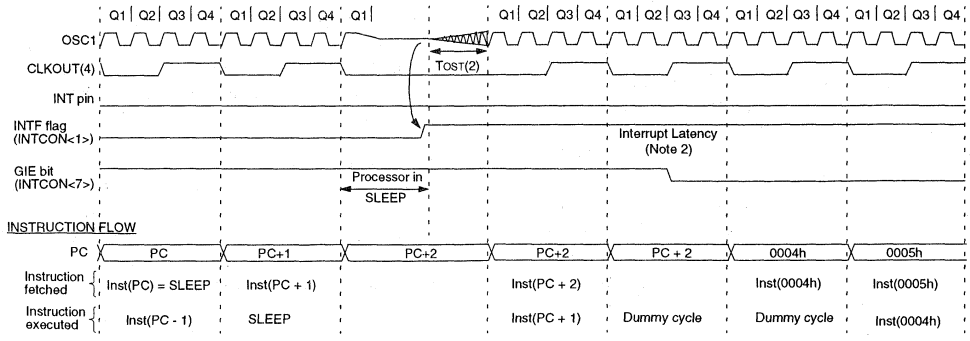
FIGURE 14-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

14.9 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

14.10 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

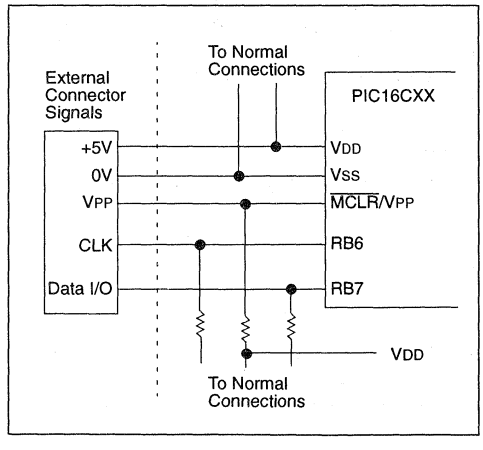
14.11 In-Circuit Serial Programming

PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into program/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

FIGURE 14-19: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



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15.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.3V to (V_{DD} + 0.3V)

Voltage on V_{DD} with respect to V_{SS} ..... 0V to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... 0V to +14V

Total power dissipation (Note 1) 1.0W

Maximum current out of V_{SS} pin ..... 300 mA

Maximum current into V_{DD} pin ..... 250 mA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 10 mA

Maximum output current sourced by any I/O pin ..... 10 mA

Maximum current sunk by all Ports combined ..... 200 mA

Maximum current sourced by all Ports combined ..... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 15-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C923-04 PIC16C924-04	PIC16C923-08 PIC16C924-08	PIC16L923-04 PIC16L924-04	CL Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 8 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 15 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 8 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 13.5 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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15.1 DC Characteristics: PIC16C923/924-04 (Commercial, Industrial) PIC16C923/924-08 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See Power-on Reset section for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	(Note 6) See Power-on Reset section for details
D010	Supply Current (Note 2)	IDD	-	2.7	5	mA	XT and RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4)
D011			-	13.5	30	µA	LP osc configuration, FOSC = 32 kHz, VDD = 4.0V
D012			-	3.5	7	mA	HS osc configuration FOSC = 8 MHz, VDD = 5.5V
D020	Power-down Current (Note 3)	IPD	-	1.5	21	µA	VDD = 4.0V
	Module Differential Current (Note 5)						
D021	Watchdog Timer	ΔIWDT	-	6.0	20	µA	VDD = 4.0V
D022	LCD internal RC osc enabled	ΔILCDRC	-	6.0	20	µA	VDD = 4.0V
D024*	LCD voltage generation	ΔILCDVG	-	TBD	TBD	µA	VDD = 4.0V
D025	Timer1 oscillator	ΔIT1OSC	-	10.6	17	µA	VDD = 4.0V
D026	A/D Converter	ΔIAD	-	1.0	-	µA	A/D on, not converting

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: PWRT must be enabled for slow ramps.

15.2 DC Characteristics: PIC16LC923/924-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	3.0	-	6.0	V	LP, XT, RC osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See Power-on Reset section for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	(Note 6) See Power-on Reset section for details
D010	Supply Current (Note 2)	IDD	-	2.0	3.8	mA	XT and RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D011			-	22.5	48	µA	LP osc configuration, FOSC = 32 kHz, VDD = 4.0V
D020	Power-down Current (Note 3)	IPD	-	0.9	5	µA	VDD = 3.0V
	Module Differential Current (Note 5)						
D021	Watchdog Timer	ΔIWDT	-	6.0	20	µA	VDD = 3.0V
D022	LCD internal RC osc enabled	ΔILCDRC	-	6.0	20	µA	VDD = 3.0V
D024*	LCD voltage generation	ΔILCDVG	-	TBD	TBD	µA	VDD = 3.0V
D025	Timer1 oscillator	ΔIT1OSC	-	3.1	6.5	µA	VDD = 3.0V
D026	A/D Converter	ΔIAD	-	1.0	-	µA	A/D on, not converting

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: PWRT must be enabled for slow ramps.

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15.3 DC Characteristics: PIC16C923/924-04 (Commercial, Industrial) PIC16C923/924-08 (Commercial, Industrial) PIC16LC923/924-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	VIL					
D030	with TTL buffer		VSS	-	0.15VDD	V	For entire VDD range
			VSS	-	0.8VDD	V	4.5V ≤ VDD ≤ 5.5V
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	Note1
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	For entire VDD range
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	
D042	$\overline{MCLR}$, RA4/T0CKI, RB0/INT		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in RC mode)		0.9VDD	-	VDD	V	
D070	PORTB weak pull-up current	IPURB	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	IIL	-	-	±0.5	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-Z
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	Vss ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	VOL	-	-	0.6	V	IOL = 4.0 mA, VDD = 4.5V
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V
	Output High Voltage						
D090	I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V
	Capacitive Loading Specs on Output Pins						
D100*	OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101*	All I/O pins and OSC2 (in RC)	CIO	-	-	50	pF	
D102*	SCL, SDA in I^2C mode	CB	-	-	400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C9XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

FIGURE 15-1: LCD VOLTAGE WAVEFORM

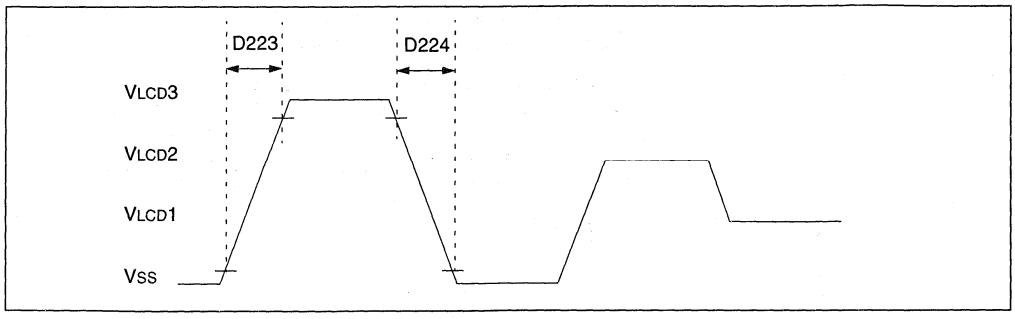

TABLE 15-2: LCD MODULE ELECTRICAL SPECIFICATIONS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D200	VLCD3	LCD Voltage on pin VLCD3	VDD - 0.3	—	VSS + 7.0	V	
D201	VLCD2	LCD Voltage on pin VLCD2	VSS - 0.3	—	VLCD3	V	
D202	VLCD1	LCD Voltage on pin VLCD1	VSS - 0.3	—	VDD	V	
D210*	RCOM	Com Output Source Impedance	—	—	1k	ohm	COM outputs
D211*	RSEG	Seg Output Source Impedance	—	—	10k	ohm	SEG outputs
D220	VOH	Output High Voltage	Max VLCDN - 0.1	—	Max VLCDN	V	COM outputs IOH = 25 µA SEG outputs IOH = 3 µA
D221	VOL	Output Low Voltage	Min VLCDN	—	Min VLCDN + 0.1	V	COM outputs IOL = 25 µA SEG outputs IOL = 3 µA
D222*	FLCDRC	LCDRC Oscillator Frequency	—	14	22	kHz	VDD = 5V, -40°C to +85°C
D223*	TrLCD	Output Rise Time	—	—	200	µs	COM outputs Cload = 5,000 pF SEG outputs Cload = 500 pF VDD = 5.0V, T = 25°C
D224*	TfLCD	Output Fall Time (1)	TrLCD - 0.05TrLCD	—	TrLCD + 0.05TrLCD	µs	COM outputs Cload = 5,000 pF SEG outputs Cload = 500 pF VDD = 5.0V, T = 25°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

(1) 0 ohm source impedance at VLCD.

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TABLE 15-3: VLCD CHARGE PUMP ELECTRICAL SPECIFICATIONS

Parameter No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D250*	IVADJ	VLCDADJ regulated current output	—	10	—	µA	
D251	Ivr	VLCDADJ Current consumption	—	—	20	µA	
D252*	Δ IVADJ/Δ VDD	VLCDADJ current VDD Rejection	—	—	0.1/1	µA/V	
D253*	Δ IVADJ/Δ T	VLCDADJ current variation with temperature	—	—	0.1/70	µA/°C	
D260*	RVADJ	VLCDADJ external resistor	100	—	230	kΩ	Note 1
D265*	VVADJ	VLCDADJ voltage limits	1.0	—	2.3	V	
D271*	CECPC	External Charge Pump Capacitance	—	0.5	—	µF	Note 1

* These parameters are characterized but not tested.

Note 1: For design guidance only.

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15.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

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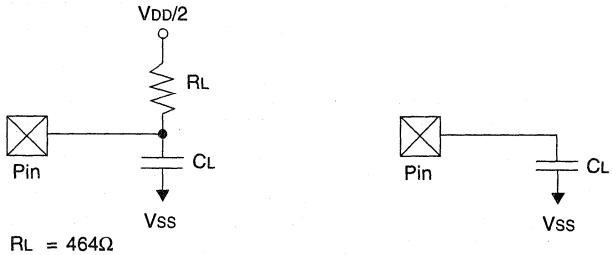
FIGURE 15-2: LOAD CONDITIONS



RL = 464Ω

CL = 50 pF for all pins except OSC2 unless otherwise noted.

15 pF for OSC2 output

15.5 Timing Diagrams and Specifications

FIGURE 15-3: EXTERNAL CLOCK TIMING

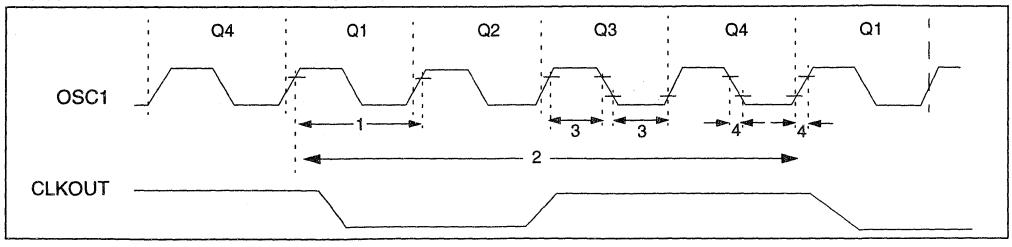


TABLE 15-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT and RC osc mode
			DC	—	8	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	8	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period (Note 1)	250	—	—	ns	XT and RC osc mode
			125	—	—	ns	HS osc mode
			5	—	—	µs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			125	—	250	ns	HS osc mode
			5	—	—	µs	LP osc mode
2	Tcy	Instruction Cycle Time (Note 1)	500	—	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	External Clock in (OSC1) High or Low Time	50	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			10	—	—	ns	HS oscillator
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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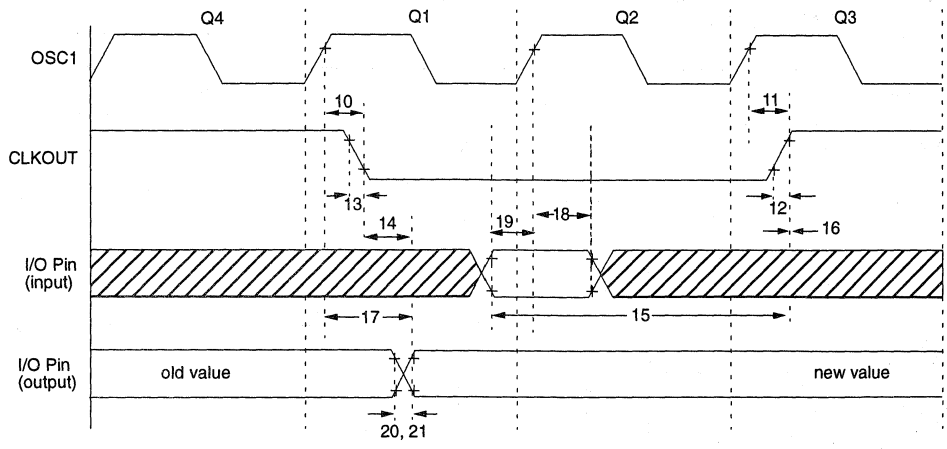
FIGURE 15-4: CLKOUT AND I/O TIMING



Refer to Figure 15-2 for load conditions.

TABLE 15-5: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	3	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	3	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 200	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		100	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C923/924	—	10	40	ns	
			PIC16LC923/924	—	—	80	ns	
21*	TioF	Port output fall time	PIC16C923/924	—	10	40	ns	
			PIC16LC923/924	—	—	80	ns	
22††*	Tinp	INT pin high or low time		Tcy	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		Tcy	—	—	ns	

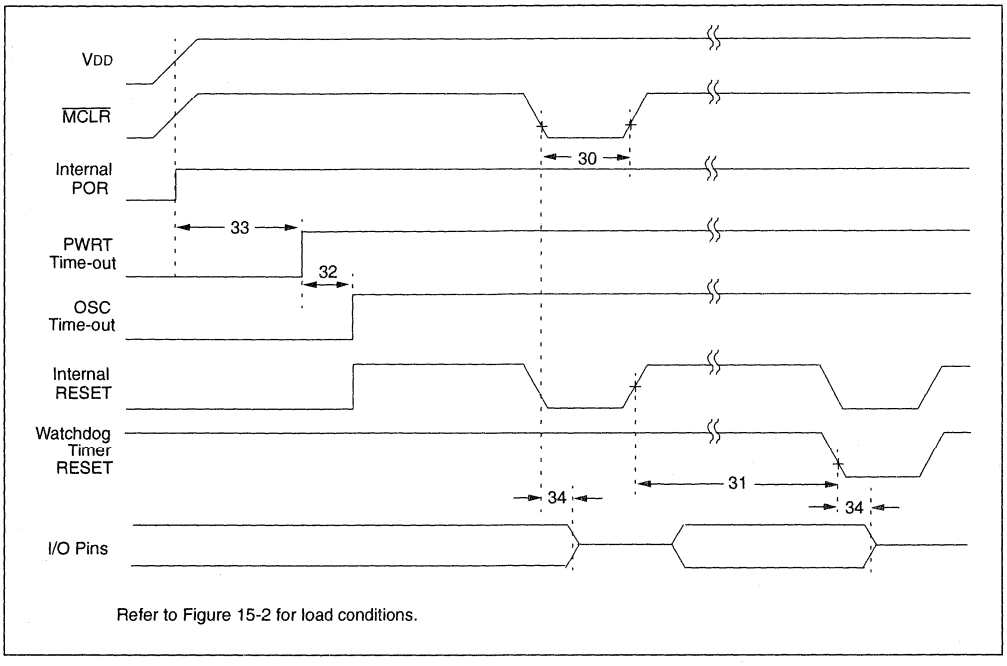
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

FIGURE 15-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Refer to Figure 15-2 for load conditions.

TABLE 15-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	2000	—	—	ns	
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34	TIOZ	I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2000	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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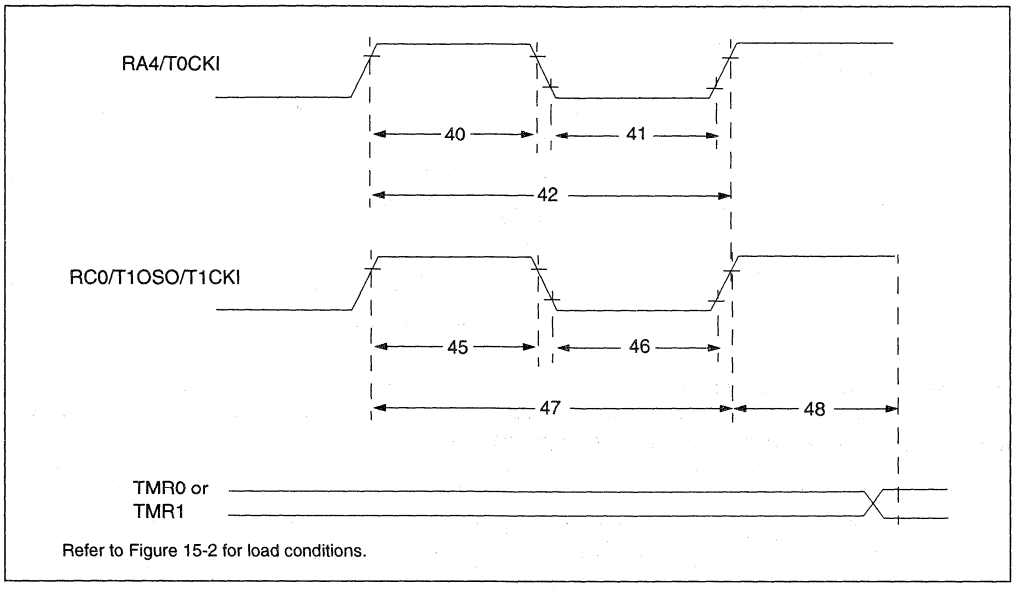
FIGURE 15-6: TIMER0 AND TIMER1 CLOCK TIMINGS



Refer to Figure 15-2 for load conditions.

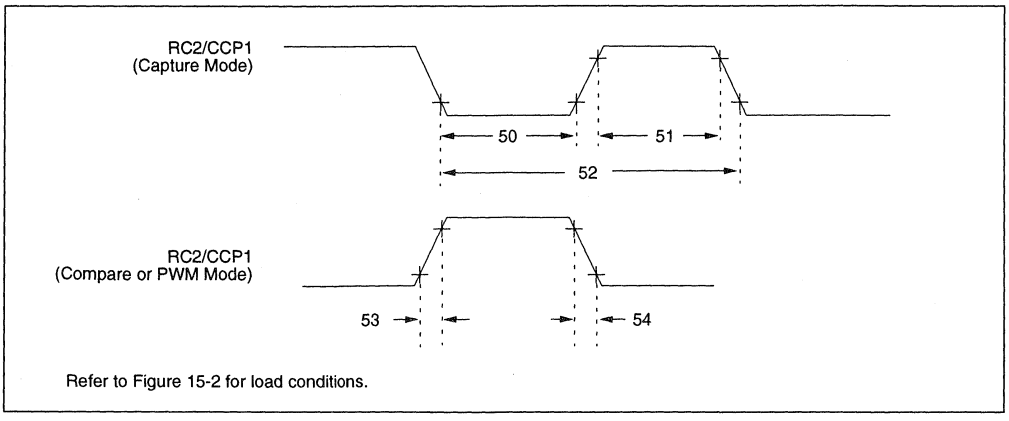
TABLE 15-7: TIMER0 AND TIMER1 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period			TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4,..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C923/924	10	—	—	ns	
				PIC16LC923/924	20	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16C923/924	10	—	—	ns	
				PIC16LC923/924	20	—	—	ns	
			Asynchronous		2TCY	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous		TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)			DC	—	200	kHz	
48	Tcke2tmrl	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-7: CAPTURE/COMPARE/PWM TIMINGS



Refer to Figure 15-2 for load conditions.

TABLE 15-8: CAPTURE/COMPARE/PWM REQUIREMENTS

Parameter No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	Input Low Time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C923/924	10	—	—	ns	
				PIC16LC923/924	20	—	—	ns	
51*	TccH	Input High Time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16C923/924	10	—	—	ns	
				PIC16LC923/924	20	—	—	ns	
52*	TccP	Input Period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	Output Rise Time			—	10	25	ns	
54*	TccF	Output Fall Time		PIC16C923/924	—	10	25	ns	
				PIC16LC923/924	—	—	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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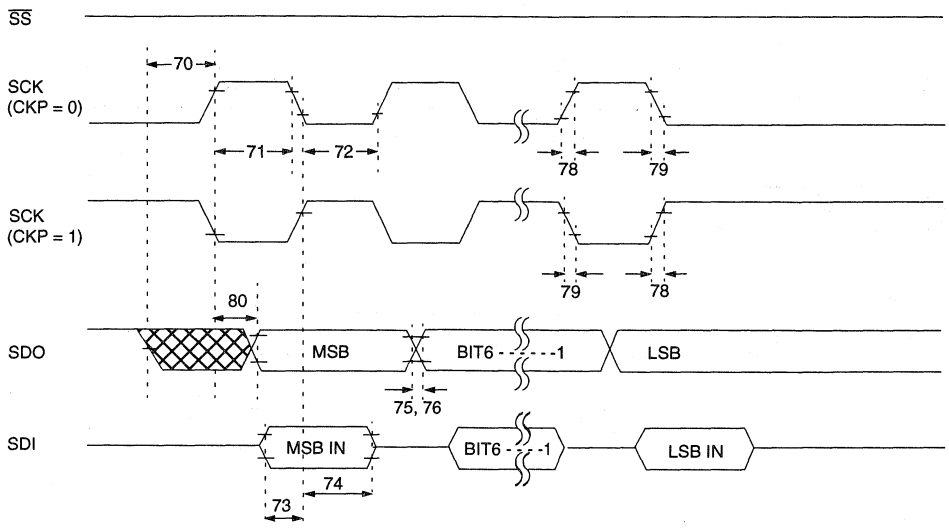
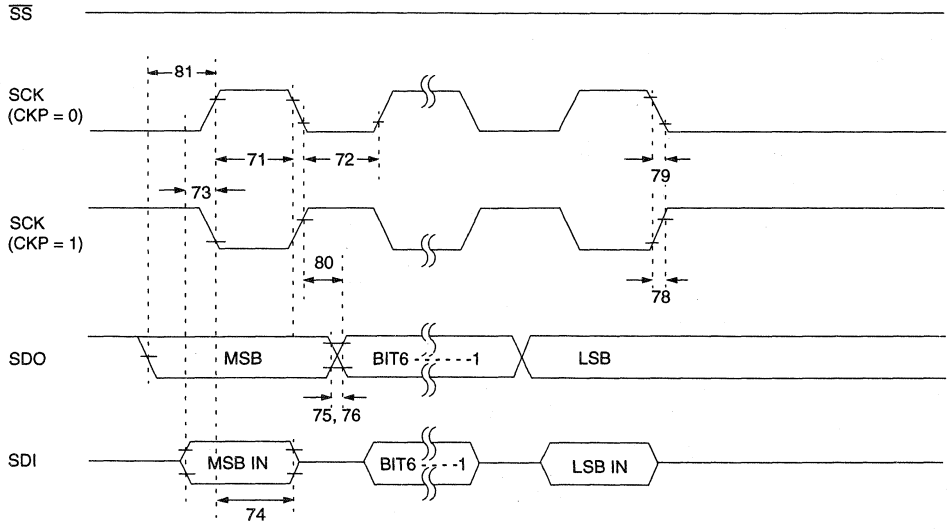
FIGURE 15-8: SPI MASTER MODE TIMING (CKE = 0)



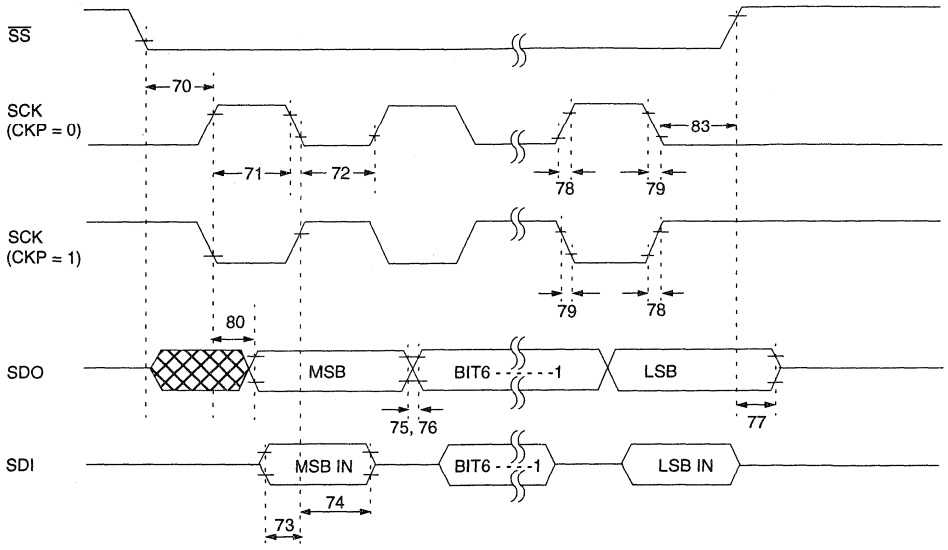
Refer to Figure 15-2 for load conditions.

FIGURE 15-9: SPI MASTER MODE TIMING (CKE = 1)



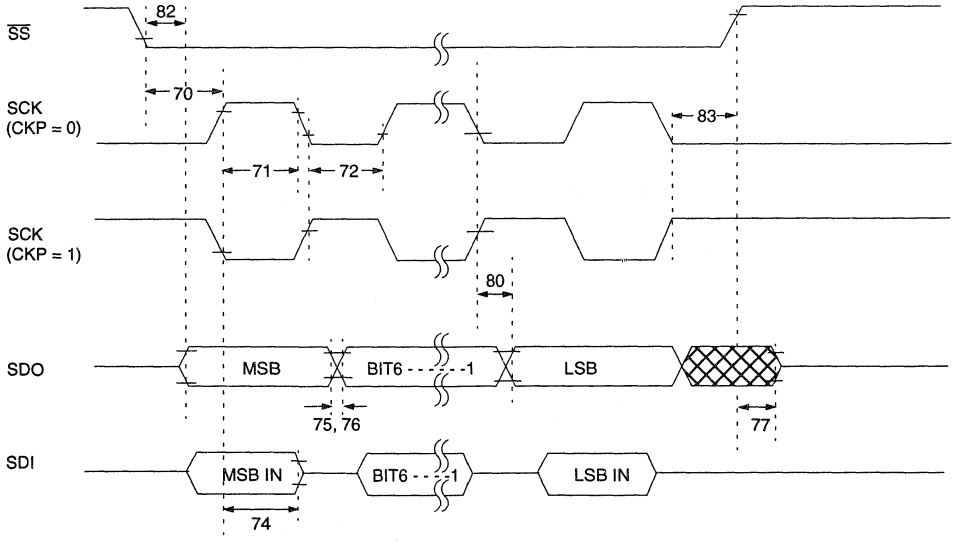
Refer to Figure 15-2 for load conditions.

FIGURE 15-10: SPI SLAVE MODE TIMING (CKE = 0)



Refer to Figure 15-2 for load conditions.

FIGURE 15-11: SPI SLAVE MODE TIMING (CKE = 1)



Refer to Figure 15-2 for load conditions.

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TABLE 15-9: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input	TCY	—	—	ns	
71*	TscH	SCK input high time (slave mode)	TCY + 20	—	—	ns	
72*	TscL	SCK input low time (slave mode)	TCY + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
75*	TdoR	SDO data output rise time	—	10	25	ns	
76*	TdoF	SDO data output fall time	—	10	25	ns	
77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output hi-impedance	10	—	50	ns	
78*	TscR	SCK output rise time (master mode)	—	10	25	ns	
79*	TscF	SCK output fall time (master mode)	—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	TCY	—	—	ns	
82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	—	—	50	ns	
83*	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge	1.5TCY + 40	—	—	ns	

* Characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 15-12: I^2C BUS START/STOP BITS TIMING

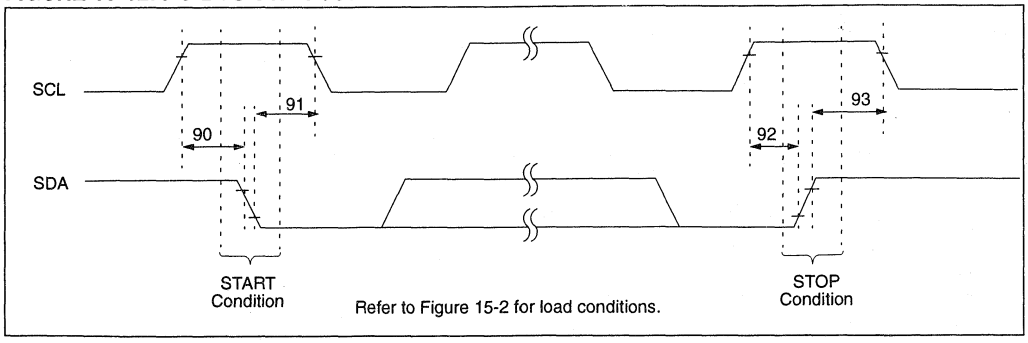

TABLE 15-10: I^2C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
91*	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
92*	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
93*	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	

* Characterized but not tested.

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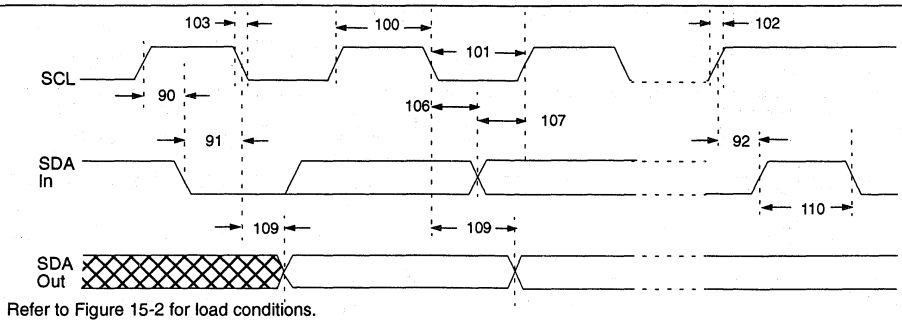
FIGURE 15-13: I²C BUS DATA TIMING



Refer to Figure 15-2 for load conditions.

TABLE 15-11: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16C9XX must operate at a minimum of 1.5 MHz
			SSP Module	1.5TCY	—		
101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16C9XX must operate at a minimum of 1.5 MHz
			SSP Module	1.5TCY	—		
102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
90*	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
91*	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	
92*	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
D102*	Cb	Bus capacitive loading		—	400	pF	

* Characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

TABLE 15-12: A/D CONVERTER CHARACTERISTICS: PIC16C923/924-04 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 5.12V, VSS ≤ AIN ≤ VREF
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	µA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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TABLE 15-13: A/D CONVERTER CHARACTERISTICS: PIC16LC923/924-04 (COMMERCIAL, INDUSTRIAL)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	VREF = VDD = 3.0V (Note 1)
	NINT	Integral error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NDIF	Differential error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NFS	Full scale error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	NOFF	Offset error	—	—	less than ±1 LSb	—	VREF = VDD = 3.0V (Note 1)
	—	Monotonicity	—	guaranteed	—	—	VSS ≤ AIN ≤ VREF
	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	IAD	A/D conversion current (VDD)	—	180	—	µA	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 3)	—	—	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

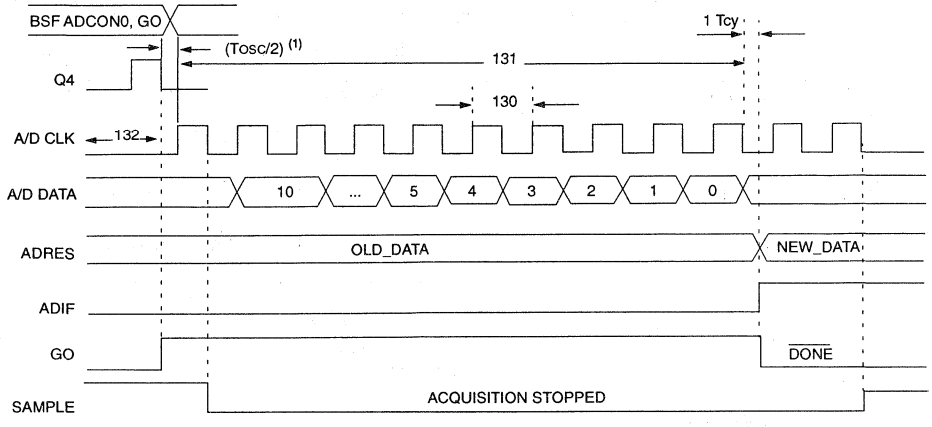
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V. Vin must be between VSS and VREF

2: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

FIGURE 15-14: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-14: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16C924	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16LC924	2.0	—	—	µs	TOSC based, VREF full range
			PIC16C924	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16LC924	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	9.5TAD	—	—	
132	TACQ	Acquisition time		Note 2	20	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See A/D spec for min conditions.

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APPENDIX A:

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (192 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. Bits PA2, PA1, PA0 are removed from STATUS register.
3. Data memory paging is redefined slightly. STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. T0CKI pin is also a port pin (RA4) now.
14. FSR is made a full eight bit register.
15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: V_{DD}, V_{SS}, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-on Reset status bit ($\overline{POR}$).
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

APPENDIX C: WHAT'S NEW

No new material was added to the data sheet.

APPENDIX D: WHAT'S CHANGED

1. New terminology for A/D sampling.

   Any reference to the A/D time it takes to charge the holding capacitor has been changed from sampling time to acquisition time.

   Any reference to the time it takes to convert an analog signal on the holding capacitor into a digital value is still called conversion time.

   The total sample time is now referred to as acquisition time + conversion time.

2. Parameter # 132 of Table 17-13 has been renamed from TSMP to TACQ.
3. The SPI module has been modified to control clock edge, clock polarity and sample phase. Changes include:
   - Data Input Sample Phase bit SMP (SSPSTAT<7>) selects the time where data is sampled.
   - Clock Edge Select bit CKE (SSPSTAT<6>) selects the edge that data is transmitted on which depends on the CKP bit.
   - Clock Polarity Select bit CKP (SSPCON<4>) selects the idle state of the SCK pin.
4. Fast mode I^2C is not supported.

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PIC16C9XX Product Identification System

To order or obtain information, e.g., on pricing or delivery refer to the factory or the listed sales office.

PART NO. -XX X /XX XXX			Examples
Pattern:	QTP, SQTP, ROM Code or Special Requirements		a) PIC16C924 - 04/P 301 Commercial Temp., PDIP Package, 4 MHz, normal VDD limits, QTP pattern #301
Package:	SP = 64-pin Shrink PDIP PT = TQFP CL = 68-pin Windowed CERQUAD L = PLCC		b) PIC16LC923 - 04/PT Commercial Temp., TQFP package, 4 MHz, extended VDD limits
Temperature Range:	- = 0°C to +70°C (T for Tape/Reel) I = -40°C to +85°C (S for Tape/Reel)		c) PIC16C923 - 08I/CL Industrial Temp., Windowed CERQUAD package, 8 MHz, normal VDD limits
Frequency Range:	04 = 200 kHz (PIC16C9XX-04) 04 = 4 MHz 08 = 8 MHz		
Device	PIC16C9XX :VDD range 4.0V to 6.0V PIC16C9XXT :VDD range 4.0V to 6.0V (Tape/Reel) PIC16LC9XX :VDD range 3.0V to 6.0V PIC16LC9XT :VDD range 3.0V to 6.0V (Tape/Reel)		

* CL Devices are UV erasable and can be programmed to any device configuration. CL Devices meet the electrical requirement of each oscillator type (including LC devices).

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SECTION 13
PIC17C4X MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC17C4X High-Performance 8-Bit CMOS EPROM/ROM Microcontroller 13-1

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MICROCHIP

PIC17C4X

High-Performance 8-Bit CMOS EPROM/ROM Microcontroller

13

Devices included in this data sheet:

- PIC17CR42
- PIC17C42A
- PIC17C43
- PIC17CR43
- PIC17C44
- PIC17C42†

Microcontroller Core Features:

- Only 58 single word instructions to learn
- All single cycle instructions (121 ns) except for program branches and table reads/writes which are two-cycle
- Operating speed:
  - ★ - DC - 33 MHz clock input
  - DC - 121 ns instruction cycle

Device	Program Memory		Data Memory
	EPROM	ROM	
PIC17CR42	-	2K	232
PIC17C42A	2K	-	232
PIC17C43	4K	-	454
PIC17CR43	-	4K	454
PIC17C44	8K	-	454
PIC17C42†	2K	-	232

- ★ Hardware Multiplier (Not available on the PIC17C42)
- Interrupt capability
- 16 levels deep hardware stack
- Direct, indirect and relative addressing modes
- Internal/External program memory execution
- 64K x 16 addressable program memory space

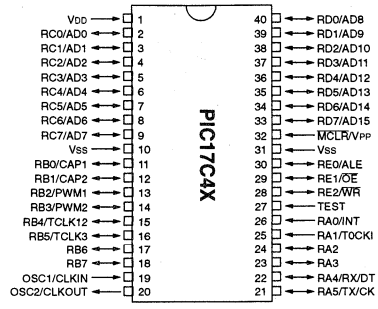
Peripheral Features:

- 33 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - RA2 and RA3 are open drain, high voltage (12V), high current (60 mA), I/O
- Two capture inputs and two PWM outputs
  - Captures are 16-bit, max resolution 160 ns
  - PWM resolution is 1- to 10-bit
- TMR0: 16-bit timer/counter with 8-bit programmable prescaler
- TMR1: 8-bit timer/counter

†NOT recommended for new designs, use 17C42A.

Pin Diagram

PDIP, CERDIP, Windowed CERDIP



- TMR2: 8-bit timer/counter
- TMR3: 16-bit timer/counter
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)

Special Microcontroller Features:

- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options

CMOS Technology:

- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide operating voltage range (2.5V to 6.0V)
- Commercial and Industrial Temperature Range
- Low-power consumption
  - < 5 mA @ 5V, 4 MHz
  - 100 µA typical @ 4.5V, 32 kHz
  - < 1 µA typical standby current @ 5V

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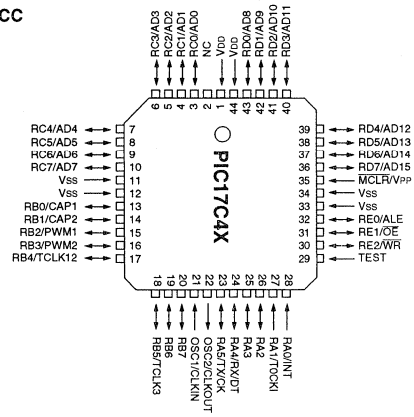
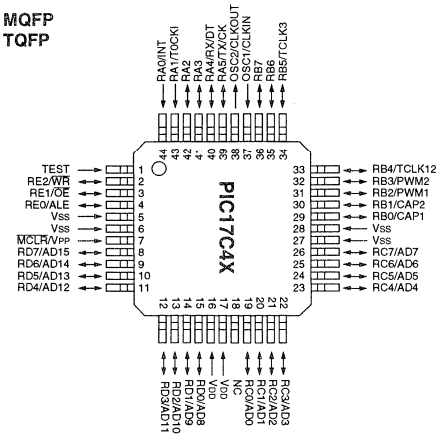
Pin Diagrams Cont.'d

PLCC



MQFP
TQFP



All devices are available in all package types, listed in Section 21.0, with the following exceptions:

- ROM devices are not available in Windowed CERDIP Packages
- TQFP is not available for the PIC17C42.

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For register and module descriptions in this data sheet, device legends show which devices apply to those sections. For example, the legend below shows that some features of only the PIC17C43, PIC17CR43, PIC17C44 are described in this section.

Applicable Devices					
42	R42	42A	43	R43	44

To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error from the previous version of the PIC17C4X Data Sheet (Literature Number DS30412B), please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

To assist you in the use of this document, Appendix C contains a list of new information in this data sheet, while Appendix D contains information that has changed

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1.0 OVERVIEW

This data sheet covers the PIC17C4X group of the PIC17CXX family of microcontrollers. The following devices are discussed in this data sheet:

- PIC17C42
- PIC17CR42
- PIC17C42A
- PIC17C43
- PIC17CR43
- PIC17C44

The PIC17CR42, PIC17C42A, PIC17C43, PIC17CR43, and PIC17C44 devices include architectural enhancements over the PIC17C42. These enhancements will be discussed throughout this data sheet.

The PIC17C4X devices are 40/44-Pin, EPROM/ROM-based members of the versatile PIC17CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC17CXX has enhanced core features, 16-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 16-bit wide instruction word with a separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 55 instructions (reduced instruction set) are available in the PIC17C42 and 58 instructions in all the other devices. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance. For mathematical intensive applications all devices, except the PIC17C42, have a single cycle 8 x 8 Hardware Multiplier.

PIC17CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

PIC17C4X devices have up to 454 bytes of RAM and 33 I/O pins. In addition, the PIC17C4X adds several peripheral features useful in many high performance applications including:

- Four timer/counters
- Two capture inputs
- Two PWM outputs
- A Universal Synchronous Asynchronous Receiver Transmitter (USART)

These special features reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LF oscillator is for low frequency crystals and minimizes power consumption, XT is a standard crystal, and the EC is for external clock input. The SLEEP (power-down) mode offers additional power saving. The user can wake-up the chip from SLEEP through several external and internal interrupts and device resets.

There are four configuration options for the device operational modes:

- Microprocessor
- Microcontroller
- Extended microcontroller
- Protected microcontroller

The microprocessor and extended microcontroller modes allow up to 64K-words of external program memory.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software malfunction.

Table 1-1 lists the features of the PIC17C4X devices.

A UV-erasable CERDIP-packaged version is ideal for code development while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

The PIC17C4X fits perfectly in applications ranging from precise motor control and industrial process control to automotive, instrumentation, and telecom applications. Other applications that require extremely fast execution of complex software programs or the flexibility of programming the software code as one of the last steps of the manufacturing process would also be well suited. The EPROM technology makes customization of application programs (with unique security codes, combinations, model numbers, parameter storage, etc.) fast and convenient. Small footprint package options make the PIC17C4X ideal for applications with space limitations that require high performance. High speed execution, powerful peripheral features, flexible I/O, and low power consumption all at low cost make the PIC17C4X ideal for a wide range of embedded control applications.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X and PIC16CXX families of microcontrollers will see the architectural enhancements that have been implemented. These enhancements allow the device to be more efficient in software and hardware requirements. Please refer to Appendix A for a detailed list of enhancements and modifications. Code written for PIC16C5X or PIC16CXX can be easily ported to PIC17CXX family of devices (Appendix B).

1.2 Development Support

The PIC17CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a universal programmer, a "C" compiler, and fuzzy logic support tools.

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TABLE 1-1: PIC17CXX FAMILY OF DEVICES

Features		PIC17C42	PIC17CR42	PIC17C42A	PIC17C43	PIC17CR43	PIC17C44
Maximum Frequency of Operation		25 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz
Operating Voltage Range		4.5 - 5.5V	2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V
Program Memory x16	(EPROM)	2K	-	2K	4K	-	8K
	(ROM)	-	2K	-	-	4K	-
Data Memory (bytes)		232	232	232	454	454	454
Hardware Multiplier (8 x 8)		-	Yes	Yes	Yes	Yes	Yes
Timer0 (16-bit + 8-bit postscaler)		Yes	Yes	Yes	Yes	Yes	Yes
Timer1 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Timer2 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Timer3 (16-bit)		Yes	Yes	Yes	Yes	Yes	Yes
Capture inputs (16-bit)		2	2	2	2	2	2
PWM outputs (up to 10-bit)		2	2	2	2	2	2
USART/SCI		Yes	Yes	Yes	Yes	Yes	Yes
Power-on Reset		Yes	Yes	Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes	Yes	Yes
External Interrupts		Yes	Yes	Yes	Yes	Yes	Yes
Interrupt Sources		11	11	11	11	11	11
Program Memory Code Protect		Yes	Yes	Yes	Yes	Yes	Yes
I/O Pins		33	33	33	33	33	33
I/O High Current Capability	Source	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA
	Sink	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)
Package Types		40-pin DIP 44-pin PLCC 44-pin MQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP

Note 1: Pins RA2 and RA3 can sink up to 60 mA.

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2.0 PIC17C4X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC17C4X Product Selection System section at the end of this data sheet. When placing orders, please use the "PIC17C4X Product Identification System" at the back of this data sheet to specify the correct part number.

For the PIC17C4X family of devices, there are four device "types" as indicated in the device number:

1. **C**, as in PIC17**C**42. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC17**LC**42. These devices have EPROM type memory, operate over an extended voltage range, and reduced frequency range.
3. **CR**, as in PIC17**CR**42. These devices have ROM type memory and operate over the standard voltage range.
4. **LCR**, as in PIC17**LCR**42. These devices have ROM type memory, operate over an extended voltage range, and reduced frequency range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes. Microchip's PRO MATE™ programmer supports programming of the PIC17C4X. Third party programmers also are available; refer to the *Third Party Guide* for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP^{SM}) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

ROM devices do not allow serialization information in the program memory space.

For information on submitting ROM code, please contact your regional sales office.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, thus giving customers a low cost option for high volume, mature products.

For information on submitting ROM code, please contact your regional sales office.

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC17C4X can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC17C4X uses a modified Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC17C4X opcodes are 16-bits wide, enabling single word instructions. The full 16-bit wide program memory bus fetches a 16-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions execute in a single cycle (121 ns @ 33 MHz), except for program branches and two special instructions that transfer data between program and data memory.

The PIC17C4X can address up to 64K x 16 of program memory space.

The **PIC17C42** and **PIC17C42A** integrate 2K x 16 of EPROM program memory on-chip, while the **PIC17CR42** has 2K x 16 of ROM program memory on-chip.

The **PIC17C43** integrates 4K x 16 of EPROM program memory, while the **PIC17CR43** has 4K x 16 of ROM program memory.

The **PIC17C44** integrates 8K x 16 EPROM program memory.

Program execution can be internal only (microcontroller or protected microcontroller mode), external only (microprocessor mode) or both (extended microcontroller mode). Extended microcontroller mode does not allow code protection.

The PIC17CXX can directly or indirectly address its register files or data memory. All special function registers, including the Program Counter (PC) and Working Register (WREG), are mapped in the data memory. The PIC17CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC17CXX simple yet efficient. In addition, the learning curve is reduced significantly.

One of the PIC17CXX family architectural enhancements from the PIC16CXX family allows two file registers to be used in some two operand instructions. This allows data to be moved directly between two registers without going through the WREG register. This increases performance and decreases program memory usage.

The PIC17CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift, and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature.

The WREG register is an 8-bit working register used for ALU operations.

All PIC17C4X devices (except the PIC17C42) have an 8 x 8 hardware multiplier. This multiplier generates a 16-bit result in a single cycle.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

Although the ALU does not perform signed arithmetic, the Overflow bit (OV) can be used to implement signed math. Signed arithmetic is comprised of a magnitude and a sign bit. The overflow bit indicates if the magnitude overflows and causes the sign bit to change state. Signed math can have greater than 7-bit values (magnitude), if more than one byte is used. The use of the overflow bit only operates on bit6 (MSb of magnitude) and bit7 (sign bit) of the value in the ALU. That is, the overflow bit is not useful if trying to implement signed math where the magnitude, for example, is 11-bits. If the signed math values are greater than 7-bits (15-, 24- or 31-bit), the algorithm must ensure that the low order bytes ignore the overflow status bit.

Care should be taken when adding and subtracting signed numbers to ensure that the correct operation is executed. Example 3-1 shows an item that must be taken into account when doing signed arithmetic on an ALU which operates as an unsigned machine.

EXAMPLE 3-1: SIGNED MATH

```
Hex Value       Signed Value      Unsigned Value
                Math              Math

  FFh             -127              255
+ 01h           +    1            +    1
=  ?            = -126 (FEh)      =    0 (00h);
                                   Carry bit = 1
```

Signed math requires the result in REG to be FEh (-126). This would be accomplished by subtracting one as opposed to adding one.

Simplified block diagrams are shown in Figure 3-1 and Figure 3-2. The descriptions of the device pins are listed in Table 3-1.

FIGURE 3-1: PIC17C42 BLOCK DIAGRAM

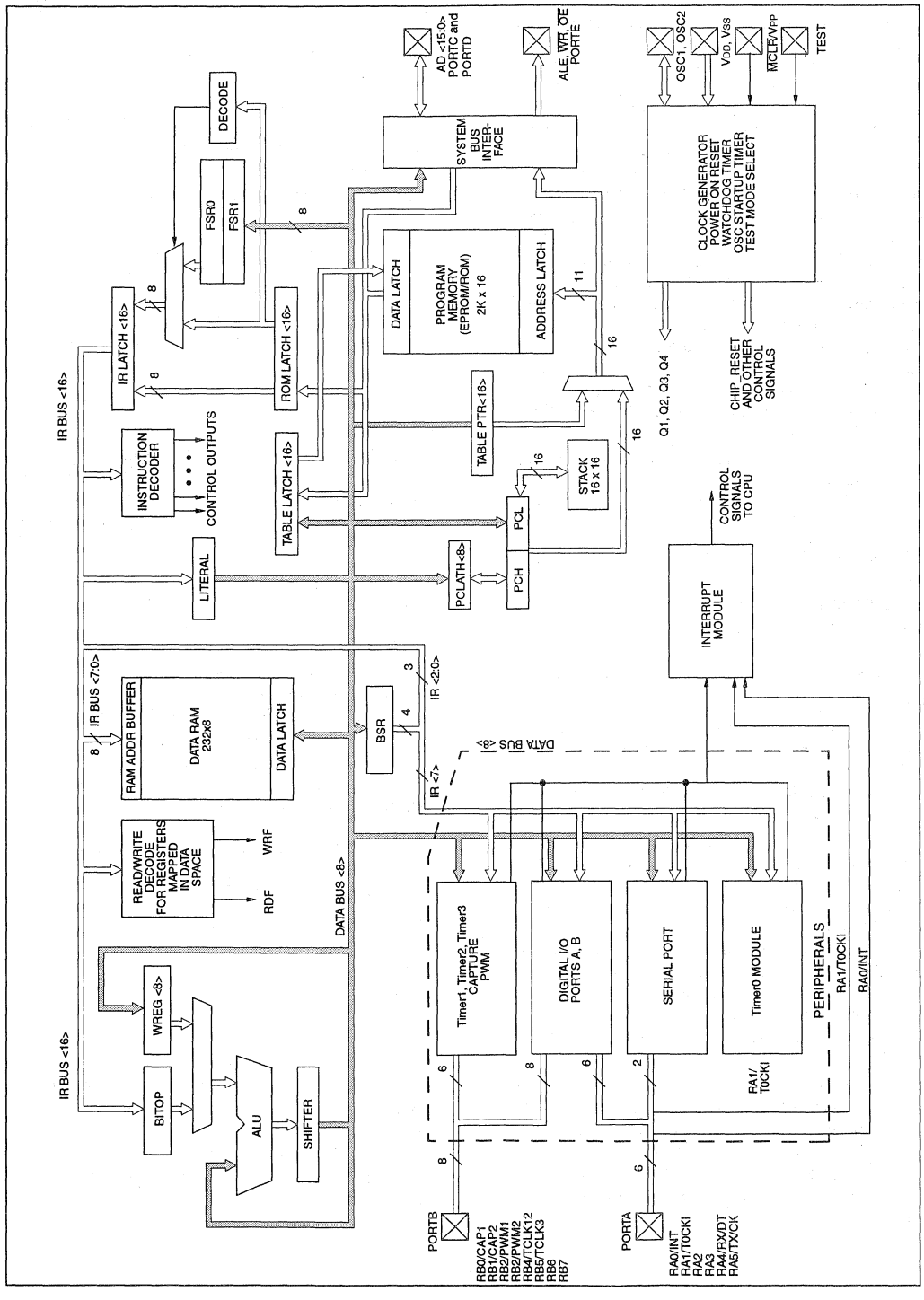

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FIGURE 3-2: PIC17CR42/42A/43/R43/44 BLOCK DIAGRAM

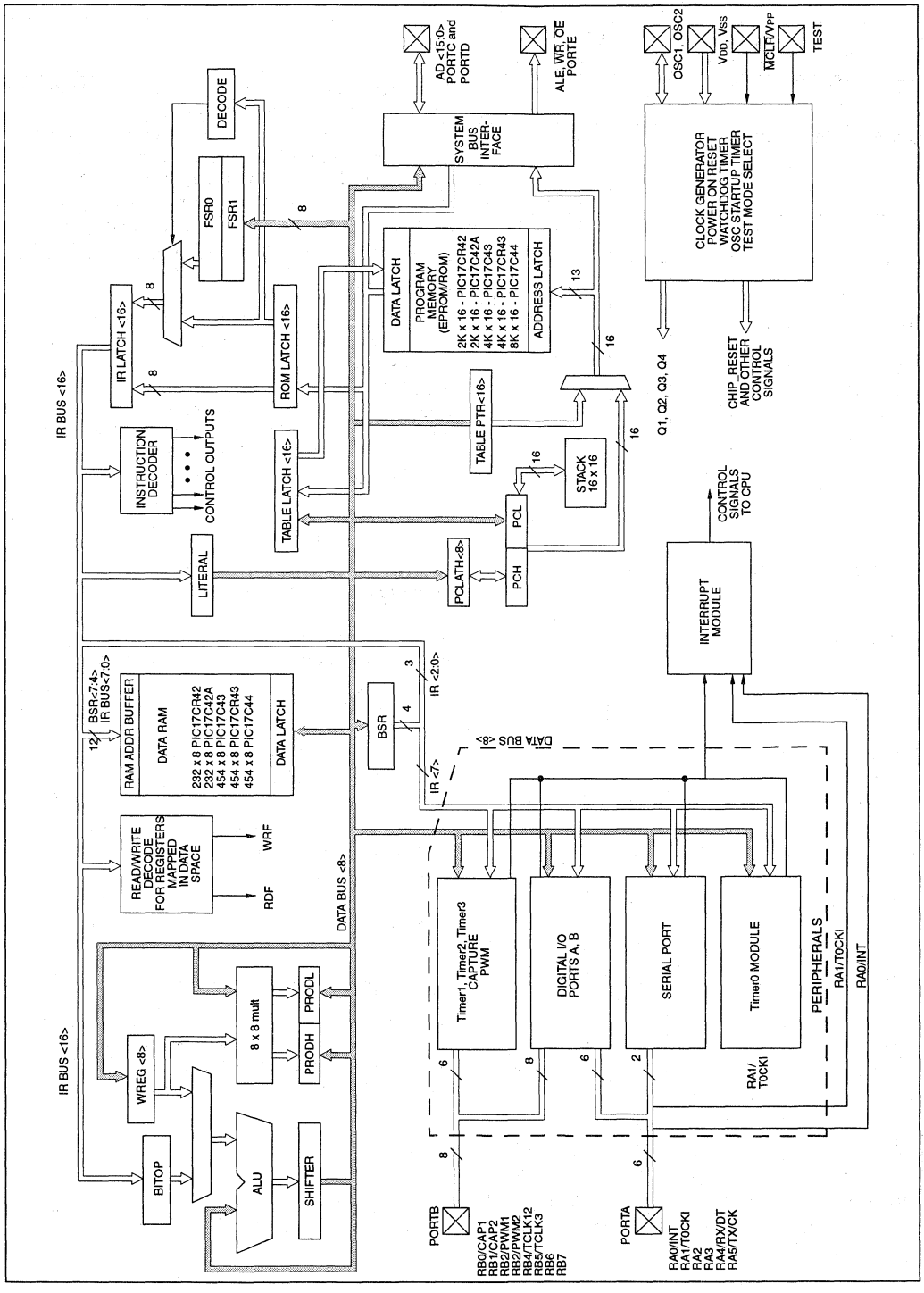

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TABLE 3-1: PINOUT DESCRIPTIONS

Name	DIP No.	PLCC No.	QFP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	19	21	37	I	ST	Oscillator input in crystal/resonator or RC oscillator mode. External clock input in external clock mode.
OSC2/CLKOUT	20	22	38	O	—	Oscillator output. Connects to crystal or resonator in crystal oscillator mode. In RC oscillator or external clock modes OSC2 pin outputs CLKOUT which has one fourth the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	32	35	7	I/P	ST	Master clear (reset) input/Programming Voltage (VPP) input. This is the active low reset input to the chip.
						PORTA is a bi-directional I/O Port except for RA0 and RA1 which are input only.
RA0/INT	26	28	44	I	ST	RA0/INT can also be selected as an external interrupt input. Interrupt can be configured to be on positive or negative edge.
RA1/T0CKI	25	27	43	I	ST	RA1/T0CKI can also be selected as an external interrupt input, and the interrupt can be configured to be on positive or negative edge. RA1/T0CKI can also be selected to be the clock input to the Timer0 timer/counter.
RA2	24	26	42	I/O	ST	High voltage, high current, open drain input/output port pins.
RA3	23	25	41	I/O	ST	High voltage, high current, open drain input/output port pins.
RA4/RX/DT	22	24	40	I/O	ST	RA4/RX/DT can also be selected as the USART (SCI) Asynchronous Receive or USART (SCI) Synchronous Data.
RA5/TX/CK	21	23	39	I/O	ST	RA5/TX/CK can also be selected as the USART (SCI) Asynchronous Transmit or USART (SCI) Synchronous Clock.
						PORTB is a bi-directional I/O Port with software configurable weak pull-ups.
RB0/CAP1	11	13	29	I/O	ST	RB0/CAP1 can also be the CAP1 input pin.
RB1/CAP2	12	14	30	I/O	ST	RB1/CAP2 can also be the CAP2 input pin.
RB2/PWM1	13	15	31	I/O	ST	RB2/PWM1 can also be the PWM1 output pin.
RB3/PWM2	14	16	32	I/O	ST	RB3/PWM2 can also be the PWM2 output pin.
RB4/TCLK12	15	17	33	I/O	ST	RB4/TCLK12 can also be the external clock input to Timer1 and Timer2.
RB5/TCLK3	16	18	34	I/O	ST	RB5/TCLK3 can also be the external clock input to Timer3.
RB6	17	19	35	I/O	ST	
RB7	18	20	36	I/O	ST	
						PORTC is a bi-directional I/O Port.
RC0/AD0	2	3	19	I/O	TTL	This is also the lower half of the 16-bit wide system bus in microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration, these pins are address output as well as data input or output.
RC1/AD1	3	4	20	I/O	TTL	
RC2/AD2	4	5	21	I/O	TTL	
RC3/AD3	5	6	22	I/O	TTL	
RC4/AD4	6	7	23	I/O	TTL	
RC5/AD5	7	8	24	I/O	TTL	
RC6/AD6	8	9	25	I/O	TTL	
RC7/AD7	9	10	26	I/O	TTL	

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input.

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TABLE 3-1: PINOUT DESCRIPTIONS

Name	DIP No.	PLCC No.	QFP No.	I/O/P Type	Buffer Type	Description
						PORTD is a bi-directional I/O Port.
RD0/AD8	40	43	15	I/O	TTL	This is also the upper byte of the 16-bit system bus in microprocessor mode or extended microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration these pins are address output as well as data input or output.
RD1/AD9	39	42	14	I/O	TTL	
RD2/AD10	38	41	13	I/O	TTL	
RD3/AD11	37	40	12	I/O	TTL	
RD4/AD12	36	39	11	I/O	TTL	
RD5/AD13	35	38	10	I/O	TTL	
RD6/AD14	34	37	9	I/O	TTL	
RD7/AD15	33	36	8	I/O	TTL	
						PORTE is a bi-directional I/O Port.
RE0/ALE	30	32	4	I/O	TTL	In microprocessor mode or extended microcontroller mode, it is the Address Latch Enable (ALE) output. Address should be latched on the falling edge of ALE output.
RE1/$\overline{OE}$	29	31	3	I/O	TTL	In microprocessor or extended microcontroller mode, it is the Output Enable ($\overline{OE}$) control output (active low).
RE2/$\overline{WR}$	28	30	2	I/O	TTL	In microprocessor or extended microcontroller mode, it is the Write Enable ($\overline{WR}$) control output (active low).
TEST	27	29	1	I	ST	Test mode selection control input. Always tie to VSS for normal operation.
VSS	10, 31	11, 12, 33, 34	5, 6, 27, 28	P		Ground reference for logic and I/O pins.
VDD	1	1, 44	16, 17	P		Positive supply for logic and I/O pins.

Legend: I = Input only; O = Output only; I/O = Input/Output; P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input.

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3, and Q4. Internally, the program counter (PC) is incremented every Q1, and the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-3.

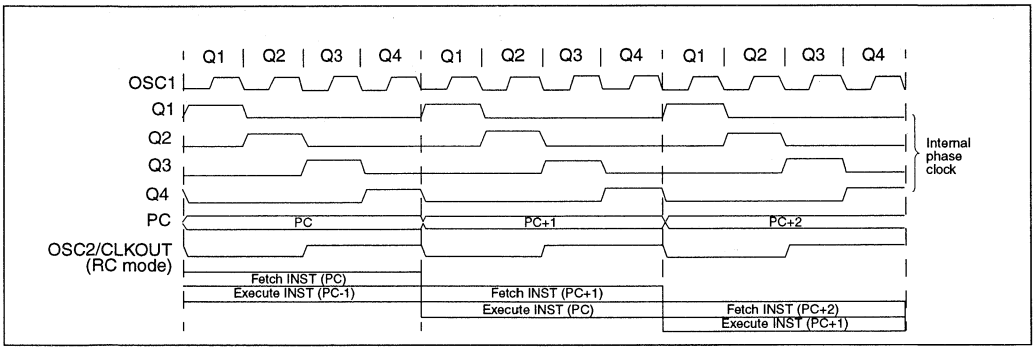
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3, and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-2).

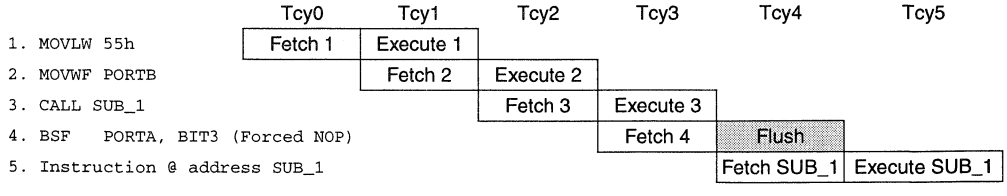
A fetch cycle begins with the program counter incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-2: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.0 RESET

The PIC17CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{MCLR}$ reset during normal operation
- WDT Reset (normal operation)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are forced to a "reset state" on Power-on Reset (POR), on $\overline{MCLR}$ or WDT Reset and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT Reset during SLEEP, since this reset is viewed as the resumption of normal operation. The $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 4-3. These bits are used in software to determine the nature of reset. See Table 4-4 for a full description of reset states of all registers.

Note:	While the device is in a reset state, the internal phase clock is held in the Q1 state. Any processor mode that allows external execution will force the RE0/ALE pin as a low output and the RE1/$\overline{OE}$ and RE2/$\overline{WR}$ pins as high outputs.

A simplified block diagram of the on-chip reset circuit is shown in Figure 4-1.

4.1 Power-on Reset (POR), Power-up Timer (PWRT), and Oscillator Start-up Timer (OST)

4.1.1 POWER-ON RESET (POR)

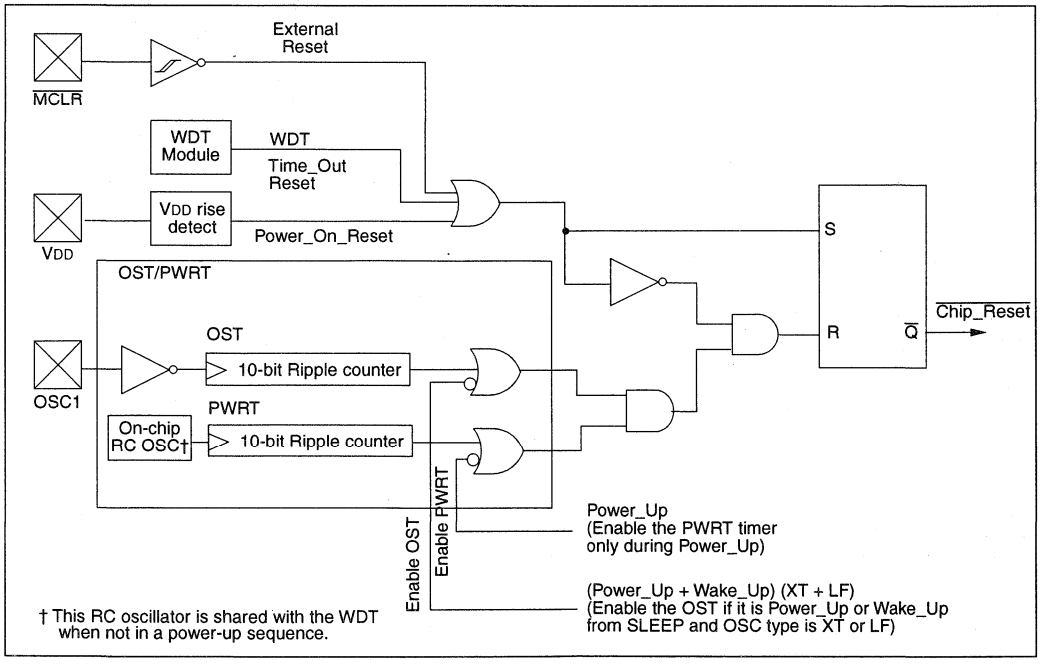
The Power-on Reset circuit holds the device in reset until VDD is above the trip point (in the range of 1.4V - 2.3V). The PIC17C42 does not produce an internal reset when VDD declines. All other devices will produce an internal reset for both rising and falling VDD. To take advantage of the POR, just tie the $\overline{MCLR}$/VPP pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD is required. See Electrical Specifications for details.

4.1.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 96 ms time-out (nominal) on power-up. This occurs from rising edge of the POR signal and after the first rising edge of $\overline{MCLR}$ (detected high). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. In most cases the PWRT delay allows the VDD to rise to an acceptable level.

The power-up time delay will vary from chip to chip and to VDD and temperature. See DC parameters for details.

FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



4.1.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (1024TOSC) delay after $\overline{MCLR}$ is detected high or a wake-up from SLEEP event occurs.

The OST time-out is invoked only for XT and LF oscillator modes on a Power-on Reset or a Wake-up from SLEEP.

The OST counts the oscillator pulses on the OSC1/CLKIN pin. The counter only starts incrementing after the amplitude of the signal reaches the oscillator input thresholds. This delay allows the crystal oscillator or resonator to stabilize before the device exits reset. The length of time-out is a function of the crystal/resonator frequency.

4.1.4 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First the internal POR signal goes high when the POR trip point is reached. If $\overline{MCLR}$ is high, then both the OST and PWRT timers start. In general the PWRT time-out is longer, except with low frequency crystals/resonators. The total time-out also varies based on oscillator configuration. Table 4-1 shows the times that are associated with the oscillator configuration. Figure 4-2 and Figure 4-3 display these time-out sequences.

If the device voltage is not within electrical specification at the end of a time-out, the $\overline{MCLR}$/VPP pin must be held low until the voltage is within the device specification. The use of an external RC delay is sufficient for many of these applications.

TABLE 4-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up	Wake up from SLEEP	$\overline{MCLR}$ Reset
XT, LF	Greater of: 96 ms or 1024TOSC	1024TOSC	—
EC, RC	Greater of: 96 ms or 1024TOSC	—	—

The time-out sequence begins from the first rising edge of $\overline{MCLR}$.

Table 4-3 shows the reset conditions for some special registers, while Table 4-4 shows the initialization conditions for all the registers. The shaded registers (in Table 4-4) are for all devices except the PIC17C42. In the PIC17C42, the PRODH and PRODL registers are general purpose RAM.

TABLE 4-2: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{TO}$	$\overline{PD}$	Event
1	1	Power-on Reset, $\overline{MCLR}$ Reset during normal operation, or CLRWDT instruction executed
1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP
0	1	WDT Reset during normal operation
0	0	WDT Reset during SLEEP

In Figure 4-2, Figure 4-3 and Figure 4-4, TPWRT > TOST, as would be the case in higher frequency crystals. For lower frequency crystals, (i.e., 32 kHz) TOST would be greater.

TABLE 4-3: RESET CONDITION FOR THE PROGRAM COUNTER AND THE CPUSTA REGISTER

Event		PCH:PCL	CPUSTA	OST Active
Power-on Reset		0000h	--11 11--	Yes
$\overline{MCLR}$ Reset during normal operation		0000h	--11 11--	No
$\overline{MCLR}$ Reset during SLEEP		0000h	--11 10--	Yes (2)
WDT Reset during normal operation		0000h	--11 01--	No
WDT Reset during SLEEP (3)		0000h	--11 00--	Yes (2)
Interrupt wake-up from SLEEP	GLINTD is set	PC + 1	--11 10--	Yes (2)
	GLINTD is clear	PC + 1 (1)	--10 10--	Yes (2)

Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.

Note 1: On wake-up, this instruction is executed. The instruction at the appropriate interrupt vector is fetched and then executed.

2: The OST is only active when the Oscillator is configured for XT or LF modes.

3: The Program Counter = 0, that is the device branches to the reset vector. This is different from the mid-range devices.

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FIGURE 4-2: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD})

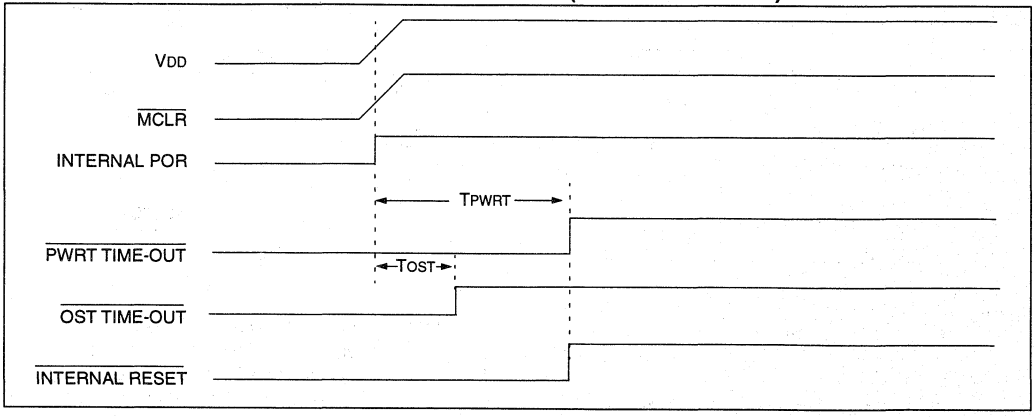

FIGURE 4-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD})

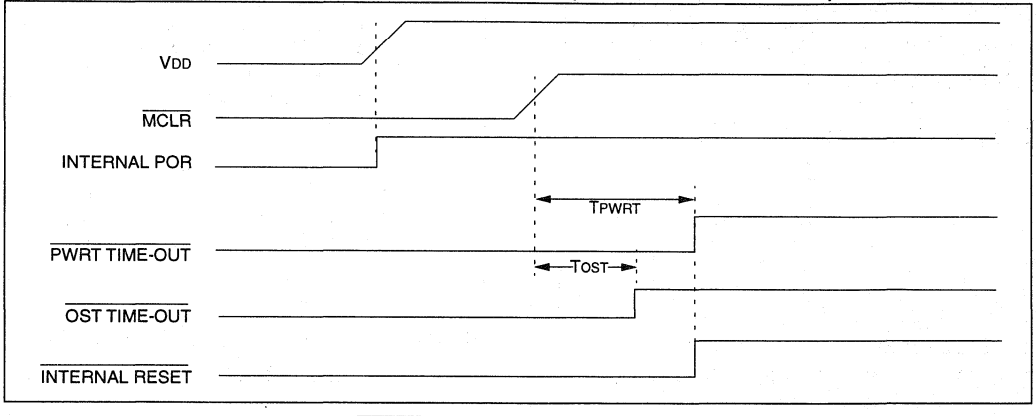

FIGURE 4-4: SLOW RISE TIME ($\overline{MCLR}$ TIED TO V_{DD})

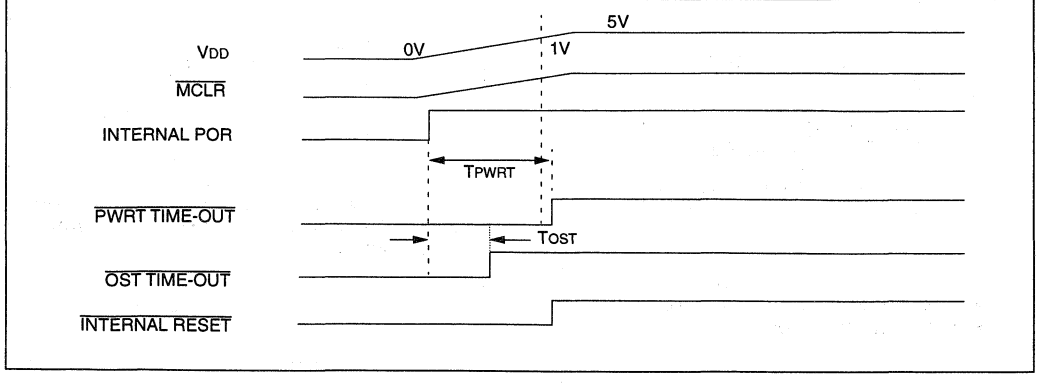

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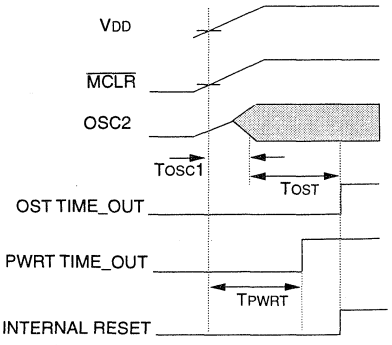
FIGURE 4-5: OSCILLATOR START-UP TIME



This figure shows in greater detail the timings involved with the oscillator start-up timer. In this example the low frequency crystal start-up time is larger than power-up time (TPWRT).
Tosc1 = time for the crystal oscillator to react to an oscillation level detectable by the Oscillator Start-up Timer (ost).
TOST = 1024TOSC.

FIGURE 4-6: USING ON-CHIP POR

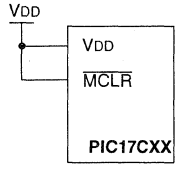
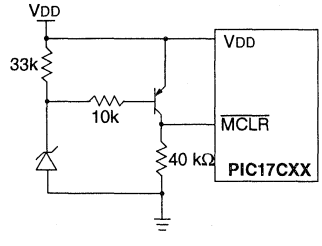
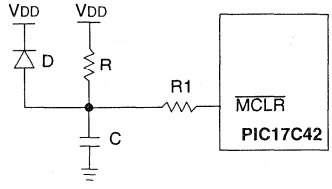


FIGURE 4-7: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 4-8: PIC17C42 EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

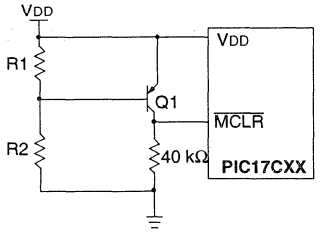


Note 1: An external Power-on Reset circuit is required only if VDD power-up time is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to ensure that the voltage drop across R does not exceed 0.2V (max. leakage current spec. on the MCLR/VPP pin is 5 μA). A larger voltage drop will degrade VIH level on the MCLR/VPP pin.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or (Electrical Overstress) EOS.

FIGURE 4-9: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

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TABLE 4-4: INITIALIZATION CONDITIONS FOR SPECIAL FUNCTION REGISTERS

Register	Address	Power-on Reset	MCLR Reset WDT Reset	Wake-up from SLEEP through interrupt
Unbanked				
INDF0	00h	0000 0000	0000 0000	0000 0000
FSR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1(2)
PCLATH	03h	0000 0000	0000 0000	uuuu uuuu
ALUSTA	04h	1111 xxxx	1111 uuuu	1111 uuuu
T0STA	05h	0000 000-	0000 000-	0000 000-
CPUSTA(3)	06h	--11 11--	--11 qq--	--uu qq--
INTSTA	07h	0000 0000	0000 0000	uuuu uuuu(1)
INDF1	08h	0000 0000	0000 0000	uuuu uuuu
FSR1	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	0Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0L	0Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0H	0Ch	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLPTRL (4)	0Dh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLPTRH (4)	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLPTRL (5)	0Dh	0000 0000	0000 0000	uuuu uuuu
TBLPTRH (5)	0Eh	0000 0000	0000 0000	uuuu uuuu
BSR	0Fh	0000 0000	0000 0000	uuuu uuuu
Bank 0				
PORTA	10h	0-xx xxxx	0-uu uuuu	uuuu uuuu
DDRB	11h	1111 1111	1111 1111	uuuu uuuu
PORTB	12h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RCSTA	13h	0000 -00x	0000 -00u	uuuu -uuu
RCREG	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA	15h	0000 --1x	0000 --1u	uuuu --uu
TXREG	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SPBRG	17h	xxxx xxxx	uuuu uuuu	uuuu uuuu
Bank 1				
DDRC	10h	1111 1111	1111 1111	uuuu uuuu
PORTC	11h	xxxx xxxx	uuuu uuuu	uuuu uuuu
DDRD	12h	1111 1111	1111 1111	uuuu uuuu
PORTD	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
DDRE	14h	---- -111	---- -111	---- -uuu
PORTE	15h	---- -xxx	---- -uuu	---- -uuu
PIR	16h	0000 0010	0000 0010	uuuu uuuu(1)
PIE	17h	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented read as '0', q = value depends on condition.

Note 1: One or more bits in INTSTA, PIR will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GLINTD bit is cleared, the PC is loaded with the interrupt vector.

3: See Table 4-3 for reset value of specific condition.

4: Only applies to the PIC17C42.

5: Does not apply to the PIC17C42.

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TABLE 4-4: INITIALIZATION CONDITIONS FOR SPECIAL FUNCTION REGISTERS (Cont.'d)

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset	Wake-up from SLEEP through interrupt
Bank 2				
TMR1	10h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR2	11h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3L	12h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3H	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PR1	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PR2	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PR3/CA1L	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PR3/CA1H	17h	xxxx xxxx	uuuu uuuu	uuuu uuuu
Bank 3				
PW1DCL	10h	xx-- ----	uu-- ----	uu-- ----
PW2DCL	11h	xx-- ----	uu-- ----	uu-- ----
PW1DCH	12h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PW2DCH	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CA2L	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CA2H	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TCON1	16h	0000 0000	0000 0000	uuuu uuuu
TCON2	17h	0000 0000	0000 0000	uuuu uuuu
Unbanked				
PRODL (5)	18h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODH (5)	19h	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented read as '0', q = value depends on condition.

Note 1: One or more bits in INTSTA, PIR will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GLINTD bit is cleared, the PC is loaded with the interrupt vector.

3: See Table 4-3 for reset value of specific condition.

4: Only applies to the PIC17C42.

5: Does not apply to the PIC17C42.

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5.0 INTERRUPTS

The PIC17C4X devices have 11 sources of interrupt:

- External interrupt from the RA0/INT pin
- Change on RB7:RB0 pins
- TMR0 Overflow
- TMR1 Overflow
- TMR2 Overflow
- TMR3 Overflow
- USART Transmit buffer empty
- USART Receive buffer full
- Capture1
- Capture2
- T0CKI edge occurred

There are four registers used in the control and status of interrupts. These are:

- CPUSTA
- INTSTA
- PIE
- PIR

The CPUSTA register contains the GLINTD bit. This is the Global Interrupt Disable bit. When this bit is set, all interrupts are disabled. This bit is part of the controller core functionality and is described in the Memory Organization section.

When an interrupt is responded to, the GLINTD bit is automatically set to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with the interrupt vector address. There are four interrupt vectors. Each vector address is for a specific interrupt source (except the peripheral interrupts which have the same vector address). These sources are:

- External interrupt from the RA0/INT pin
- TMR0 Overflow
- T0CKI edge occurred
- Any peripheral interrupt

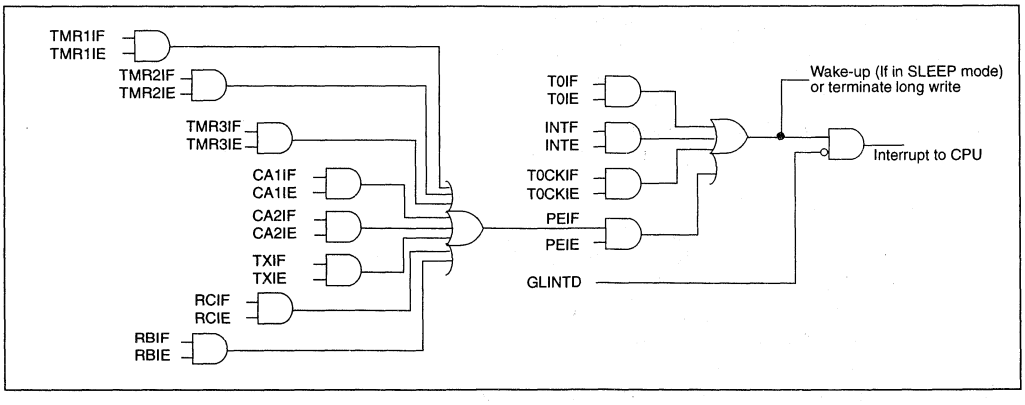
When program execution vectors to one of these interrupt vector addresses (except for the peripheral interrupt address), the interrupt flag bit is automatically cleared. Vectoring to the peripheral interrupt vector address does not automatically clear the source of the interrupt. In the peripheral interrupt service routine, the source(s) of the interrupt can be determined by testing the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

All of the individual interrupt flag bits will be set regardless of the status of their corresponding mask bit or the GLINTD bit.

For external interrupt events, there will be an interrupt latency. For two cycle instructions, the latency could be one instruction cycle longer.

The "return from interrupt" instruction, `RETFIE`, can be used to mark the end of the interrupt service routine. When this instruction is executed, the stack is "POPed", and the GLINTD bit is cleared (to re-enable interrupts).

FIGURE 5-1: INTERRUPT LOGIC



5.1 Interrupt Status Register (INTSTA)

The Interrupt Status/Control register (INTSTA) records the individual interrupt requests in flag bits, and contains the individual interrupt enable bits (not for the peripherals).

The PEIF bit is a read only, bit wise OR of all the peripheral flag bits in the PIR register (Figure 5-4).

Note: T0IF, INTF, T0CKIF, or PEIF will be set by the specified condition, even if the corresponding interrupt enable bit is clear (interrupt disabled) or the GLINTD bit is set (all interrupts disabled).

Care should be taken when clearing any of the INTSTA register enable bits when interrupts are enabled (GLINTD is clear). If any of the INTSTA flag bits (T0IF, INTF, T0CKIF, or PEIF) are set in the same instruction cycle as the corresponding interrupt enable bit is cleared, the device will vector to the reset address (0x00).

When disabling any of the INTSTA enable bits, the GLINTD bit should be set (disabled).

FIGURE 5-2: INTSTA REGISTER (ADDRESS: 07h, UNBANKED)

R - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0
PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE
bit7							bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **PEIF**: Peripheral Interrupt Flag bit
This bit is the OR of all peripheral interrupt flag bits AND'ed with their corresponding enable bits.
1 = A peripheral interrupt is pending
0 = No peripheral interrupt is pending

bit 6: **T0CKIF**: External Interrupt on T0CKI Pin Flag bit
This bit is cleared by hardware, when the interrupt logic forces program execution to vector (18h).
1 = The software specified edge occurred on the RA1/T0CKI pin
0 = The software specified edge did not occur on the RA1/T0CKI pin

bit 5: **T0IF**: TMR0 Overflow Interrupt Flag bit
This bit is cleared by hardware, when the interrupt logic forces program execution to vector (10h).
1 = TMR0 overflowed
0 = TMR0 did not overflow

bit 4: **INTF**: External Interrupt on INT Pin Flag bit
This bit is cleared by hardware, when the interrupt logic forces program execution to vector (08h).
1 = The software specified edge occurred on the RA0/INT pin
0 = The software specified edge did not occur on the RA0/INT pin

bit 3: **PEIE**: Peripheral Interrupt Enable bit
This bit enables all peripheral interrupts that have their corresponding enable bits set.
1 = Enable peripheral interrupts
0 = Disable peripheral interrupts

bit 2: **T0CKIE**: External Interrupt on T0CKI Pin Enable bit
1 = Enable software specified edge interrupt on the RA1/T0CKI pin
0 = Disable interrupt on the RA1/T0CKI pin

bit 1: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enable TMR0 overflow interrupt
0 = Disable TMR0 overflow interrupt

bit 0: **INTE**: External Interrupt on RA0/INT Pin Enable bit
1 = Enable software specified edge interrupt on the RA0/INT pin
0 = Disable software specified edge interrupt on the RA0/INT pin

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5.2 Peripheral Interrupt Enable Register (PIE)

This register contains the individual flag bits for the Peripheral interrupts.

FIGURE 5-3: PIE REGISTER (ADDRESS: 17h, BANK 1)

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0
RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE
bit7							bit0

R = Readable bit
W = Writable bit
-n = Value at POR reset

bit 7: **RBIE**: PORTB Interrupt on Change Enable bit
1 = Enable PORTB interrupt on change
0 = Disable PORTB interrupt on change

bit 6: **TMR3IE**: Timer3 Interrupt Enable bit
1 = Enable Timer3 interrupt
0 = Disable Timer3 interrupt

bit 5: **TMR2IE**: Timer2 Interrupt Enable bit
1 = Enable Timer2 interrupt
0 = Disable Timer2 interrupt

bit 4: **TMR1IE**: Timer1 Interrupt Enable bit
1 = Enable Timer1 interrupt
0 = Disable Timer1 interrupt

bit 3: **CA2IE**: Capture2 Interrupt Enable bit
1 = Enable Capture interrupt on RB1/CAP2 pin
0 = Disable Capture interrupt on RB1/CAP2 pin

bit 2: **CA1IE**: Capture1 Interrupt Enable bit
1 = Enable Capture interrupt on RB2/CAP1 pin
0 = Disable Capture interrupt on RB2/CAP1 pin

bit 1: **TXIE**: USART Transmit Interrupt Enable bit
1 = Enable Transmit buffer empty interrupt
0 = Disable Transmit buffer empty interrupt

bit 0: **RCIE**: USART Receive Interrupt Enable bit
1 = Enable Receive buffer full interrupt
0 = Disable Receive buffer full interrupt

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5.3 Peripheral Interrupt Request Register (PIR)

This register contains the individual flag bits for the peripheral interrupts.

Note: These bits will be set by the specified condition, even if the corresponding interrupt enable bit is cleared (interrupt disabled), or the GLINTD bit is set (all interrupts disabled). Before enabling an interrupt, the user may wish to clear the interrupt flag to ensure that the program does not immediately branch to the peripheral interrupt service routine.

FIGURE 5-4: PIR REGISTER (ADDRESS: 16h, BANK 1)

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R - 1	R - 0
RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF
bit7							bit0

R = Readable bit
W = Writable bit
-n = Value at POR reset

bit 7: **RBIF**: PORTB Interrupt on Change Flag bit
1 = One of the PORTB inputs changed (Software must end the mismatch condition)
0 = None of the PORTB inputs have changed

bit 6: **TMR3IF**: Timer3 Interrupt Flag bit
If Capture1 is enabled (CA1/$\overline{PR3}$ = 1)
1 = Timer3 overflowed
0 = Timer3 did not overflow

If Capture1 is disabled (CA1/$\overline{PR3}$ = 0)
1 = Timer3 value has rolled over to 0000h from equalling the period register (PR3H:PR3L) value
0 = Timer3 value has not rolled over to 0000h from equalling the period register (PR3H:PR3L) value

bit 5: **TMR2IF**: Timer2 Interrupt Flag bit
1 = Timer2 value has rolled over to 0000h from equalling the period register (PR2) value
0 = Timer2 value has not rolled over to 0000h from equalling the period register (PR2) value

bit 4: **TMR1IF**: Timer1 Interrupt Flag bit
If Timer1 is in 8-bit mode (T16 = 0)
1 = Timer1 value has rolled over to 0000h from equalling the period register (PR) value
0 = Timer1 value has not rolled over to 0000h from equalling the period register (PR2) value

If Timer1 is in 16-bit mode (T16 = 1)
1 = TMR1:TMR2 value has rolled over to 0000h from equalling the period register (PR1:PR2) value
0 = TMR1:TMR2 value has not rolled over to 0000h from equalling the period register (PR1:PR2) value

bit 3: **CA2IF**: Capture2 Interrupt Flag bit
1 = Capture event occurred on RB1/CAP2 pin
0 = Capture event did not occur on RB1/CAP2 pin

bit 2: **CA1IF**: Capture1 Interrupt Flag bit
1 = Capture event occurred on RB0/CAP1 pin
0 = Capture event did not occur on RB0/CAP1 pin

bit 1: **TXIF**: USART Transmit Interrupt Flag bit
1 = Transmit buffer is empty
0 = Transmit buffer is full

bit 0: **RCIF**: USART Receive Interrupt Flag bit
1 = Receive buffer is full
0 = Receive buffer is empty

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5.4 Interrupt Operation

Global Interrupt Disable bit, GLINTD (CPUSTA<4>), enables all unmasked interrupts (if clear) or disables all interrupts (if set). Individual interrupts can be disabled through their corresponding enable bits in the INTSTA register. Peripheral interrupts need either the global peripheral enable PEIE bit disabled, or the specific peripheral enable bit disabled. Disabling the peripherals via the global peripheral enable bit, disables all peripheral interrupts. GLINTD is set on reset (interrupts disabled).

The RETFIE instruction allows returning from interrupt and re-enable interrupts at the same time.

When an interrupt is responded to, the GLINTD bit is automatically set to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with interrupt vector. There are four interrupt vectors to reduce interrupt latency.

The peripheral interrupt vector has multiple interrupt sources. Once in the peripheral interrupt service routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The peripheral interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid continuous interrupts.

The PIC17C4X devices have four interrupt vectors. These vectors and their hardware priority are shown in Table 5-1. If two enabled interrupts occur "at the same time", the interrupt of the highest priority will be serviced first. This means that the vector address of that interrupt will be loaded into the program counter (PC).

TABLE 5-1: INTERRUPT VECTORS/ PRIORITIES

Address	Vector	Priority
0008h	External Interrupt on RA0/ INT pin (INTF)	1 (Highest)
0010h	TMR0 overflow interrupt (T0IF)	2
0018h	External Interrupt on T0CKI (T0CKIF)	3
0020h	Peripherals (PEIF)	4 (Lowest)

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GLINTD bit.

Note 2: When disabling any of the INTSTA enable bits, the GLINTD bit should be set (disabled).

Note 3: For the PIC17C42 only:
If an interrupt occurs while the Global Interrupt Disable (GLINTD) bit is being set, the GLINTD bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction). The events that would cause this to occur are:

1. An interrupt occurs simultaneously with an instruction that sets the GLINTD bit.
2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the RETFIE instruction. This causes the GLINTD bit to be cleared (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GLINTD bit was set by the instruction, as shown in the following code:

```
LOOP   BSF    CPUSTA, GLINTD ; Disable Global
                              ; Interrupt
       BTFSS  CPUSTA, GLINTD ; Global Interrupt
                              ; Disabled?
       GOTO   LOOP           ; NO, try again
                              ; YES, continue
                              ; with program
                              ; low
```

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5.5 RA0/INT Interrupt

The external interrupt on the RA0/INT pin is edge triggered. Either the rising edge, if INTEDG bit (T0STA<7>) is set, or the falling edge, if INTEDG bit is clear. When a valid edge appears on the RA0/INT pin, the INTF bit (INTSTA<4>) is set. This interrupt can be disabled by clearing the INTE control bit (INTSTA<0>). The INT interrupt can wake the processor from SLEEP. See Section 14.4 for details on SLEEP operation.

5.6 TMR0 Interrupt

An overflow (FFFFh → 0000h) in TMR0 will set the T0IF (INTSTA<5>) bit. The interrupt can be enabled/disabled by setting/clearing the T0IE control bit (INTSTA<1>). For operation of the Timer0 module, see Section 11.0.

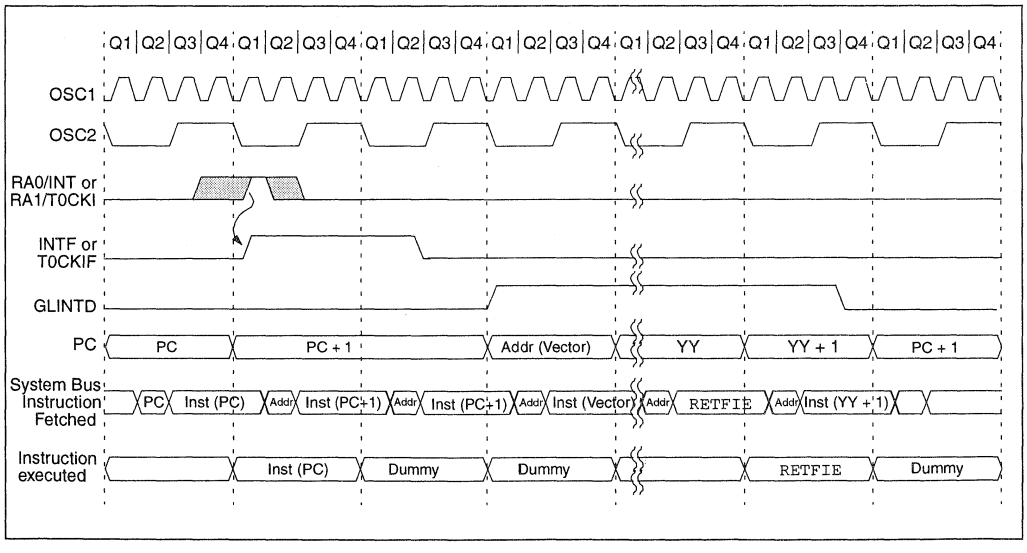
5.7 T0CKI Interrupt

The external interrupt on the RA1/T0CKI pin is edge triggered. Either the rising edge, if the T0SE bit (T0STA<6>) is set, or the falling edge, if the T0SE bit is clear. When a valid edge appears on the RA1/T0CKI pin, the T0CKIF bit (INTSTA<6>) is set. This interrupt can be disabled by clearing the T0CKIE control bit (INTSTA<2>). The T0CKI interrupt can wake up the processor from SLEEP. See Section 14.4 for details on SLEEP operation.

5.8 Peripheral Interrupt

The peripheral interrupt flag indicates that at least one of the peripheral interrupts occurred (PEIF is set). The PEIF bit is a read only bit, and is a bit wise OR of all the flag bits in the PIR register AND'ed with the corresponding enable bits in the PIE register. Some of the peripheral interrupts can wake the processor from SLEEP. See Section 14.4 for details on SLEEP operation.

FIGURE 5-5: INT PIN / T0CKI PIN INTERRUPT TIMING



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5.9 Context Saving During Interrupts

During an interrupt, only the returned PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt; e.g. WREG, ALUSTA and the BSR registers. This requires implementation in software.

Example 5-1 shows the saving and restoring of information for an interrupt service routine. The PUSH and POP routines could either be in each interrupt service routine or could be subroutines that were called. Depending on the application, other registers may also need to be saved, such as PCLATH.

EXAMPLE 5-1: SAVING STATUS AND WREG IN RAM

```
;
; The addresses that are used to store the CPUSTA and WREG values
; must be in the data memory address range of 18h - 1Fh. Up to
; 8 locations can be saved and restored using
; the MOVFP instruction. This instruction neither affects the status
; bits, nor corrupts the WREG register.
;
;
PUSH    MOVFP   WREG, TEMP_W          ; Save WREG
        MOVFP   ALUSTA, TEMP_STATUS   ; Save ALUSTA
        MOVFP   BSR, TEMP_BSR         ; Save BSR

ISR     :                             ; This is the interrupt service routine
        :
POP     MOVFP   TEMP_W, WREG          ; Restore WREG
        MOVFP   TEMP_STATUS, ALUSTA   ; Restore ALUSTA
        MOVFP   TEMP_BSR, BSR         ; Restore BSR
        RETFIE                        ; Return from Interrupts enabled
```

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NOTES:

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6.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC17C4X; program memory and data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into General Purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

6.1 Program Memory Organization

PIC17C4X devices have a 16-bit program counter capable of addressing a 64K x 16 program memory space. The reset vector is at 0000h and the interrupt vectors are at 0008h, 0010h, 0018h, and 0020h (Figure 6-1).

6.1.1 PROGRAM MEMORY OPERATION

The PIC17C4X can operate in one of four possible program memory configurations. The configuration is selected by two configuration bits. The possible modes are:

- Microprocessor
- Microcontroller
- Extended Microcontroller
- Protected Microcontroller

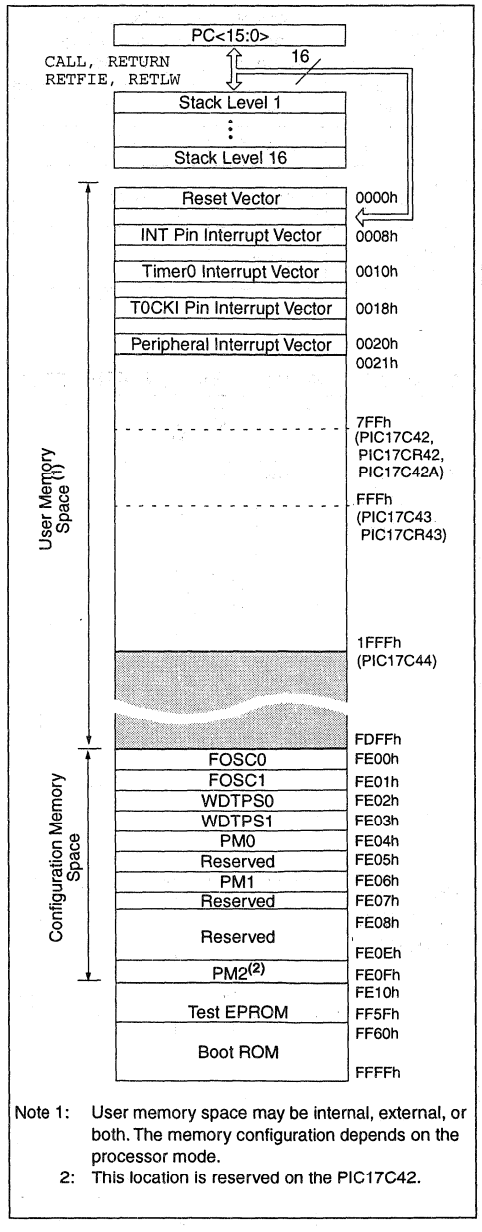
The microcontroller and protected microcontroller modes only allow internal execution. Any access beyond the program memory reads unknown data. The protected microcontroller mode also enables the code protection feature.

The extended microcontroller mode accesses both the internal program memory as well as external program memory. Execution automatically switches between internal and external memory. The 16-bits of address allow a program memory range of 64K-words.

The microprocessor mode only accesses the external program memory. The on-chip program memory is ignored. The 16-bits of address allow a program memory range of 64K-words. Microprocessor mode is the default mode of an unprogrammed device.

The different modes allow different access to the configuration bits, test memory, and boot ROM. Table 6-1 lists which modes can access which areas in memory. Test Memory and Boot Memory are not required for normal operation of the device. Care should be taken to ensure that no unintended branches occur to these areas.

FIGURE 6-1: PROGRAM MEMORY MAP AND STACK



Note 1: User memory space may be internal, external, or both. The memory configuration depends on the processor mode.
2: This location is reserved on the PIC17C42.

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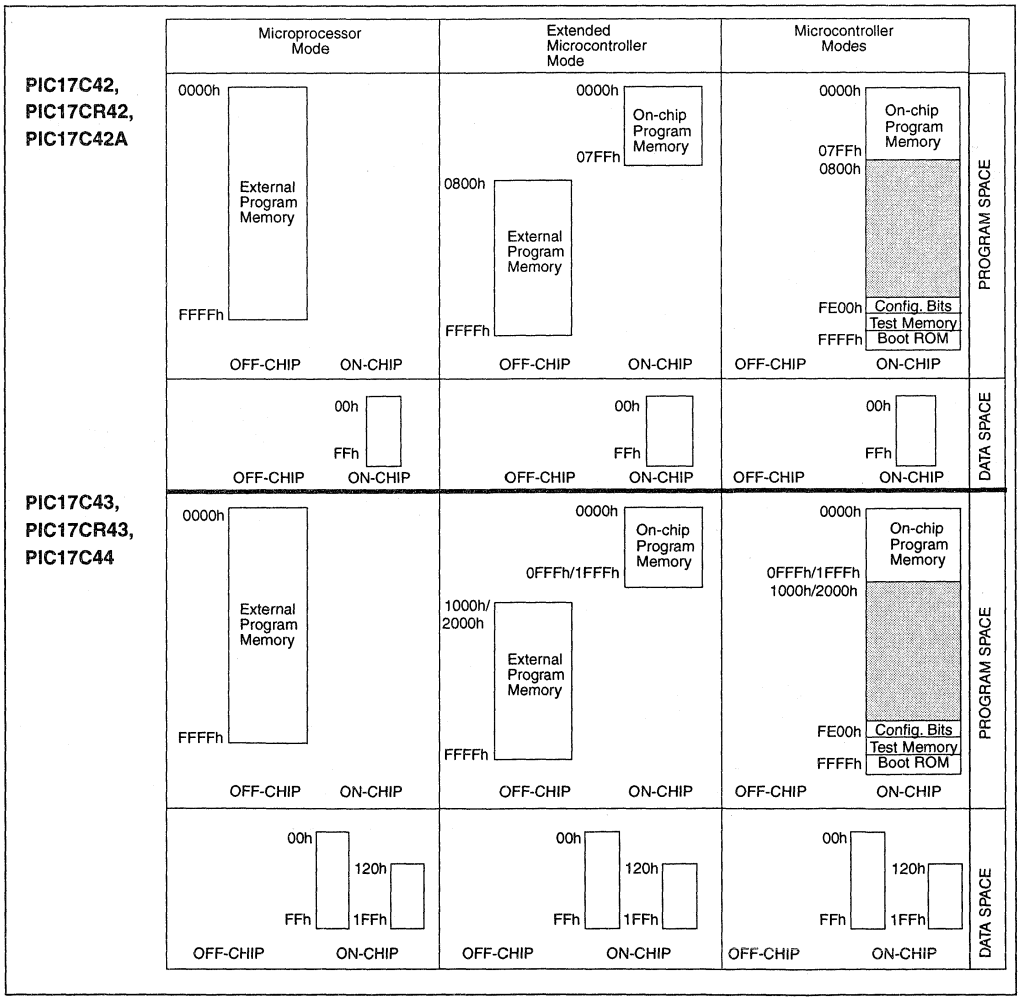
TABLE 6-1: MODE MEMORY ACCESS

Operating Mode	Internal Program Memory	Configuration Bits, Test Memory, Boot ROM
Microprocessor	No Access	No Access
Microcontroller	Access	Access
Extended Microcontroller	Access	No Access
Protected Microcontroller	Access	Access

The PIC17C4X can operate in modes where the program memory is off-chip. They are the microprocessor and extended microcontroller modes. The microprocessor mode is the default for an unprogrammed device.

Regardless of the processor mode, data memory is always on-chip.

FIGURE 6-2: MEMORY MAP IN DIFFERENT MODES



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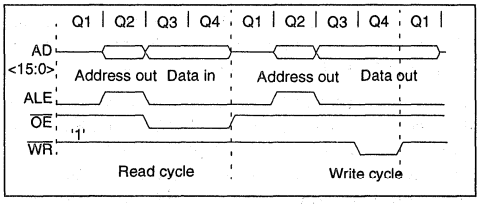
6.1.2 EXTERNAL MEMORY INTERFACE

When either microprocessor or extended microcontroller mode is selected, PORTC, PORTD and PORTE are configured as the system bus. PORTC and PORTD are the multiplexed address/data bus and PORTE is for the control signals. External components are needed to demultiplex the address and data. This can be done as shown in Figure 6-4. The waveforms of address and data are shown in Figure 6-3. For complete timings, please refer to the electrical specification section.

FIGURE 6-3: EXTERNAL PROGRAM MEMORY ACCESS WAVEFORMS



The system bus requires that there is no bus conflict (minimal leakage), so the output value (address) will be capacitively held at the desired value.

As the speed of the processor increases, external EPROM memory with faster access time must be used. Table 6-2 lists external memory speed requirements for a given PIC17C4X device frequency.

In extended microcontroller mode, when the device is executing out of internal memory, the control signals will continue to be active. That is, they indicate the action that is occurring in the internal memory. The external memory access is ignored.

This following selection is for use with Microchip EPROMs. For interfacing to other manufacturers memory, please refer to the electrical specifications of the desired PIC17C4X device, as well as the desired memory device to ensure compatibility.

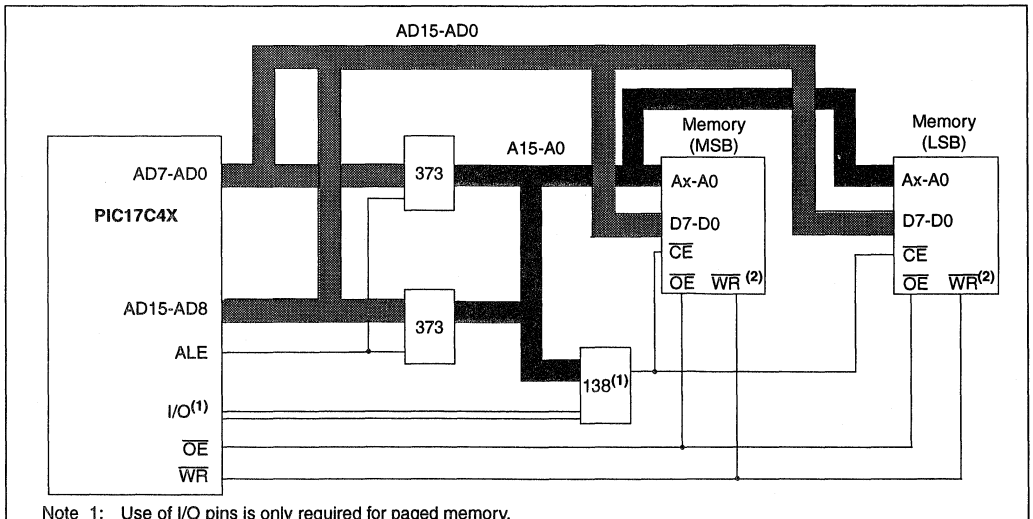
TABLE 6-2: EPROM MEMORY ACCESS TIME ORDERING SUFFIX

PIC17C4X Oscillator Frequency	Instruction Cycle Time (TCY)	EPROM Suffix	
		PIC17C42	PIC17C43 PIC17C44
8 MHz	500 ns	-25	-25
16 MHz	250 ns	-12	-15
20 MHz	200 ns	-90	-10
25 MHz	160 ns	N.A.	-70
33 MHz	121 ns	N.A.	(1)

Note 1: The access times for this requires the use of fast SRAMS.

Note: The external memory interface is not supported for the LC devices.

FIGURE 6-4: TYPICAL EXTERNAL PROGRAM MEMORY CONNECTION DIAGRAM



Note 1: Use of I/O pins is only required for paged memory.
2: This signal is unused for ROM and EPROM devices.

6.2 Data Memory Organization

Data memory is partitioned into two areas. The first is the General Purpose Registers (GPR) area, while the second is the Special Function Registers (SFR) area. The SFRs control the operation of the device.

Portions of data memory are banked, this is for both areas. The GPR area is banked to allow greater than 232 bytes of general purpose RAM. SFRs are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the Bank Select Register (BSR). If an access is made to a location outside this banked region, the BSR bits are ignored. Figure 6-5 shows the data memory map organization for the PIC17C42 and Figure 6-6 for all of the other PIC17C4X devices.

Instructions `MOVPF` and `MOVFP` provide the means to move values from the peripheral area ("P") to any location in the register file ("F"), and vice-versa. The definition of the "P" range is from 0h to 1Fh, while the "F" range is 0h to FFh. The "P" range has six more locations than peripheral registers (eight locations for the PIC17C42 device) which can be used as General Purpose Registers. This can be useful in some applications where variables need to be copied to other locations in the general purpose RAM (such as saving status information during an interrupt).

The entire data memory can be accessed either directly or indirectly through file select registers FSR0 and FSR1 (Section 6.4). Indirect addressing uses the appropriate control bits of the BSR for accesses into the banked areas of data memory. The BSR is explained in greater detail in Section 6.8.

6.2.1 GENERAL PURPOSE REGISTER (GPR)

All devices have some amount of GPR area. The GPRs are 8-bits wide. When the GPR area is greater than 232, it must be banked to allow access to the additional memory space.

Only the PIC17C43 and PIC17C44 devices have banked memory in the GPR area. To facilitate switching between these banks, the `MOVLR bank` instruction has been added to the instruction set. GPRs are not initialized by a Power-on Reset and are unchanged on all other resets.

6.2.2 SPECIAL FUNCTION REGISTERS (SFR)

The SFRs are used by the CPU and peripheral functions to control the operation of the device (Figure 6-5 and Figure 6-6). These registers are static RAM.

The SFRs can be classified into two sets, those associated with the "core" function and those related to the peripheral functions. Those registers related to the "core" are described here, while those related to a peripheral feature are described in the section for each peripheral feature.

The peripheral registers are in the banked portion of memory, while the core registers are in the unbanked region. To facilitate switching between the peripheral banks, the `MOVLB bank` instruction has been provided.

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FIGURE 6-5: PIC17C42 REGISTER FILE MAP

Addr	Unbanked			
00h	INDF0			
01h	FSR0			
02h	PCL			
03h	PCLATH			
04h	ALUSTA			
05h	T0STA			
06h	CPUSTA			
07h	INTSTA			
08h	INDF1			
09h	FSR1			
0Ah	WREG			
0Bh	TMR0L			
0Ch	TMR0H			
0Dh	TBLPTRL			
0Eh	TBLPTRH			
0Fh	BSR			
	Bank 0	**Bank 1 (1)**	**Bank 2 (1)**	**Bank 3 (1)**
10h	PORTA	DDRC	TMR1	PW1DCL
11h	DDRB	PORTC	TMR2	PW2DCL
12h	PORTB	DDRD	TMR3L	PW1DCH
13h	RCSTA	PORTD	TMR3H	PW2DCH
14h	RCREG	DDRE	PR1	CA2L
15h	TXSTA	PORTE	PR2	CA2H
16h	TXREG	PIR	PR3L/CA1L	TCON1
17h	SPBRG	PIE	PR3H/CA1H	TCON2
18h 1Fh	General Purpose RAM			
20h FFh				

Note 1: SFR file locations 10h - 17h are banked. All other SFRs ignore the Bank Select Register (BSR) bits.

FIGURE 6-6: PIC17CR42/42A/43/R43/44 REGISTER FILE MAP

Addr	Unbanked			
00h	INDF0			
01h	FSR0			
02h	PCL			
03h	PCLATH			
04h	ALUSTA			
05h	T0STA			
06h	CPUSTA			
07h	INTSTA			
08h	INDF1			
09h	FSR1			
0Ah	WREG			
0Bh	TMR0L			
0Ch	TMR0H			
0Dh	TBLPTRL			
0Eh	TBLPTRH			
0Fh	BSR			
	Bank 0	**Bank 1 (1)**	**Bank 2 (1)**	**Bank 3 (1)**
10h	PORTA	DDRC	TMR1	PW1DCL
11h	DDRB	PORTC	TMR2	PW2DCL
12h	PORTB	DDRD	TMR3L	PW1DCH
13h	RCSTA	PORTD	TMR3H	PW2DCH
14h	RCREG	DDRE	PR1	CA2L
15h	TXSTA	PORTE	PR2	CA2H
16h	TXREG	PIR	PR3L/CA1L	TCON1
17h	SPBRG	PIE	PR3H/CA1H	TCON2
18h	PRODL			
19h	PRODH			
1Ah 1Fh	General Purpose RAM (2)			
20h FFh		General Purpose RAM (2)		

Note 1: SFR file locations 10h - 17h are banked. All other SFRs ignore the Bank Select Register (BSR) bits.

2: General Purpose Registers (GPR) locations 20h - FFh and 120h - 1FFh are banked. All other GPRs ignore the Bank Select Register (BSR) bits.

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TABLE 6-3: SPECIAL FUNCTION REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (3)
Unbanked											
00h	INDF0	Uses contents of FSR0 to address data memory (not a physical register)								---- ----	---- ----
01h	FSR0	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
02h	PCL	Low order 8-bits of PC								0000 0000	0000 0000
03h(1)	PCLATH	Holding register for upper 8-bits of PC								0000 0000	uuuu uuuu
04h	ALUSTA	FS3	FS2	FS1	FS0	OV	Z	DC	C	1111 xxxx	1111 uuuu
05h	T0STA	INTEDG	T0SE	T0CS	PS3	PS2	PS1	PS0	—	0000 000-	0000 000-
06h(2)	CPUSTA	—	—	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	—	—	--11 11--	--11 qq--
07h	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
08h	INDF1	Uses contents of FSR1 to address data memory (not a physical register)								---- ----	---- ----
09h	FSR1	Indirect data memory address pointer 1								xxxx xxxx	uuuu uuuu
0Ah	WREG	Working register								xxxx xxxx	uuuu uuuu
0Bh	TMR0L	TMR0 register; low byte								xxxx xxxx	uuuu uuuu
0Ch	TMR0H	TMR0 register; high byte								xxxx xxxx	uuuu uuuu
0Dh	TBLPTRL	Low byte of program memory table pointer								(4)	(4)
0Eh	TBLPTRH	High byte of program memory table pointer								(4)	(4)
0Fh	BSR	Bank select register								0000 0000	0000 0000
Bank 0											
10h	PORTA	$\overline{RBPU}$	—	RA5	RA4	RA3	RA2	RA1/T0CKI	RA0/INT	0-xx xxxx	0-uu uuuu
11h	DDRB	Data direction register for PORTB								1111 1111	1111 1111
12h	PORTB	PORTB data latch								xxxx xxxx	uuuu uuuu
13h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h	RCREG	Serial port receive register								xxxx xxxx	uuuu uuuu
15h	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
16h	TXREG	Serial port transmit register								xxxx xxxx	uuuu uuuu
17h	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu
Bank 1											
10h	DDRC	Data direction register for PORTC								1111 1111	1111 1111
11h	PORTC	RC7/ AD7	RC6/ AD6	RC5/ AD5	RC4/ AD4	RC3/ AD3	RC2/ AD2	RC1/ AD1	RC0/ AD0	xxxx xxxx	uuuu uuuu
12h	DDRD	Data direction register for PORTD								1111 1111	1111 1111
13h	PORTD	RD7/ AD15	RD6/ AD14	RD5/ AD13	RD4/ AD12	RD3/ AD11	RD2/ AD10	RD1/ AD9	RD0/ AD8	xxxx xxxx	uuuu uuuu
14h	DDRE	Data direction register for PORTE								---- -111	---- -111
15h	PORTE	—	—	—	—	—	RE2/$\overline{WR}$	RE1/$\overline{OE}$	RE0/ALE	---- -xxx	---- -uuu
16h	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q - value depends on condition. Shaded cells are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<15:8> whose contents are updated from or transferred to the upper byte of the program counter.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in CPUSTA are not affected by a MCLR reset.

3: Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset.

4: The following values are for both TBLPTRL and TBLPTRH:
All PIC17C4X devices (Power-on Reset 0000 0000) and (All other resets 0000 0000)
except the PIC17C42 (Power-on Reset xxxx xxxx) and (All other resets uuuu uuuu)

5: The PRODL and PRODH registers are not implemented on the PIC17C42.

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TABLE 6-3: SPECIAL FUNCTION REGISTERS (Cont.'d)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (3)
Bank 2											
10h	TMR1	Timer1								xxxx xxxx	uuuu uuuu
11h	TMR2	Timer2								xxxx xxxx	uuuu uuuu
12h	TMR3L	TMR3 register; low byte								xxxx xxxx	uuuu uuuu
13h	TMR3H	TMR3 register; high byte								xxxx xxxx	uuuu uuuu
14h	PR1	Timer1 period register								xxxx xxxx	uuuu uuuu
15h	PR2	Timer2 period register								xxxx xxxx	uuuu uuuu
16h	PR3L/CA1L	Timer3 period register, low byte/capture1 register; low byte								xxxx xxxx	uuuu uuuu
17h	PR3H/CA1H	Timer3 period register, high byte/capture1 register; high byte								xxxx xxxx	uuuu uuuu
Bank 3											
10h	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx-- ----	uu-- ----
11h	PW2DCL	DC1	DC0	TM2PW2	—	—	—	—	—	xx0- ----	uu0- ----
12h	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
14h	CA2L	Capture2 low byte								xxxx xxxx	uuuu uuuu
15h	CA2H	Capture2 high byte								xxxx xxxx	uuuu uuuu
16h	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{PR3}$	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
Unbanked											
18h(5)	PRODL	Low Byte of 16-bit Product (8 x 8 Hardware Multiply)								xxxx xxxx	uuuu uuuu
19h(5)	PRODH	High Byte of 16-bit Product (8 x 8 Hardware Multiply)								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q - value depends on condition. Shaded cells are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<15:8> whose contents are updated from or transferred to the upper byte of the program counter.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in CPUSTA are not affected by a MCLR reset.

3: Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset.

4: The following values are for both TBLPTRL and TBLPTRH:
All PIC17C4X devices (Power-on Reset 0000 0000) and (All other resets 0000 0000)
except the PIC17C42 (Power-on Reset xxxx xxxx) and (All other resets uuuu uuuu)

5: The PRODL and PRODH registers are not implemented on the PIC17C42.

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6.2.2.1 ALU STATUS REGISTER (ALUSTA)

The ALUSTA register contains the status bits of the Arithmetic and Logic Unit and the mode control bits for the indirect addressing register.

As with all the other registers, the ALUSTA register can be the destination for any instruction. If the ALUSTA register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the ALUSTA register as destination may be different than intended.

For example, CLRF ALUSTA will clear the upper four bits and set the Z bit. This leaves the ALUSTA register as 0000u1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions be used to alter the ALUSTA register because these instructions do not affect any status bit. To see how other instructions affect the status bits, see the "Instruction Set Summary."

Note 1: The C and DC bits operate as a $\overline{\text{borrow}}$ out bit in subtraction. See the SUBLW and SUBWF instructions for examples.

Note 2: The overflow bit will be set if the 2's complement result exceeds +127 or is less than -128.

Arithmetic and Logic Unit (ALU) is capable of carrying out arithmetic or logical operations on two operands or a single operand. All single operand instructions operate either on the WREG register or a file register. For two operand instructions, one of the operands is the WREG register and the other one is either a file register or an 8-bit immediate constant.

FIGURE 6-7: ALUSTA REGISTER (ADDRESS: 04h, UNBANKED)

R/W - 1	R/W - 1	R/W - 1	R/W - 1	R/W - x	R/W - x	R/W - x	R/W - x
FS3	FS2	FS1	FS0	OV	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
-n = Value at POR reset
(x = unknown)

bit 7-6: **FS3:FS2**: FSR1 Mode Select bits
00 = Post auto-decrement FSR1 value
01 = Post auto-increment FSR1 value
1x = FSR1 value does not change

bit 5-4: **FS1:FS0**: FSR0 Mode Select bits
00 = Post auto-decrement FSR0 value
01 = Post auto-increment FSR0 value
1x = FSR0 value does not change

bit 3: **OV**: Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude, which causes the sign bit (bit7) to change state.
1 = Overflow occurred for signed arithmetic, (in this arithmetic operation)
0 = No overflow occurred

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The results of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{\text{borrow}}$ bit
For ADDWF and ADDLW instructions.
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result
Note: For borrow the polarity is reversed.

bit 0: **C**: carry/$\overline{\text{borrow}}$ bit
For ADDWF and ADDLW instructions.
1 = A carry-out from the most significant bit of the result occurred
Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRCF, RLCF) instructions, this bit is loaded with either the high or low order bit of the source register.
0 = No carry-out from the most significant bit of the result
Note: For borrow the polarity is reversed.

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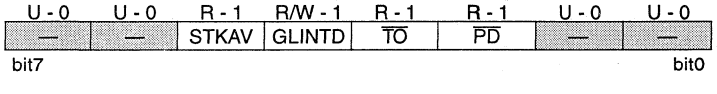
6.2.2.2 CPU STATUS REGISTER (CPUSTA)

The CPUSTA register contains the status and control bits for the CPU. This register is used to globally enable/disable interrupts. If only a specific interrupt is desired to be enabled/disabled, please refer to the INTerrupt STAtus (INTSTA) register and the Peripheral Interrupt Enable (PIE) register. This register also indicates if the stack is available and contains the Power-down ($\overline{PD}$) and Time-out ($\overline{TO}$) bits. The $\overline{TO}$, $\overline{PD}$, and STKAV bits are not writable. These bits are set and cleared according to device logic. Therefore, the result of an instruction with the CPUSTA register as destination may be different than intended.

FIGURE 6-8: CPUSTA REGISTER (ADDRESS: 06h, UNBANKED)



R = Readable bit
W = Writable bit
U = Unimplemented bit, Read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented**: Read as '0'

bit 5: **STKAV**: Stack Available bit
This bit indicates that the 4-bit stack pointer value is Fh, or has rolled over from Fh → 0h (stack overflow).
1 = Stack is available
0 = Stack is full, or a stack overflow may have occurred (Once this bit has been cleared by a stack overflow, only a device reset will set this bit)

bit 4: **GLINTD**: Global Interrupt Disable bit
This bit disables all interrupts. When enabling interrupts, only the sources with their enable bits set can cause an interrupt.
1 = Disable all interrupts
0 = Enables all un-masked interrupts

bit 3: $\overline{TO}$: WDT Time-out Status bit
1 = After power-up or by a `CLRWDT` instruction
0 = A Watchdog Timer time-out occurred

bit 2: $\overline{PD}$: Power-down Status bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 1-0: **Unimplemented**: Read as '0'

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6.2.2.3 TMR0 STATUS/CONTROL REGISTER (T0STA)

This register contains various control bits. Bit7 (INTEDG) is used to control the edge upon which a signal on the RA0/INT pin will set the RB0/INT interrupt flag. The other bits configure the Timer0 prescaler and clock source. (Figure 11-1).

FIGURE 6-9: T0STA REGISTER (ADDRESS: 05h, UNBANKED)

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	U - 0
INTEDG	T0SE	T0CS	PS3	PS2	PS1	PS0	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, reads as '0'
-n = Value at POR reset

bit 7: **INTEDG**: RA0/INT Pin Interrupt Edge Select bit
This bit selects the edge upon which the interrupt is detected.
1 = Rising edge of RA0/INT pin generates interrupt
0 = Falling edge of RA0/INT pin generates interrupt

bit 6: **T0SE**: Timer0 Clock Input Edge Select bit
This bit selects the edge upon which TMR0 will increment.
When T0CS = 0
1 = Rising edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
0 = Falling edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
When T0CS = 1
Don't care

bit 5: **T0CS**: Timer0 Clock Source Select bit
This bit selects the clock source for Timer0.
1 = Internal instruction clock cycle (TCY)
0 = T0CKI pin

bit 4-1: **PS3:PS0**: Timer0 Prescale Selection bits
These bits select the prescale value for Timer0.

PS3:PS0	Prescale Value
0000	1:1
0001	1:2
0010	1:4
0011	1:8
0100	1:16
0101	1:32
0110	1:64
0111	1:128
1xxx	1:256

bit 0: **Unimplemented**: Read as '0'

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6.3 Stack Operation

The PIC17C4X devices have a 16 x 16-bit wide hardware stack (Figure 6-1). The stack is not part of either the program or data memory space, and the stack pointer is neither readable nor writable. The PC is "PUSHed" onto the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is "POPed" in the event of a RETURN, RETLW, or a RETFIE instruction execution. PCLATH is not affected by a "PUSH" or a "POP" operation.

The stack operates as a circular buffer, with the stack pointer initialized to '0' after all resets. There is a stack available bit (STKAV) to allow software to ensure that the stack has not overflowed. The STKAV bit is set after a device reset. When the stack pointer equals Fh, STKAV is cleared. When the stack pointer rolls over from Fh to 0h, the STKAV bit will be held clear until a device reset.

Note 1: There is not a status bit for stack underflow. The STKAV bit can be used to detect the underflow which results in the stack pointer being at the top of stack.

Note 2: There are no instruction mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt vector.

Note 3: After a reset, if a "POP" operation occurs before a "PUSH" operation, the STKAV bit will be cleared. This will appear as if the stack is full (underflow has occurred). If a "PUSH" operation occurs next (before another "POP"), the STKAV bit will be locked clear. Only a device reset will cause this bit to set.

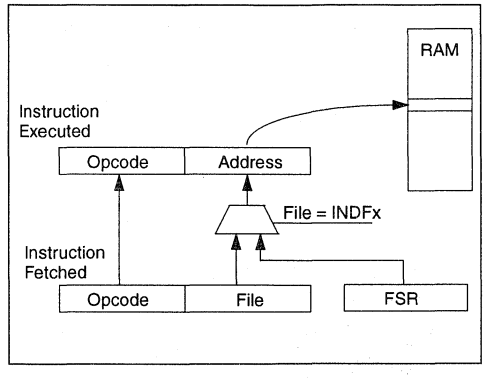
After the device is "PUSHed" sixteen times (without a "POP"), the seventeenth push overwrites the value from the first push. The eighteenth push overwrites the second push (and so on).

6.4 Indirect Addressing

Indirect addressing is a mode of addressing data memory where the data memory address in the instruction is not fixed. That is, the register that is to be read or written can be modified by the program. This can be useful for data tables in the data memory. Figure 6-10 shows the operation of indirect addressing. This shows the moving of the value to the data memory address specified by the value of the FSR register.

Example 6-1 shows the use of indirect addressing to clear RAM in a minimum number of instructions. A similar concept could be used to move a defined number of bytes (block) of data to the USART transmit register (TXREG). The starting address of the block of data to be transmitted could easily be modified by the program.

FIGURE 6-10: INDIRECT ADDRESSING



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6.4.1 INDIRECT ADDRESSING REGISTERS

The PIC17C4X has four registers for indirect addressing. These registers are:

- INDF0 and FSR0
- INDF1 and FSR1

Registers INDF0 and INDF1 are not physically implemented. Reading or writing to these registers activates indirect addressing, with the value in the corresponding FSR register being the address of the data. The FSR is an 8-bit register and allows addressing anywhere in the 256-byte data memory address range. For banked memory, the bank of memory accessed is specified by the value in the BSR.

If file INDF0 (or INDF1) itself is read indirectly via an FSR, all '0's are read (Zero bit is set). Similarly, if INDF0 (or INDF1) is written to indirectly, the operation will be equivalent to a NOP, and the status bits are not affected.

6.4.2 INDIRECT ADDRESSING OPERATION

The indirect addressing capability has been enhanced over that of the PIC16CXX family. There are two control bits associated with each FSR register. These two bits configure the FSR register to:

- Auto-decrement the value (address) in the FSR after an indirect access
- Auto-increment the value (address) in the FSR after an indirect access
- No change to the value (address) in the FSR after an indirect access

These control bits are located in the ALUSTA register. The FSR1 register is controlled by the FS3:FS2 bits and FSR0 is controlled by the FS1:FS0 bits.

When using the auto-increment or auto-decrement features, the effect on the FSR is not reflected in the ALUSTA register. For example, if the indirect address causes the FSR to equal '0', the Z bit will not be set.

If the FSR register contains a value of 0h, an indirect read will read 0h (Zero bit is set) while an indirect write will be equivalent to a NOP (status bits are not affected).

Indirect addressing allows single cycle data transfers within the entire data space. This is possible with the use of the MOVPF and MOVFP instructions, where either 'p' or 'f' is specified as INDF0 (or INDF1).

If the source or destination of the indirect address is in banked memory, the location accessed will be determined by the value in the BSR.

A simple program to clear RAM from 20h - FFh is shown in Example 6-1.

EXAMPLE 6-1: INDIRECT ADDRESSING

```
    MOVLW   0x20          ;
    MOVWF   FSR0          ; FSR0 = 20h
    BCF     ALUSTA, FS1   ; Increment FSR
    BSF     ALUSTA, FS0   ; after access
    BCF     ALUSTA, C     ; C = 0
    MOVLW   END_RAM + 1   ;
LP  CLRF    INDF0         ; Addr(FSR) = 0
    CPFSEQ  FSR0          ; FSR0 = END_RAM+1?
    GOTO    LP            ; NO, clear next
    :                     ; YES, All RAM is
    :                     ; cleared
```

6.5 Table Pointer (TBLPTRL and TBLPTRH)

File registers TBLPTRL and TBLPTRH form a 16-bit pointer to address the 64K program memory space. The table pointer is used by instructions TABLWT and TABLRD.

The TABLRD and the TABLWT instructions allow transfer of data between program and data space. The table pointer serves as the 16-bit address of the data word within the program memory. For a more complete description of these registers and the operation of Table Reads and Table Writes, see Section 7.0.

6.6 Table Latch (TBLATH, TBLATL)

The table latch (TBLAT) is a 16-bit register, with TBLATH and TBLATL referring to the high and low bytes of the register. It is not mapped into data or program memory. The table latch is used as a temporary holding latch during data transfer between program and data memory (see descriptions of instructions TABLRD, TABLWT, TLRD and TLWT). For a more complete description of these registers and the operation of Table Reads and Table Writes, see Section 7.0.

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6.7 Program Counter Module

The Program Counter (PC) is a 16-bit register. PCL, the low byte of the PC, is mapped in the data memory. PCL is readable and writable just as is any other register. PCH is the high byte of the PC and is not directly addressable. Since PCH is not mapped in data or program memory, an 8-bit register PCLATH (PC high latch) is used as a holding latch for the high byte of the PC. PCLATH is mapped into data memory. The user can read or write PCH through PCLATH.

The 16-bit wide PC is incremented after each instruction fetch during Q1 unless:

- Modified by GOTO, CALL, LCALL, RETURN, RETLW, or RETFIE instruction
- Modified by an interrupt response
- Due to destination write to PCL by an instruction

"Skips" are equivalent to a forced NOP cycle at the skipped address.

Figure 6-11 and Figure 6-12 show the operation of the program counter for various situations.

FIGURE 6-11: PROGRAM COUNTER OPERATION

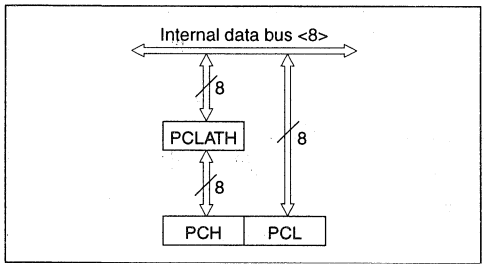
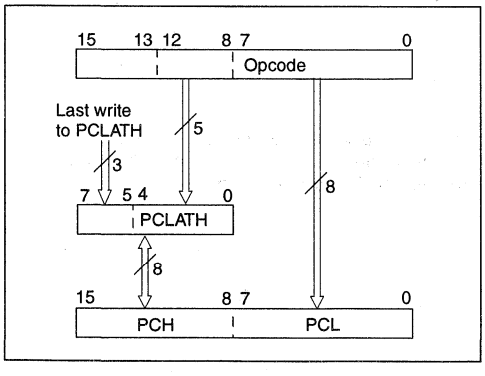


FIGURE 6-12: PROGRAM COUNTER USING THE CALL AND GOTO INSTRUCTIONS



Using Figure 6-11, the operations of the PC and PCLATH for different instructions are as follows:

a) LCALL instructions:
   An 8-bit destination address is provided in the instruction (opcode). PCLATH is unchanged.
   PCLATH → PCH
   Opcode<7:0> → PCL

b) Read instructions on PCL:
   Any instruction that reads PCL.
   PCL → data bus → ALU or destination
   PCH → PCLATH

c) Write instructions on PCL:
   Any instruction that writes to PCL.
   8-bit data → data bus → PCL
   PCLATH → PCH

d) Read-Modify-Write instructions on PCL:
   Any instruction that does a read-write-modify operation on PCL, such as ADDWF PCL.
   Read: PCL → data bus → ALU
   Write: 8-bit result → data bus → PCL
   PCLATH → PCH

e) RETURN instruction:
   PCH → PCLATH
   Stack<MRU> → PC<15:0>

Using Figure 6-12, the operation of the PC and PCLATH for GOTO and CALL instructions is a follows:

CALL, GOTO instructions:
A 13-bit destination address is provided in the instruction (opcode).
Opcode<12:0> → PC <12:0>
PC<15:13> → PCLATH<7:5>
Opcode<12:8> → PCLATH <4:0>

The read-modify-write only affects the PCL with the result. PCH is loaded with the value in the PCLATH. For example, ADDWF PCL will result in a jump within the current page. If PC = 03F0h, WREG = 30h and PCLATH = 03h before instruction, PC = 0320h after the instruction. To accomplish a true 16-bit computed jump, the user needs to compute the 16-bit destination address, write the high byte to PCLATH and then write the low value to PCL.

The following PC related operations do not change PCLATH:

a) LCALL, RETLW, and RETFIE instructions.
b) Interrupt vector is forced onto the PC.
c) Read-modify-write instructions on PCL (e.g. BSF PCL).

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6.8 Bank Select Register (BSR)

The BSR is used to switch between banks in the data memory area (Figure 6-13). In the PIC17C42, PIC17CR42, and PIC17C42A only the lower nibble is implemented. While in the PIC17C43, PIC17CR43, and PIC17C44 devices, the entire byte is implemented. The lower nibble is used to select the peripheral register bank. The upper nibble is used to select the general purpose memory bank.

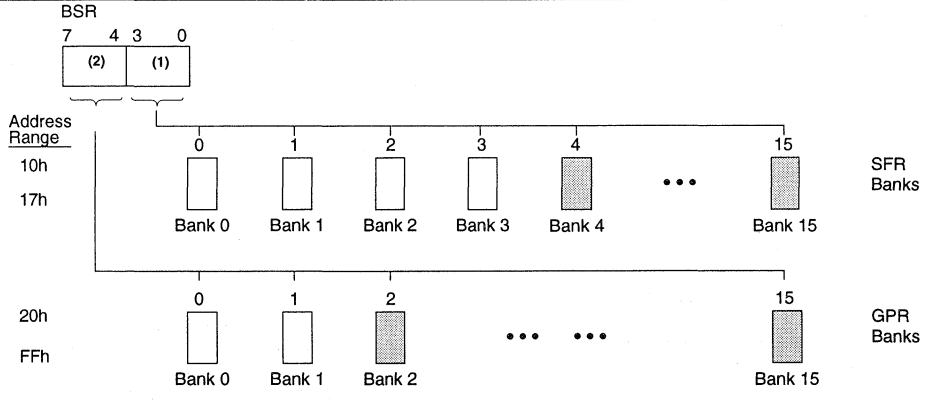
All the Special Function Registers (SFRs) are mapped into the data memory space. In order to accommodate the large number of registers, a banking scheme has been used. A segment of the SFRs, from address 10h to address 17h, is banked. The lower nibble of the bank select register (BSR) selects the currently active "peripheral bank." Effort has been made to group the peripheral registers of related functionality in one bank. However, it will still be necessary to switch from bank to bank in order to address all peripherals related to a single task. To assist this, a `MOVLB bank` instruction is in the instruction set.

For the PIC17C43, PIC17CR43, and PIC17C44 devices, the need for a large general purpose memory space dictated a general purpose RAM banking scheme. The upper nibble of the BSR selects the currently active general purpose RAM bank. To assist this, a `MOVLR bank` instruction has been provided in the instruction set.

If the currently selected bank is not implemented (such as Bank 13), any read will read all '0's. Any write is completed to the bit bucket and the ALU status bits will be set/cleared as appropriate.

Note:	Registers in Bank 15 in the Special Function Register area, are reserved for Microchip use. Reading of registers in this bank may cause random values to be read.

FIGURE 6-13: BSR OPERATION (PIC17C43/R43/44)



Note 1: Only Banks 0 through Bank 3 are implemented. Selection of an unimplemented bank is not recommended.
Bank 15 is reserved for Microchip use, reading of registers in this bank may cause random values to be read.
2: Only Banks 0 and Bank 1 are implemented. Selection of an unimplemented bank is not recommended.

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7.0 TABLE READS AND TABLE WRITES

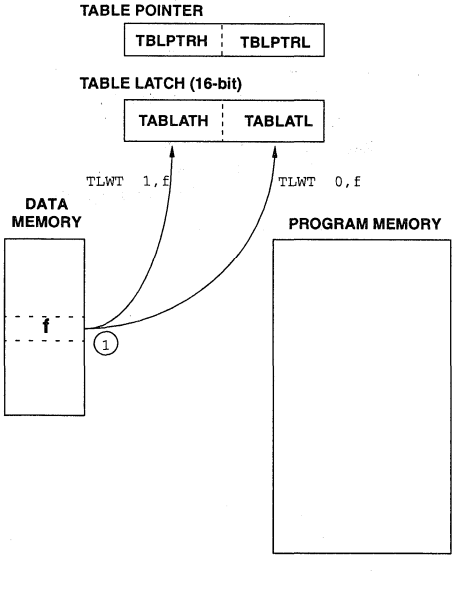
The PIC17C4X has four instructions that allow the processor to move data from the data memory space to the program memory space, and vice versa. Since the program memory space is 16-bits wide and the data memory space is 8-bits wide, two operations are required to move 16-bit values to/from the data memory.

The `TLWT t,f` and `TABLWT t,i,f` instructions are used to write data from the data memory space to the program memory space. The `TLRD t,f` and `TABLRD t,i,f` instructions are used to write data from the program memory space to the data memory space.

The program memory can be internal or external. For the program memory access to be external, the device needs to be operating in extended microcontroller or microprocessor mode.

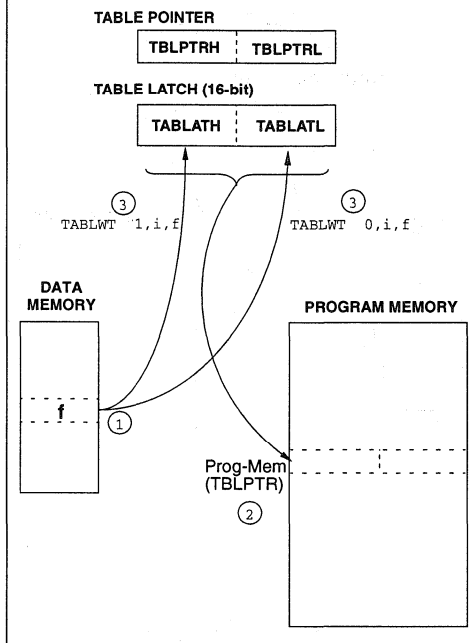
Figure 7-1 through Figure 7-4 show the operation of these four instructions.

FIGURE 7-1: TLWT INSTRUCTION OPERATION



Note 1: 8-bit value, from register 'f', loaded into the high or low byte in TABLAT (16-bit).

FIGURE 7-2: TABLWT INSTRUCTION OPERATION



Note 1: 8-bit value, from register 'f', loaded into the high or low byte in TABLAT (16-bit).
2: 16-bit TABLAT value written to address Program Memory (TBLPTR).
3: If "i" = 1, then TBLPTR = TBLPTR + 1, If "i" = 0, then TBLPTR is unchanged.

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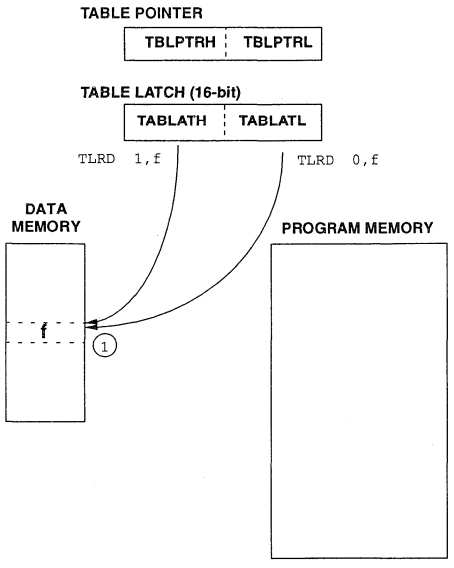
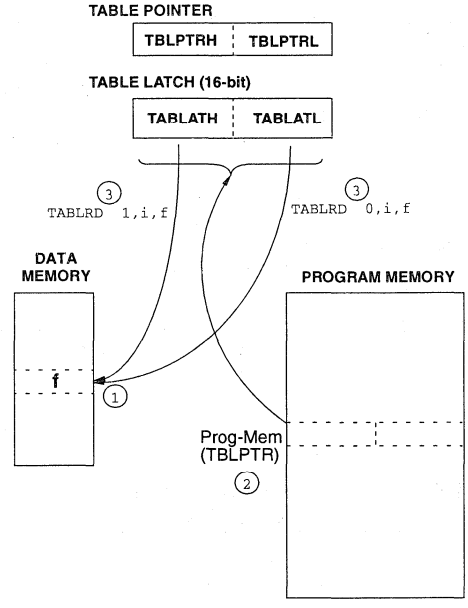
FIGURE 7-3: TLRD INSTRUCTION OPERATION



Note 1: 8-bit value, from TABLAT (16-bit) high or low byte, loaded into register 'f'.

FIGURE 7-4: TABLRD INSTRUCTION OPERATION



Note 1: 8-bit value, from TABLAT (16-bit) high or low byte, loaded into register 'f'.
2: 16-bit value at Program Memory (TBLPTR) loaded into TABLAT register.
3: If "i" = 1, then TBLPTR = TBLPTR + 1, If "i" = 0, then TBLPTR is unchanged.

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7.1 Table Writes to Internal Memory

A table write operation to internal memory causes a long write operation. The long write is necessary for programming the internal EPROM. Instruction execution is halted while in a long write cycle. The long write will be terminated by any enabled interrupt. To ensure that the EPROM location has been well programmed, a minimum programming time is required (see specification #D114). Having only one interrupt enabled to terminate the long write ensures that no unintentional interrupts will prematurely terminate the long write.

The sequence of events for programming an internal program memory location should be:

1. Disable all interrupt sources, except the source to terminate EPROM program write.
2. Raise $\overline{MCLR}/V_{PP}$ pin to the programming voltage.
3. Clear the WDT.
4. Do the table write. The interrupt will terminate the long write.
5. Verify the memory location (table read).

Note: Programming requirements must be met. See timing specification in electrical specifications for the desired device. Violating these specifications (including temperature) may result in EPROM locations that are not fully programmed and may lose their state over time.

7.1.1 TERMINATING LONG WRITES

An interrupt source or reset are the only events that terminate a long write operation. Terminating the long write from an interrupt source requires that the interrupt enable and flag bits are set. The GLINTD bit only enables the vectoring to the interrupt address.

If the T0CKI, RA0/INT, or TMR0 interrupt source is used to terminate the long write; the interrupt flag, of the highest priority enabled interrupt, will terminate the long write and automatically be cleared.

Note 1: If an interrupt is pending, the TABLWT is aborted (an NOP is executed). The highest priority pending interrupt, from the T0CKI, RA0/INT, or TMR0 sources that is enabled, has its flag cleared.

Note 2: If the interrupt is not being used for the program write timing, the interrupt should be disabled. This will ensure that the interrupt is not lost, nor will it terminate the long write prematurely.

If a peripheral interrupt source is used to terminate the long write, the interrupt enable and flag bits must be set. The interrupt flag will not be automatically cleared upon the vectoring to the interrupt vector address.

If the GLINTD bit is cleared prior to the long write, when the long write is terminated, the program will branch to the interrupt vector.

If the GLINTD bit is set prior to the long write, when the long write is terminated, the program will not vector to the interrupt address.

TABLE 7-1: INTERRUPT - TABLE WRITE INTERACTION

Interrupt Source	GLINTD	Enable Bit	Flag Bit	Action
RA0/INT, TMR0, T0CKI	0	1	1	Terminate long table write (to internal program memory), branch to interrupt vector (branch clears flag bit).
	0	1	0	None
	1	0	x	None
	1	1	1	Terminate table write, do not branch to interrupt vector (flag is automatically cleared).
Peripheral	0	1	1	Terminate table write, branch to interrupt vector.
	0	1	0	None
	1	0	x	None
	1	1	1	Terminate table write, do not branch to interrupt vector (flag is set).

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7.2 Table Writes to External Memory

Table writes to external memory are always two-cycle instructions. The second cycle writes the data to the external memory location. The sequence of events for an external memory write are the same for an internal write.

Note: If an interrupt is pending or occurs during the TABLWT, the two cycle table write completes. The RA0/INT, TMR0, or T0CKI interrupt flag is automatically cleared or the pending peripheral interrupt is acknowledged.

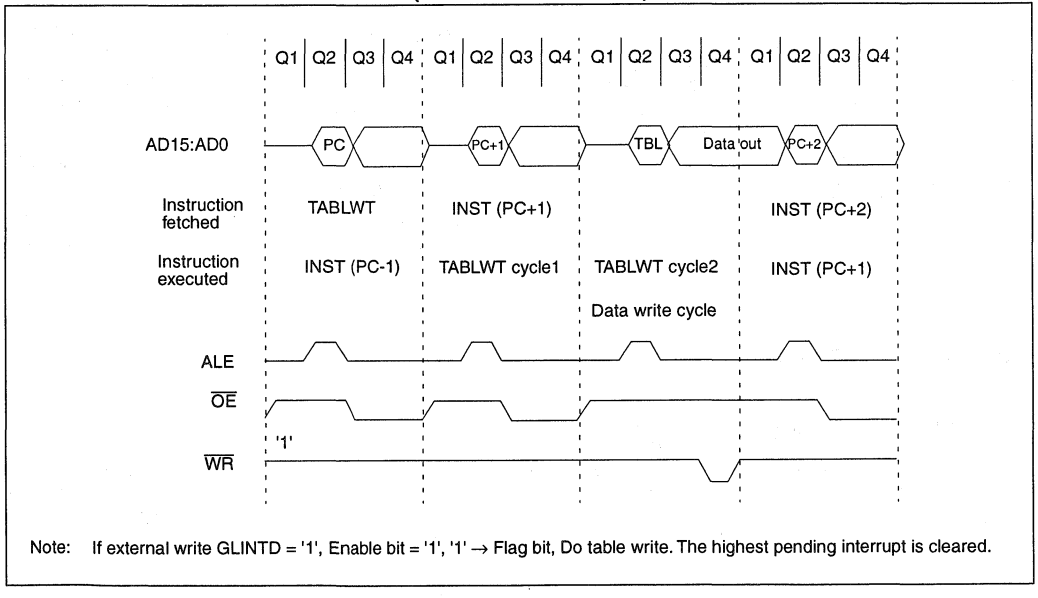
7.2.2 TABLE WRITE CODE

The "i" operand of the TABLWT instruction can specify that the value in the 16-bit TBLPTR register is automatically incremented for the next write. In Example 7-1, the TBLPTR register is not automatically incremented.

EXAMPLE 7-1: TABLE WRITE

```
CLRWDT                      ; Clear WDT
MOVLW   HIGH (TBL_ADDR)     ; Load the Table
MOVWF   TBLPTRH             ;   address
MOVLW   LOW (TBL_ADDR)      ;
MOVWF   TBLPTRL             ;
MOVLW   HIGH (DATA)         ; Load HI byte
TLWT    1, WREG             ;   in TABLATCH
MOVLW   LOW (DATA)          ; Load LO byte
TABLWT  0,0,WREG            ;   in TABLATCH
                            ;   and write to
                            ;   program memory
                            ;   (Ext. SRAM)
```

FIGURE 7-5: TABLWT WRITE TIMING (EXTERNAL MEMORY)



Note: If external write GLINTD = '1', Enable bit = '1', '1' → Flag bit, Do table write. The highest pending interrupt is cleared.

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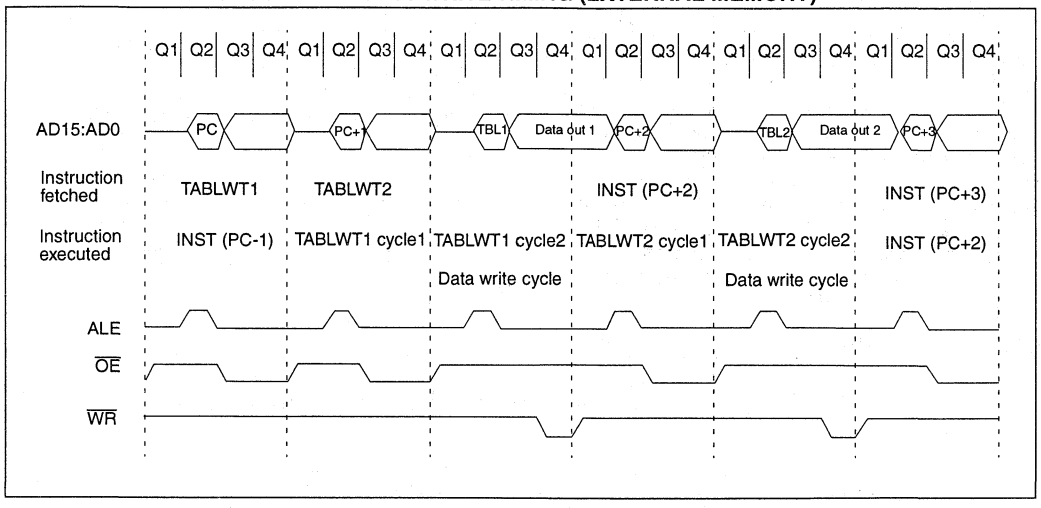
FIGURE 7-6: CONSECUTIVE TABLWT WRITE TIMING (EXTERNAL MEMORY)



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7.3 Table Reads

The table read allows the program memory to be read. This allows constant data to be stored in the program memory space, and retrieved into data memory when needed. Example 7-2 reads the 16-bit value at program memory address TBLPTR. After the dummy byte has been read from the TABLATH, the TABLATH is loaded with the 16-bit data from program memory address TBLPTR + 1. The first read loads the data into the latch, and can be considered a dummy read (unknown data loaded into 'f'). INDF0 should be configured for either auto-increment or auto-decrement.

EXAMPLE 7-2: TABLE READ

```
MOVLW   HIGH (TBL_ADDR) ; Load the Table
MOVWF   TBLPTRH         ;   address
MOVLW   LOW (TBL_ADDR)  ;
MOVWF   TBLPTRL         ;
TABLRD  0,0,DUMMY       ; Dummy read,
                        ;  Updates TABLATCH
TLRD    1, INDF0        ; Read HI byte
                        ;   of TABLATCH
TABLRD  0,1,INDF0       ; Read LO byte
                        ;   of TABLATCH and
                        ;   Update TABLATCH
```

FIGURE 7-7: TABLRD TIMING

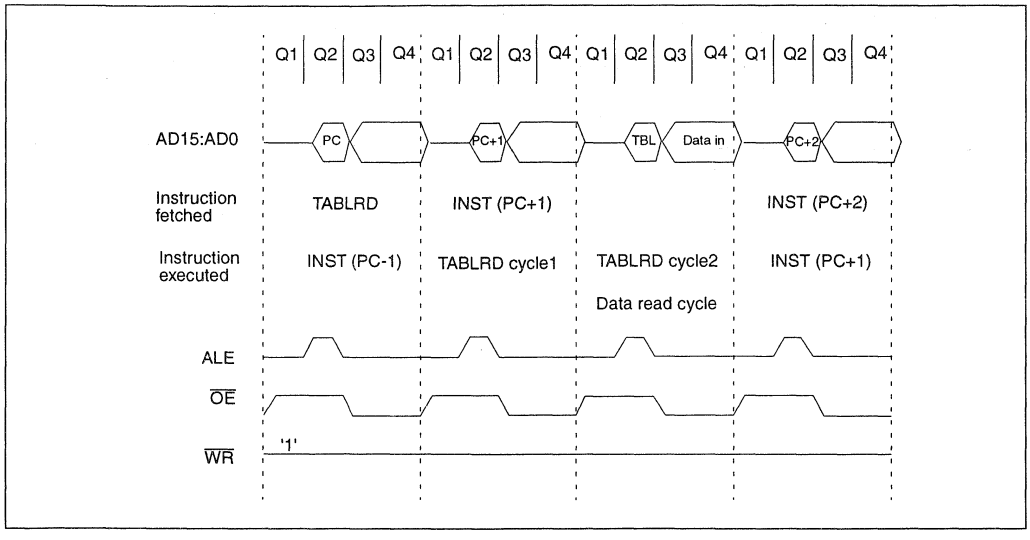
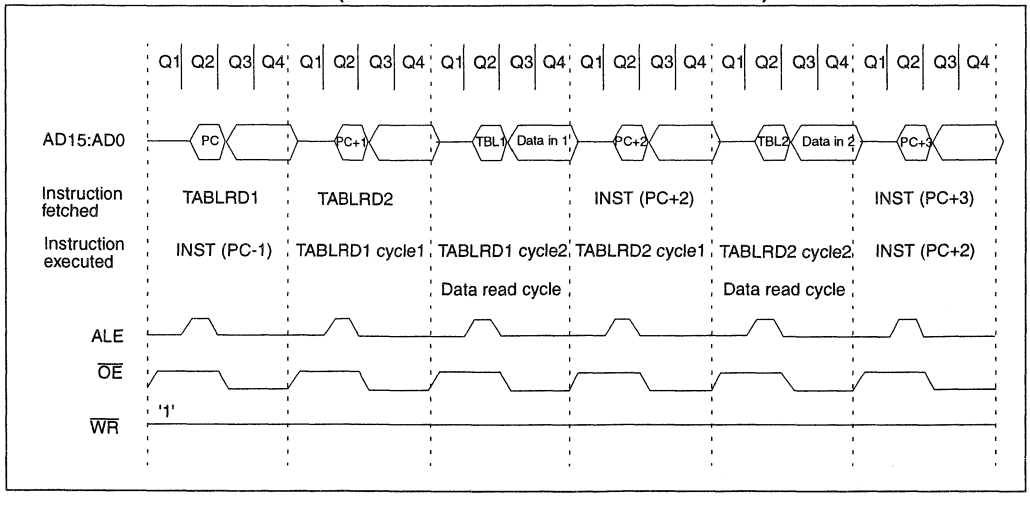


FIGURE 7-8: TABLRD TIMING (CONSECUTIVE TABLRD INSTRUCTIONS)



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8.0 HARDWARE MULTIPLIER

All PIC17C4X devices except the PIC17C42, have an 8 x 8 hardware multiplier included in the ALU of the device. By making the multiply a hardware operation, it completes in a single instruction cycle. This is an unsigned multiply that gives a 16-bit result. The result is stored into the 16-bit PRODuct register (PRODH:PRODL). The multiplier does not affect any flags in the ALUSTA register.

Making the 8 x 8 multiplier execute in a single cycle gives the following advantages:

- Higher computational throughput
- Reduces code size requirements for multiply algorithms

The performance increase allows the device to be used in applications previously reserved for Digital Signal Processors.

Table 8-1 shows a performance comparison between the PIC17C42 and all other PIC17CXX devices, which have the single cycle hardware multiply.

Example 8-1 shows the sequence to do an 8 x 8 unsigned multiply. Only one instruction is required when one argument of the multiply is already loaded in the WREG register.

Example 8-2 shows the sequence to do an 8 x 8 signed multiply. To account for the sign bits of the arguments, each argument's most significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 8-1: 8 x 8 MULTIPLY ROUTINE

```
MOVFP   ARG1, WREG
MULWF   ARG2            ; ARG1 * ARG2 ->
                        ;   PRODH:PRODL
```

EXAMPLE 8-2: 8 x 8 SIGNED MULTIPLY ROUTINE

```
MOVFP   ARG1, WREG
MULWF   ARG2            ; ARG1 * ARG2 ->
                        ;   PRODH:PRODL
BTFSC   ARG2, SB        ; Test Sign Bit
SUBWF   PRODH, F        ; PRODH = PRODH
                        ;         - ARG1
MOVFP   ARG2, WREG
BTFSC   ARG1, SB        ; Test Sign Bit
SUBWF   PRODH, F        ; PRODH = PRODH
                        ;         - ARG2
```

TABLE 8-1: PERFORMANCE COMPARISON

Routine	Device	Program Memory (Words)	Cycles (Max)	Time	
				@ 25 MHz	@ 33 MHz
8 x 8 unsigned	PIC17C42	13	69	11.04 µs	N/A
	All other PIC17CXX devices	1	1	160 ns	121 ns
8 x 8 signed	PIC17C42	—	—	—	N/A
	All other PIC17CXX devices	6	6	960 ns	727 ns
16 x 16 unsigned	PIC17C42	21	242	38.72 µs	N/A
	All other PIC17CXX devices	24	24	3.84 µs	2.91 µs
16 x 16 signed	PIC17C42	52	254	40.64 µs	N/A
	All other PIC17CXX devices	36	36	5.76 µs	4.36 µs

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Example 8-3 shows the sequence to do a 16 x 16 unsigned multiply. Equation 8-1 shows the algorithm that is used. The 32-bit result is stored in 4 registers RES3:RES0.

EQUATION 8-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM

$$
\begin{aligned}
RES3:RES0 &= ARG1H:ARG1L * ARG2H:ARG2L \\
&= (ARG1H * ARG2H * 2^{16}) + \\
&\quad (ARG1H * ARG2L * 2^{8}) + \\
&\quad (ARG1L * ARG2H * 2^{8}) + \\
&\quad (ARG1L * ARG2L)
\end{aligned}
$$

EXAMPLE 8-3: 16 x 16 MULTIPLY ROUTINE

```
    MOVFP   ARG1L, WREG
    MULWF   ARG2L       ; ARG1L * ARG2L ->
                        ;   PRODH:PRODL
    MOVPF   PRODH, RES1 ;
    MOVPF   PRODL, RES0 ;
;
    MOVFP   ARG1H, WREG
    MULWF   ARG2H       ; ARG1H * ARG2H ->
                        ;   PRODH:PRODL
    MOVPF   PRODH, RES3 ;
    MOVPF   PRODL, RES2 ;
;
    MOVFP   ARG1L, WREG
    MULWF   ARG2H       ; ARG1L * ARG2H ->
                        ;   PRODH:PRODL
    MOVFP   PRODL, WREG ;
    ADDWF   RES1, F     ; Add cross
    MOVFP   PRODH, WREG ;    products
    ADDWFC  RES2, F     ;
    CLRF    WREG, F     ;
    ADDWFC  RES3, F     ;
;
    MOVFP   ARG1H, WREG ;
    MULWF   ARG2L       ; ARG1H * ARG2L ->
                        ;   PRODH:PRODL

    MOVFP   PRODL, WREG ;
    ADDWF   RES1, F     ; Add cross
    MOVFP   PRODH, WREG ;    products
    ADDWFC  RES2, F     ;
    CLRF    WREG, F     ;
    ADDWFC  RES3, F     ;
```


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Example 8-4 shows the sequence to do an 16 x 16 signed multiply. Equation 8-2 shows the algorithm that used. The 32-bit result is stored in four registers RES3:RES0. To account for the sign bits of the arguments, each argument pairs most significant bit (MSb) is tested and the appropriate subtractions are done.

EQUATION 8-2: 16 x 16 SIGNED MULTIPLICATION ALGORITHM

RES3:RES0

= ARG1H:ARG1L * ARG2H:ARG2L

= (ARG1H * ARG2H * 2^{16}) +
(ARG1H * ARG2L * 2^{8}) +
(ARG1L * ARG2H * 2^{8}) +
(ARG1L * ARG2L) +
(-1 * ARG2H<7> * ARG1H:ARG1L * 2^{16}) +
(-1 * ARG1H<7> * ARG2H:ARG2L * 2^{16})

EXAMPLE 8-4: 16 x 16 SIGNED MULTIPLY ROUTINE

```
   MOVFP    ARG1L, WREG
   MULWF    ARG2L         ; ARG1L * ARG2L ->
                          ;   PRODH:PRODL
   MOVPF    PRODH, RES1 ;
   MOVPF    PRODL, RES0 ;
;
   MOVFP    ARG1H, WREG
   MULWF    ARG2H         ; ARG1H * ARG2H ->
                          ;   PRODH:PRODL
   MOVPF    PRODH, RES3 ;
   MOVPF    PRODL, RES2 ;
;
   MOVFP    ARG1L, WREG
   MULWF    ARG2H         ; ARG1L * ARG2H ->
                          ;   PRODH:PRODL
   MOVPF    PRODL, WREG ;
   ADDWF    RES1, F       ; Add cross
   MOVFP    PRODH, WREG ;    products
   ADDWFC   RES2, F       ;
   CLRF     WREG, F       ;
   ADDWFC   RES3, F       ;
;
   MOVFP    ARG1H, WREG ;
   MULWF    ARG2L         ; ARG1H * ARG2L ->
                          ;   PRODH:PRODL

   MOVFP    PRODL, WREG ;
   ADDWF    RES1, F       ; Add cross
   MOVFP    PRODH, WREG ;    products
   ADDWFC   RES2, F       ;
   CLRF     WREG, F       ;
   ADDWFC   RES3, F       ;
;
   BTFSS    ARG2H, 7      ; ARG2H:ARG2L neg?
   GOTO     SIGN_ARG1     ; no, check ARG1
   MOVFP    ARG1L, WREG ;
   SUBWF    RES2          ;
   MOVFP    ARG1H, WREG ;
   SUBWFB   RES3
;
SIGN_ARG1
   BTFSS    ARG1H, 7      ; ARG1H:ARG1L neg?
   GOTO     CONT_CODE     ; no, done
   MOVFP    ARG2L, WREG ;
   SUBWF    RES2          ;
   MOVFP    ARG2H, WREG ;
   SUBWFB   RES3
;
CONT_CODE
     :
```


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NOTES:

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9.0 I/O PORTS

The PIC17C4X devices have five I/O ports, PORTA through PORTE. PORTB through PORTE have a corresponding Data Direction Register (DDR), which is used to configure the port pins as inputs or outputs. These five ports are made up of 33 I/O pins. Some of these ports pins are multiplexed with alternate functions.

PORTC, PORTD, and PORTE are multiplexed with the system bus. These pins are configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, these pins are general purpose I/O.

PORTA and PORTB are multiplexed with the peripheral features of the device. These peripheral features are:

- Timer modules
- Capture module
- PWM module
- USART/SCI module
- External Interrupt pin

When some of these peripheral modules are turned on, the port pin will automatically configure to the alternate function. The modules that do this are:

- PWM module
- USART/SCI module

When a pin is automatically configured as an output by a peripheral module, the pins data direction (DDR) bit is unknown. After disabling the peripheral module, the user should re-initialize the DDR bit to the desired configuration.

The other peripheral modules (which require an input) must have their data direction bit configured appropriately.

Note:	A pin that is a peripheral input, can be configured as an output (DDRx<y> is cleared). The peripheral events will be determined by the action output on the port pin.

9.1 PORTA Register

PORTA is a 6-bit wide latch. PORTA does not have a corresponding Data Direction Register (DDR).

Reading PORTA reads the status of the pins.

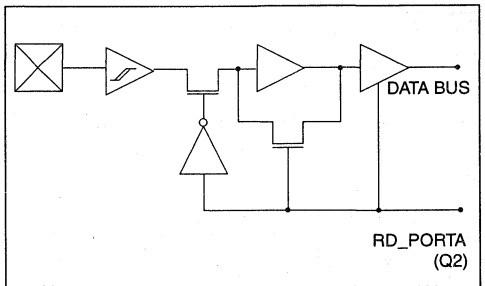
The RA1 pin is multiplexed with TMR0 clock input, and RA4 and RA5 are multiplexed with the USART functions. The control of RA4 and RA5 as outputs is automatically configured by the USART module.

9.1.1 USING RA2, RA3 AS OUTPUTS

The RA2 and RA3 pins are open drain outputs. To use the RA2 or the RA3 pin(s) as output(s), simply write to the PORTA register the desired value. A '0' will cause the pin to drive low, while a '1' will cause the pin to float (hi-impedance). An external pull-up resistor should be used to pull the pin high. Writes to PORTA will not affect the other pins.

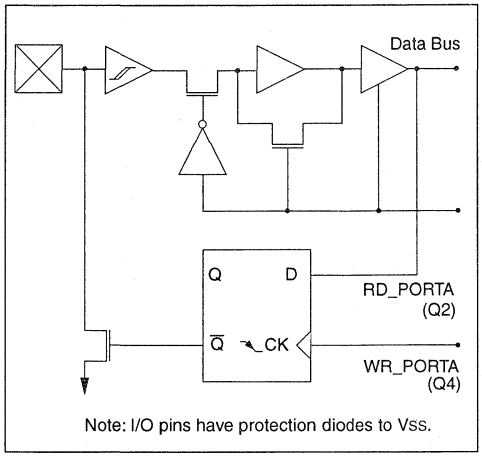
Note:	When using the RA2 or RA3 pin(s) as output(s), read-modify-write instructions (such as BCF, BSF, BTG) on PORTA are not recommended. Such operations read the port pins, do the desired operation, and then write this value to the data latch. This may inadvertently cause the RA2 or RA3 pins to switch from input to output (or vice-versa). It is recommended to use a shadow register for PORTA. Do the bit operations on this shadow register and then move it to PORTA.

FIGURE 9-1: RA0 AND RA1 BLOCK DIAGRAM



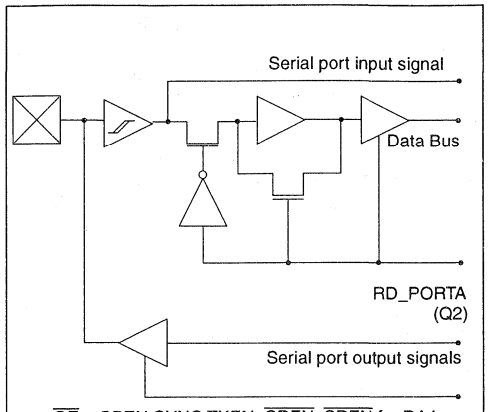
Note: I/O pins have protection diodes to VDD and VSS.

FIGURE 9-2: RA2 AND RA3 BLOCK DIAGRAM



Note: I/O pins have protection diodes to VSS.

FIGURE 9-3: RA4 AND RA5 BLOCK DIAGRAM



$\overline{OE}$ = SPEN,SYNC,TXEN, $\overline{CREN}$, $\overline{SREN}$ for RA4

$\overline{OE}$ = SPEN ($\overline{SYNC}$+SYNC,$\overline{CSRC}$) for RA5

Note: I/O pins have protection diodes to VDD and VSS.

TABLE 9-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0/INT	bit0	ST	Input or external interrupt input.
RA1/T0CKI	bit1	ST	Input or clock input to the TMR0 timer/counter, and/or an external interrupt input.
RA2	bit2	ST	Input/Output. Output is open drain type.
RA3	bit3	ST	Input/Output. Output is open drain type.
RA4/RX/DT	bit4	ST	Input or USART Asynchronous Receive or USART Synchronous Data.
RA5/TX/CK	bit5	ST	Input or USART Asynchronous Transmit or USART Synchronous Clock.
$\overline{RBPU}$	bit7	—	Control bit for PORTB weak pull-ups.

Legend: ST = Schmitt Trigger input.

TABLE 9-2: REGISTERS/BITS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
10h, Bank 0	PORTA	$\overline{RBPU}$	—	RA5	RA4	RA3	RA2	RA1/T0CKI	RA0/INT	0-xx xxxx	0-uu uuuu
05h, Unbanked	T0STA	INTEDG	T0SE	T0CS	PS3	PS2	PS1	PS0	—	0000 000-	0000 000-
13h, Bank 0	RCSTA	SPEN	RC9	SREN	CREN	—	FERR	OERR	RC9D	0000 -00x	0000 -00u
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u

Legend: x = unknown, u = unchanged, - = unimplemented reads as '0'. Shaded cells are not used by PORTA.
Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

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9.2 PORTB and DDRB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is DDRB. A '1' in DDRB configures the corresponding port pin as an input. A '0' in the DDRB register configures the corresponding port pin as an output. Reading PORTB reads the status of the pins, whereas writing to it will write to the port latch.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBPU}}$ (PORTA<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are enabled on any reset.

PORTB also has an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB0 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB0) are compared with the value in the PORTB data latch. The "mismatch" outputs of RB7:RB0 are OR'ed together to generate the PORTB Interrupt Flag RBIF (PIR<7>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt by:

a) Read-Write PORTB (such as; `MOVPF PORTB, PORTB`). This will end mismatch condition.

b) Then, clear the RBIF bit.

A mismatch condition will continue to set the RBIF bit. Reading then writing PORTB will end the mismatch condition, and allow the RBIF bit to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on this port, allows easy interface to a key pad and make it possible for wake-up on key-depression. For an example, refer to AN552 in the *Embedded Control Handbook*.

The interrupt on change feature is recommended for wake-up on operations where PORTB is only used for the interrupt on change feature and key depression operation.

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FIGURE 9-4: BLOCK DIAGRAM OF RB<7:4> AND RB<1:0> PORT PINS

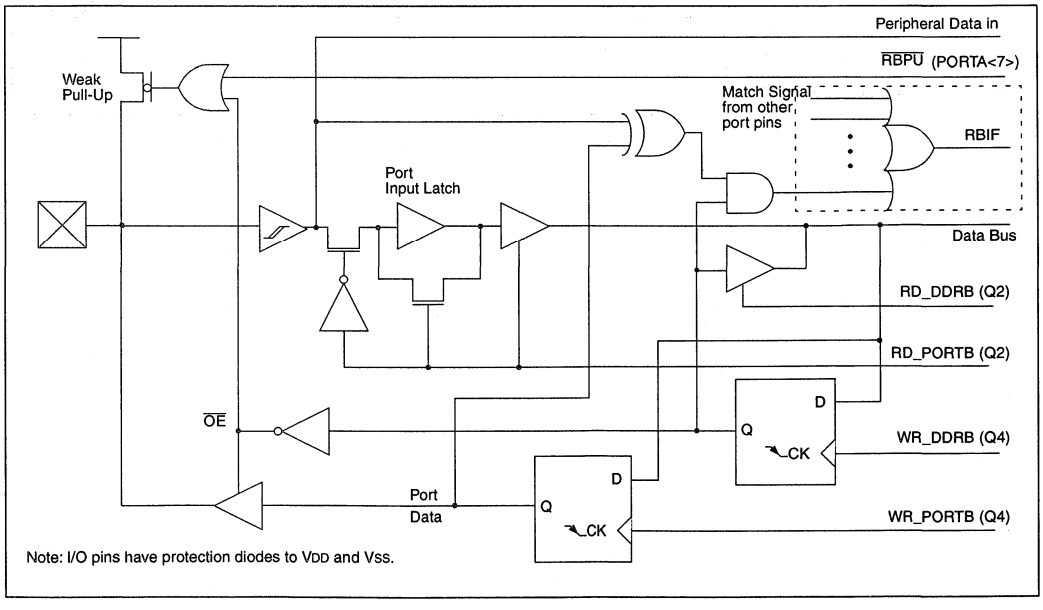
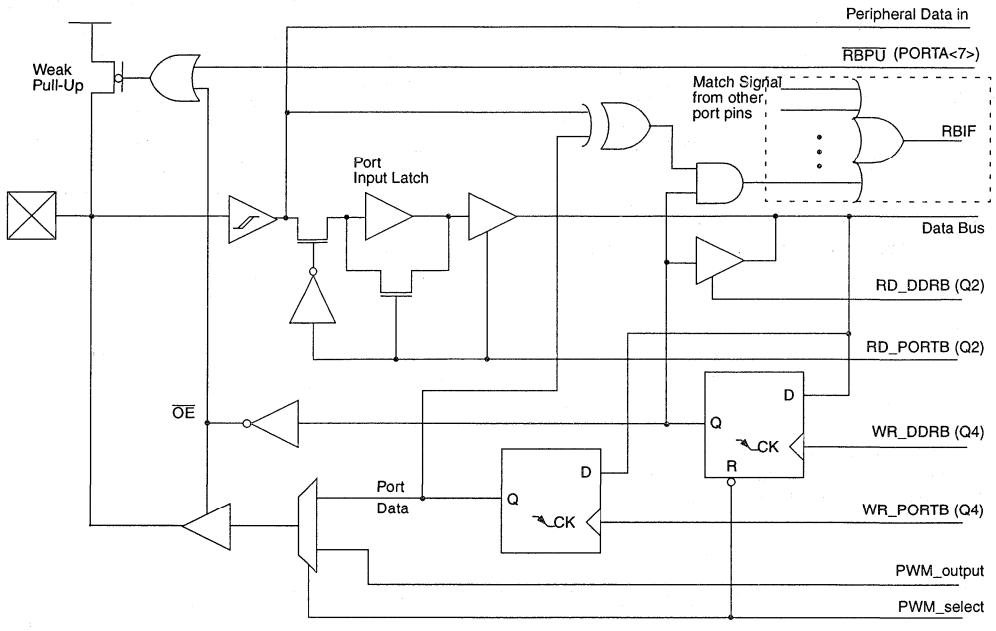


FIGURE 9-5: BLOCK DIAGRAM OF RB3 AND RB2 PORT PINS



Note: I/O pins have protection diodes to VDD and Vss.

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Example 9-1 shows the instruction sequence to initialize PORTB. The Bank Select Register (BSR) must be selected to Bank 0 for the port to be initialized.

EXAMPLE 9-1: INITIALIZING PORTB

```
MOVLB  0        ; Select Bank 0
CLRF   PORTB    ; Initialize PORTB by clearing
                ;  output data latches
MOVLW  0xCF     ; Value used to initialize
                ;  data direction
MOVWF  DDRB     ;  Set RB<3:0> as inputs
                ;   RB<5:4> as outputs
                ;   RB<7:6> as inputs
```


TABLE 9-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	Function
RB0/CAP1	bit0	ST	Input/Output or the RB0/CAP1 input pin. Software programmable weak pull-up and interrupt on change features.
RB1/CAP2	bit1	ST	Input/Output or the RB1/CAP2 input pin. Software programmable weak pull-up and interrupt on change features.
RB2/PWM1	bit2	ST	Input/Output or the RB2/PWM1 output pin. Software programmable weak pull-up and interrupt on change features.
RB3/PWM2	bit3	ST	Input/Output or the RB3/PWM2 output pin. Software programmable weak pull-up and interrupt on change features.
RB4/TCLK12	bit4	ST	Input/Output or the external clock input to Timer1 and Timer2. Software programmable weak pull-up and interrupt on change features.
RB5/TCLK3	bit5	ST	Input/Output or the external clock input to Timer3. Software programmable weak pull-up and interrupt on change features.
RB6	bit6	ST	Input/Output pin. Software programmable weak pull-up and interrupt on change features.
RB7	bit7	ST	Input/Output pin. Software programmable weak pull-up and interrupt on change features.

Legend: ST = Schmitt Trigger input.

TABLE 9-4: REGISTERS/BITS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
12h, Bank 0	PORTB	PORTB data latch								xxxx xxxx	uuuu uuuu
11h, Bank 0	DDRB	Data direction register for PORTB								1111 1111	1111 1111
10h, Bank 0	PORTA	$\overline{RBPU}$	—	RA5	RA4	RA3	RA2	RA1/T0CKI	RA0/INT	0-xx xxxx	0-uu uuuu
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	—	—	--11 11--	--11 qq--
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{PR3}$	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = Value depends on condition.
Shaded cells are not used by PORTB.

Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

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9.3 PORTC and DDRC Registers

PORTC is an 8-bit bi-directional port. The corresponding data direction register is DDRC. A '1' in DDRC configures the corresponding port pin as an input. A '0' in the DDRC register configures the corresponding port pin as an output. Reading PORTC reads the status of the pins, whereas writing to it will write to the port latch. PORTC is multiplexed with the system bus. When operating as the system bus, PORTC is the low order byte of the address/data bus (AD7:AD0). The timing for the system bus is shown in the Electrical Characteristics section.

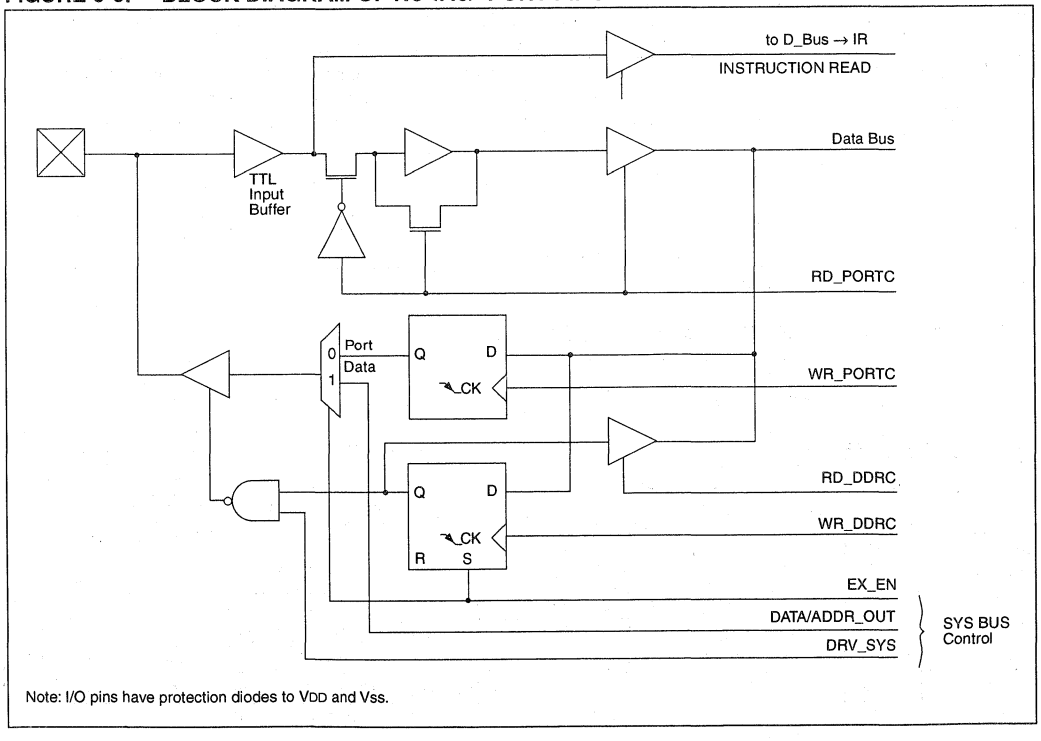
Note: This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O.

Example 9-2 shows the instruction sequence to initialize PORTC. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

EXAMPLE 9-2: INITIALIZING PORTC

```
MOVLB  1          ; Select Bank 1
CLRF   PORTC      ; Initialize PORTC data
                  ;  latches before setting
                  ;  the data direction
                  ;  register
MOVLW  0xCF       ; Value used to initialize
                  ;  data direction
MOVWF  DDRC       ; Set RC<3:0> as inputs
                  ;  RC<5:4> as outputs
                  ;  RC<7:6> as inputs
```

FIGURE 9-6: BLOCK DIAGRAM OF RC<7:0> PORT PINS



Note: I/O pins have protection diodes to VDD and Vss.

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TABLE 9-5: PORTC FUNCTIONS

Name	Bit	Buffer Type	Function
RC0/AD0	bit0	TTL	Input/Output or system bus address/data pin.
RC1/AD1	bit1	TTL	Input/Output or system bus address/data pin.
RC2/AD2	bit2	TTL	Input/Output or system bus address/data pin.
RC3/AD3	bit3	TTL	Input/Output or system bus address/data pin.
RC4/AD4	bit4	TTL	Input/Output or system bus address/data pin.
RC5/AD5	bit5	TTL	Input/Output or system bus address/data pin.
RC6/AD6	bit6	TTL	Input/Output or system bus address/data pin.
RC7/AD7	bit7	TTL	Input/Output or system bus address/data pin.

Legend: TTL = TTL input.

TABLE 9-6: REGISTERS/BITS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
11h, Bank 1	PORTC	RC7/ AD7	RC6/ AD6	RC5/ AD5	RC4/ AD4	RC3/ AD3	RC2/ AD2	RC1/ AD1	RC0/ AD0	xxxx xxxx	uuuu uuuu
10h, Bank 1	DDRC	Data direction register for PORTC								1111 1111	1111 1111

Legend: x = unknown, u = unchanged.
Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and the Watchdog Timer Reset.

9.4 PORTD and DDRD Registers

PORTD is an 8-bit bi-directional port. The corresponding data direction register is DDRD. A '1' in DDRD configures the corresponding port pin as an input. A '0' in the DDRC register configures the corresponding port pin as an output. Reading PORTD reads the status of the pins, whereas writing to it will write to the port latch. PORTD is multiplexed with the system bus. When operating as the system bus, PORTD is the high order byte of the address/data bus (AD15:AD8). The timing for the system bus is shown in the Electrical Characteristics section.

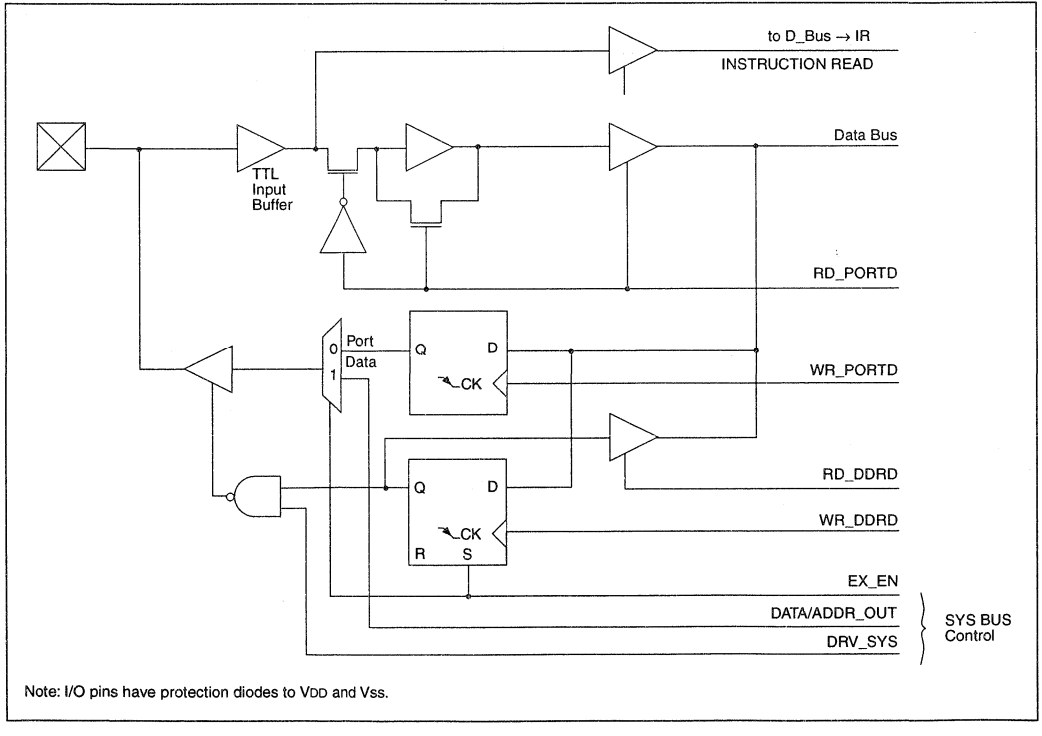
Note: This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O.

Example 9-3 shows the instruction sequence to initialize PORTD. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

EXAMPLE 9-3: INITIALIZING PORTD

```
MOVLB  1          ; Select Bank 1
CLRF   PORTD      ; Initialize PORTD data
                  ;  latches before setting
                  ;  the data direction
                  ;  register
MOVLW  0xCF       ; Value used to initialize
                  ;  data direction
MOVWF  DDRD       ; Set RD<3:0> as inputs
                  ;  RD<5:4> as outputs
                  ;  RD<7:6> as inputs
```

FIGURE 9-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and Vss.

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TABLE 9-7: PORTD FUNCTIONS

Name	Bit	Buffer Type	Function
RD0/AD8	bit0	TTL	Input/Output or system bus address/data pin.
RD1/AD9	bit1	TTL	Input/Output or system bus address/data pin.
RD2/AD10	bit2	TTL	Input/Output or system bus address/data pin.
RD3/AD11	bit3	TTL	Input/Output or system bus address/data pin.
RD4/AD12	bit4	TTL	Input/Output or system bus address/data pin.
RD5/AD13	bit5	TTL	Input/Output or system bus address/data pin.
RD6/AD14	bit6	TTL	Input/Output or system bus address/data pin.
RD7/AD15	bit7	TTL	Input/Output or system bus address/data pin.

Legend: TTL = TTL input.

TABLE 9-8: REGISTERS/BITS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
13h, Bank 1	PORTD	RD7/ AD15	RD6/ AD14	RD5/ AD13	RD4/ AD12	RD3/ AD11	RD2/ AD10	RD1/ AD9	RD0/ AD8	xxxx xxxx	uuuu uuuu
12h, Bank 1	DDRD	Data direction register for PORTD								1111 1111	1111 1111

Legend: x = unknown, u = unchanged.
Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and the Watchdog Timer Reset.

9.4.1 PORTE AND DDRE REGISTER

PORTE is a 3-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE configures the corresponding port pin as an input. A '0' in the DDRE register configures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to it will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable ($\overline{OE}$), and Write ($\overline{WR}$). The control signals $\overline{OE}$ and $\overline{WR}$ are active low signals. The timing for the system bus is shown in the Electrical Characteristics section.

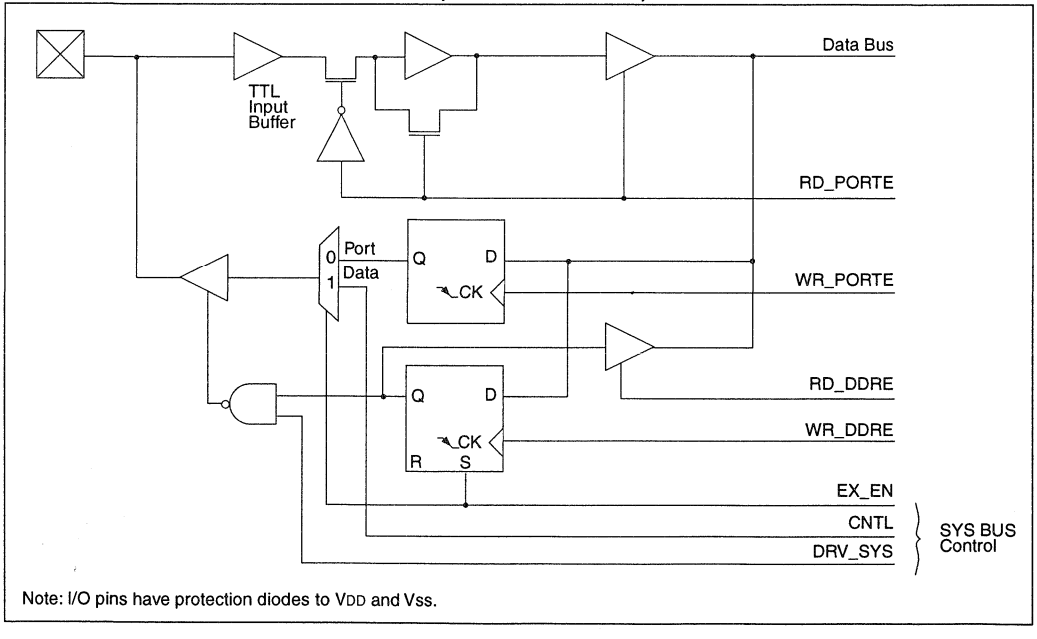
Note: This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O.

Example 9-4 shows the instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized.

EXAMPLE 9-4: INITIALIZING PORTE

```
MOVLB  1          ; Select Bank 1
CLRF   PORTE      ; Initialize PORTE data
                  ;  latches before setting
                  ;  the data direction
                  ;  register
MOVLW  0x03       ; Value used to initialize
                  ;  data direction
MOVWF  DDRE       ; Set RE<1:0> as inputs
                  ;  RE<2> as outputs
                  ;  RE<7:3> are always
                  ;  read as '0'
```

FIGURE 9-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and Vss.

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TABLE 9-9: PORTE FUNCTIONS

Name	Bit	Buffer Type	Function
RE0/ALE	bit0	TTL	Input/Output or system bus Address Latch Enable (ALE) control pin.
RE1/$\overline{OE}$	bit1	TTL	Input/Output or system bus Output Enable ($\overline{OE}$) control pin.
RE2/$\overline{WR}$	bit2	TTL	Input/Output or system bus Write ($\overline{WR}$) control pin.

Legend: TTL = TTL input.

TABLE 9-10: REGISTERS/BITS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
15h, Bank 1	PORTE	—	—	—	—	—	RE2/$\overline{WR}$	RE1/$\overline{OE}$	RE0/ALE	---- -xxx	---- -uuu
14h, Bank 1	DDRE	Data direction register for PORTE								---- -111	---- -111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTE.
Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

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9.5 I/O Programming Considerations

9.5.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. For example, the BCF and BSF instructions read the register into the CPU, execute the bit operation, and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g. bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading a port reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (BCF, BSF, BTG, etc.) on a port, the value of the port pins is read, the desired operation is performed with this value, and the value is then written to the port latch.

Example 9-5 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 9-5: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

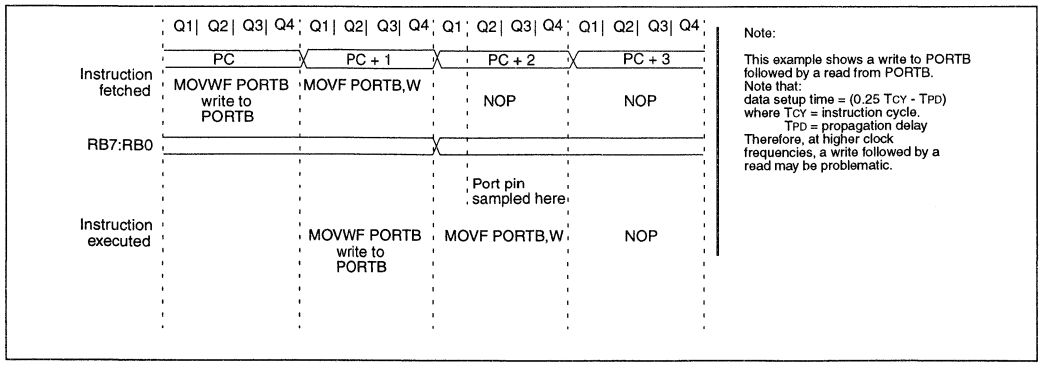
```
; Initial PORT settings: PORTB<7:4> Inputs
;                        PORTB<3:0> Outputs
; PORTB<7:6> have pull-ups and are
; not connected to other circuitry
;
;                        PORT latch  PORT pins
;                        ----------  ---------
;
   BCF   PORTB, 7        01pp pppp   11pp pppp
   BCF   PORTB, 6        10pp pppp   11pp pppp
;
   BCF   DDRB, 7         10pp pppp   11pp pppp
   BCF   DDRB, 6         10pp pppp   10pp pppp
;
; Note that the user may have expected the
; pin values to be 00pp pppp. The 2nd BCF
; caused RB7 to be latched as the pin value
; (High).
```

Note: A pin actively outputting a Low or High should not be driven from external devices in order to change the level on this pin (i.e. "wired-or", "wired-and"). The resulting high output currents may damage the device.

9.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 9-9). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before executing the instruction that reads the values on that I/O port. Otherwise, the previous state of that pin may be read into the CPU rather than the "new" state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 9-9: SUCCESSIVE I/O OPERATION



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10.0 OVERVIEW OF TIMER RESOURCES

The PIC17C4X has four timer modules. Each module can generate an interrupt to indicate that an event has occurred. These timers are called:

- Timer0 - 16-bit timer with programmable 8-bit prescaler
- Timer1 - 8-bit timer
- Timer2 - 8-bit timer
- Timer3 - 16-bit timer

For enhanced time-base functionality, two input Captures and two Pulse Width Modulation (PWM) outputs are possible. The PWMs use the TMR1 and TMR2 resources and the input Captures use the TMR3 resource.

10.1 Timer0 Overview

The Timer0 module is a simple 16-bit overflow counter. The clock source can be either the internal system clock (Fosc/4) or an external clock.

The Timer0 module also has a programmable prescaler option. The PS3:PS0 bits (T0STA<4:1>) determine the prescaler value. TMR0 can increment at the following rates: 1:1, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, 1:256.

When TImer0's clock source is an external clock, the Timer0 module can be selected to increment on either the rising or falling edge.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

10.2 Timer1 Overview

The TImer0 module is an 8-bit timer/counter with an 8-bit period register (PR1). When the TMR1 value rolls over from the period match value to 0h, the TMR1IF flag is set, and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB4/TCLK12 pin, which can also be selected to be the clock for the Timer2 module.

TMR1 can be concatenated to TMR2 to form a 16-bit timer. The TMR1 register is the LSB and TMR2 is the MSB. When in the 16-bit timer mode, there is a corresponding 16-bit period register (PR2:PR1). When the TMR2:TMR1 value rolls over from the period match value to 0h, the TMR1IF flag is set, and an interrupt will be generated when enabled.

10.3 Timer2 Overview

The TMR2 module is an 8-bit timer/counter with an 8-bit period register (PR2). When the TMR2 value rolls over from the period match value to 0h, the TMR2IF flag is set, and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB4/TCLK12 pin, which can also be selected to be the clock for the TMR1 module.

TMR1 can be concatenated to TMR2 to form a 16-bit timer. The TMR2 register is the MSB and TMR1 is the LSB. When in the 16-bit timer mode, there is a corresponding 16-bit period register (PR2:PR1). When the TMR2:TMR1 value rolls over from the period match value to 0h, the TMR1IF flag is set, and an interrupt will be generated when enabled.

10.4 Timer3 Overview

The TImer3 module is a 16-bit timer/counter with a 16-bit period register. When the TMR3H:TMR3L value rolls over to 0h, the TMR3IF bit is set and an interrupt will be generated when enabled. In counter mode, the clock comes from the RB5/TCLK3 pin.

When operating in the dual capture mode, the period registers become the second 16-bit capture register.

10.5 Role of the Timer/Counters

The timer modules are general purpose, but have dedicated resources associated with them. TImer1 and Timer2 are the time-bases for the two Pulse Width Modulation (PWM) outputs, while Timer3 is the time-base for the two input captures.

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NOTES:

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11.0 TIMER0

The Timer0 module consists of a 16-bit timer/counter, TMR0. The high byte is TMR0H and the low byte is TMR0L. A software programmable 8-bit prescaler makes an effective 24-bit overflow timer. The clock source is also software programmable as either the internal instruction clock or the RA1/T0CKI pin. The control bits for this module are in register T0STA (Figure 11-1).

FIGURE 11-1: T0STA REGISTER (ADDRESS: 05h, UNBANKED)

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	U - 0
INTEDG	T0SE	T0CS	PS3	PS2	PS1	PS0	—
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented, Read as '0'
-n = Value at POR reset

bit 7: **INTEDG**: RA0/INT Pin Interrupt Edge Select bit
This bit selects the edge upon which the interrupt is detected
1 = Rising edge of RA0/INT pin generates interrupt
0 = Falling edge of RA0/INT pin generates interrupt

bit 6: **T0SE**: Timer0 Clock Input Edge Select bit
This bit selects the edge upon which TMR0 will increment
When T0CS = 0
1 = Rising edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
0 = Falling edge of RA1/T0CKI pin increments TMR0 and/or generates a T0CKIF interrupt
When T0CS = 1
Don't care

bit 5: **T0CS**: Timer0 Clock Source Select bit
This bit selects the clock source for TMR0.
1 = Internal instruction clock cycle (TCY)
0 = T0CKI pin

bit 4-1: **PS3:PS0**: Timer0 Prescale Selection bits
These bits select the prescale value for TMR0.

PS3:PS0	Prescale Value
0000	1:1
0001	1:2
0010	1:4
0011	1:8
0100	1:16
0101	1:32
0110	1:64
0111	1:128
1xxx	1:256

bit 0: **Unimplemented**: Read as '0'

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11.1 Timer0 Operation

When the T0CS (T0STA<5>) bit is set, TMR0 increments on the internal clock. When T0CS is clear, TMR0 increments on the external clock (RA1/T0CKI pin). The external clock edge can be configured in software. When the T0SE (T0STA<6>) bit is set, the timer will increment on the rising edge of the RA1/T0CKI pin. When T0SE is clear, the timer will increment on the falling edge of the RA1/T0CKI pin. The prescaler can be programmed to introduce a prescale of 1:1 to 1:256. The timer increments from 0000h to FFFFh and rolls over to 0000h. On overflow, the TMR0 Interrupt Flag bit (T0IF) is set. The TMR0 interrupt can be masked by clearing the corresponding TMR0 Interrupt Enable bit (T0IE). The TMR0 Interrupt Flag bit (T0IF) is automatically cleared when vectoring to the TMR0 interrupt vector.

11.2 Using Timer0 with External Clock

When the external clock input is used for Timer0, it is synchronized with the internal phase clocks. Figure 11-3 shows the synchronization of the external clock. This synchronization is done after the prescaler. The output of the prescaler (PSOUT) is sampled twice in every instruction cycle to detect a rising or a falling edge. The timing requirements for the external clock are detailed in the electrical specification section for the desired device.

11.2.1 DELAY FROM EXTERNAL CLOCK EDGE

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time TMR0 is actually incremented. Figure 11-3 shows that this delay is between 3TOSC and 7TOSC. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4TOSC (±121 ns @ 33 MHz).

FIGURE 11-2: TIMER0 MODULE BLOCK DIAGRAM

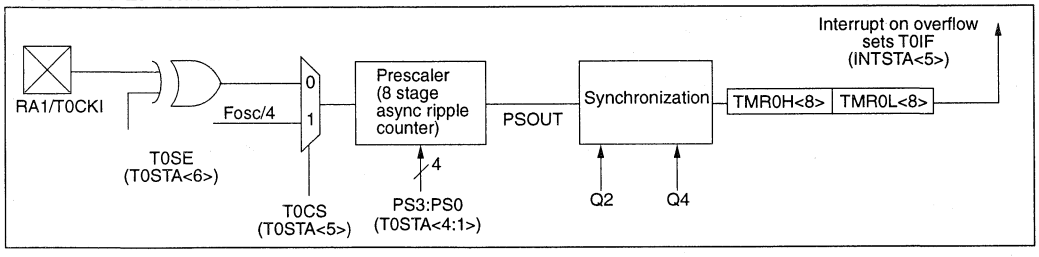
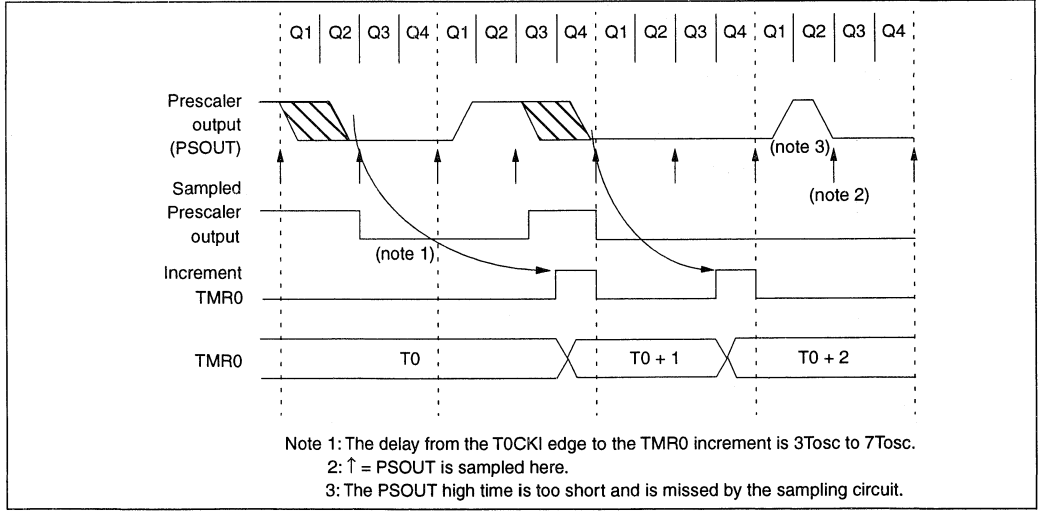


FIGURE 11-3: TMR0 TIMING WITH EXTERNAL CLOCK (INCREMENT ON FALLING EDGE)



Note 1: The delay from the T0CKI edge to the TMR0 increment is 3Tosc to 7Tosc.
2: ↑ = PSOUT is sampled here.
3: The PSOUT high time is too short and is missed by the sampling circuit.

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11.3 Read/Write Consideration for TMR0

Although TMR0 is a 16-bit timer/counter, only 8-bits at a time can be read or written during a single instruction cycle. Care must be taken during any read or write.

11.3.1 READING 16-BIT VALUE

The problem in reading the entire 16-bit value is that after reading the low (or high) byte, its value may change from FFh to 00h.

Example 11-1 shows a 16-bit read. To ensure a proper read, interrupts must be disabled during this routine.

EXAMPLE 11-1: 16-BIT READ

```
MOVPF   TMR0L, TMPLO    ;read low tmr0
MOVPF   TMR0H, TMPHI    ;read high tmr0
MOVPF   TMPLO, WREG     ;tmplo -> wreg
CPFSLT  TMR0L           ;tmr0l < wreg?
RETURN                  ;no then return
MOVPF   TMR0L, TMPLO    ;read low tmr0
MOVPF   TMR0H, TMPHI    ;read high tmr0
RETURN                  ;return
```

11.3.2 WRITING A 16-BIT VALUE TO TMR0

Since writing to either TMR0L or TMR0H will effectively inhibit increment of that half of the TMR0 in the next cycle (following write), but not inhibit increment of the other half, the user must write to TMR0L first and TMR0H next in two consecutive instructions, as shown in Example 11-2. The interrupt must be disabled. Any write to either TMR0L or TMR0H clears the prescaler.

EXAMPLE 11-2: 16-BIT WRITE

```
BSF   CPUSTA, GLINTD ; Disable interrupt
MOVFP RAM_L, TMR0L   ;
MOVFP RAM_H, TMR0H   ;
BCF   CPUSTA, GLINTD ; Done, enable interrupt
```

11.4 Prescaler Assignments

Timer0 has an 8-bit prescaler. The prescaler assignment is fully under software control; i.e., it can be changed "on the fly" during program execution. When changing the prescaler assignment, clearing the prescaler is recommended before changing assignment. The value of the prescaler is "unknown," and assigning a value that is less then the present value makes it difficult to take this unknown time into account.

FIGURE 11-4: TMR0 TIMING: WRITE HIGH OR LOW BYTE

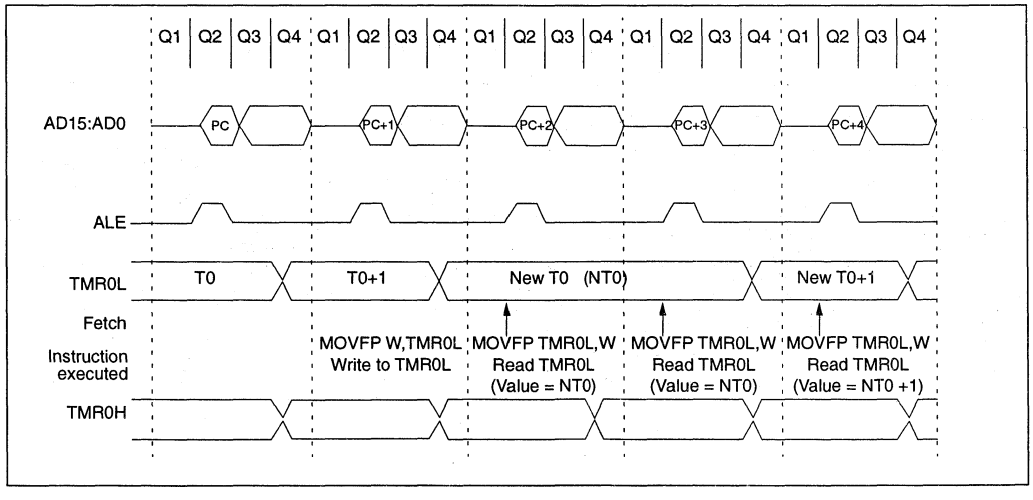
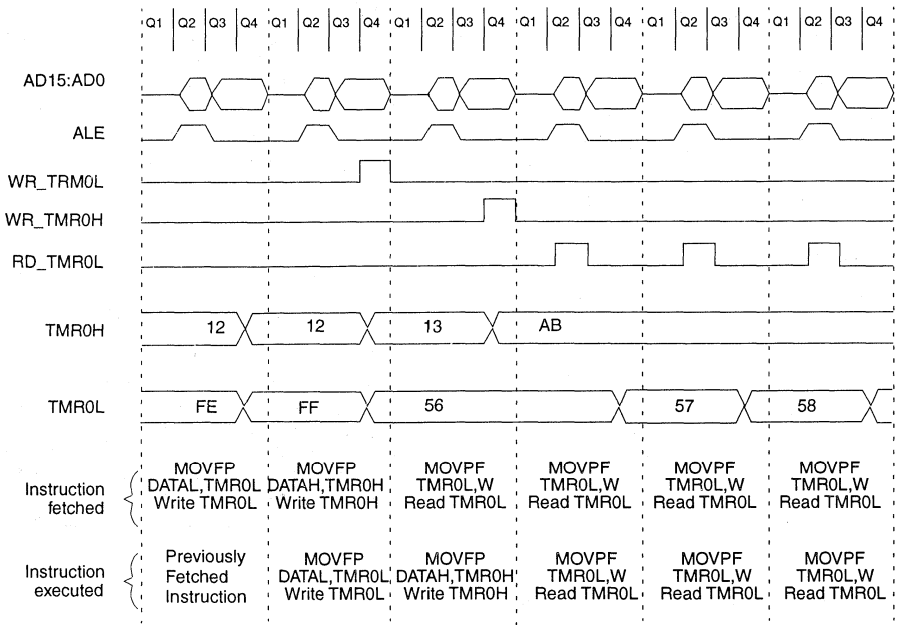


FIGURE 11-5: TMR0 READ/WRITE IN TIMER MODE



In this example, old TMR0 value is 12FEh, new value of AB56h is written.

TABLE 11-1: REGISTERS/BITS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
05h, Unbanked	T0STA	INTEDG	T0SE	T0CS	PS3	PS2	PS1	PS0	—	0000 000-	0000 000-
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	—	—	--11 11--	--11 qq--
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
0Bh, Unbanked	TMR0L	TMR0 register; low byte								xxxx xxxx	uuuu uuuu
0Ch, Unbanked	TMR0H	TMR0 register; high byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', q - value depends on condition, Shaded cells are not used by Timer0.
Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

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12.0 TIMER1, TIMER2, TIMER3, PWMS AND CAPTURES

The PIC17C4X has a wealth of timers and time-based functions to ease the implementation of control applications. These time-base functions include two PWM outputs and two Capture inputs.

Timer1 and Timer2 are two 8-bit incrementing timers, each with a period register (PR1 and PR2 respectively) and separate overflow interrupt flags. Timer1 and Timer2 can operate either as timers (increment on internal Fosc/4 clock) or as counters (increment on falling edge of external clock on pin RB4/TCLK12). They are also software configurable to operate as a single 16-bit timer. These timers are also used as the time-base for the PWM (pulse width modulation) module.

Timer3 is a 16-bit timer/counter consisting of the TMR3H and TMR3L registers. This timer has four other associated registers. Two registers are used as a 16-bit period register or a 16-bit Capture1 register (PR3H/CA1H:PR3L/CA1L). The other two registers are strictly the Capture2 registers (CA2H:CA2L). Timer3 is the time-base for the two 16-bit captures.

TMR3 can be software configured to increment from the internal system clock or from an external signal on the RB5/TCLK3 pin.

Figure 12-1 and Figure 12-2 are the control registers for the operation of Timer1, Timer2, and Timer3, as well as PWM1, PWM2, Capture1, and Capture2.

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FIGURE 12-1: TCON1 REGISTER (ADDRESS: 16h, BANK 3)

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0
CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS
bit7							bit0

R = Readable bit
W = Writable bit
-n = Value at POR reset

bit 7-6: **CA2ED1:CA2ED0**: Capture2 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 5-4: **CA1ED1:CA1ED0**: Capture1 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 3: **T16**: Timer1:Timer2 Mode Select bit
1 = Timer1 and Timer2 form a 16-bit timer
0 = Timer1 and Timer2 are two 8-bit timers

bit 2: **TMR3CS**: Timer3 Clock Source Select bit
1 = TMR3 increments off the falling edge of the RB5/TCLK3 pin
0 = TMR3 increments off the internal clock

bit 1: **TMR2CS**: Timer2 Clock Source Select bit
1 = TMR2 increments off the falling edge of the RB4/TCLK12 pin
0 = TMR2 increments off the internal clock

bit 0: **TMR1CS**: Timer1 Clock Source Select bit
1 = TMR1 increments off the falling edge of the RB4/TCLK12 pin
0 = TMR1 increments off the internal clock

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FIGURE 12-2: TCON2 REGISTER (ADDRESS: 17h, BANK 3)

R - 0	R - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0
CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{PR3}$	TMR3ON	TMR2ON	TMR1ON
bit7							bit0

R = Readable bit
W = Writable bit
-n = Value at POR reset

bit 7: **CA2OVF**: Capture2 Overflow Status bit
This bit indicates that the capture value had not been read from the capture register pair (CA2H:CA2L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the Timer3 value until the capture register has been read (both bytes).
1 = Overflow occurred on Capture2 register
0 = No overflow occurred on Capture2 register

bit 6: **CA1OVF**: Capture1 Overflow Status bit
This bit indicates that the capture value had not been read from the capture register pair (PR3H/CA2H:PR3L/CA2L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).
1 = Overflow occurred on Capture1 register
0 = No overflow occurred on Capture1 register

bit 5: **PWM2ON**: PWM2 On bit
1 = PWM2 is enabled (The RB3/PWM2 pin ignores the state of the DDRB<3> bit)
0 = PWM2 is disabled (The RB3/PWM2 pin uses the state of the DDRB<3> bit for data direction)

bit 4: **PWM1ON**: PWM1 On bit
1 = PWM1 is enabled (The RB2/PWM1 pin ignores the state of the DDRB<2> bit)
0 = PWM1 is disabled (The RB2/PWM1 pin uses the state of the DDRB<2> bit for data direction)

bit 3: **CA1/$\overline{PR3}$**: CA1/$\overline{PR3}$ Register Mode Select bit
1 = Enables Capture1 (PR3H/CA1H:PR3L/CA1L is the Capture1 register. Timer3 runs without a period register)
0 = Enables the Period register (PR3H/CA1H:PR3L/CA1L is the Period register for Timer3)

bit 2: **TMR3ON**: Timer3 On bit
1 = Starts Timer3
0 = Stops Timer3

bit 1: **TMR2ON**: Timer2 On bit
This bit controls the incrementing of the Timer2 register. When Timer2:Timer1 form the 16-bit timer (T16 is set), TMR2ON must be set. This allows the MSB of the timer to increment.
1 = Starts Timer2 (Must be enabled if the T16 bit (TCON1<3>) is set)
0 = Stops Timer2

bit 0: **TMR1ON**: Timer1 On bit
When T16 is set (in 16-bit Timer Mode)
1 = Starts 16-bit Timer2:Timer1
0 = Stops 16-bit Timer2:Timer1

When T16 is clear (in 8-bit Timer Mode)
1 = Starts 8-bit Timer1
0 = Stops 8-bit Timer1

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12.1 Timer1 and Timer2

12.1.1 TIMER1, TIMER2 IN 8-BIT MODE

Both Timer1 and Timer2 will operate in 8-bit mode when the T16 bit is clear. These two timers can be independently configured to increment from the internal instruction cycle clock or from an external clock source on the RB4/TCLK12 pin. The timer clock source is configured by the TMRxCS bit (x = 1 for Timer1 or = 2 for Timer2). When TMRxCS is clear, the clock source is internal and increments once every instruction cycle (Fosc/4). When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge of the RB4/TCLK12 pin.

The timer increments from 00h until it equals the Period register (PRx). It then resets to 00h at the next increment cycle. The timer interrupt flag is set when the timer is reset. TMR1 and TMR2 have individual interrupt flag bits. The TMR1 interrupt flag bit is latched into TMR1IF, and the TMR2 interrupt flag bit is latched into TMR2IF.

Each timer also has a corresponding interrupt enable bit (TMRxIE). The timer interrupt can be enabled by setting this bit and disabled by clearing this bit. For peripheral interrupts to be enabled, the Peripheral Interrupt Enable bit must be enabled (PEIE is set) and global interrupts must be enabled (GLINTD is cleared).

The timers can be turned on and off under software control. When the Timerx On control bit (TMRxON) is set, the timer increments from the clock source. When TMRxON is cleared, the timer is turned off and cannot cause the timer interrupt flag to be set.

12.1.1.1 EXTERNAL CLOCK INPUT FOR TIMER1 OR TIMER2

When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the timer will increment on every falling edge on the RB4/TCLK12 pin. The TCLK12 input is synchronized with internal phase clocks. This causes a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section.

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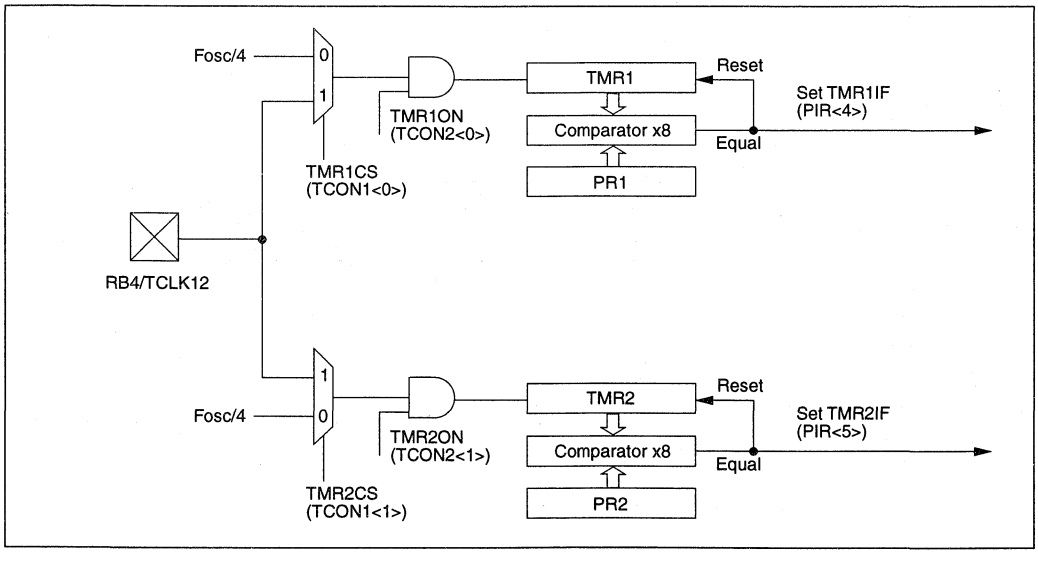
FIGURE 12-3: TIMER1 AND TIMER2 IN TWO 8-BIT TIMER/COUNTER MODE



12.1.2 TIMER1 & TIMER2 IN 16-BIT MODE

To select 16-bit mode, the T16 bit must be set. In this mode TMR1 and TMR2 are concatenated to form a 16-bit timer (TMR2:TMR1). The 16-bit timer increments until it matches the 16-bit period register (PR2:PR1). On the following timer clock, the timer value is reset to 0h, and the TMR1IF bit is set.

When selecting the clock source for the16-bit timer, the TMR1CS bit controls the entire 16-bit timer and TMR2CS is a "don't care." When TMR1CS is clear, the timer increments once every instruction cycle (Fosc/4). When TMR1CS is set, the timer increments on every falling edge of the RB4/TCLK12 pin. For the 16-bit timer to increment, both TMR1ON and TMR2ON bits must be set (Table 12-1).

12.1.2.1 EXTERNAL CLOCK INPUT FOR TMR1:TMR2

When TMR1CS is set, the 16-bit TMR2:TMR1 increments on the falling edge of clock input TCLK12. The input on the RB4/TCLK12 pin is sampled and synchronized by the internal phase clocks twice every instruction cycle. This causes a delay from the time a falling edge appears on RB4/TCLK12 to the time TMR2:TMR1 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section.

TABLE 12-1: TURNING ON 16-BIT TIMER

TMR2ON	TMR1ON	Result
1	1	16-bit timer (TMR2:TMR1) ON
0	1	Only TMR1 increments
x	0	16-bit timer OFF

FIGURE 12-4: TMR1 AND TMR2 IN 16-BIT TIMER/COUNTER MODE

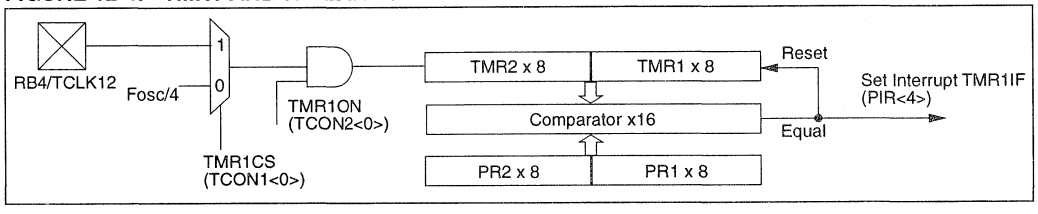


TABLE 12-2: SUMMARY OF TIMER1 AND TIMER2 REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
10h, Bank 2	TMR1	Timer1 register								xxxx xxxx	uuuu uuuu
11h, Bank 2	TMR2	Timer2 register								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	—	—	--11 11--	--11 qq--
14h, Bank 2	PR1	Timer1 period register								xxxx xxxx	uuuu uuuu
15h, Bank 2	PR2	Timer2 period register								xxxx xxxx	uuuu uuuu
10h, Bank 3	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx-- ----	uu-- ----
11h, Bank 3	PW2DCL	DC1	DC0	TM2PW2	—	—	—	—	—	xx0- ----	uu0- ----
12h, Bank 3	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h, Bank 3	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', q - value depends on condition, shaded cells are not used by Timer1 or Timer2.

Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and WDT Timer Reset.

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12.1.3 USING PULSE WIDTH MODULATION (PWM) OUTPUTS WITH TMR1 AND TMR2

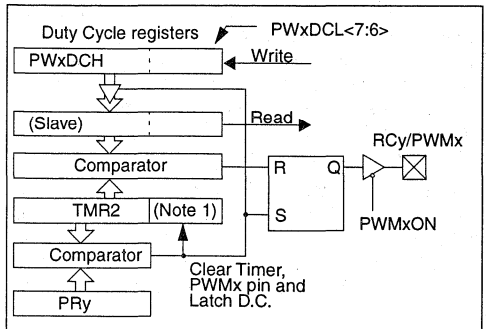
Two high speed pulse width modulation (PWM) outputs are provided. The PWM1 output uses Timer1 as its time-base, while PWM2 may be software configured to use either Timer1 or Timer2 as the time-base. The PWM outputs are on the RB2/PWM1 and RB3/PWM2 pins.

Each PWM output has a maximum resolution of 10-bits. At 10-bit resolution, the PWM output frequency is 24.4 kHz (@ 25 MHz clock) and at 8-bit resolution the PWM output frequency is 97.7 kHz. The duty cycle of the output can vary from 0% to 100%.

Figure 12-5 shows a simplified block diagram of the PWM module. The duty cycle register is double buffered for glitch free operation. Figure 12-6 shows how a glitch could occur if the duty cycle registers were not double buffered.

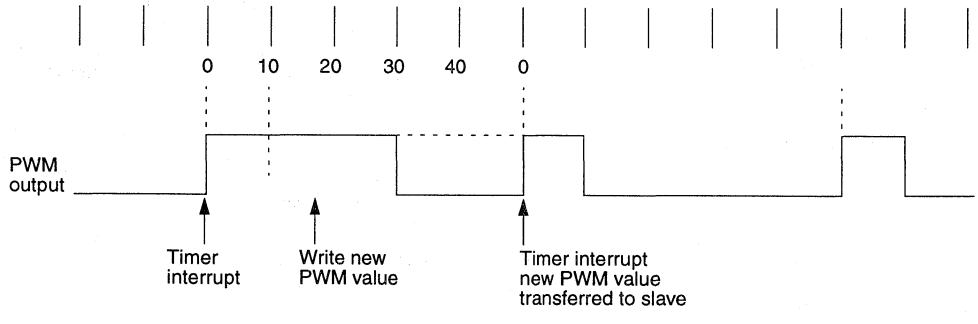
The user needs to set the PWM1ON bit (TCON2<4>) to enable the PWM1 output. When the PWM1ON bit is set, the RB2/PWM1 pin is configured as PWM1 output and forced as an output irrespective of the data direction bit (DDRB<2>). When the PWM1ON bit is clear, the pin behaves as a port pin and its direction is controlled by its data direction bit (DDRB<2>). Similarly, the PWM2ON (TCON2<5>) bit controls the configuration of the RB3/PWM2 pin.

FIGURE 12-5: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time-base.

FIGURE 12-6: PWM OUTPUT



Note The dotted line shows PWM output if duty cycle registers were not double buffered. If the new duty cycle is written after the timer has passed that value, then the PWM does not reset at all during the current cycle causing a "glitch".

In this example, PWM period = 50. Old duty cycle is 30. New duty cycle value is 10.

12.1.3.1 PWM PERIODS

The period of the PWM1 output is determined by Timer1 and its period register (PR1). The period of the PWM2 output can be software configured to use either Timer1 or Timer2 as the time-base. When TM2PW2 bit (PW2DCL<5>) is clear, the time-base is determined by TMR1 and PR1. When TM2PW2 is set, the time-base is determined by Timer2 and PR2.

Running two different PWM outputs on two different timers allows different PWM periods. Running both PWMs from Timer1 allows the best use of resources by freeing Timer2 to operate as an 8-bit timer. Timer1 and Timer2 can not be used as a 16-bit timer if either PWM is being used.

The PWM periods can be calculated as follows:

period of PWM1 =[(PR1) + 1] x 4TOSC

period of PWM2 =[(PR1) + 1] x 4TOSC or
[(PR2) + 1] x 4TOSC

The duty cycle of PWMx is determined by the 10-bit value DCx<9:0>. The upper 8-bits are from register PWxDCH and the lower 2-bits are from PWxDCL<7:6> (PWxDCH:PWxDCL<7:6>). Table 12-3 shows the maximum PWM frequency (FPWM) given the value in the period register.

The number of bits of resolution that the PWM can achieve depends on the operation frequency of the device as well as the PWM frequency (FPWM).

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)} \text{ bits}$$

The PWMx duty cycle is as follows:

PWMx Duty Cycle = (DCx) x TOSC

where DCx represents the 10-bit value from PWxDCH:PWxDCL.

If DCx = 0, then the duty cycle is zero. If PRx = PWxDCH, then the PWM output will be low for one to four Q-clock (depending on the state of the PWxDCL<7:6> bits). For a Duty Cycle to be 100%, the PWxDCH value must be greater then the PRx value.

The duty cycle registers for both PWM outputs are double buffered. When the user writes to these registers, they are stored in master latches. When TMR1 (or TMR2) overflows and a new PWM period begins, the master latch values are transferred to the slave latches and the PWMx pin is forced high.

Note: For PW1DCH, PW1DCL, PW2DCH and PW2DCL registers, a write operation writes to the "master latches" while a read operation reads the "slave latches". As a result, the user may not read back what was just written to the duty cycle registers.

The user should also avoid any "read-modify-write" operations on the duty cycle registers, such as: `ADDWF PW1DCH`. This may cause duty cycle outputs that are unpredictable.

TABLE 12-3: PWM FREQUENCY vs. RESOLUTION AT 25 MHz

PWM Frequency	Frequency (kHz)				
	24.4	48.8	65.104	97.66	390.6
PRx Value	0xFF	0x7F	0x5F	0x3F	0x0F
High Resolution	10-bit	9-bit	8.5-bit	8-bit	6-bit
Standard Resolution	8-bit	7-bit	6.5-bit	6-bit	4-bit

12.1.3.2 PWM INTERRUPTS

The PWM module makes use of TMR1 or TMR2 interrupts. A timer interrupt is generated when TMR1 or TMR2 equals its period register and is cleared to zero. This interrupt also marks the beginning of a PWM cycle. The user can write new duty cycle values before the timer roll-over. The TMR1 interrupt is latched into the TMR1IF bit and the TMR2 interrupt is latched into the TMR2IF bit. These flags must be cleared in software.

12.1.3.3 EXTERNAL CLOCK SOURCE

The PWMs will operate regardless of the clock source of the timer. The use of an external clock has ramifications that must be understood. Because the external TCLK12 input is synchronized internally (sampled once per instruction cycle), the time TCLK12 changes to the time the timer increments will vary by as much as TCY (one instruction cycle). This will cause jitter in the duty cycle as well as the period of the PWM output.

This jitter will be ±TCY, unless the external clock is synchronized with the processor clock. Use of one of the PWM outputs as the clock source to the TCLKx input, will supply a synchronized clock.

In general, when using an external clock source for PWM, its frequency should be much less than the device frequency (Fosc).

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12.1.3.3.1 MAX RESOLUTION/FREQUENCY FOR EXTERNAL CLOCK INPUT

The use of an external clock for the PWM time-base (Timer1 or Timer2) limits the PWM output to a maximum resolution of 8-bits. The PWxDCL<7:6> bits must be kept cleared. Use of any other value will distort the PWM output. All resolutions are supported when internal clock mode is selected. The maximum attainable frequency is also lower. This is a result of the timing requirements of an external clock input for a timer (see the Electrical Specification section). The maximum PWM frequency, when the timers clock source is the RB4/TCLK12 pin, is shown in Table 12-3 (standard resolution mode).

12.2 Timer3

Timer3 is a 16-bit timer consisting of the TMR3H and TMR3L registers. TMR3H is the high byte of the timer and TMR3L is the low byte. This timer has an associated 16-bit period register (PR3H/CA1H:PR3L/CA1L). This period register can be software configured to be a second 16-bit capture register.

When the TMR3CS bit (TCON1<2>) is clear, the timer increments every instruction cycle (Fosc/4). When TMR3CS is set, the timer increments on every falling edge of the RB5/TCLK3 pin. In either mode, the TMR3ON bit must be set for the timer to increment. When TMR3ON is clear, the timer will not increment or set the TMR3IF bit.

Timer3 has two modes of operation, depending on the CA1/$\overline{PR3}$ bit (TCON2<3>). These modes are:

- One capture and one period register mode
- Dual capture register mode

The PIC17C4X has up to two 16-bit capture registers that capture the 16-bit value of TMR3 when events are detected on capture pins. There are two capture pins (RB0/CAP1 and RB1/CAP2), one for each capture register. The capture pins are multiplexed with PORTB pins. An event can be:

- a rising edge
- a falling edge
- every 4th rising edge
- every 16th rising edge

Each 16-bit capture register has an interrupt flag associated with it. The flag is set when a capture is made. The capture module is truly part of the Timer3 block. Figure 12-7 and Figure 12-8 show the block diagrams for the two modes of operation.

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TABLE 12-4: REGISTERS/BITS ASSOCIATED WITH PWM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{PR3}$	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
10h, Bank 2	TMR1	Timer1 register								xxxx xxxx	uuuu uuuu
11h, Bank 2	TMR2	Timer2 register								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	—	—	--11 11--	--11 qq--
10h, Bank 3	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx-- ----	uu-- ----
11h, Bank 3	PW2DCL	DC1	DC0	TM2PW2	—	—	—	—	—	xx0- ----	uu0- ----
12h, Bank 3	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h, Bank 3	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on conditions, shaded cells are not used by PWM.

12.2.1 ONE CAPTURE AND ONE PERIOD REGISTER MODE

In this mode registers PR3H/CA1H and PR3L/CA1L constitute a 16-bit period register. A block diagram is shown in Figure 12-7. The timer increments until it equals the period register and then resets to 0000h. TMR3 Interrupt Flag bit (TMR3IF) is set at this point. This interrupt can be disabled by clearing the TMR3 Interrupt Enable bit (TMR3IE). TMR3IF must be cleared in software.

This mode is selected if control bit CA1/$\overline{PR3}$ is clear. In this mode, the Capture1 register, consisting of high byte (PR3H/CA1H) and low byte (PR3L/CA1L), is configured as the period control register for TMR3. Capture1 is disabled in this mode, and the corresponding Interrupt bit CA1IF is never set. TMR3 increments until it equals the value in the period register and then resets to 0000h.

Capture2 is active in this mode. The CA2ED1 and CA2ED0 bits determine the event on which capture will occur. The possible events are:

- Capture on every falling edge
- Capture on every rising edge
- Capture every 4th rising edge
- Capture every 16th rising edge

When a capture takes place, an interrupt flag is latched into the CA2IF bit. This interrupt can be enabled by setting the corresponding mask bit CA2IE. The Peripheral Interrupt Enable bit (PEIE) must be set and the Global Interrupt Disable bit (GLINTD) must be cleared for the interrupt to be acknowledged. The CA2IF interrupt flag bit must be cleared in software.

When the capture prescale select is changed, the prescaler is not reset and an event may be generated. Therefore, the first capture after such a change will be ambiguous. However, it sets the time-base for the next capture. The prescaler is reset upon chip reset.

Capture pin RB1/CAP2 is a multiplexed pin. When used as a port pin, Capture2 is not disabled. However, the user can simply disable the Capture2 interrupt by clearing CA2IE. If RB1/CAP2 is used as an output pin, the user can activate a capture by writing to the port pin. This may be useful during development phase to emulate a capture interrupt.

The input on capture pin RB1/CAP2 is synchronized internally to internal phase clocks. This imposes certain restrictions on the input waveform (see the Electrical Specification section for timing).

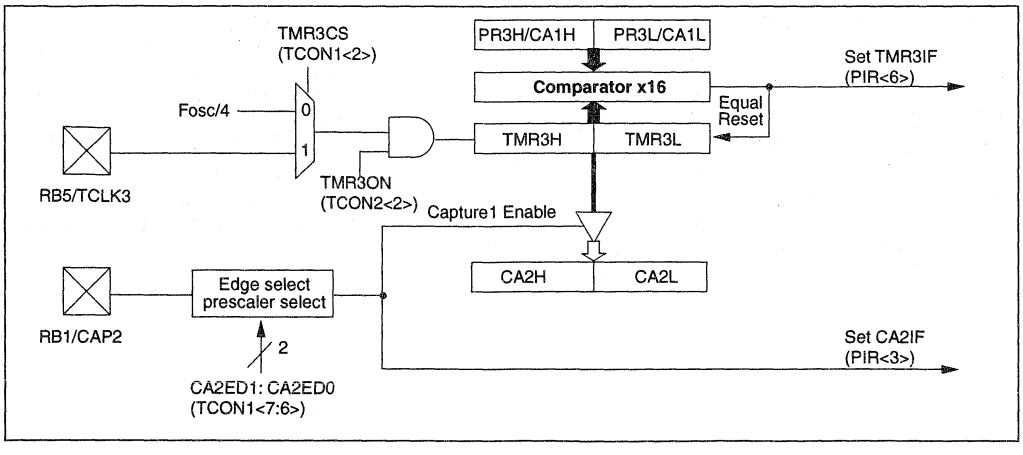
The Capture2 overflow status flag bit is double buffered. The master bit is set if one captured word is already residing in the Capture2 register and another "event" has occurred on the RB1/CA2 pin. The new event will not transfer the Timer3 value to the capture register, protecting the previous unread capture value. When the user reads both the high and the low bytes (in any order) of the Capture2 register, the master overflow bit is transferred to the slave overflow bit (CA2OVF) and then the master bit is reset. The user can then read TCON2 to determine the value of CA2OVF.

The recommended sequence to read capture registers and capture overflow flag bits is shown in Example 12-1.

EXAMPLE 12-1: SEQUENCE TO READ CAPTURE REGISTERS

```
MOVLB 3                 ;Select Bank 3
MOVPF CA2L,LO_BYTE      ;Read Capture2 low
                        ;byte, store in LO_BYTE
MOVPF CA2H,HI_BYTE      ;Read Capture2 high
                        ;byte, store in HI_BYTE
MOVPF TCON2,STAT_VAL    ;Read TCON2 into file
                        ;STAT_VAL
```

FIGURE 12-7: TIMER3 WITH ONE CAPTURE AND ONE PERIOD REGISTER BLOCK DIAGRAM



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12.2.2 DUAL CAPTURE REGISTER MODE

This mode is selected by setting CA1/$\overline{PR3}$. A block diagram is shown in Figure 12-8. In this mode, TMR3 runs without a period register and increments from 0000h to FFFFh and rolls over to 0000h. The TMR3 interrupt Flag (TMR3IF) is set on this roll over. The TMR3IF bit must be cleared in software.

Registers PR3H/CA1H and PR3L/CA1L make a 16-bit capture register (Capture1). It captures events on pin RB0/CAP1. Capture mode is configured by the CA1ED1 and CA1ED0 bits. Capture1 Interrupt Flag bit (CA1IF) is set on the capture event. The corresponding interrupt mask bit is CA1IE. The Capture1 Overflow Status bit is CA1OVF.

The Capture2 overflow status flag bit is double buffered. The master bit is set if one captured word is already residing in the Capture2 register and another "event" has occurred on the RB1/CA2 pin. The new event will not transfer the TMR3 value to the capture register which protects the previous unread capture value. When the user reads both the high and the low bytes (in any order) of the Capture2 register, the master overflow bit is transferred to the slave overflow bit (CA2OVF) and then the master bit is reset. The user can then read TCON2 to determine the value of CA2OVF.

The operation of the Capture1 feature is identical to Capture2 (as described in Section 12.2.1).

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FIGURE 12-8: TIMER3 WITH TWO CAPTURE REGISTERS BLOCK DIAGRAM

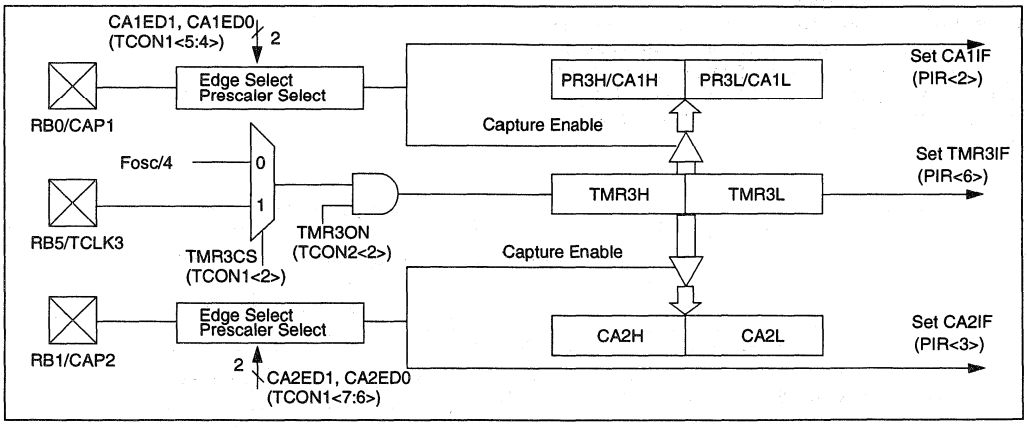


TABLE 12-5: REGISTERS ASSOCIATED WITH CAPTURE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{PR3}$	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
12h, Bank 2	TMR3L	TMR3 register; low byte								xxxx xxxx	uuuu uuuu
13h, Bank 2	TMR3H	TMR3 register; high byte								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	---	---	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	---	---	--11 11--	--11 qq--
16h, Bank 2	PR3L/CA1L	Timer3 period register, low byte/capture1 register, low byte								xxxx xxxx	uuuu uuuu
17h, Bank 2	PR3H/CA1H	Timer3 period register, high byte/capture1 register, high byte								xxxx xxxx	uuuu uuuu
14h, Bank 3	CA2L	Capture2 low byte								xxxx xxxx	uuuu uuuu
15h, Bank 3	CA2H	Capture2 high byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q - value depends on condition, shaded cells are not used by Capture.

Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and WDT Timer Reset.

12.2.3 EXTERNAL CLOCK INPUT FOR TIMER3

When TMR3CS is set, the 16-bit TMR3 increments on the falling edge of clock input TCLK3. The input on the RB5/TCLK3 pin is sampled and synchronized by the internal phase clocks twice every instruction cycle. This causes a delay from the time a falling edge appears on TCLK3 to the time TMR3 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section. Figure 12-9 shows the timing diagram when operating from an external clock.

12.2.4 READING/WRITING TIMER3

Since Timer3 is a 16-bit timer and only 8-bits at a time can be read or written, care should be taken when reading or writing while the timer is running. The best method to read or write the timer is to stop the timer, perform any read or write operation, and then restart Timer3 (using the TMR3ON bit). However, if it is necessary to keep Timer3 free-running, care must be taken. For writing to the 16-bit TMR3, Example 12-2 may be used. For reading the 16-bit TMR3, Example 12-3 may be used. Interrupts must be disabled during this routine.

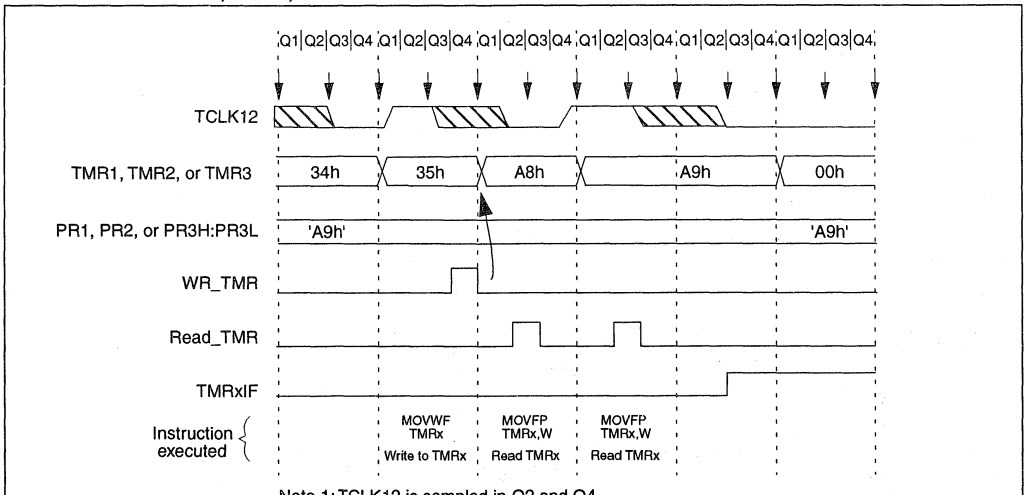
EXAMPLE 12-2: WRITING TO TMR3

```
BSF    CPUSTA, GLINTD ;Disable interrupt
MOVFP  RAM_L,  TMR3L  ;
MOVFP  RAM_H,  TMR3H  ;
BCF    CPUSTA, GLINTD ;Done,enable interrupt
```

EXAMPLE 12-3: READING FROM TMR3

```
MOVPF   TMR3L, TMPLO    ;read low tmr0
MOVPF   TMR3H, TMPHI    ;read high tmr0
MOVFP   TMPLO, WREG     ;tmplo -> wreg
CPFSLT  TMR3L, WREG     ;tmr0l < wreg?
RETURN                  ;no then return
MOVPF   TMR3L, TMPLO    ;read low tmr0
MOVPF   TMR3H, TMPHI    ;read high tmr0
RETURN                  ;return
```

FIGURE 12-9: TMR1, TMR2, AND TMR3 OPERATION IN EXTERNAL CLOCK MODE



Note 1: TCLK12 is sampled in Q2 and Q4.
2: ↓ indicates a sampling point.
3: The latency from TCLK12 ↓ to timer increment is between 2Tosc and 6Tosc.

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FIGURE 12-10: TMR1, TMR2, AND TMR3 OPERATION IN TIMER MODE

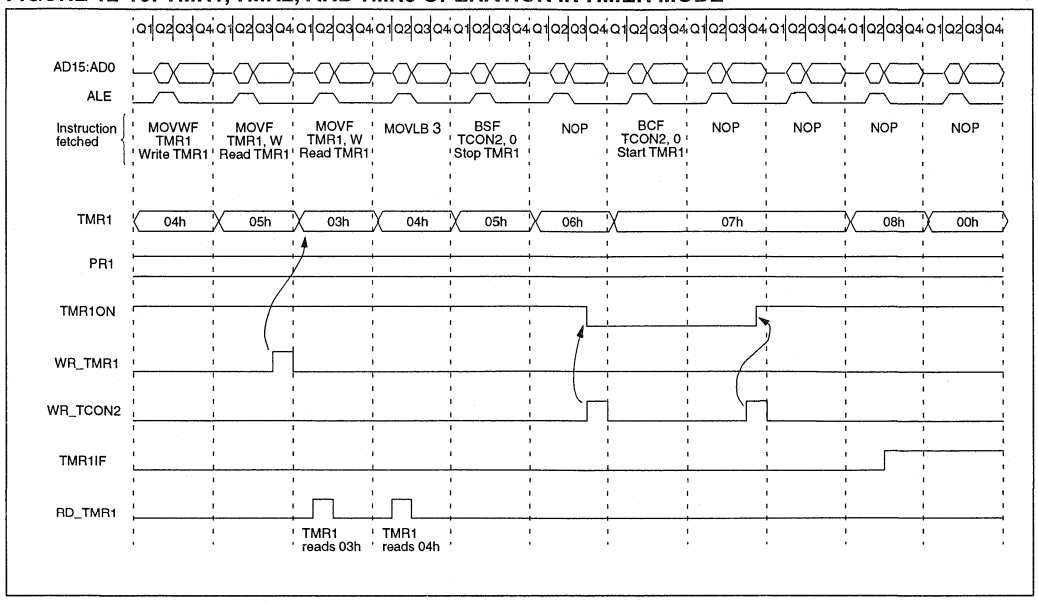

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TABLE 12-6: SUMMARY OF TMR1, TMR2, AND TMR3 REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{PR3}$	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
10h, Bank 2	TMR1	Timer1 register								xxxx xxxx	uuuu uuuu
11h, Bank 2	TMR2	Timer2 register								xxxx xxxx	uuuu uuuu
12h, Bank 2	TMR3L	TMR3 register; low byte								xxxx xxxx	uuuu uuuu
13h, Bank 2	TMR3H	TMR3 register; high byte								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	—	—	--11 11--	--11 qq--
14h, Bank 2	PR1	Timer1 period register								xxxx xxxx	uuuu uuuu
15h, Bank 2	PR2	Timer2 period register								xxxx xxxx	uuuu uuuu
16h, Bank 2	PR3L/CA1L	Timer3 period/capture1 register; low byte								xxxx xxxx	uuuu uuuu
17h, Bank 2	PR3H/CA1H	Timer3 period/capture1 register; high byte								xxxx xxxx	uuuu uuuu
10h, Bank 3	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx-- ----	uu-- ----
11h, Bank 3	PW2DCL	DC1	DC0	TM2PW2	—	—	—	—	—	xx0- ----	uu0- ----
12h, Bank 3	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h, Bank 3	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
14h, Bank 3	CA2L	Capture2 low byte								xxxx xxxx	uuuu uuuu
15h, Bank 3	CA2H	Capture2 high byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q - value depends on condition, shaded cells are not used by TMR1, TMR2 or TMR3.

Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and WDT Timer Reset.

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NOTES:

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13.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART) MODULE

The USART module is a serial I/O module. The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc. The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

The SPEN (RCSTA<7>) bit has to be set in order to configure RA4 and RA5 as the Serial Communication Interface.

The USART module will control the direction of the RA4/RX/DT and RA5/TX/CK pins, depending on the states of the USART configuration bits in the RCSTA and TXSTA registers. The bits that control I/O direction are:

- SPEN
- TXEN
- SREN
- CREN
- CSRC

The Transmit Status And Control Register is shown in Figure 13-1, while the Receive Status And Control Register is shown in Figure 13-2.

FIGURE 13-1: TXSTA REGISTER (ADDRESS: 15h, BANK 0)

R/W - 0	R/W - 0	R/W - 0	R/W - 0	U - 0	U - 0	R - 1	R/W - x
CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D
bit7							bit0

R = Readable bit
W = Writable bit
-n = Value at POR reset
(x = unknown)

bit 7: **CSRC**: Clock Source Select bit
Synchronous mode:
1 = Master Mode (Clock generated internally from BRG)
0 = Slave mode (Clock from external source)
Asynchronous mode:
Don't care

bit 6: **TX9**: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5: **TXEN**: Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled
SREN/CREN overrides TXEN in SYNC mode

bit 4: **SYNC**: USART mode Select bit
(Synchronous/Asynchronous)
1 = Synchronous mode
0 = Asynchronous mode

bit 3-2: **Unimplemented**: Read as '0'

bit 1: **TRMT**: Transmit Shift Register (TSR) Empty bit
1 = TSR empty
0 = TSR full

bit 0: **TX9D**: 9th bit of transmit data (can be used to calculated the parity in software)

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FIGURE 13-2: RCSTA REGISTER (ADDRESS: 13h, BANK 0)

R/W - 0	R/W - 0	R/W - 0	R/W - 0	U - 0	R - 0	R - 0	R - x
SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D
bit7							bit 0

R = Readable bit
W = Writable bit
-n = Value at POR reset
(x = unknown)

bit 7: **SPEN**: Serial Port Enable bit
1 = Configures RA5/RX/DT and RA4/TX/CK pins as serial port pins
0 = Serial port disabled

bit 6: **RX9**: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5: **SREN**: Single Receive Enable bit
This bit enables the reception of a single byte. After receiving the byte, this bit is automatically cleared.
Synchronous mode:
1 = Enable reception
0 = Disable reception
Note: This bit is ignored in synchronous slave reception.
Asynchronous mode:
Don't care

bit 4: **CREN**: Continuous Receive Enable bit
This bit enables the continuous reception of serial data.
Asynchronous mode:
1 = Enable reception
0 = Disables reception
Synchronous mode:
1 = Enables continuous reception until CREN is cleared (CREN overrides SREN)
0 = Disables continuous reception

bit 3: **Unimplemented**: Read as '0'

bit 2: **FERR**: Framing Error bit
1 = Framing error (Updated by reading RCREG)
0 = No framing error

bit 1: **OERR**: Overrun Error bit
1 = Overrun (Cleared by clearing CREN)
0 = No overrun error

bit 0: **RX9D**: 9th bit of receive data (can be the software calculated parity bit)

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FIGURE 13-3: USART TRANSMIT

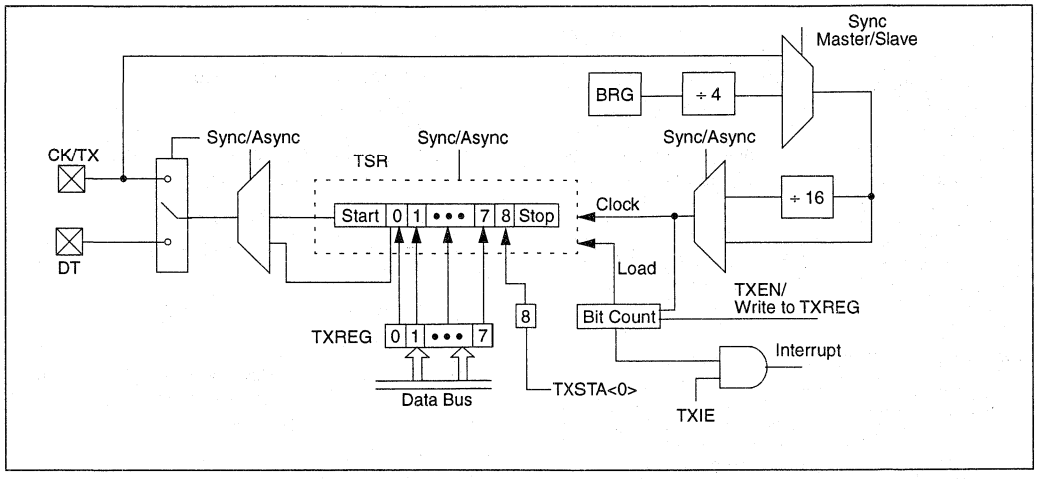
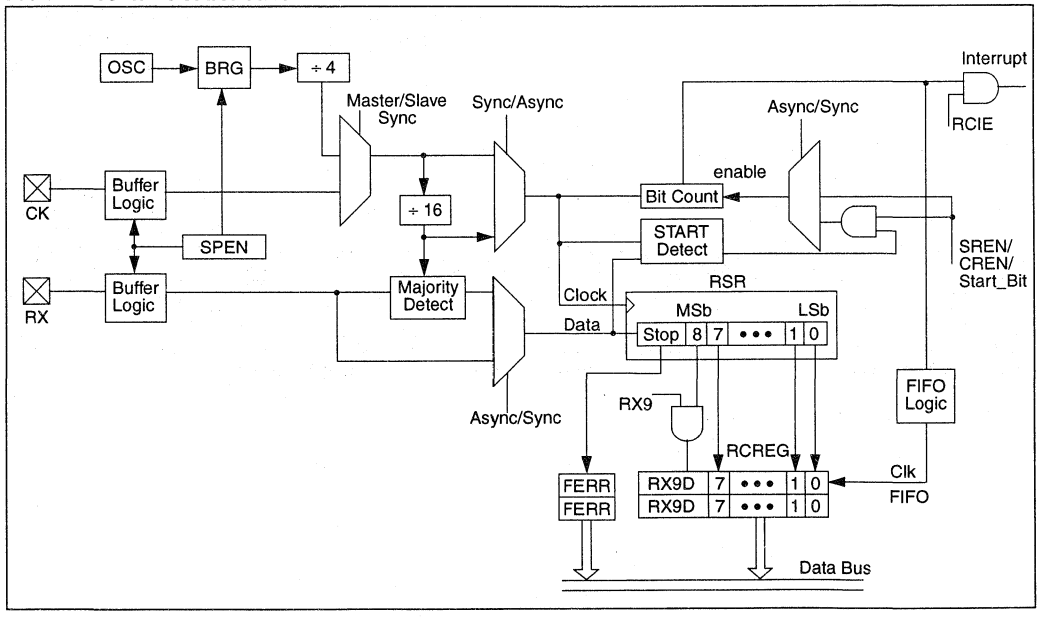


FIGURE 13-4: USART RECEIVE



13.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. Table 13-1 shows the formula for computation of the baud rate for different USART modes. These only apply when the USART is in synchronous master mode (internal clock) and asynchronous mode.

Given the desired baud rate and Fosc, the nearest integer value between 0 and 255 can be calculated using the formula below. The error in baud rate can then be determined.

TABLE 13-1: BAUD RATE FORMULA

SYNC	Mode	Baud Rate
0	Asynchronous	Fosc/(64(X+1))
1	Synchronous	Fosc/(4(X+1))

X = value in SPBRG (0 to 255)

Example 13-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz
Desired Baud Rate = 9600
SYNC = 0

EXAMPLE 13-1: CALCULATING BAUD RATE ERROR

Desired Baud rate=Fosc / (64 (X + 1))

9600 = 16000000 /(64 (X + 1))

X = 25.042 = 25

Calculated Baud Rate=16000000 / (64 (25 + 1))

= 9615

$$\text{Error} = \frac{\text{(Calculated Baud Rate - Desired Baud Rate)}}{\text{Desired Baud Rate}}$$

= (9615 - 9600) / 9600

= 0.16%

Writing a new value to the SPBRG, causes the BRG timer to be reset (or cleared), this ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

TABLE 13-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used by the Baud Rate Generator.
Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

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TABLE 13-3: BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	FOSC = 33 MHz			FOSC = 25 MHz			FOSC = 20 MHz			FOSC = 16 MHz		
	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	—	—	NA	—	—	NA	—	—	NA	—	—
1.2	NA	—	—	NA	—	—	NA	—	—	NA	—	—
2.4	NA	—	—	NA	—	—	NA	—	—	NA	—	—
9.6	NA	—	—	NA	—	—	NA	—	—	NA	—	—
19.2	NA	—	—	NA	—	—	19.53	+1.73	255	19.23	+0.16	207
76.8	77.10	+0.39	106	77.16	+0.47	80	76.92	+0.16	64	76.92	+0.16	51
96	95.93	-0.07	85	96.15	+0.16	64	96.15	+0.16	51	95.24	-0.79	41
300	294.64	-1.79	27	297.62	-0.79	20	294.1	-1.96	16	307.69	+2.56	12
500	485.29	-2.94	16	480.77	-3.85	12	500	0	9	500	0	7
HIGH	8250	—	0	6250	—	0	5000	—	0	4000	—	0
LOW	32.22	—	255	24.41	—	255	19.53	—	255	15.625	—	255

BAUD RATE (K)	FOSC = 10 MHz			FOSC = 7.159 MHz			FOSC = 5.068 MHz		
	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	—	—	NA	—	—	NA	—	—
1.2	NA	—	—	NA	—	—	NA	—	—
2.4	NA	—	—	NA	—	—	NA	—	—
9.6	9.766	+1.73	255	9.622	+0.23	185	9.6	0	131
19.2	19.23	+0.16	129	19.24	+0.23	92	19.2	0	65
76.8	75.76	-1.36	32	77.82	+1.32	22	79.2	+3.13	15
96	96.15	+0.16	25	94.20	-1.88	18	97.48	+1.54	12
300	312.5	+4.17	7	298.3	-0.57	5	316.8	+5.60	3
500	500	0	4	NA	—	—	NA	—	—
HIGH	2500	—	0	1789.8	—	0	1267	—	0
LOW	9.766	—	255	6.991	—	255	4.950	—	255

BAUD RATE (K)	FOSC = 3.579 MHz			FOSC = 1 MHz			FOSC = 32.768 kHz		
	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	—	—	NA	—	—	0.303	+1.14	26
1.2	NA	—	—	1.202	+0.16	207	1.170	-2.48	6
2.4	NA	—	—	2.404	+0.16	103	NA	—	—
9.6	9.622	+0.23	92	9.615	+0.16	25	NA	—	—
19.2	19.04	-0.83	46	19.24	+0.16	12	NA	—	—
76.8	74.57	-2.90	11	83.34	+8.51	2	NA	—	—
96	99.43	-3.57	8	NA	—	—	NA	—	—
300	298.3	-0.57	2	NA	—	—	NA	—	—
500	NA	—	—	NA	—	—	NA	—	—
HIGH	894.9	—	0	250	—	0	8.192	—	0
LOW	3.496	—	255	0.976	—	255	0.032	—	255

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TABLE 13-4: BAUD RATES FOR ASYNCHRONOUS MODE

BAUD RATE (K)	Fosc = 33 MHz			Fosc = 25 MHz			Fosc = 20 MHz			Fosc = 16 MHz		
	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	—	—	NA	—	—	NA	—	—	NA	—	—
1.2	NA	—	—	NA	—	—	1.221	+1.73	255	1.202	+0.16	207
2.4	2.398	-0.07	214	2.396	0.14	162	2.404	+0.16	129	2.404	+0.16	103
9.6	9.548	-0.54	53	9.53	-0.76	40	9.469	-1.36	32	9.615	+0.16	25
19.2	19.09	-0.54	26	19.53	+1.73	19	19.53	+1.73	15	19.23	+0.16	12
76.8	73.66	-4.09	6	78.13	+1.73	4	78.13	+1.73	3	83.33	+8.51	2
96	103.12	+7.42	4	97.65	+1.73	3	104.2	+8.51	2	NA	—	—
300	257.81	-14.06	1	390.63	+30.21	0	312.5	+4.17	0	NA	—	—
500	515.62	+3.13	0	NA	—	—	NA	—	—	NA	—	—
HIGH	515.62	—	0	—	—	0	312.5	—	0	250	—	0
LOW	2.014	—	255	1.53	—	255	1.221	—	255	0.977	—	255

BAUD RATE (K)	Fosc = 10 MHz			Fosc = 7.159 MHz			Fosc = 5.068 MHz		
	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	—	—	NA	—	—	0.31	+3.13	255
1.2	1.202	+0.16	129	1.203	_0.23	92	1.2	0	65
2.4	2.404	+0.16	64	2.380	-0.83	46	2.4	0	32
9.6	9.766	+1.73	15	9.322	-2.90	11	9.9	-3.13	7
19.2	19.53	+1.73	7	18.64	-2.90	5	19.8	+3.13	3
76.8	78.13	+1.73	1	NA	—	—	79.2	+3.13	0
96	NA	—	—	NA	—	—	NA	—	—
300	NA	—	—	NA	—	—	NA	—	—
500	NA	—	—	NA	—	—	NA	—	—
HIGH	156.3	—	0	111.9	—	0	79.2	—	0
LOW	0.610	—	255	0.437	—	255	0.309	—	255

BAUD RATE (K)	Fosc = 3.579 MHz			Fosc = 1 MHz			Fosc = 32.768 kHz		
	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)	KBAUD	%ERROR	SPBRG value (decimal)
0.3	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.190	-0.83	46	1.202	+0.16	12	NA	—	—
2.4	2.432	+1.32	22	2.232	-6.99	6	NA	—	—
9.6	9.322	-2.90	5	NA	—	—	NA	—	—
19.2	18.64	-2.90	2	NA	—	—	NA	—	—
76.8	NA	—	—	NA	—	—	NA	—	—
96	NA	—	—	NA	—	—	NA	—	—
300	NA	—	—	NA	—	—	NA	—	—
500	NA	—	—	NA	—	—	NA	—	—
HIGH	55.93	—	0	15.63	—	0	0.512	—	0
LOW	0.218	—	255	0.061	—	255	0.002	—	255

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13.2 USART Asynchronous Mode

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits, and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock x64 of the bit shift rate. Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

The asynchronous mode is selected by clearing the SYNC bit (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

13.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 13-3. The heart of the transmitter is the transmit shift register (TSR). The shift register obtains its data from the read/write transmit buffer (TXREG). TXREG is loaded with data in software. The TSR is not loaded until the stop bit has been transmitted from the previous load. As soon as the stop bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once TXREG transfers the data to the TSR (occurs in one TCY at the end of the current BRG cycle), the TXREG is empty and an interrupt bit, TXIF (PIR<1>) is set. This interrupt can be enabled or disabled by the TXIE bit (PIE<1>). TXIF will be set regardless of TXIE and cannot be reset in software. It will reset only when new data is loaded into TXREG. While TXIF indicates the status of the TXREG, the TRMT (TXSTA<1>) bit shows the status of the TSR. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR is empty.

Note:	The TSR is not mapped in data memory, so it is not available to the user.

Transmission is enabled by setting the TXEN (TXSTA<5>) bit. The actual transmission will not occur until TXREG has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 13-5). The transmission can also be started by first loading TXREG and then setting TXEN. Normally when transmission is first started, the TSR is empty, so a transfer to TXREG will result in an immediate transfer to TSR resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 13-6). Clearing TXEN during a transmission will cause the transmission to be aborted. This will reset the transmitter and the RA5/TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG. This is because a data write to TXREG can result in an immediate transfer of the data to the TSR (if the TSR is empty).

Steps to follow when setting up an Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate.
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If interrupts are desired, then set the TXIE bit.
4. If 9-bit transmission is desired, then set the TX9 bit.
5. Load data to the TXREG register.
6. If 9-bit transmission is selected, the ninth bit should be loaded in TX9D.
7. Enable the transmission by setting TXEN (starts transmission).

Writing the transmit data to the TXREG, then enabling the transmit (setting TXEN) allows transmission to start sooner then doing these two events in the opposite order.

Note:	To terminate a transmission, either clear the SPEN bit, or the TXEN bit. This will reset the transmit logic, so that it will be in the proper state when transmit is re-enabled.

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FIGURE 13-5: ASYNCHRONOUS MASTER TRANSMISSION

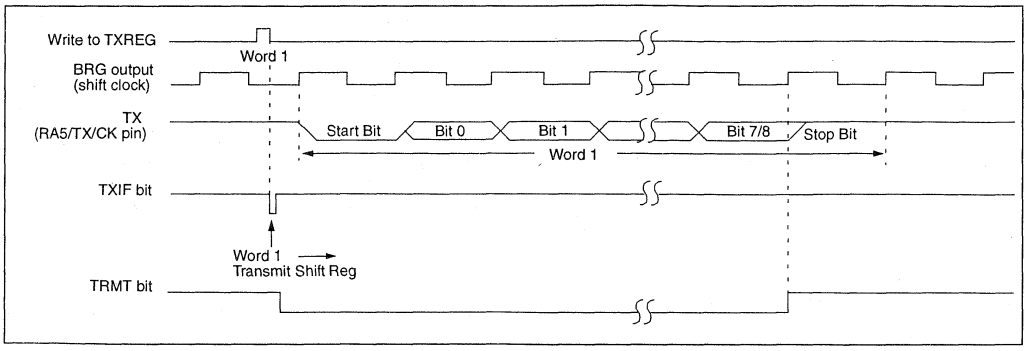
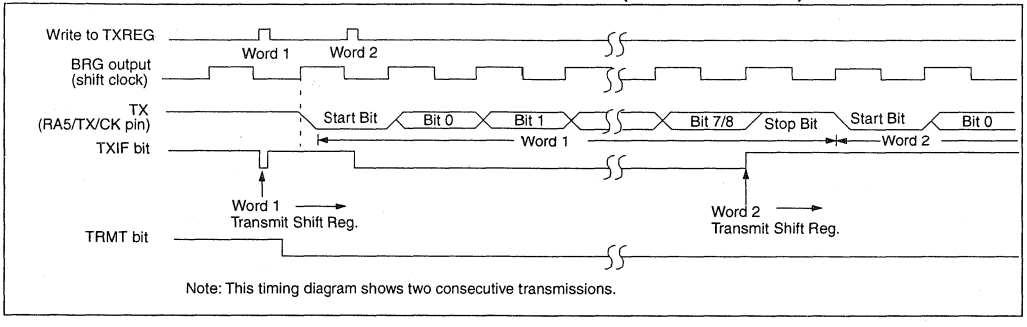


FIGURE 13-6: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 13-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 0	TXREG	Serial port transmit register								xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for asynchronous transmission.

Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

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13.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 13-4. The data comes in the RA4/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at 16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at FOSC.

Once asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the stop bit, the received data in the RSR is transferred to the RCREG (if it is empty). If the transfer is complete, the interrupt bit RCIF (PIR<0>) is set. The actual interrupt can be enabled/disabled by setting/clearing the RCIE (PIE<0>) bit. RCIF is a read only bit which is cleared by the hardware. It is cleared when RCREG has been read and is empty. RCREG is a double buffered register; (i.e. it is a two deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR. On detection of the stop bit of the third byte, if the RCREG is still full, then the overrun error bit, OERR (RCSTA<1>) will be set. The word in the RSR will be lost. RCREG can be read twice to retrieve the two bytes in the FIFO. The OERR bit has to be cleared in software which is done by resetting the receive logic (CREN is set). If the OERR bit is set, transfers from the RSR to RCREG are inhibited, so it is essential to clear the OERR bit if it is set. The framing error bit FERR (RCSTA<2>) is set if a stop bit is not detected.

Note: The FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG register will allow the RX9D and FERR bits to be loaded with values for the next received Received data; therefore, it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old FERR and RX9D information.

13.2.3 SAMPLING

The data on the RA4/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RA4/RX/DT pin. The sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 11-3).

The x16 clock is a free running clock, and the three sample points occur at a frequency of every 16 falling edges.

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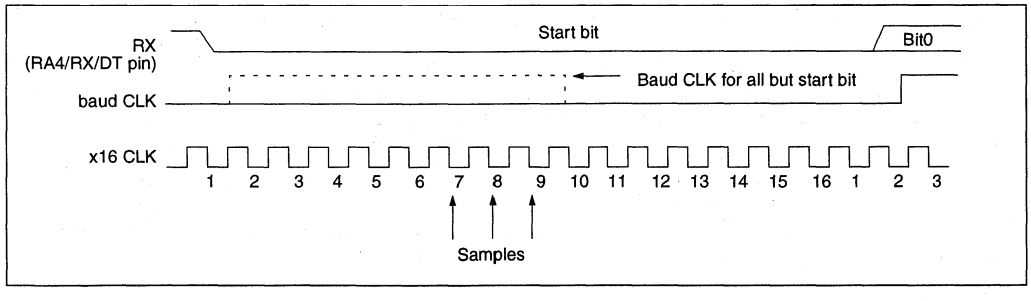
FIGURE 13-7: RX PIN SAMPLING SCHEME

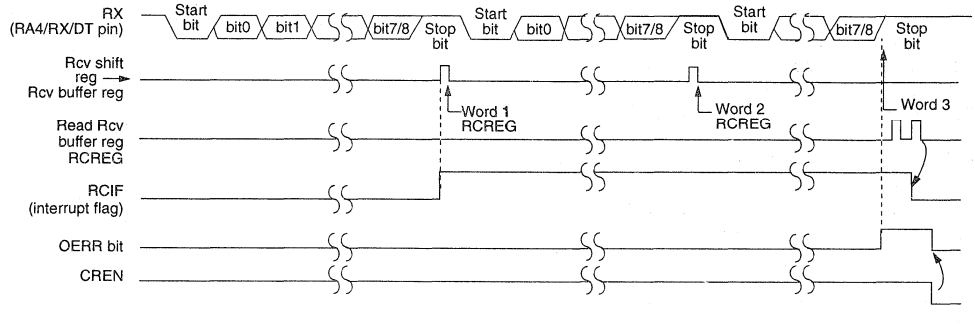


Steps to follow when setting up an Asynchronous Reception:

1. Initialize the SPBRG register for the appropriate baud rate.
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If interrupts are desired, then set the RCIE bit.
4. If 9-bit reception is desired, then set the RX9 bit.
5. Enable the reception by setting the CREN bit.
6. The RCIF bit will be set when reception completes and an interrupt will be generated if the RCIE bit was set.
7. Read RCSTA to get the ninth bit (if enabled) and FERR bit to determine if any error occurred during reception.
8. Read RCREG for the 8-bit received data.
9. If an overrun error occurred, clear the error by clearing the OERR bit.

Note: To terminate a reception, either clear the SREN and CREN bits, or the SPEN bit. This will reset the receive logic, so that it will be in the proper state when receive is re-enabled.

FIGURE 13-8: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

TABLE 13-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank 0	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for asynchronous reception.
Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and Watchdog Timer Reset.

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13.3 USART Synchronous Master Mode

In Master Synchronous mode, the data is transmitted in a half-duplex manner; i.e. transmission and reception do not occur at the same time: when transmitting data, the reception is inhibited and vice versa. The synchronous mode is entered by setting the SYNC (TXSTA<4>) bit. In addition, the SPEN (RCSTA<7>) bit is set in order to configure the RA5 and RA4 I/O ports to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting the CSRC (TXSTA<7>) bit.

13.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 13-3. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer TXREG. TXREG is loaded with data in software. The TSR is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from TXREG (if available). Once TXREG transfers the data to the TSR (occurs in one TCY at the end of the current BRG cycle), TXREG is empty and the TXIF (PIR<1>) bit is set. This interrupt can be enabled/disabled by setting/clearing the TXIE bit (PIE<1>). TXIF will be set regardless of the state of bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into TXREG. While TXIF indicates the status of TXREG, TRMT (TXSTA<1>) shows the status of the TSR. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR is empty. The TSR is not mapped in data memory, so it is not available to the user.

Transmission is enabled by setting the TXEN (TXSTA<5>) bit. The actual transmission will not occur until TXREG has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the RA5/TX/CK pin. Data out is stable around the falling edge of the synchronous clock (Figure 13-10). The transmission can also be started by first loading TXREG and then setting TXEN. This is advantageous when slow baud rates are selected, since BRG is kept in RESET when the TXEN, CREN, and SREN bits are clear. Setting the TXEN bit will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR is empty, so a transfer to TXREG will result in an immediate transfer to the TSR, resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. The RA4/RX/DT and RA5/TX/CK pins will revert to hi-impedance. If either CREN or SREN are set during a transmission, the transmission is aborted and the RA4/RX/DT pin reverts to a hi-impedance state (for a reception). The RA5/TX/CK pin will remain an output if the CSRC bit is set (internal clock). The transmitter logic is not reset, although it is disconnected from the pins. In order to reset the transmitter, the user has to clear the TXEN bit. If the SREN bit is set (to interrupt an ongoing transmission and receive a single word), then after the single word is received, SREN will be cleared and the serial port will revert back to transmitting, since the TXEN bit is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, TXEN should be cleared.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to TXREG. This is because a data write to TXREG can result in an immediate transfer of the data to the TSR (if the TSR is empty). If the TSR was empty and TXREG was written before writing the "new" TX9D, the "present" value of TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

1. Initialize the SPBRG register for the appropriate baud rate (see Baud Rate Generator Section for details).
2. Enable the synchronous master serial port by setting the SYNC, SPEN, and CSRC bits.
3. Ensure that the CREN and SREN bits are clear (these bits override transmission when set).
4. If interrupts are desired, then set the TXIE bit (the GLINTD bit must be clear and the PEIE bit must be set).
5. If 9-bit transmission is desired, then set the TX9 bit.
6. Start transmission by loading data to the TXREG register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in TX9D.
8. Enable the transmission by setting TXEN.

Writing the transmit data to the TXREG, then enabling the transmit (setting TXEN) allows transmission to start sooner then doing these two events in the reverse order.

Note:	To terminate a transmission, either clear the SPEN bit, or the TXEN bit. This will reset the transmit logic, so that it will be in the proper state when transmit is re-enabled.

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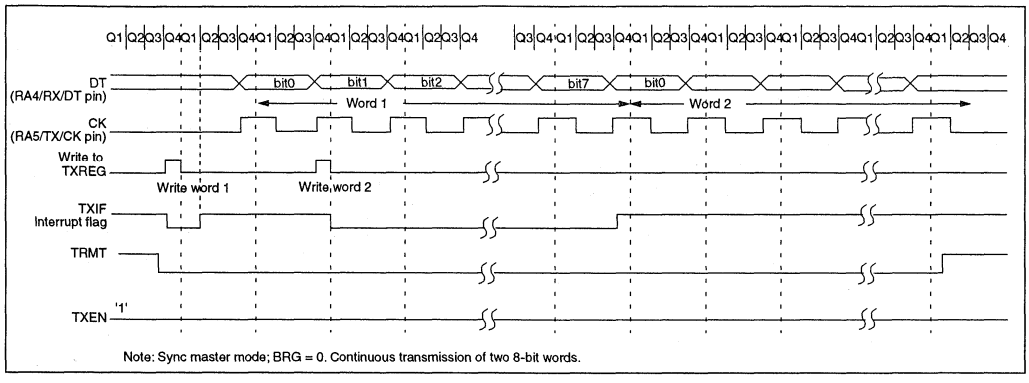
TABLE 13-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 0	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous master transmission.

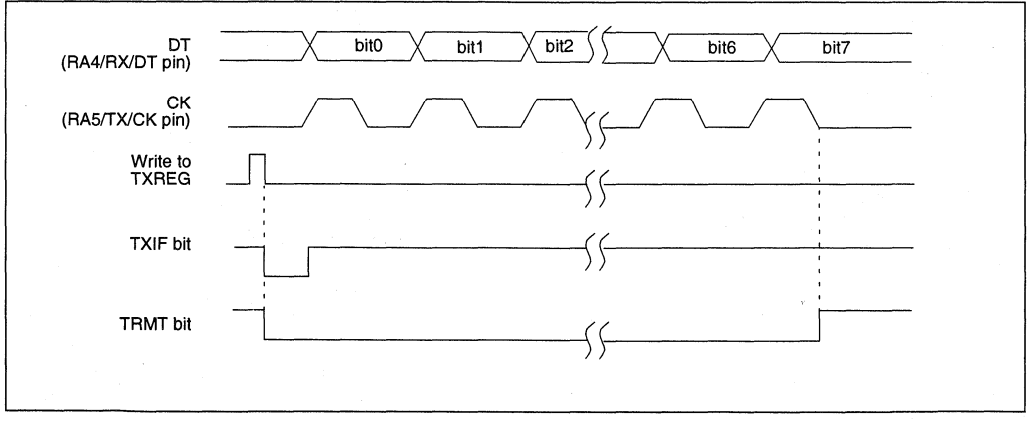
Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

FIGURE 13-9: SYNCHRONOUS TRANSMISSION



Note: Sync master mode; BRG = 0. Continuous transmission of two 8-bit words.

FIGURE 13-10: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



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13.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once synchronous mode is selected, reception is enabled by setting either the SREN (RCSTA<5>) bit or the CREN (RCSTA<4>) bit. Data is sampled on the RA4/RX/DT pin on the falling edge of the clock. If SREN is set, then only a single word is received. If CREN is set, the reception is continuous until CREN is reset. If both bits are set, then CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to RCREG (if it is empty). If the transfer is complete, the interrupt bit RCIF (PIR<0>) is set. The actual interrupt can be enabled/disabled by setting/clearing the RCIE (PIE<0>) bit. RCIF is a read only bit which is RESET by the hardware. In this case it is reset when RCREG has been read and is empty. RCREG is a double buffered register; i.e., it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR. On the clocking of the last bit of the third byte, if RCREG is still full, then the overrun error bit OERR (RCSTA<1>) is set. The word in the RSR will be lost. RCREG can be read twice to retrieve the two bytes in the FIFO. The OERR bit has to be cleared in software. This is done by clearing the CREN bit. If OERR bit is set, transfers from RSR to RCREG are inhibited, so it is essential to clear OERR bit if it is set. The 9th receive bit is buffered the same way as the receive data. Reading the RCREG register will allow the RX9D and FERR bits to be loaded with values for the next received data; therefore, it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old FERR and RX9D information.

Steps to follow when setting up a Synchronous Master Reception:

1. Initialize the SPBRG register for the appropriate baud rate. See Section 13.1 for details.
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, then set the RCIE bit.
4. If 9-bit reception is desired, then set the RX9 bit.
5. If a single reception is required, set bit SREN. For continuous reception set bit CREN.
6. The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit was set.
7. Read RCSTA to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading RCREG.
9. If any error occurred, clear the error by clearing CREN.

Note: To terminate a reception, either clear the SREN and CREN bits, or the SPEN bit. This will reset the receive logic, so that it will be in the proper state when receive is re-enabled.

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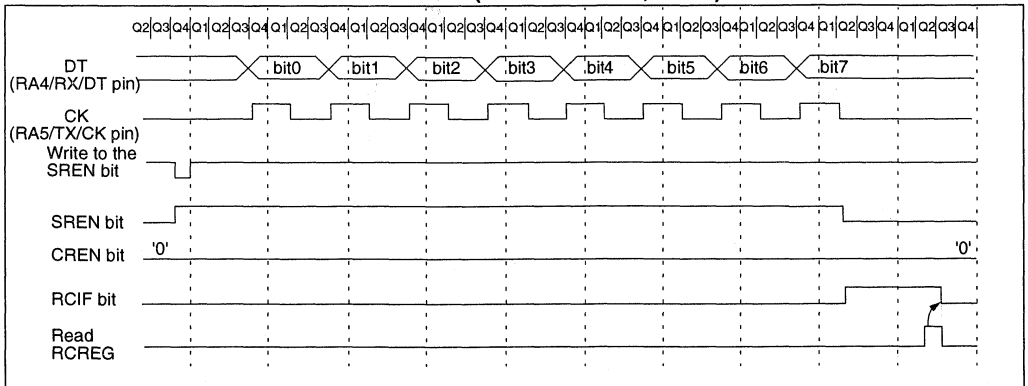
FIGURE 13-11: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates SYNC master mode with SREN = 1.

TABLE 13-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank 0	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous master reception.

Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

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13.4 USART Synchronous Slave Mode

The synchronous slave mode differs from the master mode in the fact that the shift clock is supplied externally at the RA5/TX/CK pin (instead of being supplied internally in the master mode). This allows the device to transfer or receive data in the SLEEP mode. The slave mode is entered by clearing the CSRC (TXSTA<7>) bit.

13.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the sync master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to TXREG and then the SLEEP instruction executes, the following will occur. The first word will immediately transfer to the TSR and will transmit as the shift clock is supplied. The second word will remain in TXREG. TXIF will not be set. When the first word has been shifted out of TSR, TXREG will transfer the second word to the TSR and the TXIF flag will now be set. If TXIE is enabled, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, then the program will branch to interrupt vector (0020h).

Steps to follow when setting up a Synchronous Slave Transmission:

1. Enable the synchronous slave serial port by setting the SYNC and SPEN bits and clearing the CSRC bit.
2. Clear the CREN bit.
3. If interrupts are desired, then set the TXIE bit.
4. If 9-bit transmission is desired, then set the TX9 bit.
5. Start transmission by loading data to TXREG.
6. If 9-bit transmission is selected, the ninth bit should be loaded in TX9D.
7. Enable the transmission by setting TXEN.

Writing the transmit data to the TXREG, then enabling the transmit (setting TXEN) allows transmission to start sooner then doing these two events in the reverse order.

Note:	To terminate a transmission, either clear the SPEN bit, or the TXEN bit. This will reset the transmit logic, so that it will be in the proper state when transmit is re-enabled.

13.4.2 USART SYNCHRONOUS SLAVE RECEPTION

Operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode. Also, SREN is a don't care in slave mode.

If receive is enabled (CREN) prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR will transfer the data to RCREG (setting RCIF) and if the RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0020h).

Steps to follow when setting up a Synchronous Slave Reception:

1. Enable the synchronous master serial port by setting the SYNC and SPEN bits and clearing the CSRC bit.
2. If interrupts are desired, then set the RCIE bit.
3. If 9-bit reception is desired, then set the RX9 bit.
4. To enable reception, set the CREN bit.
5. The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit was set.
6. Read RCSTA to get the ninth bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading RCREG.
8. If any error occurred, clear the error by clearing the CREN bit.

Note:	To abort reception, either clear the SPEN bit, the SREN bit (when in single receive mode), or the CREN bit (when in continuous receive mode). This will reset the receive logic, so that it will be in the proper state when receive is re-enabled.

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TABLE 13-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank 1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank 0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 0	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	xxxx xxxx	uuuu uuuu
17h, Bank 1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous slave transmission.

Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

TABLE 13-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
16h, Bank1	PIR	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TXIF	RCIF	0000 0010	0000 0010
13h, Bank0	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank0	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
17h, Bank1	PIE	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TXIE	RCIE	0000 0000	0000 0000
15h, Bank 0	TXSTA	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank0	SPBRG	Baud rate generator register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as a '0', shaded cells are not used for synchronous slave reception.

Note 1: Other (non power-up) resets include: external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

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14.0 SPECIAL FEATURES OF THE CPU

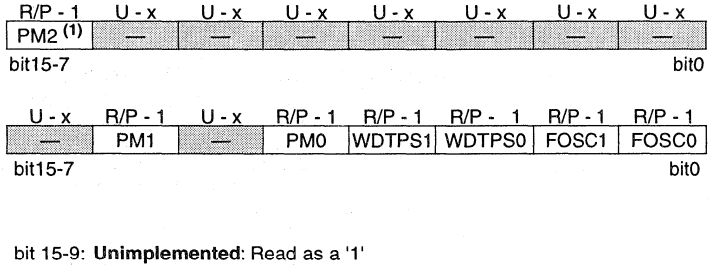
What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC17CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- OSC selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection

The PIC17CXX has a Watchdog Timer which can be shut off only through EPROM bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 96 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external reset, Watchdog Timer Reset or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LF crystal option saves power. Configuration bits are used to select various options. This configuration word has the format shown in Figure 14-1.

FIGURE 14-1: CONFIGURATION WORD



bit 15-9: **Unimplemented**: Read as a '1'

bit 15,6,4:**PM2, PM1, PM0**, Processor Mode Select bits
111 = Microprocessor Mode
110 = Microcontroller mode
101 = Extended microcontroller mode
000 = Code protected microcontroller mode

bit 7, 5: **Unimplemented**: Read as a '0'

bit 3-2: **WDTPS1:WDTPS0**, WDT Postscaler Select bits
11 = WDT enabled, postscaler = 1
10 = WDT enabled, postscaler = 256
01 = WDT enabled, postscaler = 64
00 = WDT disabled, 16-bit overflow timer

bit 1-0: **FOSC1:FOSC0**, Oscillator Select bits
11 = EC oscillator
10 = XT oscillator
01 = RC oscillator
00 = LF oscillator

Note 1: This bit does not exist on the PIC17C42. Reading this bit will return an unknown value (x).

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14.1 Configuration Bits

The PIC17CXX has up to seven configuration locations (Table 14-1). These locations can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. Any write to a configuration location, regardless of the data, will program that configuration bit. A TABLWT instruction is required to write to program memory locations. The configuration bits can be read by using the TABLRD instructions. Reading any configuration location between FE00h and FE07h will read the low byte of the configuration word (Figure 14-1) into the TABLATL register. The TABLATH register will be FFh. Reading a configuration location between FE08h and FE0Fh will read the high byte of the configuration word into the TABLATL register. The TABLATH register will be FFh.

Addresses FE00h thorough FE0Fh are only in the program memory space for microcontroller and code protected microcontroller modes. A device programmer will be able to read the configuration word in any processor mode. See programming specifications for more detail.

TABLE 14-1: CONFIGURATION LOCATIONS

Bit	Address
FOSC0	FE00h
FOSC1	FE01h
WDTPS0	FE02h
WDTPS1	FE03h
PM0	FE04h
PM1	FE06h
PM2 (1)	FE0Fh (1)

Note 1: This location does not exist on the PIC17C42.

Note: When programming the desired configuration locations, they must be programmed in ascending order. Starting with address FE00h.

14.2 Oscillator Configurations

14.2.1 OSCILLATOR TYPES

The PIC17CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

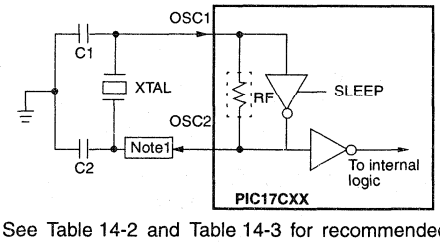
- LF: Low Power Crystal
- XT: Crystal/Resonator
- EC: External Clock Input
- RC: Resistor/Capacitor

14.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT or LF modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 14-2). The PIC17CXX Oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications.

For frequencies above 20 MHz, it is common for the crystal to be an overtone mode crystal. Use of overtone mode crystals require a tank circuit to attenuate the gain at the fundamental frequency. Figure 14-3 shows an example of this.

FIGURE 14-2: CRYSTAL OR CERAMIC RESONATOR OPERATION (XT OR LF OSC CONFIGURATION)



See Table 14-2 and Table 14-3 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.

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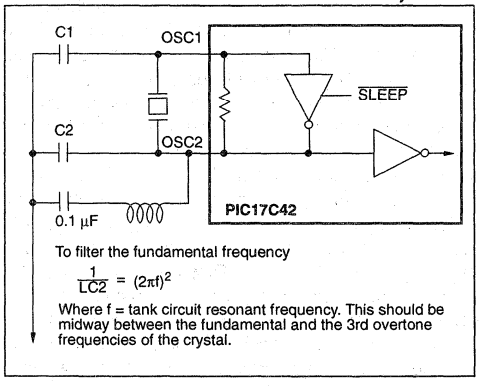
FIGURE 14-3: CRYSTAL OPERATION, OVERTONE CRYSTALS (XT OSC CONFIGURATION)



To filter the fundamental frequency

$$\frac{1}{LC2} = (2\pi f)^2$$

Where f = tank circuit resonant frequency. This should be midway between the fundamental and the 3rd overtone frequencies of the crystal.

TABLE 14-2: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
LF	455 kHz 2.0 MHz	15 - 68 pF 10 - 33 pF
XT	4.0 MHz 8.0 MHz 16.0 MHz	22 - 68 pF 33 - 100 pF 33 - 100 pF

Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

Resonators Used:

455 kHz	Panasonic EFO-A455K04B	± 0.3%
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%

Resonators used did not have built-in capacitors.

TABLE 14-3: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LF	32 kHz(1) 1 MHz 2 MHz	100-150 pF 10-33 pF 10-33 pF	100-150 pF 10-33 pF 10-33 pF
XT	2 MHz 4 MHz 8 MHz (2) 16 MHz 25 MHz 32 MHz (3)	47-100 pF 15-68 pF 15-47 pF TBD 15-47 pF 0 (3)	47-100 pF 15-68 pF 15-47 pF TBD 15-47 pF 0 (3)

Higher capacitance increases the stability of the oscillator but also increases the start-up time and the oscillator current. These values are for design guidance only. Rs may be required in XT mode to avoid overdriving the crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values for external components.

Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.
2: Rs of 330Ω is required for a capacitor combination of 15/15 pF.
3: Only the capacitance of the board was present.

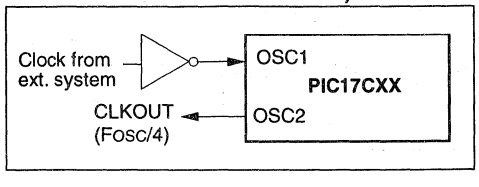
Crystals Used:

32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
1.0 MHz	ECS-10-13-1	± 50 PPM
2.0 MHz	ECS-20-20-1	± 50 PPM
4.0 MHz	ECS-40-20-1	± 50 PPM
8.0 MHz	ECS ECS-80-S-4 ECS-80-18-1	± 50 PPM
16.0 MHz	ECS-160-20-1	TBD
25 MHz	CTS CTS25M	± 50 PPM
32 MHz	CRYSTEK HF-2	± 50 PPM

14.2.3 EXTERNAL CLOCK OSCILLATOR

In the EC oscillator mode, the OSC1 input can be driven by CMOS drivers. In this mode, the OSC1/CLKIN pin is hi-impedance and the OSC2/CLKOUT pin is the CLKOUT output (4 TOSC).

FIGURE 14-4: EXTERNAL CLOCK INPUT OPERATION (EC OSC CONFIGURATION)



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14.2.4 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with series resonance, or one with parallel resonance.

Figure 14-5 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 14-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

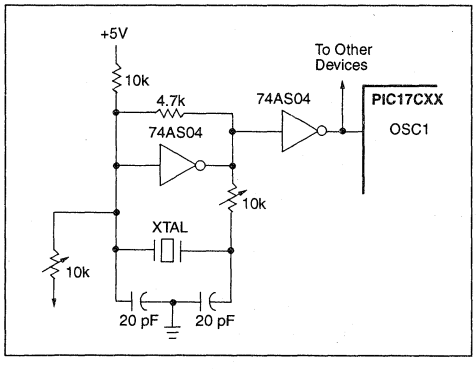
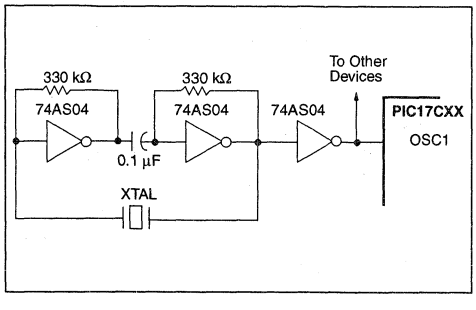


Figure 14-6 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 14-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



14.2.5 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 14-6 shows how the R/C combination is connected to the PIC17CXX. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kΩ and 100 kΩ.

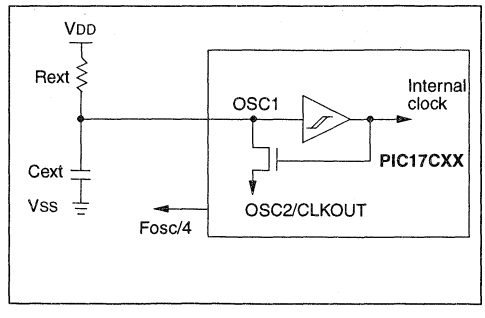
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With little or no external capacitance, oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-2 for waveform).

FIGURE 14-7: RC OSCILLATOR MODE



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14.3 Watchdog Timer (WDT)

The Watchdog Timer's function is to recover from software malfunction. The WDT uses an internal free running on-chip RC oscillator for its clock source. This does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation and SLEEP mode, a WDT time-out generates a device RESET. The WDT can be permanently disabled by programming the configuration bits WDTPS1:WDTPS0 as '00' (Section 14.1).

Under normal operation, the WDT must be cleared on a regular interval. This time is less the minimum WDT overflow time. Not clearing the WDT in this time frame will cause the WDT to overflow and reset the device.

14.3.1 WDT PERIOD

The WDT has a nominal time-out period of 12 ms, (with postscaler = 1). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a postscaler with a division ratio of up to 1:256 can be assigned to the WDT. Thus, typical time-out periods up to 3.0 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out thus generating a device RESET condition.

The $\overline{TO}$ bit in the CPUSTA register will be cleared upon a WDT time-out.

14.3.2 CLEARING THE WDT AND POSTSCALER

The WDT and postscaler are cleared when:

- The device is in the reset state
- A SLEEP instruction is executed
- A CLRWDT instruction is executed
- Wake-up from SLEEP by an interrupt

The WDT counter/postscaler will start counting on the first edge after the device exits the reset state.

14.3.3 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT postscaler) it may take several seconds before a WDT time-out occurs.

The WDT and postscaler is the Power-up Timer during the Power-on Reset sequence.

14.3.4 WDT AS NORMAL TIMER

When the WDT is selected as a normal timer, the clock source is the device clock. Neither the WDT nor the postscaler are directly readable or writable. The overflow time is 65536 TOSC cycles. On overflow, the $\overline{TO}$ bit is cleared (device is not reset). The CLRWDT instruction can be used to set the $\overline{TO}$ bit. This allows the WDT to be a simple overflow timer. When in sleep, the WDT does not increment.

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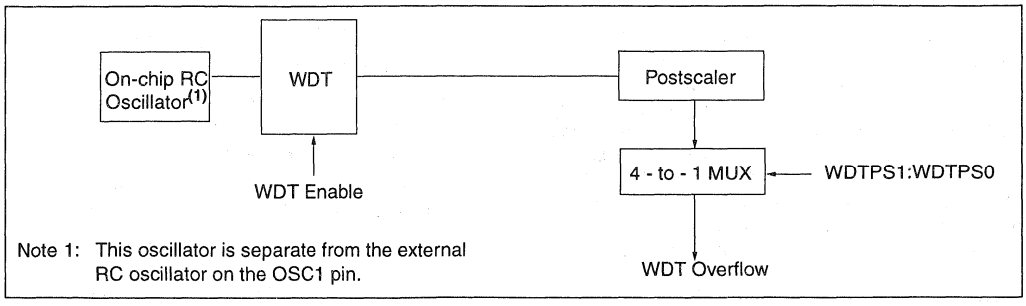
FIGURE 14-8: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: This oscillator is separate from the external RC oscillator on the OSC1 pin.

TABLE 14-4: REGISTERS/BITS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note1)
—	Config	—	PM1	—	PM0	WDTPS1	WDTPS0	FOSC1	FOSC0	(Note 2)	(Note 2)
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	$\overline{TO}$	$\overline{PD}$	—	—	--11 11--	--11 qq--

Legend: - = unimplemented read as '0', q - value depends on condition, shaded cells are not used by the WDT.
Note 1: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and Watchdog Timer Reset.
2: This value will be as the device was programmed, or if unprogrammed, will read as all '1's.

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14.4 Power-down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction. This clears the Watchdog Timer and postscaler (if enabled). The $\overline{PD}$ bit is cleared and the $\overline{TO}$ bit is set (in the CPUSTA register). In SLEEP mode, the oscillator driver is turned off. The I/O ports maintain their status (driving high, low, or hi-impedance).

The $\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC). A WDT time-out RESET does not drive the $\overline{MCLR}$/VPP pin low.

14.4.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- A POR reset
- External reset input on $\overline{MCLR}$/VPP pin
- WDT Reset (if WDT was enabled)
- Interrupt from RA0/INT pin, RB port change, T0CKI interrupt, or some Peripheral Interrupts

The following peripheral interrupts can wake-up from SLEEP:

- Capture1 interrupt
- Capture2 interrupt
- USART synchronous slave transmit interrupt
- USART synchronous slave receive interrupt

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

Any reset event will cause a device reset. Any interrupt event is considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the CPUSTA register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GLINTD bit. If the GLINTD bit is set (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GLINTD bit is clear (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt vector address. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GLINTD is set), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from sleep. The $\overline{TO}$ bit is set, and the $\overline{PD}$ bit is cleared.

The WDT is cleared when the device wake from SLEEP, regardless of the source of wake-up.

14.4.1.1 WAKE-UP DELAY

When the oscillator type is configured in XT or LF mode, the Oscillator Start-up Timer (OST) is activated on wake-up. The OST will keep the device in reset for 1024TOSC. This needs to be taken into account when considering the interrupt response time when coming out of SLEEP.

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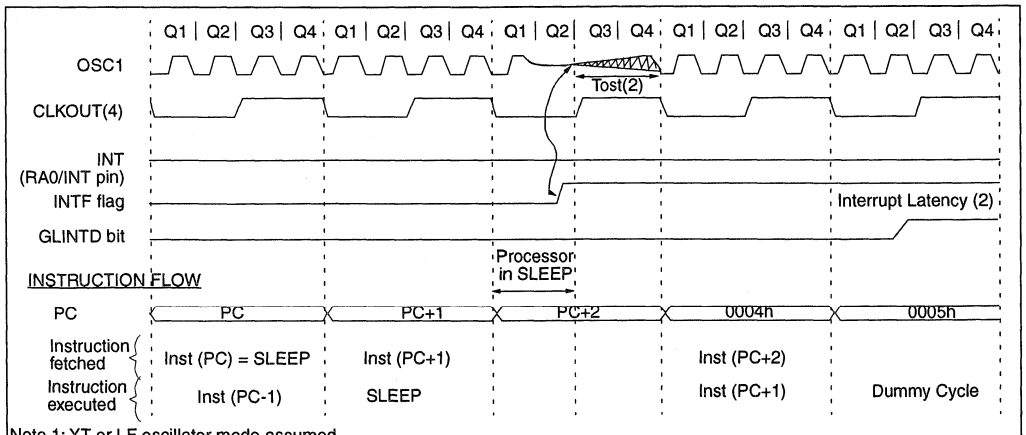
FIGURE 14-9: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT or LF oscillator mode assumed.
2: Tost = 1024Tosc (drawing not to scale). This delay will not be there for RC osc mode.
3: When GLINTD = 0 processor jumps to interrupt routine after wake-up. If GLINTD = 1, execution will continue in line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

14.4.2 MINIMIZING CURRENT CONSUMPTION

To minimize current consumption, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should be at VDD or VSS. The contributions from on-chip pull-ups on PORTB should also be considered, and disabled when possible.

14.5 Code Protection

The code in the program memory can be protected by selecting the microcontroller in code protected mode (PM2:PM0 = '000').

Note:	PM2 does not exist on the PIC17C42. To select code protected microcontroller mode, PM1:PM0 = '00'.

In this mode, instructions that are in the on-chip program memory space, can continue to read or write the program memory. An instruction that is executed outside of the internal program memory range will be inhibited from writing to or reading from program memory.

Note:	Microchip does not recommend code protecting windowed devices.

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

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15.0 PIC17C42 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2) ..... -0.6V to +14V

Voltage on RA2 and RA3 with respect to V_{SS} ..... -0.6V to +12V

Voltage on all other pins with respect to V_{SS} ..... -0.6V to V_{DD} + 0.6V

Total power dissipation (Note 1) 1.0W

Maximum current out of V_{SS} pin(s) - Total ..... 250 mA

Maximum current into V_{DD} pin(s) - Total ..... 200 mA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum output current sunk by any I/O pin (except RA2 and RA3) ..... 35 mA

Maximum output current sunk by RA2 or RA3 pins ..... 60 mA

Maximum output current sourced by any I/O pin ..... 20 mA

Maximum current sunk by PORTA and PORTB (combined) ..... 150 mA

Maximum current sourced by PORTA and PORTB (combined) ..... 100 mA

Maximum current sunk by PORTC, PORTD and PORTE (combined) ..... 150 mA

Maximum current sourced by PORTC, PORTD and PORTE (combined) ..... 100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 15-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC17C42-16	PIC17C42-25
RC	VDD: 4.5V to 5.5V IDD: 6 mA max. IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 6 mA max. IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 4 MHz max.
XT	VDD: 4.5V to 5.5V IDD: 24 mA max. IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 16 MHz max.	VDD: 4.5V to 5.5V IDD: 38 mA max. IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 25 MHz max.
EC	VDD: 4.5V to 5.5V IDD: 24 mA max. IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 16 MHz max.	VDD: 4.5V to 5.5V IDD: 38 mA max. IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 25 MHz max.
LF	VDD: 4.5V to 5.5V IDD: 150 µA max. at 32 kHz (WDT enabled) IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 2 MHz max.	VDD: 4.5V to 5.5V IDD: 150 µA max. at 32 kHz (WDT enabled) IPD: 5 µA max. at 5.5V (WDT disabled) Freq: 2 MHz max.

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15.1 DC CHARACTERISTICS: PIC17C42-16 (Commercial, Industrial) PIC17C42-25 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	4.5	–	5.5	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	1.5 *	–	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	–	VSS	–	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060*	–	–	mV/ms	See section on Power-on Reset for details
D010	IDD	Supply Current (Note 2)	–	3	6	mA	FOSC = 4 MHz (Note 4)
D011			–	6	12 *	mA	FOSC = 8 MHz
D012			–	11	24 *	mA	FOSC = 16 MHz
D013			–	19	38	mA	FOSC = 25 MHz
D014			–	95	150	µA	FOSC = 32 kHz WDT enabled (EC osc configuration)
D020	IPD	Power-down Current (Note 3)	–	10	40	µA	VDD = 5.5V, WDT enabled
D021			–	< 1	5	µA	VDD = 5.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
Current consumed from the oscillator and I/O's driving external capacitive or resistive loads need to be considered.
For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VDD / (2 • R).
For capacitive loads, The current can be estimated (for an individual I/O pin) as (CL • VDD) • f
CL = Total capacitive load on the I/O pin; f = average frequency on the I/O pin switches.
The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

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15.2 DC CHARACTERISTICS: PIC17C42-16 (Commercial, Industrial)
PIC17C42-25 (Commercial, Industrial)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in Section 15.1

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Input Low Voltage					
	VIL	I/O ports					
D030		with TTL buffer	VSS	–	0.8	V	
D031		with Schmitt Trigger buffer	VSS	–	0.2VDD	V	
D032		$\overline{MCLR}$, OSC1 (in EC and RC mode)	VSS	–	0.2VDD	V	Note1
D033		OSC1 (in XT, and LF mode)	–	0.5VDD	–	V	
		Input High Voltage					
	VIH	I/O ports		–			
D040		with TTL buffer	2.0	–	VDD	V	
D041		with Schmitt Trigger buffer	0.8VDD	–	VDD	V	
D042		$\overline{MCLR}$	0.8VDD	–	VDD	V	Note1
D043		OSC1 (XT, and LF mode)	–	0.5VDD	–	V	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15VDD*	–	–	V	
		Input Leakage Current (Notes 2, 3)					
D060	IIL	I/O ports (except RA2, RA3)	–	–	±1	µA	VSS ≤ VPIN ≤ VDD, I/O Pin at hi-impedance PORTB weak pull-ups disabled
D061		$\overline{MCLR}$	–	–	±2	µA	VPIN = VSS or VPIN = VDD
D062		RA2, RA3			±2	µA	VSS ≤ VRA2, VRA3 ≤ 12V
D063		OSC1, TEST	–	–	±1	µA	VSS ≤ VPIN ≤ VDD
D064		$\overline{MCLR}$	–	–	10	µA	VMCLR = VPP = 12V (when not programming)
D070	IPURB	PORTB weak pull-up current	60	200	400	µA	VPIN = VSS, $\overline{RBPU}$ = 0

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

†† Design guidance to attain the AC timing specifications. These loads are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The $\overline{MCLR}$/Vpp pin may be kept in this range at times other than programming, but this is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

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DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in Section 15.1

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Output Low Voltage					
D080	VOL	I/O ports (except RA2 and RA3)	–	–	0.1VDD	V	IOL = 4 mA
D081		with TTL buffer	–	–	0.4	V	IOL = 6 mA, VDD = 4.5V Note 6
D082		RA2 and RA3	–	–	3.0	V	IOL = 60.0 mA, VDD = 5.5V
D083		OSC2/CLKOUT (RC and EC osc modes)	–	–	0.4	V	IOL = 2 mA, VDD = 4.5V
		Output High Voltage (Note 3)					
D090	VOH	I/O ports (except RA2 and RA3)	0.9VDD	–	–	V	IOH = -2 mA
D091		with TTL buffer	2.4	–	–	V	IOH = -6.0 mA, VDD = 4.5V Note 6
D092		RA2 and RA3	–	–	12	V	Pulled-up to externally applied voltage
D093		OSC2/CLKOUT (RC and EC osc modes)	2.4	–	–	V	IOH = -5 mA, VDD = 4.5V
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	–	–	25 ††	pF	In EC or RC osc modes when OSC2 pin is outputting CLKOUT. External clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	–	–	50 ††	pF	
D102	CAD	System Interface Bus (PORTC, PORTD and PORTE)	–	–	100 ††	pF	In Microprocessor or Extended Microcontroller mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

†† Design guidance to attain the AC timing specifications. These loads are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The $\overline{MCLR}$/Vpp pin may be kept in this range at times other than programming, but this is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

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DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +40°C Operating voltage VDD range as described in Section 15.1				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Internal Program Memory Programming Specs (Note 4)					
D110	VPP	Voltage on MCLR/VPP pin	12.75	–	13.25	V	Note 5
D111	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
D112	IPP	Current into MCLR/VPP pin	–	25 ‡	50 ‡	mA	
D113	IDDP	Supply current during programming	–	–	30 ‡	mA	
D114	TPROG	Programming pulse width	10	100	1000	µs	Terminated via internal/external interrupt or a reset

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

Note: When using the Table Write for internal programming, the device temperature must be less than 40°C.

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15.3 Timing Parameter Symbology

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase symbols (pp) and their meanings:

pp			
ad	Address/Data	ost	Oscillator Start-up Timer
al	ALE	pwrt	Power-up Timer
cc	Capture1 and Capture2	rb	PORTB
ck	CLKOUT or clock	rd	$\overline{RD}$
dt	Data in	rw	$\overline{RD}$ or $\overline{WR}$
in	INT pin	t0	T0CKI
io	I/O port	t123	TCLK12 and TCLK3
mc	$\overline{MCLR}$	wdt	Watchdog Timer
oe	$\overline{OE}$	wr	$\overline{WR}$
os	OSC1		

Uppercase symbols and their meanings:

S			
D	Driven	L	Low
E	Edge	P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance

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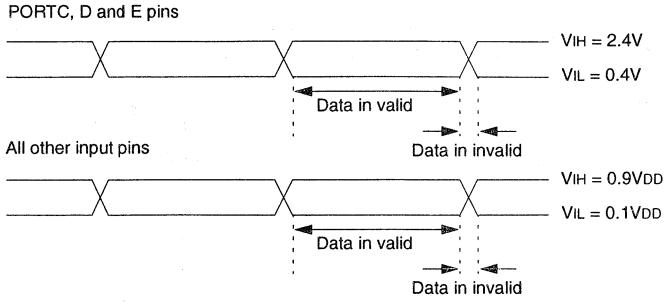
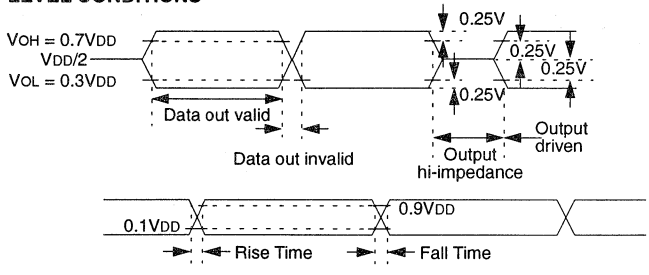
FIGURE 15-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.

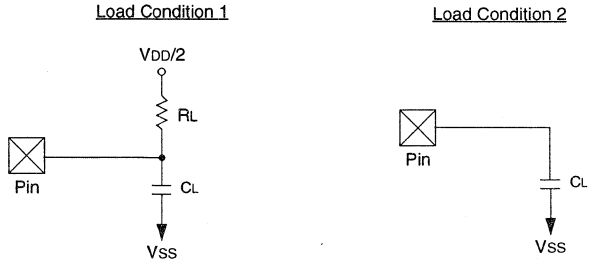
INPUT LEVEL CONDITIONS



OUTPUT LEVEL CONDITIONS



LOAD CONDITIONS



RL = 464
CL ≤ 50 pF

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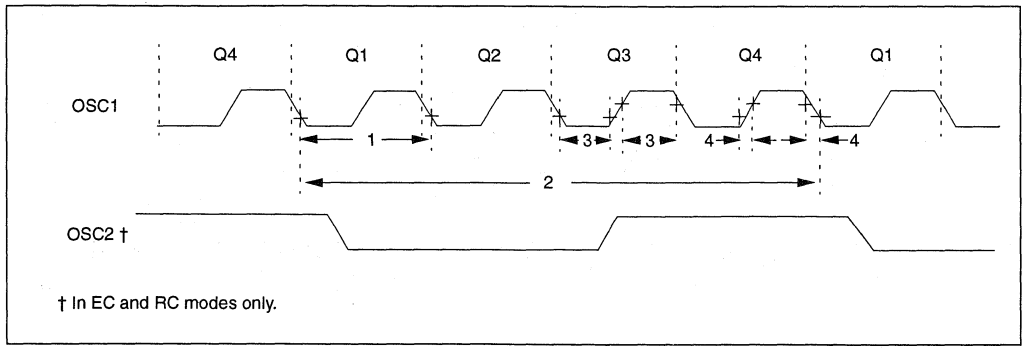
15.4 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING



† In EC and RC modes only.

TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency**	DC	—	16	MHz	EC osc mode - PIC17C42-16
		(Note 1)	DC	—	25	MHz	- PIC17C42-25
		Oscillator Frequency	DC	—	4	MHz	RC osc mode
		(Note 1)	1	—	16	MHz	XT osc mode - PIC17C42-16
			1	—	25	MHz	- PIC17C42-25
			DC	—	2	MHz	LF osc mode
1	Tosc	**External CLKIN Period**	62.5	—	—	ns	EC osc mode - PIC17C42-16
		(Note 1)	40	—	—	ns	- PIC17C42-25
		Oscillator Period	250	—	—	ns	RC osc mode
		(Note 1)	62.5	—	1,000	ns	XT osc mode - PIC17C42-16
			40	—	1,000	ns	- PIC17C42-25
			500	—	—	ns	LF osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	160	4/Fosc	DC	ns	
3	TosL, TosH	**Clock in (OSC1) High or Low Time**	10 ‡	—	—	ns	EC oscillator
4	TosR, TosF	**Clock in (OSC1) Rise or Fall Time**	—	—	5 ‡	ns	EC oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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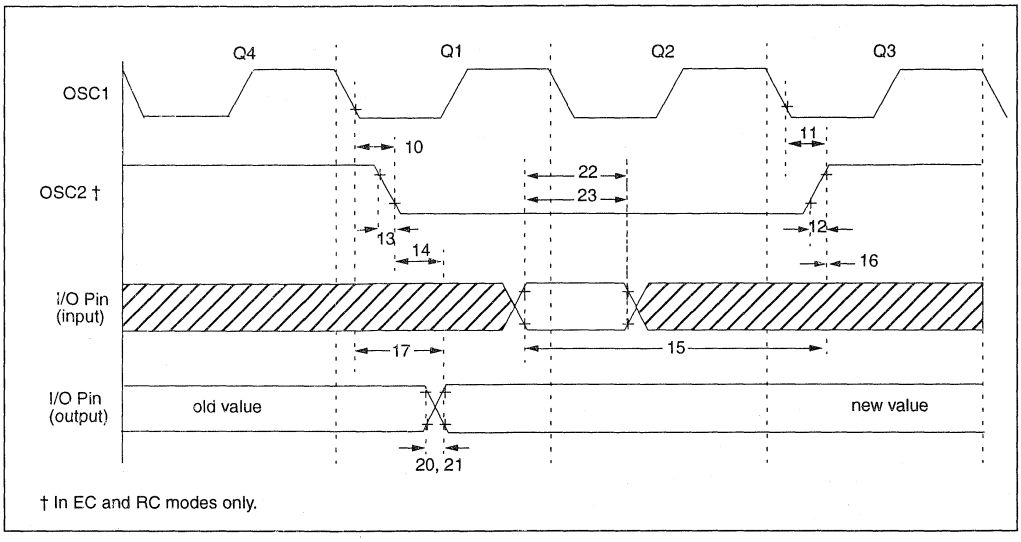
FIGURE 15-3: CLKOUT AND I/O TIMING



† In EC and RC modes only.

TABLE 15-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	—	15 ‡	30 ‡	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	15 ‡	30 ‡	ns	Note 1
12	TckR	CLKOUT rise time	—	5 ‡	15 ‡	ns	Note 1
13	TckF	CLKOUT fall time	—	5 ‡	15 ‡	ns	Note 1
14	TckH2ioV	CLKOUT↑ to Port out valid	—	—	0.5TCY + 20‡	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	0.25TCY + 25 ‡	—	—	ns	Note 1
16	TckH2ioI	Port in hold after CLKOUT↑	0 ‡	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	100 ‡	ns	
20	TioR	Port output rise time	—	10 ‡	35 ‡	ns	
21	TioF	Port output fall time	—	10 ‡	35 ‡	ns	
22	TinHL	INT pin high or low time	25 *	—	—	ns	
23	TrbHL	RB7:RB0 change INT high or low time	25 *	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where OSC2 output = 4 x TOSC = TCY.

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FIGURE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

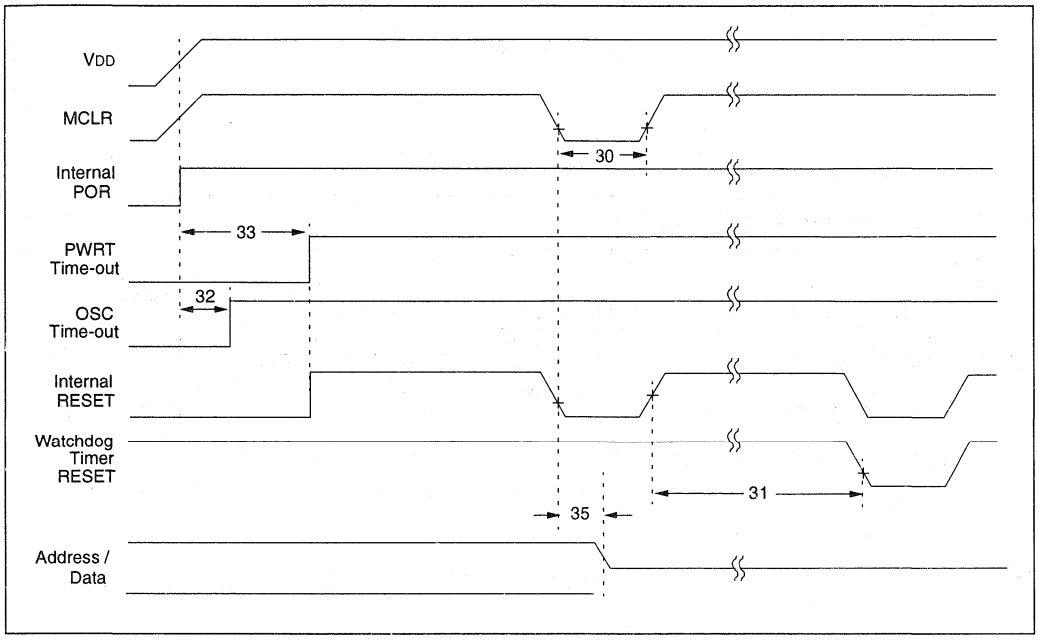

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	100 *	—	—	ns	
31	Twdt	Watchdog Timer Time-out Period (Prescale = 1)	5 *	12	25 *	ms	
32	Tost	Oscillation Start-up Timer Period		1024 Tosc §		ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	40 *	96	200 *	ms	
35	TmcL2adl	$\overline{\text{MCLR}}$ to System Interface bus (AD15:AD0) invalid	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

§ This specification ensured by design.

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FIGURE 15-5: TIMER0 CLOCK TIMINGS

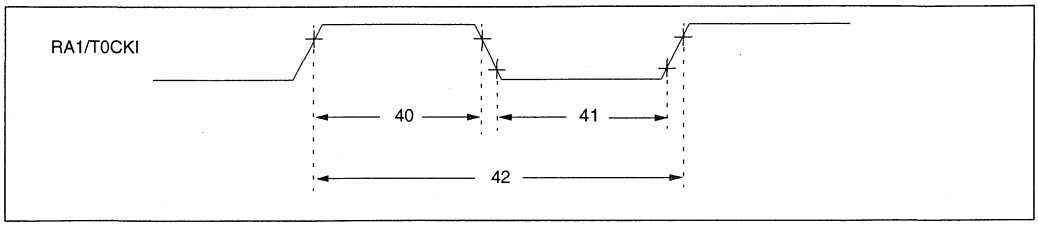

TABLE 15-5: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20 §	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20 §	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		TCY + 40 § / N	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 15-6: TIMER1, TIMER2, AND TIMER3 CLOCK TIMINGS

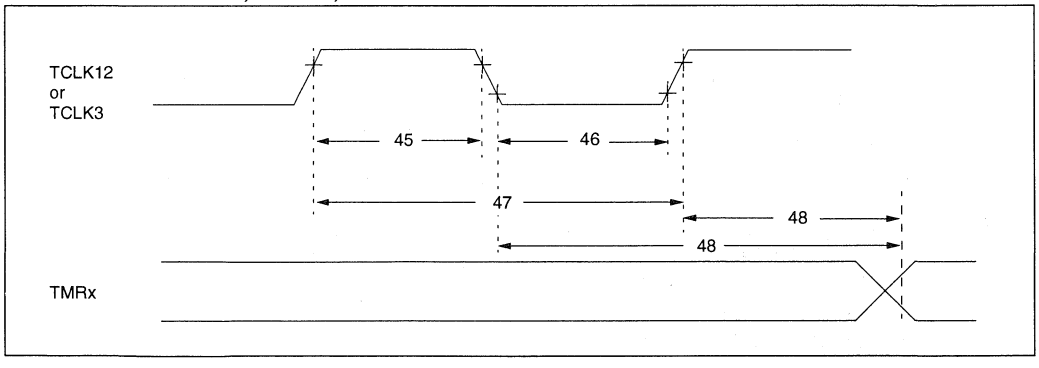

TABLE 15-6: TIMER1, TIMER2, AND TIMER3 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
45	Tt123H	TCLK12 and TCLK3 high time	0.5 TCY + 20 §	—	—	ns	
46	Tt123L	TCLK12 and TCLK3 low time	0.5 TCY + 20 §	—	—	ns	
47	Tt123P	TCLK12 and TCLK3 input period	TCY + 40 § / N	—	—	ns	N = prescale value (1, 2, 4, 8)
48	TckE2tmrI	Delay from selected External Clock Edge to Timer increment	2TOSC §	—	6 TOSC §	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

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FIGURE 15-7: CAPTURE TIMINGS

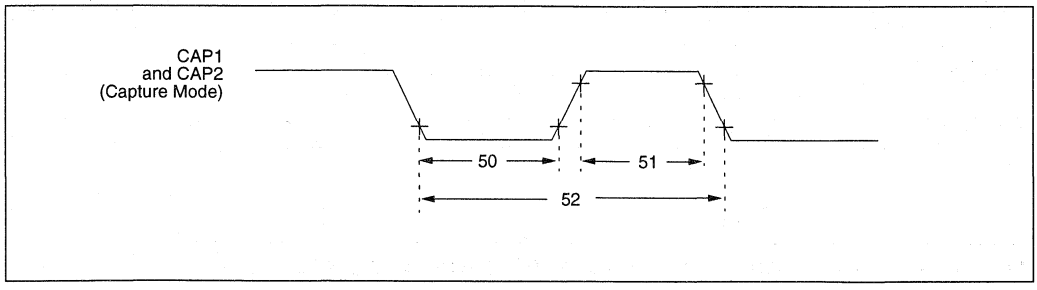

TABLE 15-7: CAPTURE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
50	TccL	Capture1 and Capture2 input low time	10 *	—	—	ns	
51	TccH	Capture1 and Capture2 input high time	10 *	—	—	ns	
52	TccP	Capture1 and Capture2 input period	$\frac{2\,T_{CY}}{N}$ §	—	—	ns	N = prescale value (4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 15-8: PWM TIMINGS

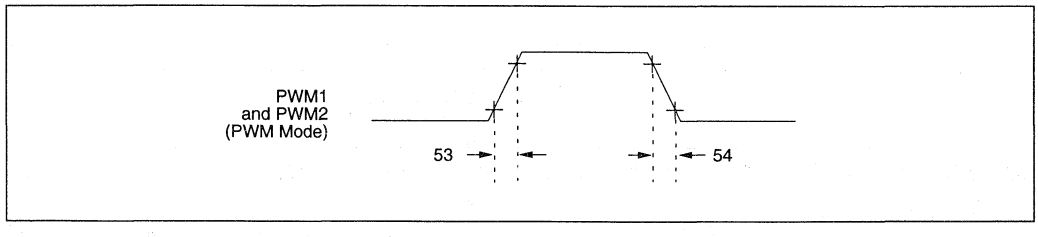

TABLE 15-8: PWM REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
53	TccR	PWM1 and PWM2 output rise time	—	10 *	35 *§	ns	
54	TccF	PWM1 and PWM2 output fall time	—	10 *	35 *§	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

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Applicable Devices	42	R42	42A	43	R43	44

FIGURE 15-9: USART MODULE: SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

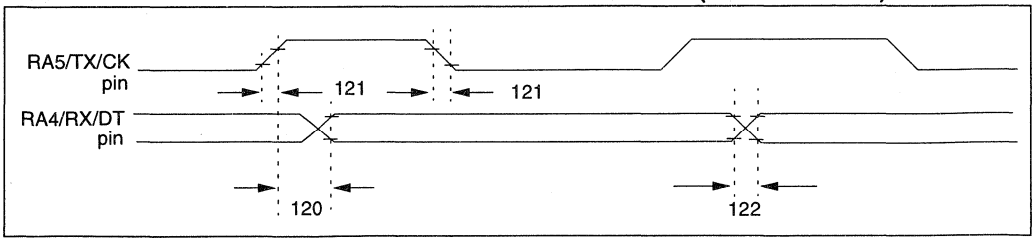

TABLE 15-9: SERIAL PORT SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	—	—	65	ns	
121	TckRF	Clock out rise time and fall time (Master Mode)	—	10	35	ns	
122	TdtRF	Data out rise time and fall time	—	10	35	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-10: USART MODULE: SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

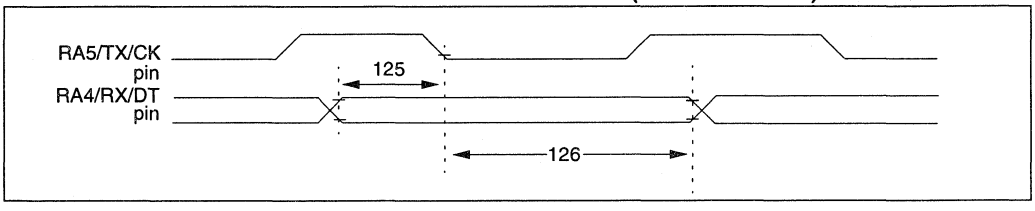

TABLE 15-10: SERIAL PORT SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data hold before CK↓ (DT hold time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK↓ (DT hold time)	15	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 15-11: MEMORY INTERFACE WRITE TIMING

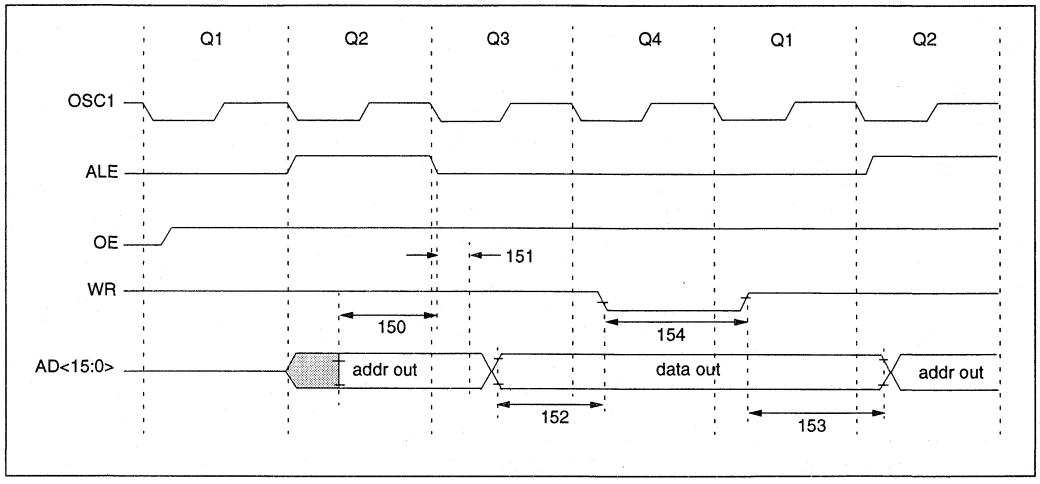

TABLE 15-11: MEMORY INTERFACE WRITE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
150	TadV2alL	AD<15:0> (address) valid to ALE↓ (address setup time)	0.25Tcy - 30	—	—	ns	
151	TalL2adI	ALE↓ to address out invalid (address hold time)	0	—	—	ns	
152	TadV2wrL	Data out valid to $\overline{WR}$↓ (data setup time)	0.25Tcy - 40	—	—	ns	
153	TwrH2adI	$\overline{WR}$↑ to data out invalid (data hold time)	—	0.25Tcy §	—	ns	
154	TwrL	$\overline{WR}$ pulse width	—	0.25Tcy §	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification is guaranteed by design.

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Applicable Devices 42 | R42 | 42A | 43 | R43 | 44

FIGURE 15-12: MEMORY INTERFACE READ TIMING

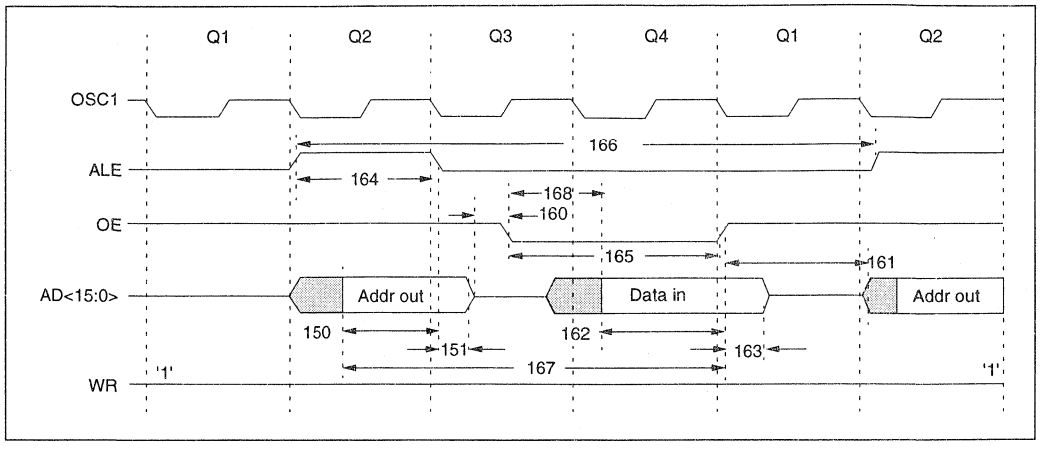

TABLE 15-12: MEMORY INTERFACE READ REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
150	TadV2alL	AD<15:0> (address) valid to ALE↓ (address setup time)	0.25Tcy - 30	—	—	ns	
151	TalL2adI	ALE↓ to address out invalid (address hold time)	5*	—	—	ns	
160	TadZ2oeL	AD<15:0> high impedance to $\overline{OE}$↓	0*	—	—	ns	
161	ToeH2adD	$\overline{OE}$↑ to AD<15:0> driven	0.25Tcy - 15	—	—	ns	
162	TadV2oeH	Data in valid before $\overline{OE}$↑ (data setup time)	35	—	—	ns	
163	ToeH2adI	$\overline{OE}$↑to data in invalid (data hold time)	0	—	—	ns	
164	TalH	ALE pulse width	—	0.25TCY §	—	ns	
165	ToeL	$\overline{OE}$ pulse width	0.5Tcy - 35 §	—	—	ns	
166	TalH2alH	ALE↑ to ALE↑ (cycle time)	—	TCY §	—	ns	
167	Tacc	Address access time	—	—	0.75 TCY-40	ns	
168	Toe	Output enable access time ($\overline{OE}$ low to Data Valid)	—	—	0.5 TCY - 60	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification guaranteed by design.

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16.0 PIC17C42 DC AND AC CHARACTERISTICS

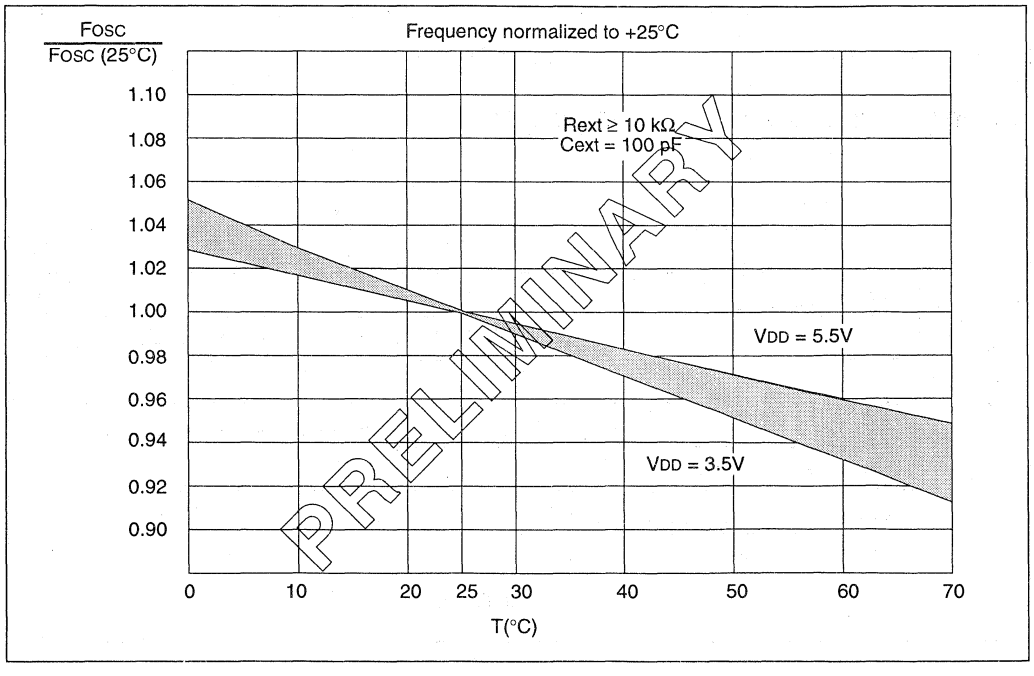
The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are ensured to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

TABLE 16-1: PIN CAPACITANCE PER PACKAGE TYPE

Pin Name	Typical Capacitance (pF)			
	40-pin DIP	44-pin PLCC	44-pin MQFP	44-pin TQFP
All pins, except $\overline{MCLR}$, VDD, and VSS	10	10	10	10
$\overline{MCLR}$ pin	20	20	20	20

FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE



Applicable Devices	42	R42	42A	43	R43	44

FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

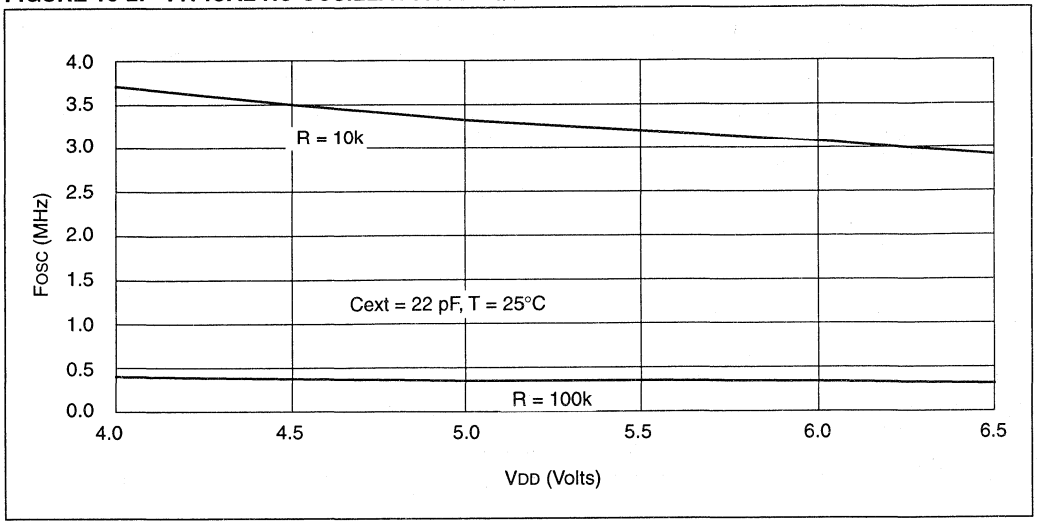


FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

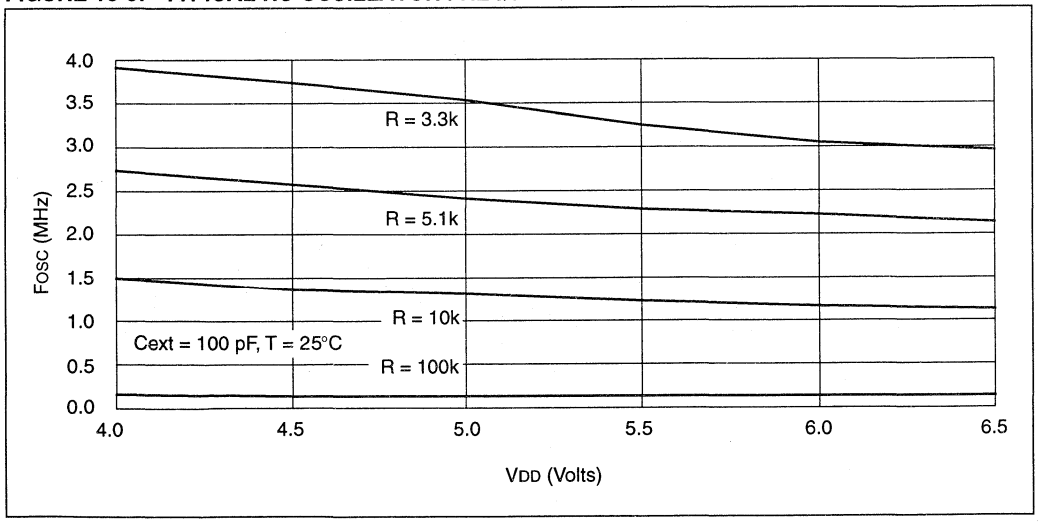


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FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

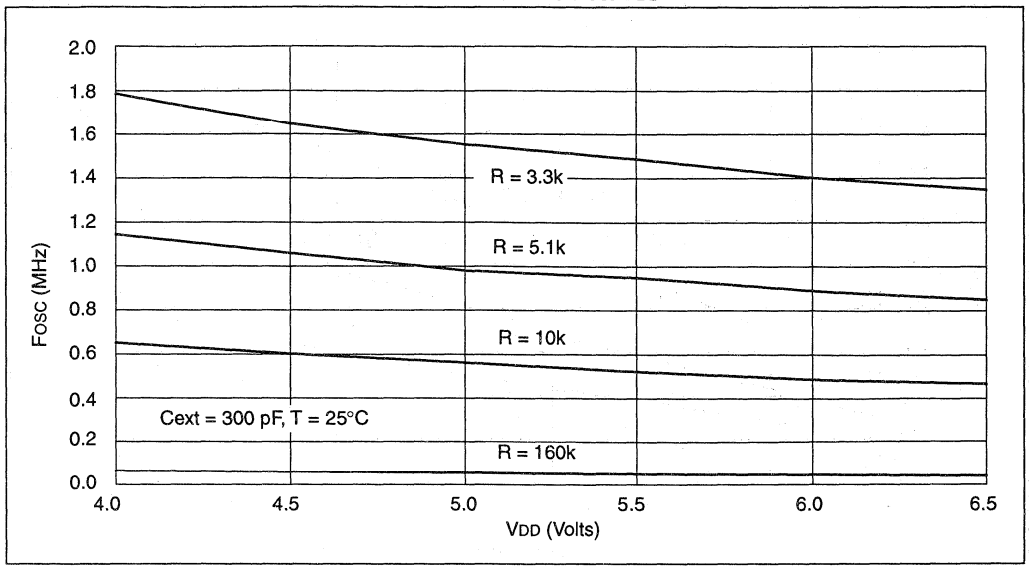

TABLE 16-2: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
22 pF	10k	3.33 MHz	± 12%
	100k	353 kHz	± 13%
100 pF	3.3k	3.54 MHz	± 10%
	5.1k	2.43 MHz	± 14%
	10k	1.30 MHz	± 17%
	100k	129 kHz	± 10%
300 pF	3.3k	1.54 MHz	± 14%
	5.1k	980 kHz	± 12%
	10k	564 kHz	± 16%
	160k	35 kHz	± 18%

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Applicable Devices	42	R42	42A	43	R43	44

FIGURE 16-5: TRANSCONDUCTANCE (gm) OF LF OSCILLATOR vs. VDD

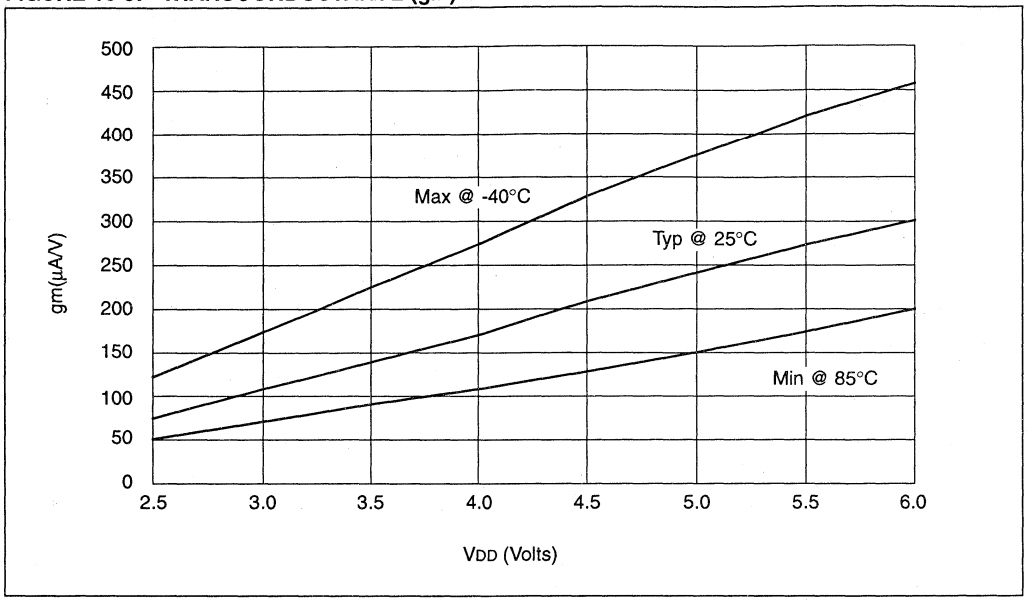
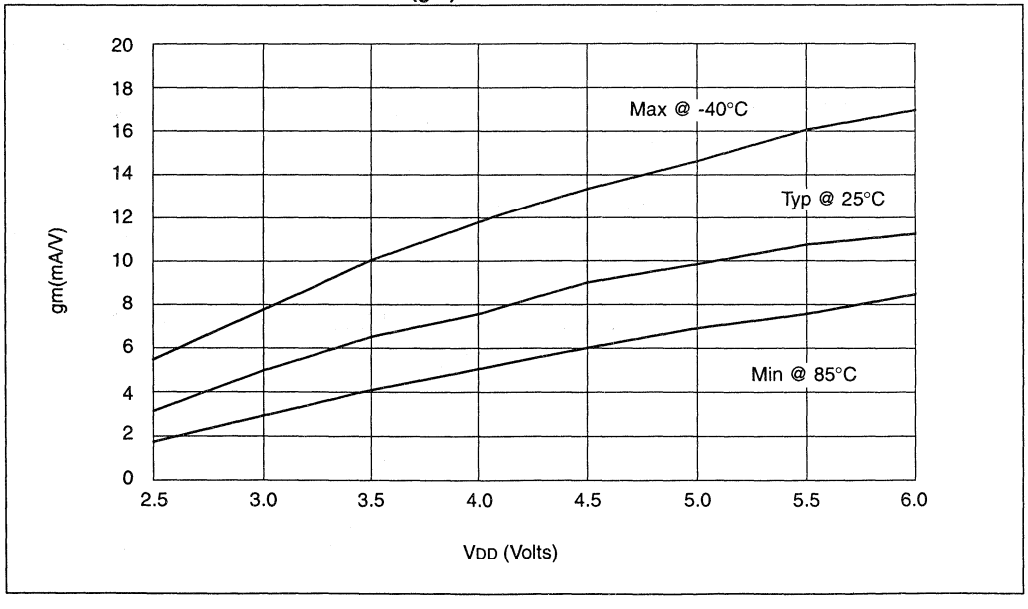


FIGURE 16-6: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



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Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44

FIGURE 16-7: TYPICAL IDD vs. FREQUENCY (EXTERNAL CLOCK 25°C)

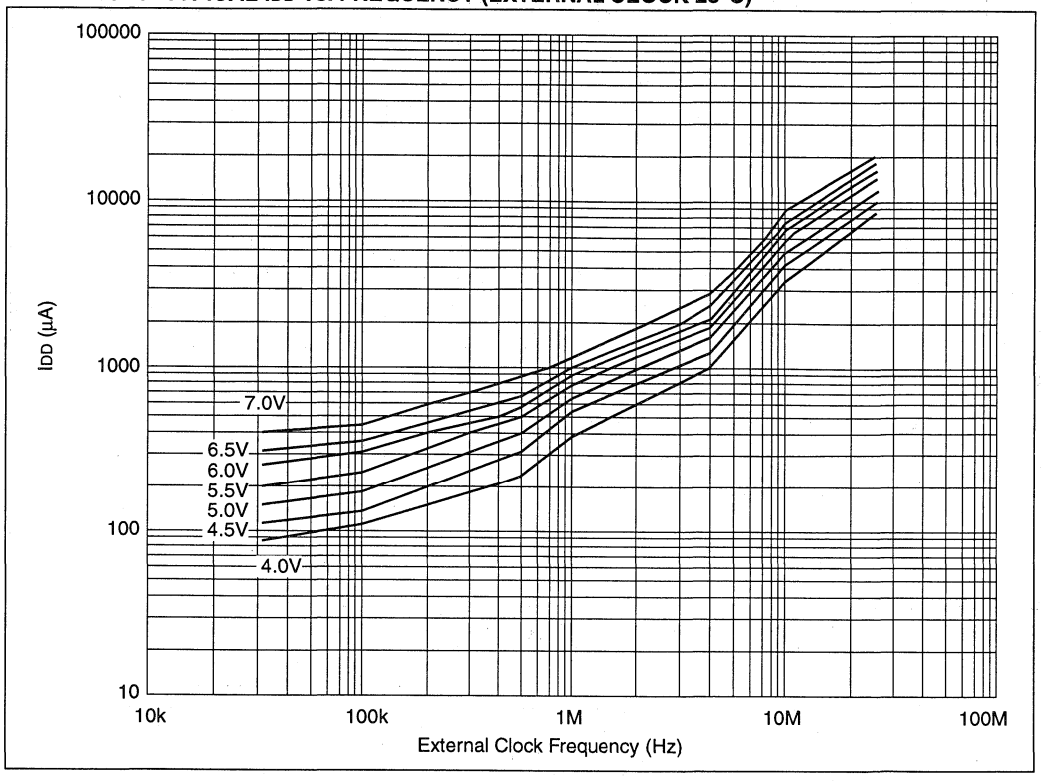
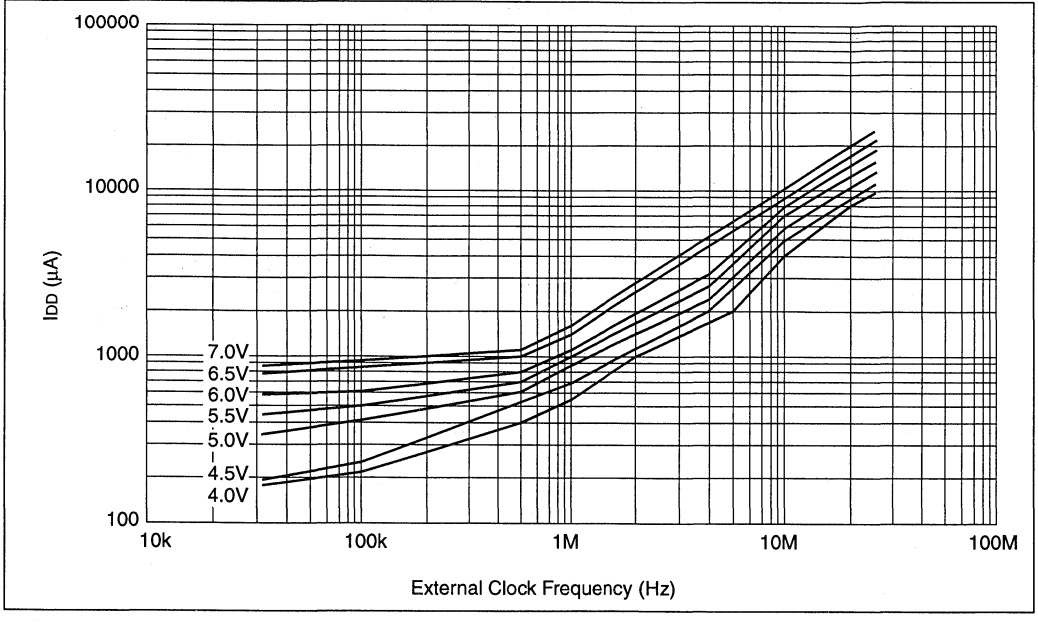


FIGURE 16-8: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK 125°C TO -40°C)



Applicable Devices	42	R42	42A	43	R43	44

FIGURE 16-9: TYPICAL IPD vs. VDD WATCHDOG DISABLED 25°C

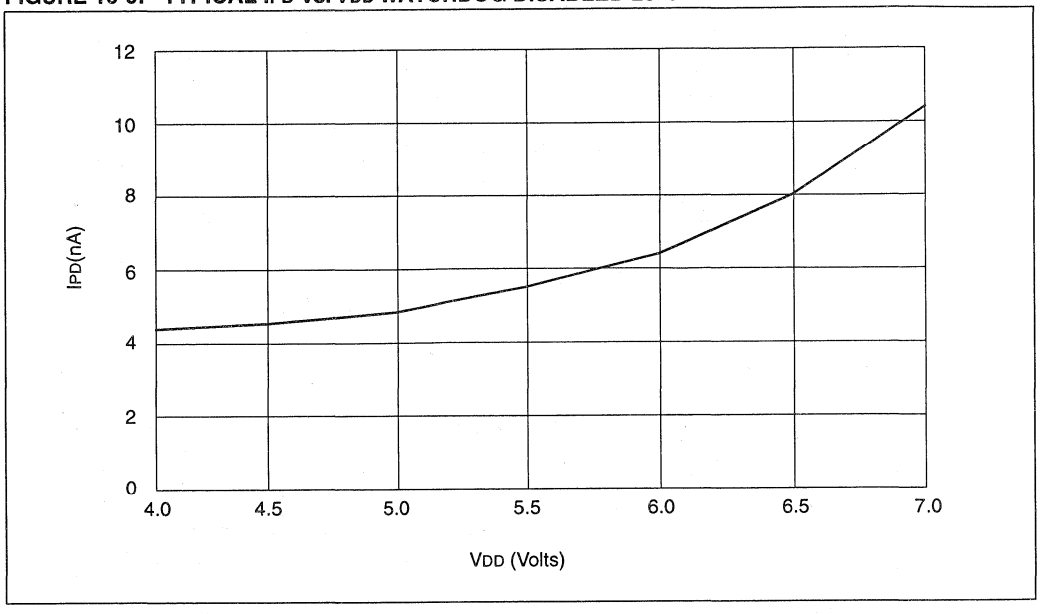


FIGURE 16-10: MAXIMUM IPD vs. VDD WATCHDOG DISABLED

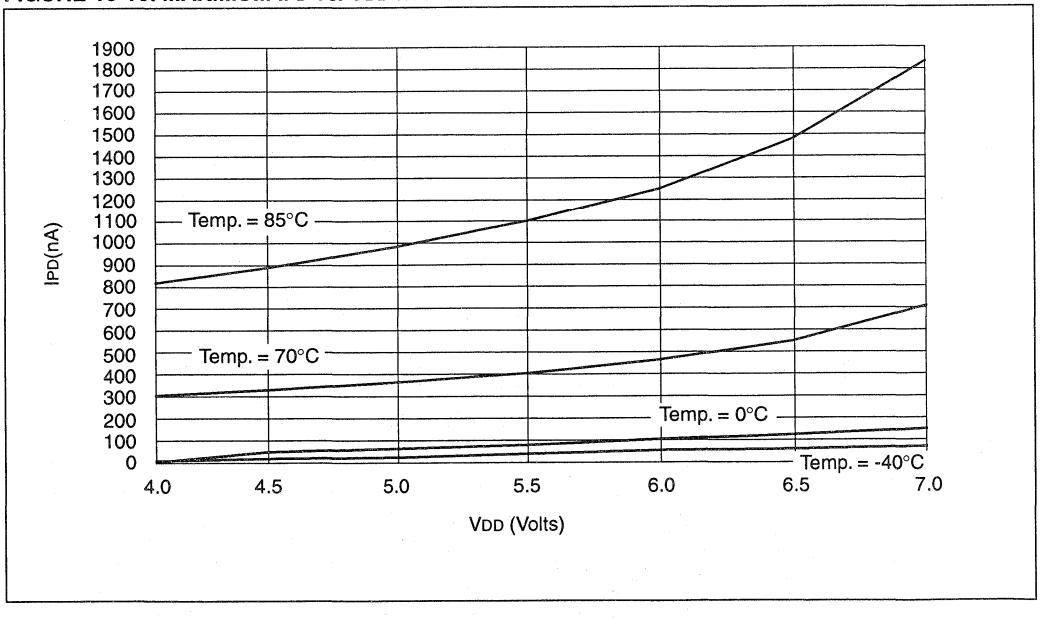


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FIGURE 16-11: TYPICAL IPD vs. VDD WATCHDOG ENABLED 25°C

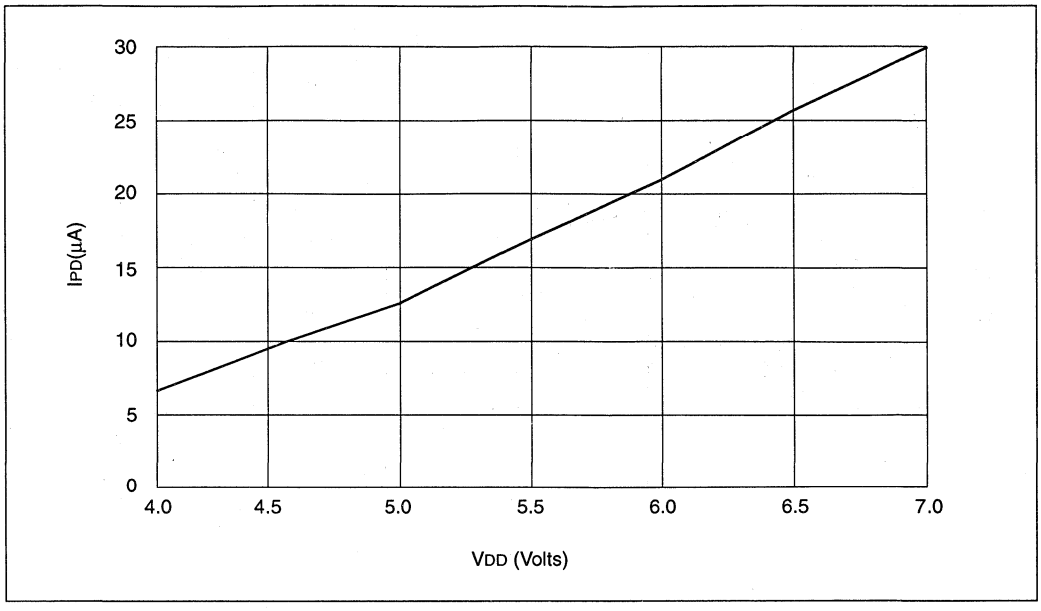
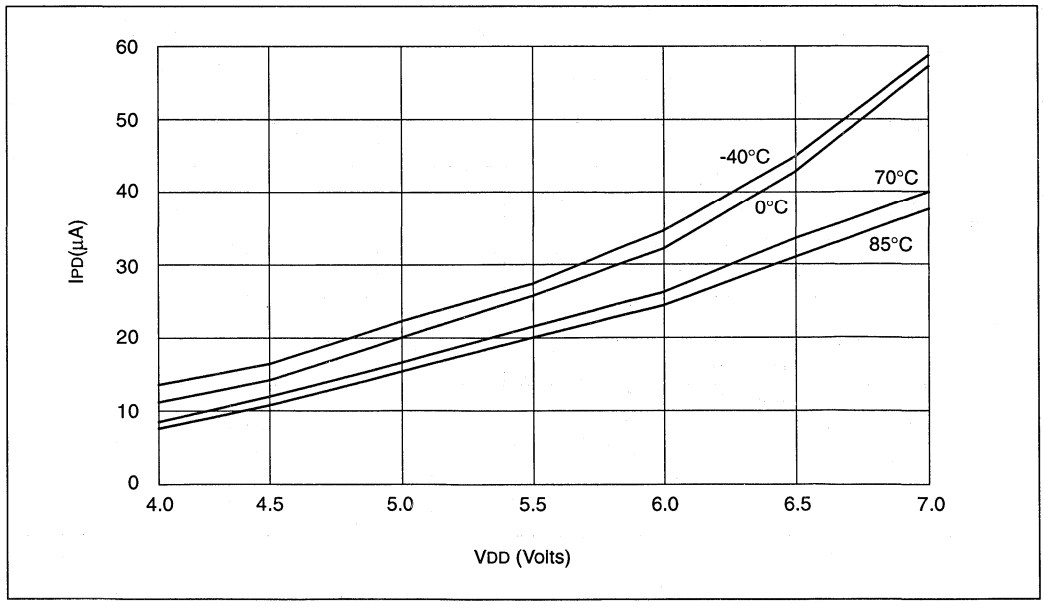


FIGURE 16-12: MAXIMUM IPD vs. VDD WATCHDOG ENABLED



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Applicable Devices	42	R42	42A	43	R43	44

FIGURE 16-13: WDT TIMER TIME-OUT PERIOD vs. VDD

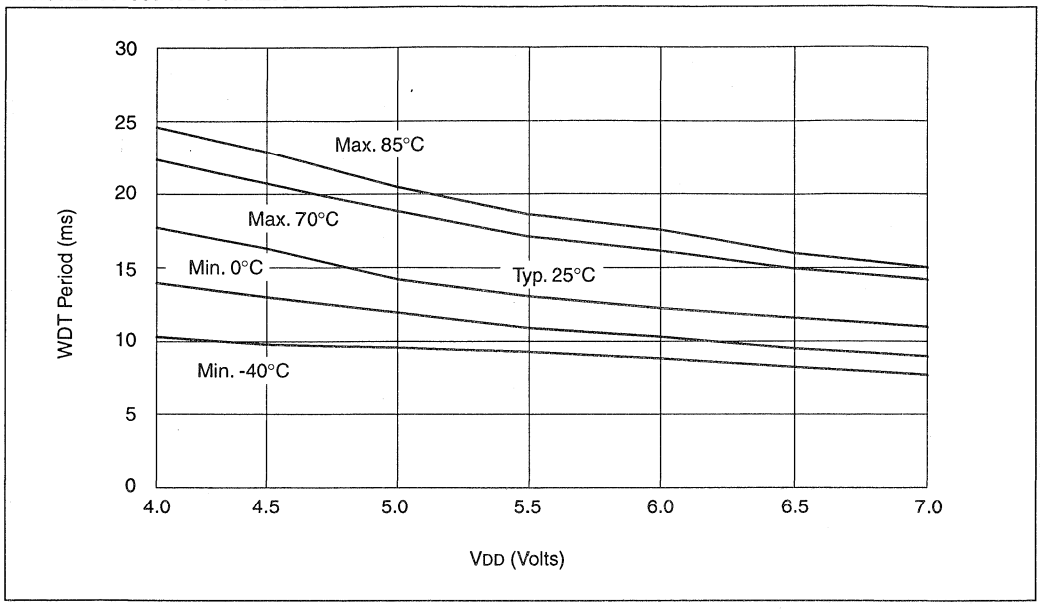

FIGURE 16-14: IOH vs. VOH, VDD = 3V

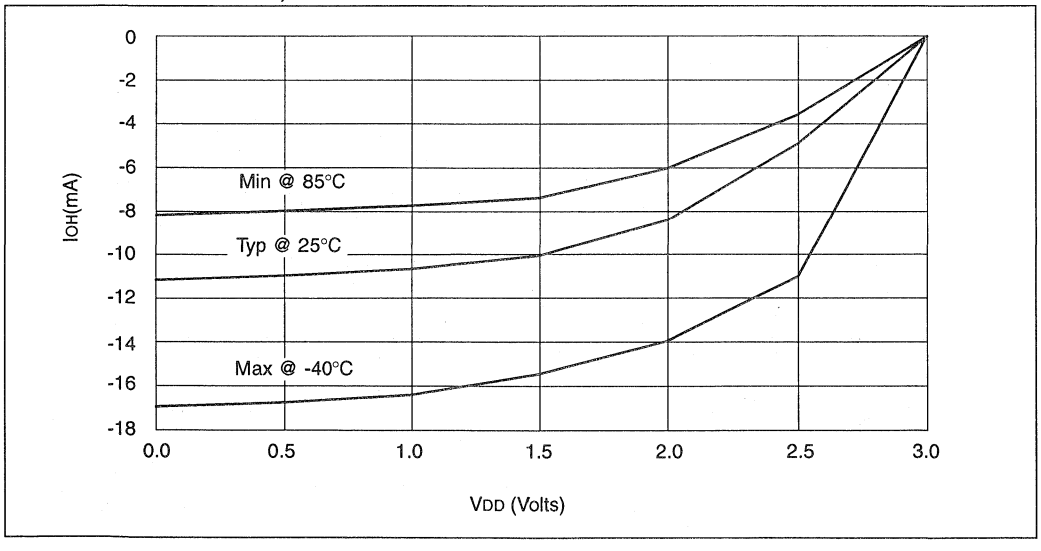

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FIGURE 16-15: I_{OH} vs. V_{OH}, V_{DD} = 5V

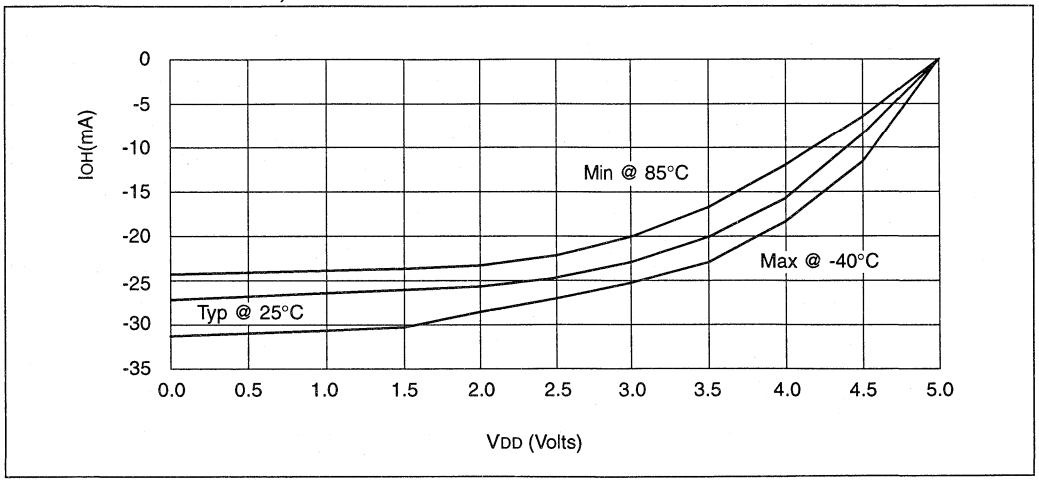

FIGURE 16-16: I_{OL} vs. V_{OL}, V_{DD} = 3V

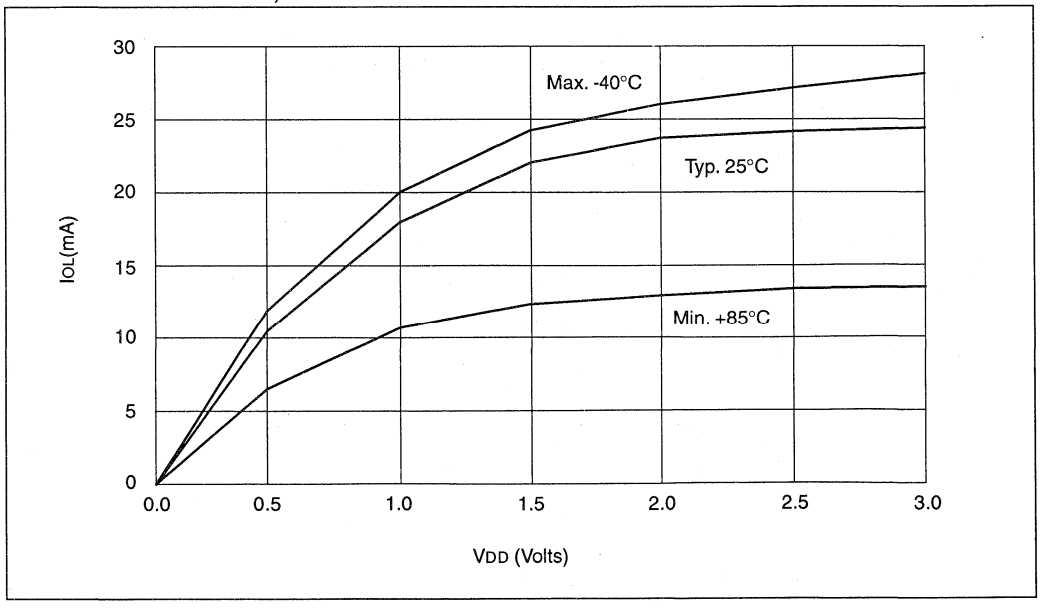

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FIGURE 16-17: IOL vs. VOL, VDD = 5V

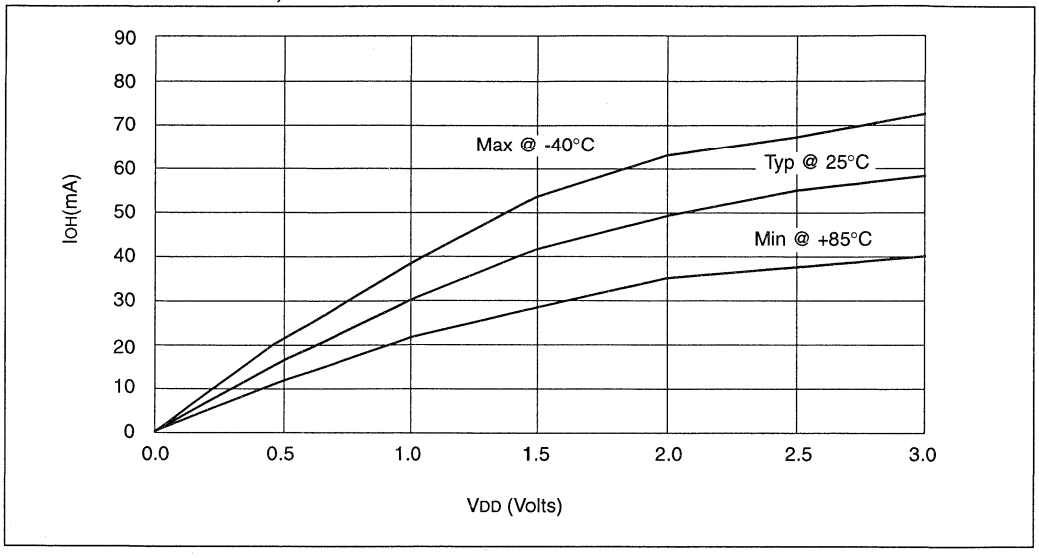
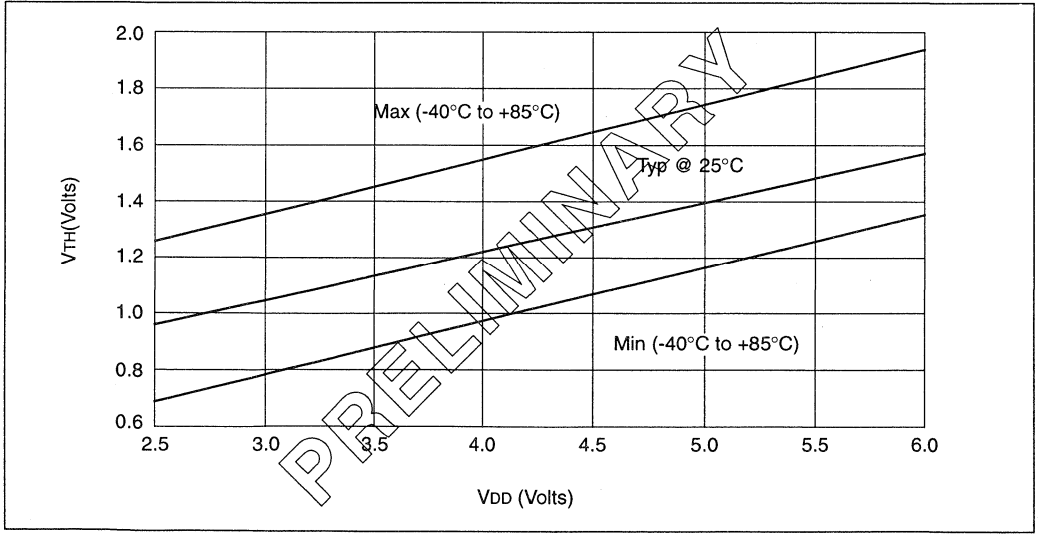


FIGURE 16-18: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS (TTL) vs. VDD



PRELIMINARY

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FIGURE 16-19: VTH, VIL of I/O PINS (SCHMITT TRIGGER) vs. VDD

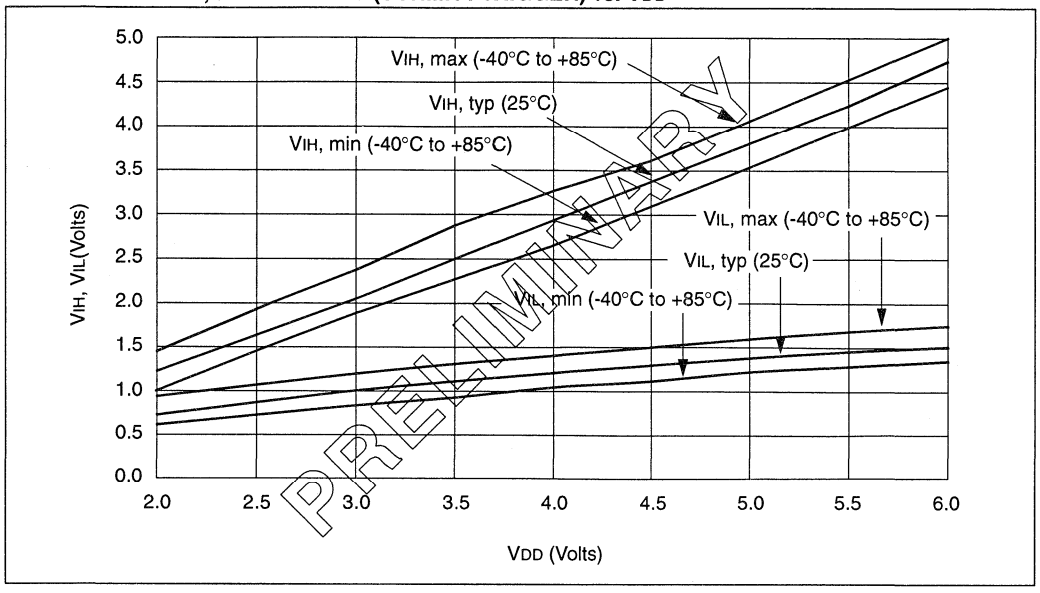
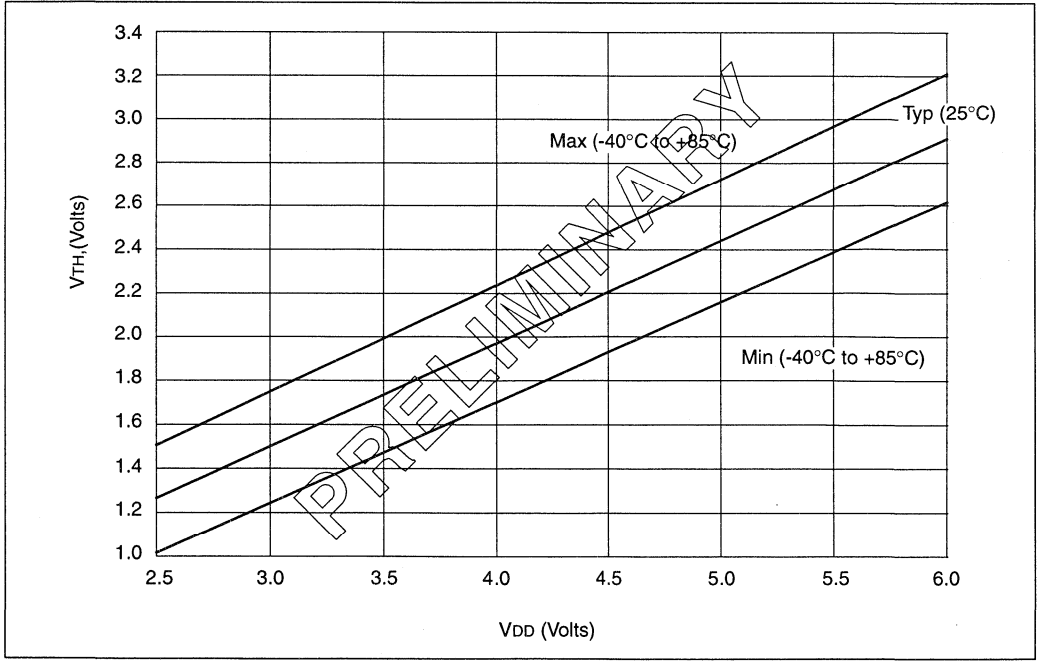


FIGURE 16-20: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT AND LF MODES) vs. VDD



NOTES:

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Applicable Devices	42	R42	42A	43	R43	44

17.0 PIC17CR42/42A/43/R43/44 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2) ..... -0.6V to +14V
Voltage on RA2 and RA3 with respect to V_{SS} ..... -0.6V to +14V
Voltage on all other pins with respect to V_{SS} ..... -0.6V to V_{DD} + 0.6V
Total power dissipation (Note 1) 1.0W
Maximum current out of V_{SS} pin(s) - total ..... 250 mA
Maximum current into V_{DD} pin(s) - total ..... 200 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any I/O pin (except RA2 and RA3) ..... 35 mA
Maximum output current sunk by RA2 or RA3 pins ..... 60 mA
Maximum output current sourced by any I/O pin ..... 20 mA
Maximum current sunk by PORTA and PORTB (combined) ..... 150 mA
Maximum current sourced by PORTA and PORTB (combined) ..... 100 mA
Maximum current sunk by PORTC, PORTD and PORTE (combined) ..... 150 mA
Maximum current sourced by PORTC, PORTD and PORTE (combined) ..... 100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Applicable Devices 42 | R42 | 42A | 43 | R43 | 44

TABLE 17-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC17LCR42-08 PIC17LC42A-08 PIC17LC43-08 PIC17LCR43-08 PIC17LC44-08	PIC17CR42-16 PIC17C42A-16 PIC17C43-16 PIC17CR43-16 PIC17C44-16	PIC17CR42-25 PIC17C42A-25 PIC17C43-25 PIC17CR43-25 PIC17C44-25	PIC17CR42-33 PIC17C42A-33 PIC17C43-33 PIC17CR43-33 PIC17C44-33	JW Devices (Ceramic Windowed Devices)
RC	VDD: 2.5V to 6.0V IDD: 6 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 4 MHz max.	VDD: 4.5V to 6.0V IDD: 6 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 4 MHz max.	VDD: 4.5V to 6.0V IDD: 6 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 4 MHz max.	VDD: 4.5V to 6.0V IDD: 6 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 4 MHz max.	VDD: 4.5V to 6.0V IDD: 6 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 4 MHz max.
XT	VDD: 2.5V to 6.0V IDD: 12 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 8 MHz max.	VDD: 4.5V to 6.0V IDD: 24 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 16 MHz max.	VDD: 4.5V to 6.0V IDD: 38 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 25 MHz max.	VDD: 4.5V to 6.0V IDD: 38 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 33 MHz max.	VDD: 4.5V to 6.0V IDD: 38 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 33 MHz max.
EC	VDD: 2.5V to 6.0V IDD: 12 mA max. IPD: 5 µA max at 5.5V WDT disabled Freq: 8 MHz max.	VDD: 4.5V to 6.0V IDD: 24 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 16 MHz Max	VDD: 4.5V to 6.0V IDD: 38 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 25 MHz max.	VDD: 4.5V to 6.0V IDD: 38 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 33 MHz max.	VDD: 4.5V to 6.0V IDD: 38 mA max. IPD: 5 µA max. at 5.5V WDT disabled Freq: 33 MHz max.
LF	VDD: 2.5V to 6.0V IDD: 150 µA max. at 32 kHz IPD: 5 µA max at 5.5V WDT disabled Freq: 2 MHz max.	VDD: 4.5V to 6.0V IDD: 95 µA typ. at 32 kHz IPD: < 1 µA typ. at 5.5V WDT disabled Freq: 2 MHz max.	VDD: 4.5V to 6.0V IDD: 95 µA typ. at 32 kHz IPD: < 1 µA typ. at 5.5V WDT disabled Freq: 2 MHz max.	VDD: 4.5V to 6.0V IDD: 95 µA typ. at 32 kHz IPD: < 1 µA typ. at 5.5V WDT disabled Freq: 2 MHz max.	VDD: 2.5V to 6.0V IDD: 150 µA max. at 32 kHz IPD: 5 µA max. at 5.5V WDT disabled Freq: 2 MHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

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Applicable Devices	42	R42	42A	43	R43	44

17.1 DC CHARACTERISTICS: PIC17CR42/42A/43/R43/44-16 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-25 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-33 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	4.5	–	6.0	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	1.5 *	–	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	–	VSS	–	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060 *	–	–	mV/ms	See section on Power-on Reset for details
D010	IDD	Supply Current (Note 2)	–	3	6	mA	FOSC = 4 MHz (Note 4)
D011			–	6	12 *	mA	FOSC = 8 MHz
D012			–	11	24 *	mA	FOSC = 16 MHz
D013			–	19	38	mA	FOSC = 25 MHz
D015			–	25	50	mA	FOSC = 33 MHz
D014			–	95	150	µA	FOSC = 32 kHz, WDT enabled (EC osc configuration)
D020	IPD	Power-down Current (Note 3)	–	10	40	µA	VDD = 5.5V, WDT enabled
D021			–	< 1	5	µA	VDD = 5.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
Current consumed from the oscillator and I/O's driving external capacitive or resistive loads needs to be considered.
For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VDD / (2 • R).
For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL • VDD) • f
CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.
The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

Applicable Devices 42 | R42 | 42A | 43 | R43 | 44

17.2 DC CHARACTERISTICS: PIC17LC42A/43/LC44 (Commercial, Industrial) PIC17LCR42/43 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.5	–	6.0	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	1.5 *	–	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	–	VSS	–	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.060 *	–	–	mV/ms	See section on Power-on Reset for details
D010	IDD	Supply Current (Note 2)	–	3	6	mA	FOSC = 4 MHz (Note 4)
D011			–	6	12 *	mA	FOSC = 8 MHz
D014			–	95	150	µA	FOSC = 32 kHz, WDT disabled (EC osc configuration)
D020	IPD	Power-down Current (Note 3)	–	10	40	µA	VDD = 5.5V, WDT enabled
D021			–	< 1	5	µA	VDD = 5.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD or VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
Current consumed from the oscillator and I/O's driving external capacitive or resistive loads needs to be considered.
For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: VDD / (2 • R).
For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL • VDD) • f
CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.
The capacitive currents are most significant when the device is configured for external execution (includes extended microcontroller mode).

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula IR = VDD/2Rext (mA) with Rext in kOhm.

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Applicable Devices	42	R42	42A	43	R43	44

17.3 DC CHARACTERISTICS: PIC17CR42/42A/43/R43/44-16 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-25 (Commercial, Industrial) PIC17CR42/42A/43/R43/44-33 (Commercial, Industrial) PIC17LCR42/42A/43/R43/44-08 (Commercial, Industrial)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in Section 17.1

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Input Low Voltage					
	VIL	I/O ports					
D030		with TTL buffer	VSS	–	0.8	V	4.5V ≤ VDD ≤ 5.5V
			VSS	–	0.2VDD	V	2.5V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer	VSS	–	0.2VDD	V	
D032		MCLR, OSC1 (in EC and RC mode)	VSS	–	0.2VDD	V	Note1
D033		OSC1 (in XT, and LF mode)	–	0.5VDD	–	V	
		Input High Voltage					
	VIH	I/O ports					
D040		with TTL buffer	2.0	–	VDD	V	4.5V ≤ VDD ≤ 5.5V
			1 + 0.2VDD	–	VDD	V	2.5V ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8VDD	–	VDD	V	
D042		MCLR	0.8VDD	–	VDD	V	Note1
D043		OSC1 (XT, and LF mode)	–	0.5VDD	–	V	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15VDD *	–	–	V	
		Input Leakage Current (Notes 2, 3)					
D060	IIL	I/O ports (except RA2, RA3)	–	–	±1	µA	VSS ≤ VPIN ≤ VDD, I/O Pin at hi-impedance PORTB weak pull-ups disabled
D061		MCLR	–	–	±2	µA	VPIN = VSS or VPIN = VDD
D062		RA2, RA3			±2	µA	VSS ≤ VRA2, VRA3 ≤ 12V
D063		OSC1, TEST (EC, RC modes)	–	–	±1	µA	VSS ≤ VPIN ≤ VDD
D063B		OSC1, TEST (XT, LF modes)	–	–	VPIN	µA	RF ≥ 1 MΩ, see Figure 14.2
D064		MCLR	–	–	10	µA	VMCLR = VPP = 12V (when not programming)
D070	IPURB	PORTB weak pull-up current	60	200	400	µA	VPIN = VSS, RBPU = 0 4.5V ≤ VDD ≤ 6.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

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DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in Section 17.1

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Output Low Voltage					
D080	VOL	I/O ports (except RA2 and RA3)					IOL = VDD/1.250 mA
			–	–	0.1VDD	V	4.5V ≤ VDD ≤ 6.0V
			–	–	0.1VDD *	V	VDD = 2.5V
D081		with TTL buffer	–	–	0.4	V	IOL = 6 mA, VDD = 4.5V Note 6
D082		RA2 and RA3	–	–	3.0	V	IOL = 60.0 mA, VDD = 6.0V
D083		OSC2/CLKOUT	–	–	0.4	V	IOL = 1 mA, VDD = 4.5V
D084		(RC and EC osc modes)	–	–	0.1VDD *	V	IOL = VDD/5 mA (PIC17LC43/LC44 only)
		Output High Voltage (Note 3)					
D090	VOH	I/O ports (except RA2 and RA3)					IOH = -VDD/2.500 mA
			0.9VDD	–	–	V	4.5V ≤ VDD ≤ 6.0V
			0.9VDD *	–	–	V	VDD = 2.5V
D091		with TTL buffer	2.4	–	–	V	IOH = -6.0 mA, VDD=4.5V Note 6
D092		RA2 and RA3	–	–	12	V	Pulled-up to externally applied voltage
D093		OSC2/CLKOUT	2.4	–	–	V	IOH = -5 mA, VDD = 4.5V
D094		(RC and EC osc modes)	0.9VDD *	–	–	V	IOH = -VDD/5 mA (PIC17LC43/LC44 only)
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2/CLKOUT pin	–	–	25	pF	In EC or RC osc modes when OSC2 pin is outputting CLKOUT. external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	–	–	50	pF	
D102	CAD	System Interface Bus (PORTC, PORTD and PORTE)	–	–	50	pF	In Microprocessor or Extended Microcontroller mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The $\overline{MCLR}$/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

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DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +40°C Operating voltage VDD range as described in Section 17.1				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Internal Program Memory Programming Specs (Note 4)					
D110	VPP	Voltage on $\overline{MCLR}$/VPP pin	12.75	–	13.25	V	Note 5
D111	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
D112	IPP	Current into $\overline{MCLR}$/VPP pin	–	25 ‡	50 ‡	mA	
D113	IDDP	Supply current during programming	–	–	30 ‡	mA	
D114	TPROG	Programming pulse width	10	100	1000	µs	Terminated via internal/ external interrupt or a reset

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXX devices be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17CXX Programming Specifications (Literature number DS30139).

5: The $\overline{MCLR}$/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

Note: When using the Table Write for internal programming, the device temperature must be less than 40°C.

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17.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I²C specifications only)
4. Ts (I²C specifications only)

T			
F	Frequency	T	Time

Lowercase symbols (pp) and their meanings:

pp			
ad	Address/Data	ost	Oscillator Start-Up Timer
al	ALE	pwrt	Power-Up Timer
cc	Capture1 and Capture2	rb	PORTB
ck	CLKOUT or clock	rd	$\overline{RD}$
dt	Data in	rw	$\overline{RD}$ or $\overline{WR}$
in	INT pin	t0	T0CKI
io	I/O port	t123	TCLK12 and TCLK3
mc	$\overline{MCLR}$	wdt	Watchdog Timer
oe	$\overline{OE}$	wr	$\overline{WR}$
os	OSC1		

Uppercase symbols and their meanings:

S			
D	Driven	L	Low
E	Edge	P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance

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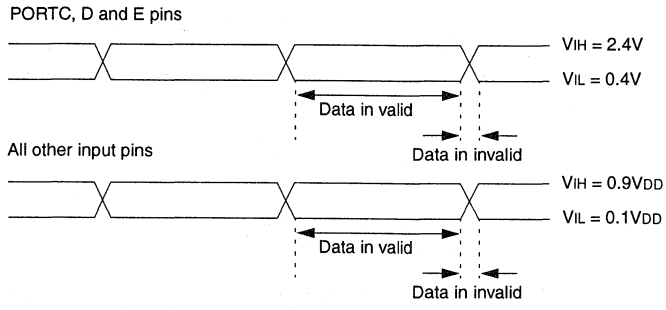
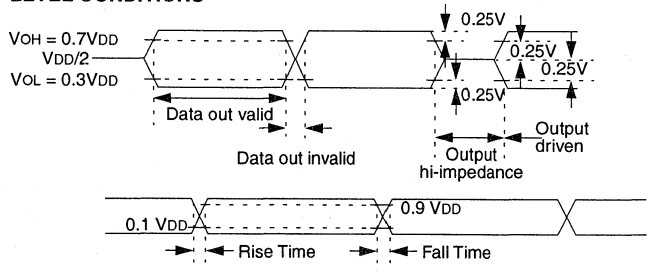
FIGURE 17-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.

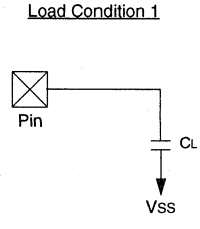
INPUT LEVEL CONDITIONS



OUTPUT LEVEL CONDITIONS



LOAD CONDITIONS



50 pF ≤ CL

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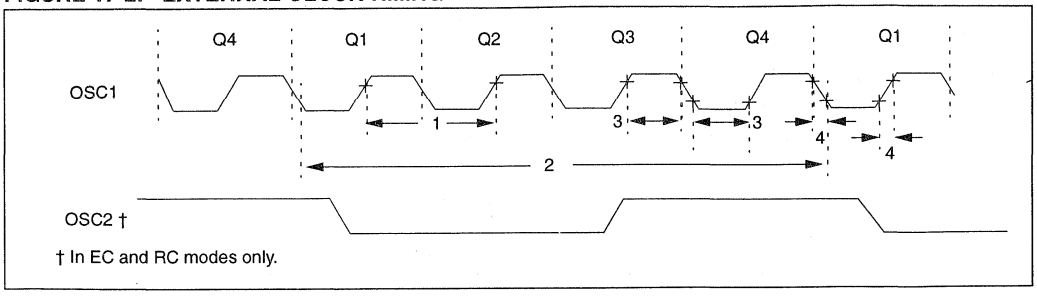
17.5 Timing Diagrams and Specifications

FIGURE 17-2: EXTERNAL CLOCK TIMING



† In EC and RC modes only.

TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency (Note 1)**	DC	—	8	MHz	EC osc mode - 08 devices (8 MHz devices)
			DC	—	16	MHz	- 16 devices (16 MHz devices)
			DC	—	25	MHz	- 25 devices (25 MHz devices)
			DC	—	33	MHz	- 33 devices (33 MHz devices)
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			1	—	8	MHz	XT osc mode - 08 devices (8 MHz devices)
			1	—	16	MHz	- 16 devices (16 MHz devices)
			1	—	25	MHz	- 25 devices (25 MHz devices)
			1	—	33	MHz	- 33 devices (33 MHz devices)
			DC	—	2	MHz	LF osc mode
1	Tosc	**External CLKIN Period (Note 1)**	125	—	—	ns	EC osc mode - 08 devices (8 MHz devices)
			62.5	—	—	ns	- 16 devices (16 MHz devices)
			40	—	—	ns	- 25 devices (25 MHz devices)
			30.3	—	—	ns	- 33 devices (33 MHz devices)
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			125	—	1,000	ns	XT osc mode - 08 devices (8 MHz devices)
			62.5	—	1,000	ns	- 16 devices (16 MHz devices)
			40	—	1,000	ns	- 25 devices (25 MHz devices)
			30.3	—	1,000	ns	- 33 devices (33 MHz devices)
			500	—	—	ns	LF osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	121.2	4/Fosc	DC	ns	
3	TosL, TosH	**Clock in (OSC1) high or low time**	10 ‡	—	—	ns	EC oscillator
4	TosR, TosF	**Clock in (OSC1) rise or fall time**	—	—	5 ‡	ns	EC oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

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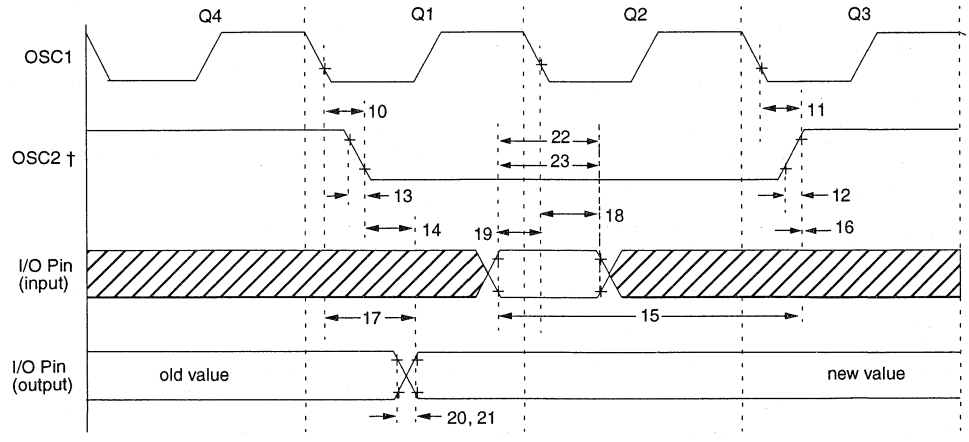
FIGURE 17-3: CLKOUT AND I/O TIMING



† In EC and RC modes only.

TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↓ to CLKOUT↓		—	15 ‡	30 ‡	ns	Note 1
11	TosH2ckH	OSC1↓ to CLKOUT↑		—	15 ‡	30 ‡	ns	Note 1
12	TckR	CLKOUT rise time		—	5 ‡	15 ‡	ns	Note 1
13	TckF	CLKOUT fall time		—	5 ‡	15 ‡	ns	Note 1
14	TckH2ioV	CLKOUT ↑ to Port out valid	PIC17CR42/42A/43/R43/44	—	—	0.5TCY + 20 ‡	ns	Note 1
			PIC17LCR42/42A/43/R43/44	—	—	0.5TCY + 50 ‡	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	PIC17CR42/42A/43/R43/44	0.25TCY + 25 ‡	—	—	ns	Note 1
			PIC17LCR42/42A/43/R43/44	0.25TCY + 50 ‡	—	—	ns	Note 1
16	TckH2ioI	Port in hold after CLKOUT↑		0 ‡	—	—	ns	Note 1
17	TosH2ioV	OSC1↓ (Q1 cycle) to Port out valid		—	—	100 ‡	ns	
18	TosH2ioI	OSC1↓ (Q2 cycle) to Port input invalid (I/O in hold time)		0 ‡	—	—	ns	
19	TioV2osH	Port input valid to OSC1↓ (I/O in setup time)		30 ‡	—	—	ns	
20	TioR	Port output rise time		—	10 ‡	35 ‡	ns	
21	TioF	Port output fall time		—	10 ‡	35 ‡	ns	
22	TinHL	INT pin high or low time		25 *	—	—	ns	
23	TrbHL	RB7:RB0 change INT high or low time		25 *	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Measurements are taken in EC Mode where CLKOUT output is 4 x TOSC.

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FIGURE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

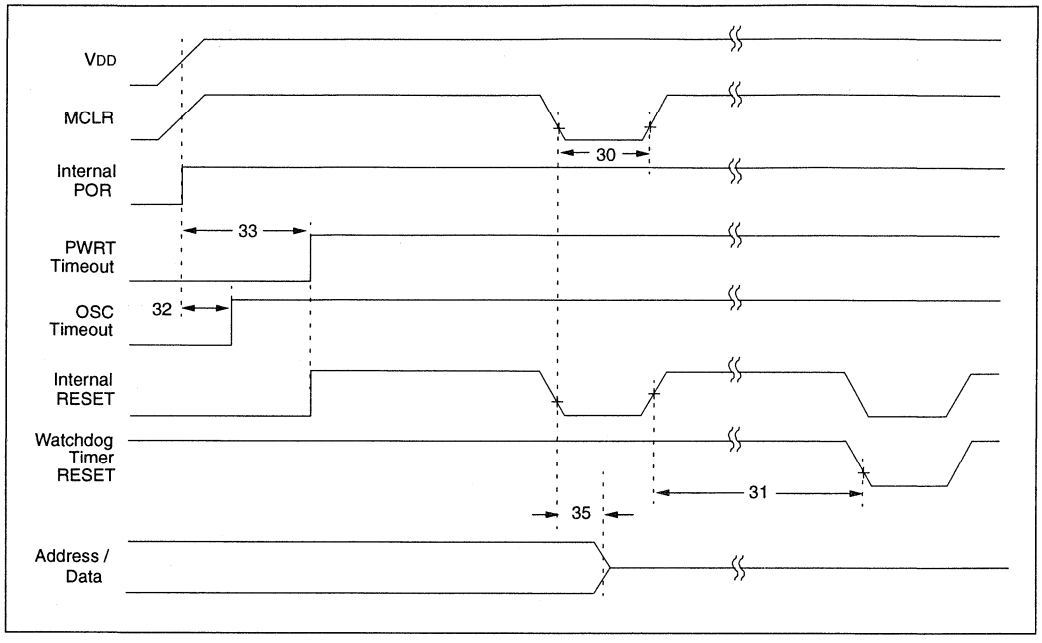

TABLE 17-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)		100 *	—	—	ns	VDD = 5V
31	Twdt	Watchdog Timer Time-out Period (Prescale = 1)		5 *	12	25 *	ms	VDD = 5V
32	Tost	Oscillation Start-up Timer Period		—	1024Tosc§	—	ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period		40 *	96	200 *	ms	VDD = 5V
35	TmcL2adl	$\overline{MCLR}$ to System Interface bus (AD15:AD0>) invalid	PIC17CR42/42A/43/R43/44	—	—	100 *	ns	
			PIC17LCR42/42A/43/R43/44	—	—	120 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

‡ These parameters are for design guidance only and are not tested, nor characterized.

§ This specification ensured by design.

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FIGURE 17-5: TIMER0 CLOCK TIMINGS

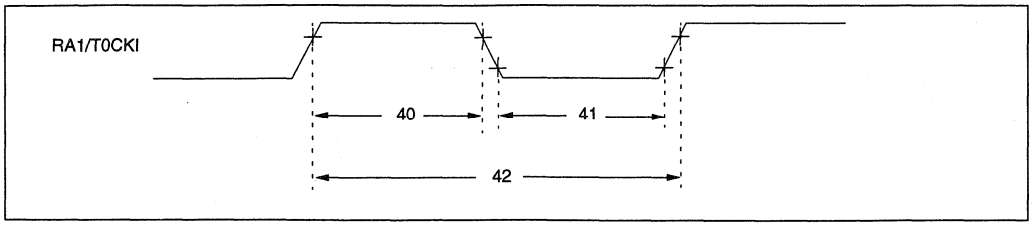

TABLE 17-5: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20 §	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20 §	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		Greater of: 20 ns or $\frac{Tcy + 40}{N}$ §	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 17-6: TIMER1, TIMER2, AND TIMER3 CLOCK TIMINGS

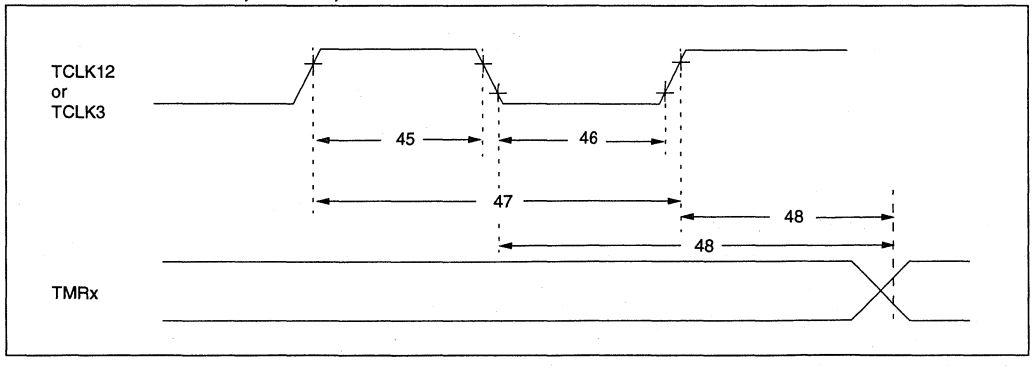

TABLE 17-6: TIMER1, TIMER2, AND TIMER3 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
45	Tt123H	TCLK12 and TCLK3 high time	0.5TCY + 20 §	—	—	ns	
46	Tt123L	TCLK12 and TCLK3 low time	0.5TCY + 20 §	—	—	ns	
47	Tt123P	TCLK12 and TCLK3 input period	$\frac{Tcy + 40}{N}$ §	—	—	ns	N = prescale value (1, 2, 4, 8)
48	TckE2tmrI	Delay from selected External Clock Edge to Timer increment	2Tosc §		6Tosc §		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Applicable Devices	42	R42	42A	43	R43	44

FIGURE 17-7: CAPTURE TIMINGS

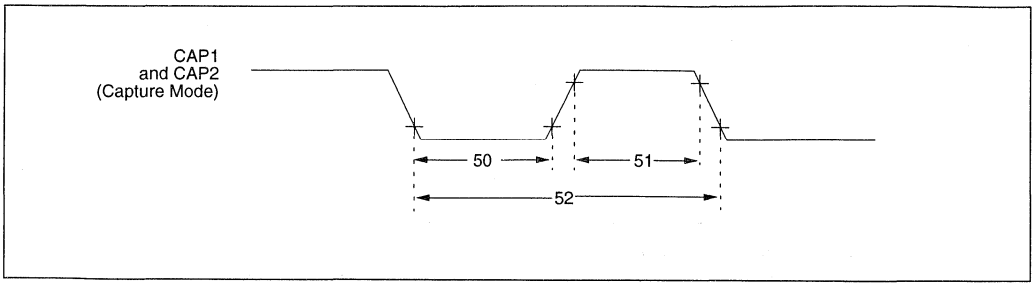

TABLE 17-7: CAPTURE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
50	TccL	Capture1 and Capture2 input low time	10 *	—	—	ns	
51	TccH	Capture1 and Capture2 input high time	10 *	—	—	ns	
52	TccP	Capture1 and Capture2 input period	$\frac{2T_{CY}}{N}$ §	—	—	ns	N = prescale value (4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

FIGURE 17-8: PWM TIMINGS

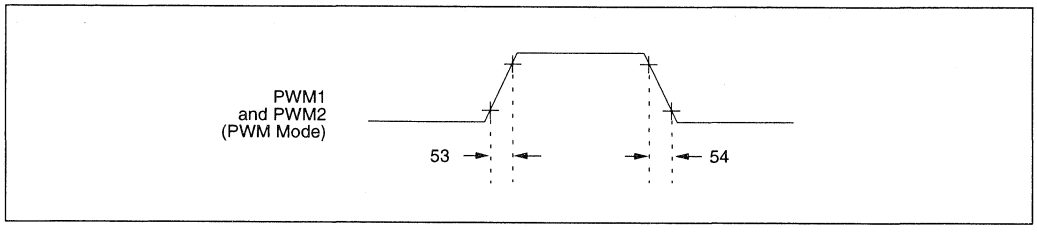

TABLE 17-8: PWM REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
53	TccR	PWM1 and PWM2 output rise time	—	10 *	35 *§	ns	
54	TccF	PWM1 and PWM2 output fall time	—	10 *	35 *§	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 17-9: USART MODULE: SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

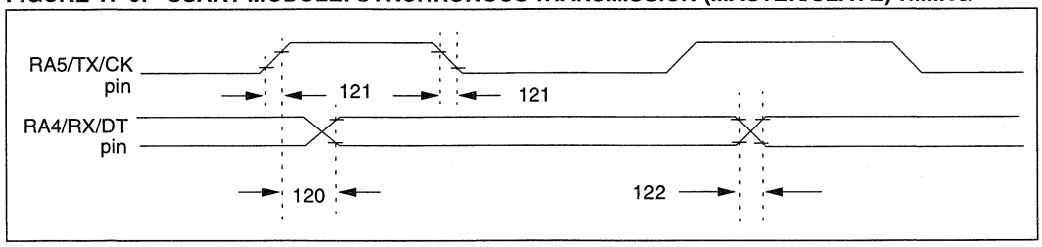

TABLE 17-9: SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC17CR42/42A/43/R43/44	—	—	50	ns	
			PIC17LCR42/42A/43/R43/44	—	—	75	ns	
121	TckRF	Clock out rise time and fall time (Master Mode)	PIC17CR42/42A/43/R43/44	—	—	25	ns	
			PIC17LCR42/42A/43/R43/44	—	—	40	ns	
122	TdtRF	Data out rise time and fall time	PIC17CR42/42A/43/R43/44	—	—	25	ns	
			PIC17LCR42/42A/43/R43/44	—	—	40	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-10: USART MODULE: SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

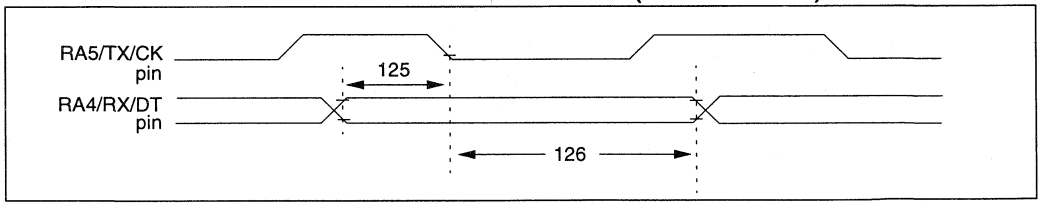

TABLE 17-10: SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data hold before CK↓ (DT hold time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK↓ (DT hold time)	15	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	42	R42	42A	43	R43	44

FIGURE 17-11: MEMORY INTERFACE WRITE TIMING (NOT SUPPORTED IN PIC17LC4X DEVICES)

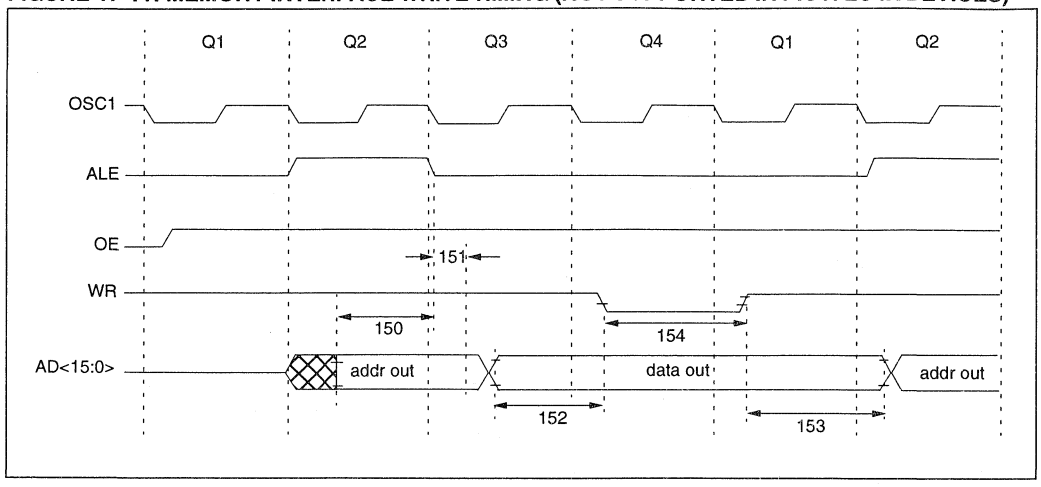

TABLE 17-11: MEMORY INTERFACE WRITE REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
150	TadV2alL	AD<15:0> (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	—	—	ns	
151	TalL2adI	ALE↓ to address out invalid (address hold time)	0	—	—	ns	
152	TadV2wrL	Data out valid to $\overline{WR}$↓ (data setup time)	0.25Tcy - 40	—	—	ns	
153	TwrH2adI	$\overline{WR}$↑ to data out invalid (data hold time)	—	0.25TCY §	—	ns	
154	TwrL	$\overline{WR}$ pulse width	—	0.25TCY §	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

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Applicable Devices | 42 | R42 | 42A | 43 | R43 | 44

FIGURE 17-12: MEMORY INTERFACE READ TIMING (NOT SUPPORTED IN PIC17LC4X DEVICES)

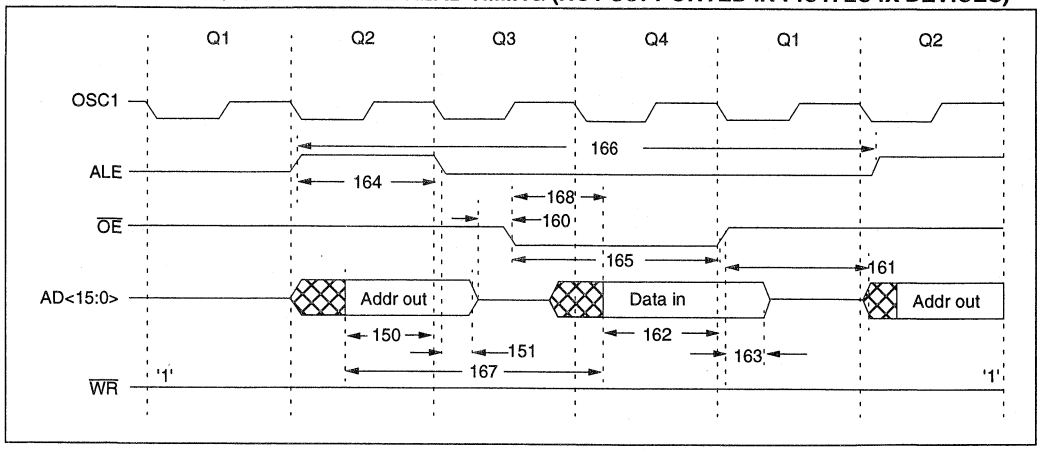

TABLE 17-12: MEMORY INTERFACE READ REQUIREMENTS (NOT SUPPORTED IN PIC17LC4X DEVICES)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
150	TadV2alL	AD15:AD0 (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	—	—	ns	
151	TalL2adI	ALE↓ to address out invalid (address hold time)	5*	—	—	ns	
160	TadZ2oeL	AD15:AD0 hi-impedance to $\overline{OE}$↓	0*	—	—	ns	
161	ToeH2adD	$\overline{OE}$↑ to AD15:AD0 driven	0.25Tcy - 15	—	—	ns	
162	TadV2oeH	Data in valid before $\overline{OE}$↑ (data setup time)	35	—	—	ns	
163	ToeH2adI	$\overline{OE}$↑to data in invalid (data hold time)	0	—	—	ns	
164	TalH	ALE pulse width	—	0.25TCY §	—	ns	
165	ToeL	$\overline{OE}$ pulse width	0.5Tcy - 35 §	—	—	ns	
166	TalH2alH	ALE↑ to ALE↑(cycle time)	—	TCY §	—	ns	
167	Tacc	Address access time	—	—	0.75TCY - 30	ns	
168	Toe	Output enable access time ($\overline{OE}$ low to Data Valid)	—	—	0.5TCY - 45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

NOTES:

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Applicable Devices 42 | R42 | 42A | 43 | R43 | 44

18.0 PIC17CR42/42A/43/R43/44 DC AND AC CHARACTERISTICS

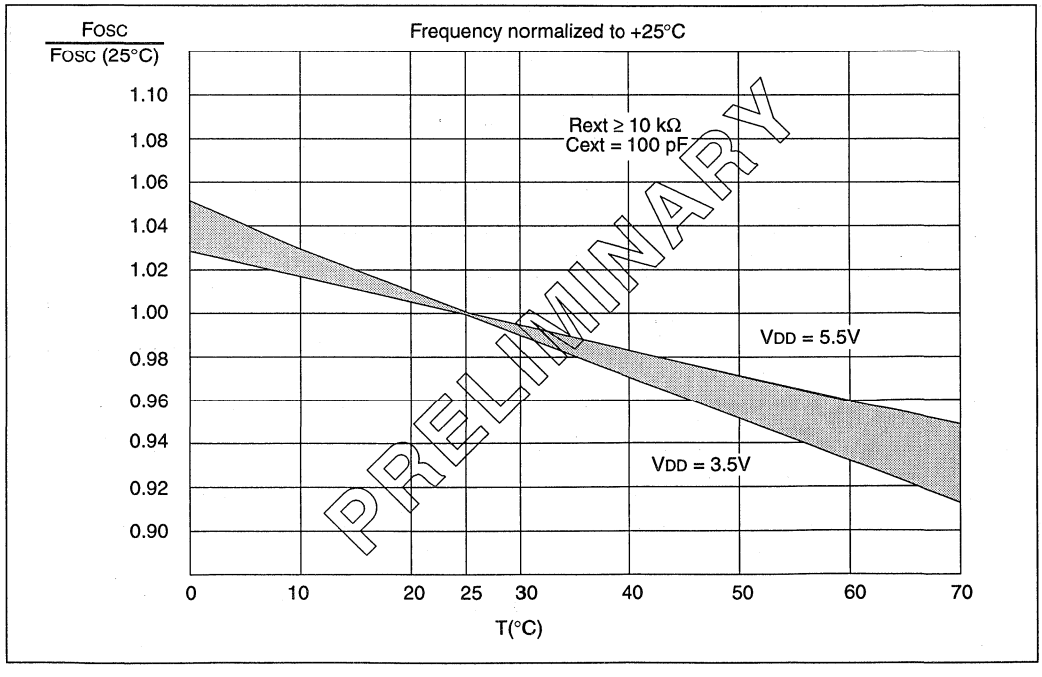
The graphs and tables provided in this section are for design guidance and are not tested nor guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are ensured to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

TABLE 18-1: PIN CAPACITANCE PER PACKAGE TYPE

Pin Name	Typical Capacitance (pF)			
	40-pin DIP	44-pin PLCC	44-pin MQFP	44-pin TQFP
All pins, except $\overline{MCLR}$, VDD, and VSS	10	10	10	10
$\overline{MCLR}$ pin	20	20	20	20

FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE



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Applicable Devices	42	R42	42A	43	R43	44

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

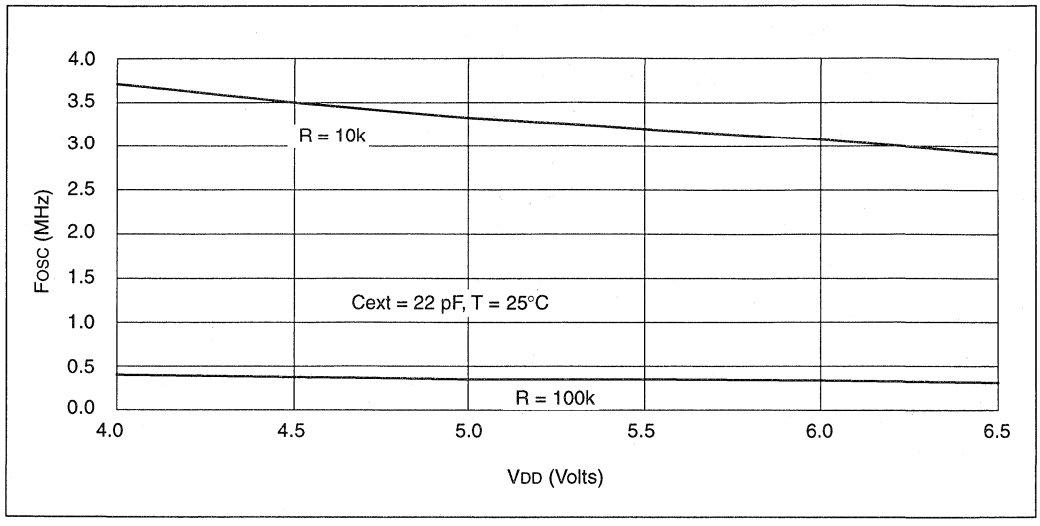

FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

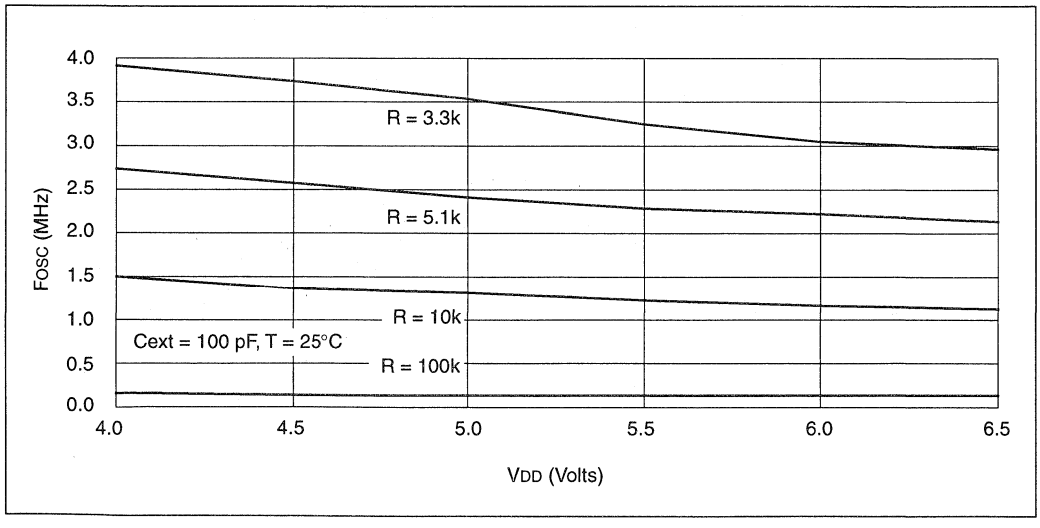

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FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

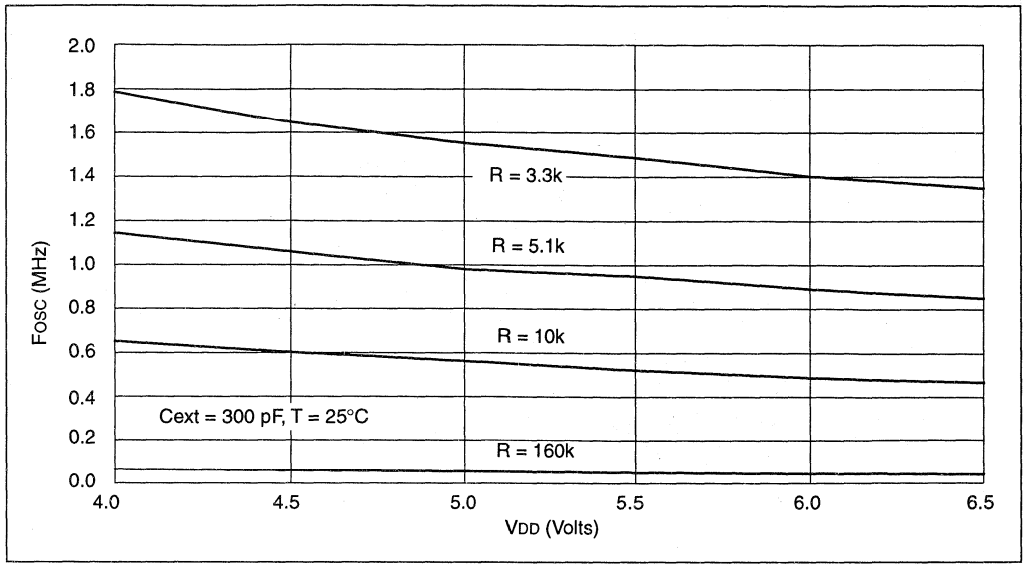

TABLE 18-2: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
22 pF	10k	3.33 MHz	± 12%
	100k	353 kHz	± 13%
100 pF	3.3k	3.54 MHz	± 10%
	5.1k	2.43 MHz	± 14%
	10k	1.30 MHz	± 17%
	100k	129 kHz	± 10%
300 pF	3.3k	1.54 MHz	± 14%
	5.1k	980 kHz	± 12%
	10k	564 kHz	± 16%
	160k	35 kHz	± 18%

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Applicable Devices	42	R42	42A	43	R43	44

FIGURE 18-5: TRANSCONDUCTANCE (gm) OF LF OSCILLATOR vs. VDD

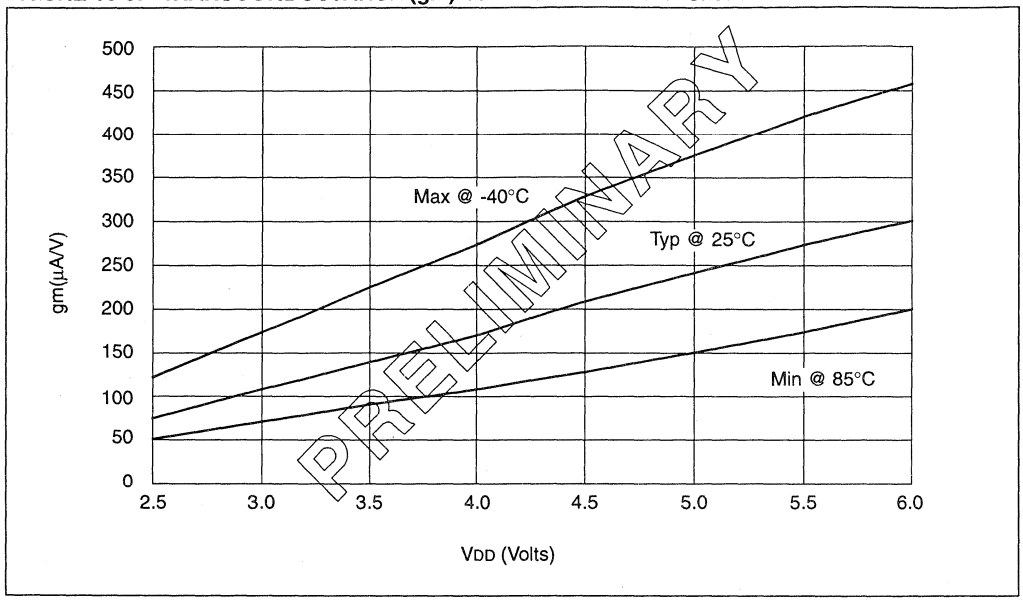

FIGURE 18-6: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

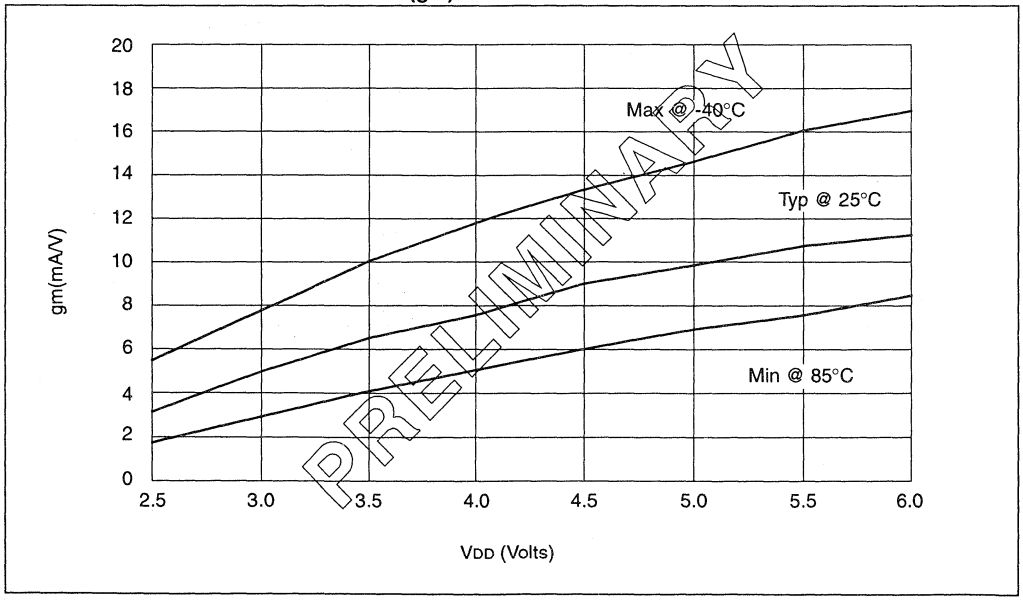

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FIGURE 18-7: TYPICAL IDD vs. FREQUENCY (EXTERNAL CLOCK 25°C)

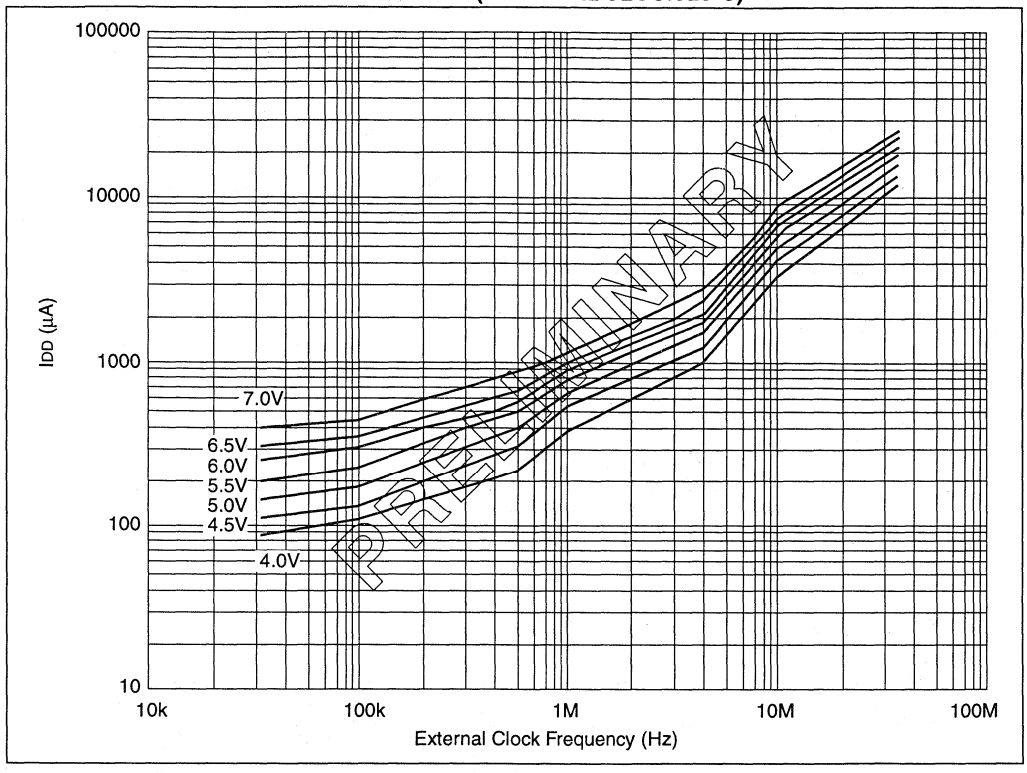
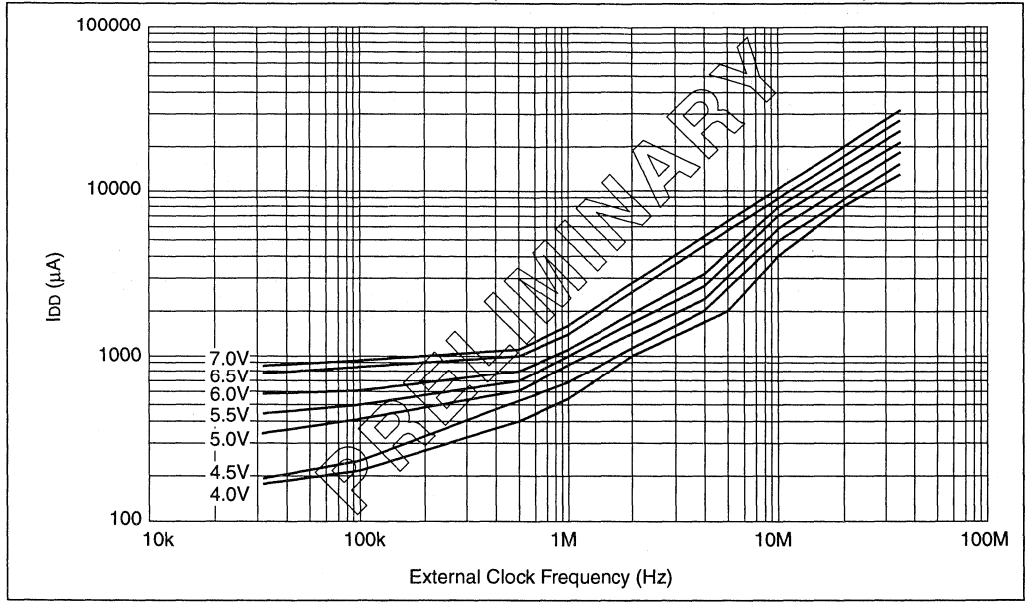


FIGURE 18-8: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK 125°C TO -40°C)



Applicable Devices 42 | R42 | 42A | 43 | R43 | 44

FIGURE 18-9: TYPICAL IPD vs. VDD WATCHDOG DISABLED 25°C

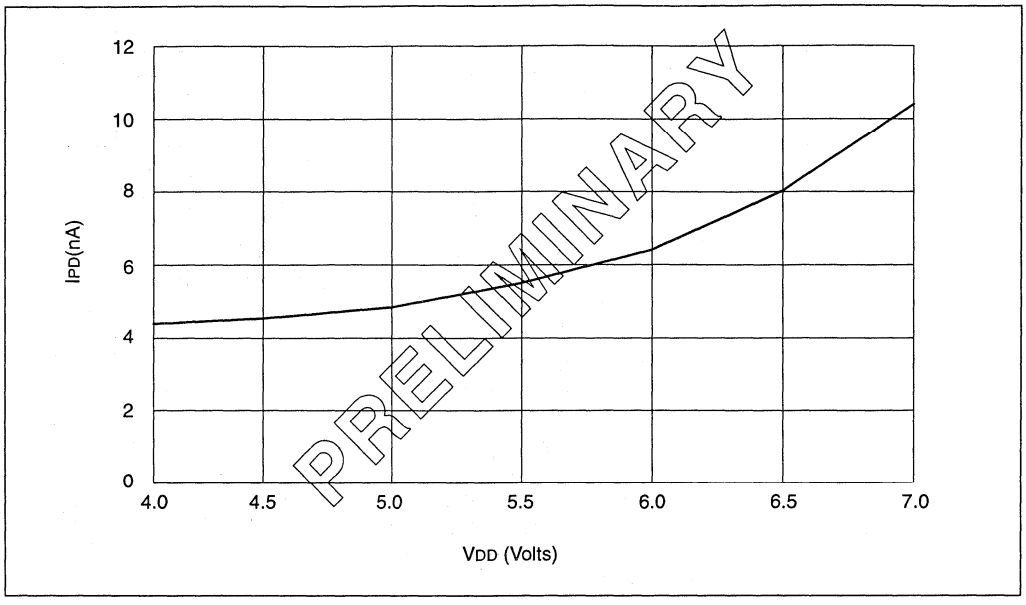


FIGURE 18-10: MAXIMUM IPD vs. VDD WATCHDOG DISABLED

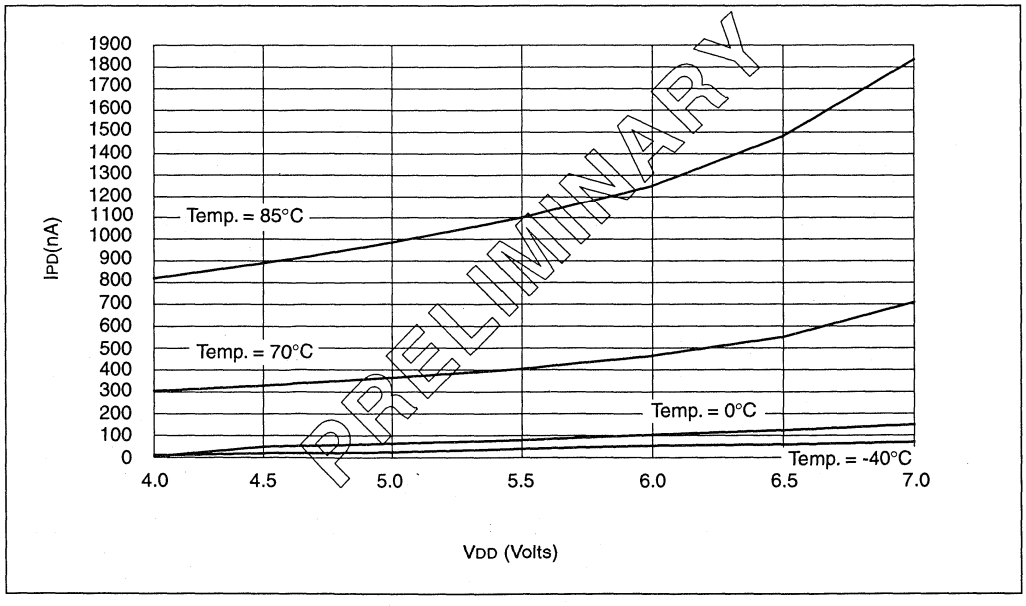


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FIGURE 18-11: TYPICAL IPD vs. VDD WATCHDOG ENABLED 25°C

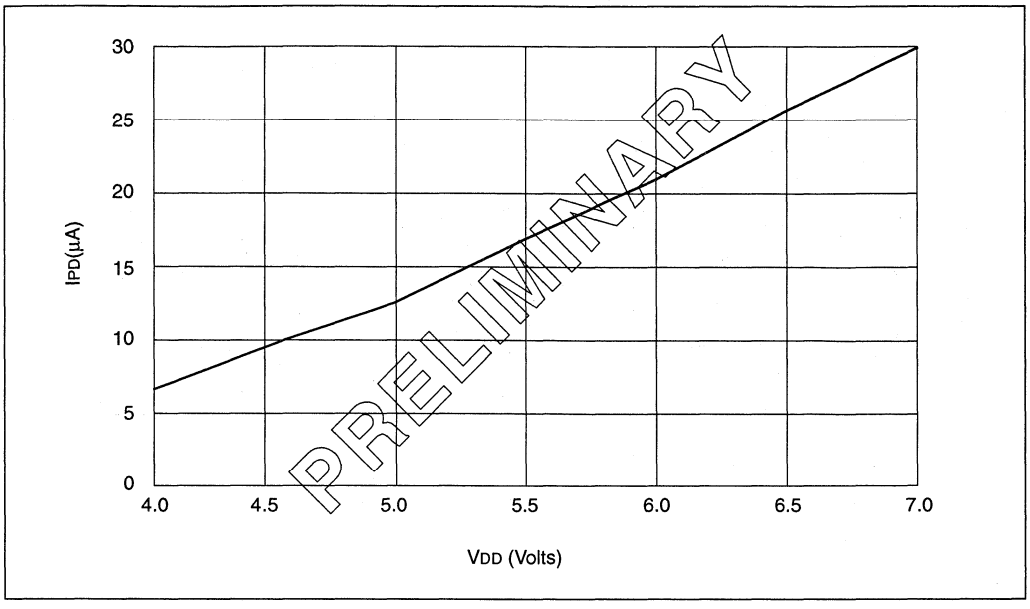
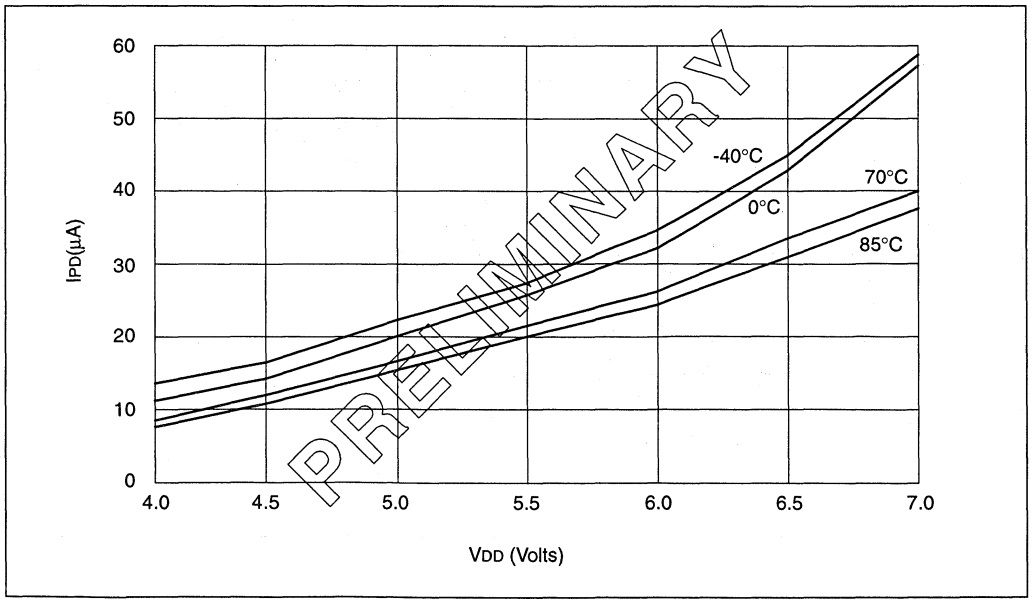


FIGURE 18-12: MAXIMUM IPD vs. VDD WATCHDOG ENABLED



Applicable Devices	42	R42	42A	43	R43	44

FIGURE 18-13: WDT TIMER TIME-OUT PERIOD vs. VDD

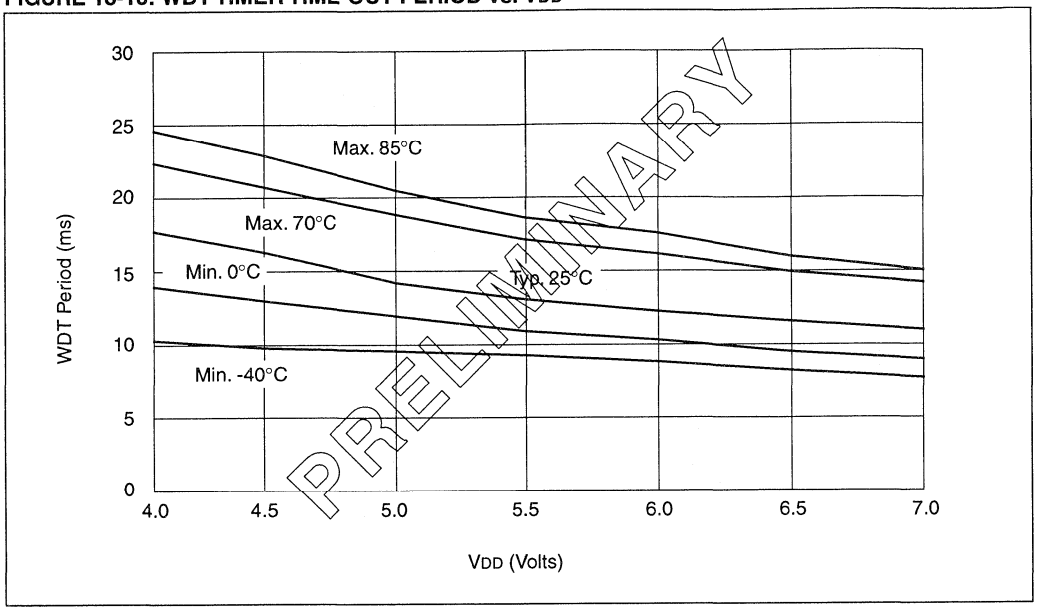
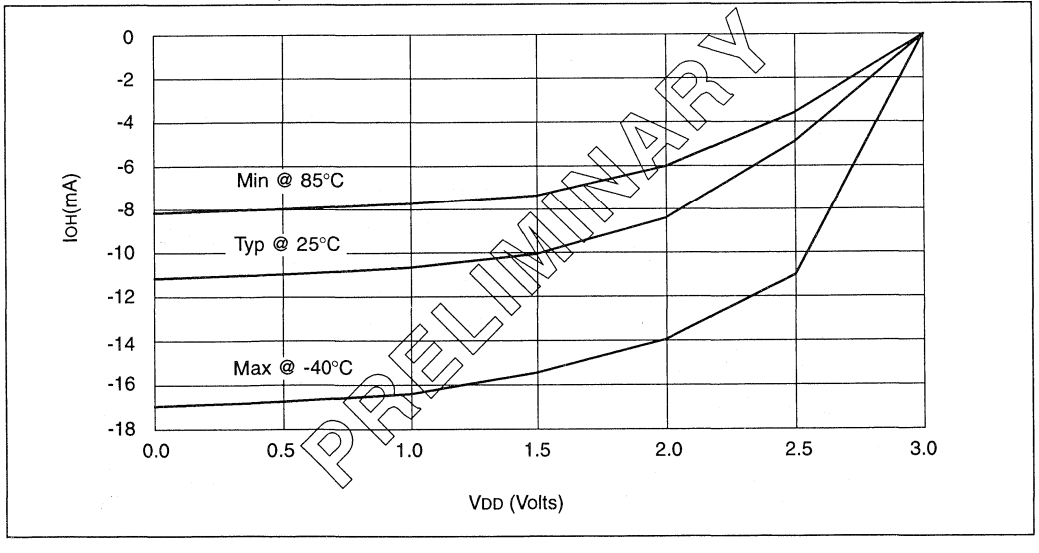


FIGURE 18-14: IOH vs. VOH, VDD = 3V



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Applicable Devices	42	R42	42A	43	R43	44

FIGURE 18-15: IOH vs. VOH, VDD = 5V

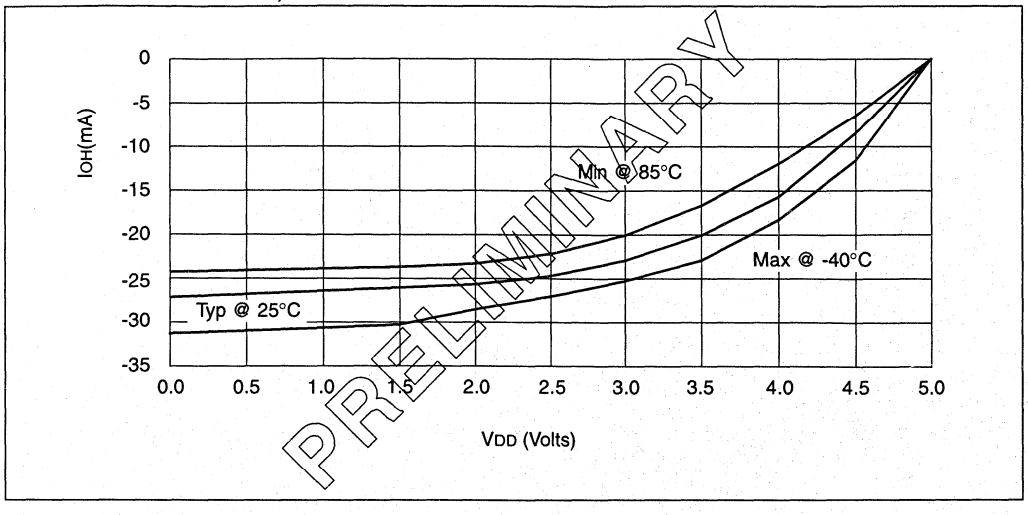
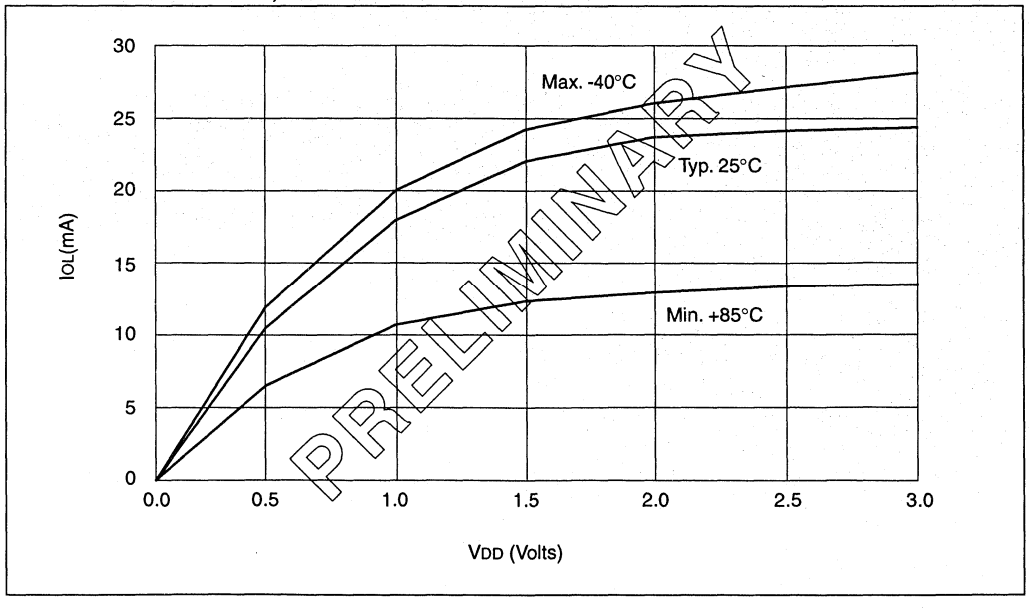


FIGURE 18-16: IOL vs. VOL, VDD = 3V



Applicable Devices	42	R42	42A	43	R43	44

FIGURE 18-17: IOL vs. VOL, VDD = 5V

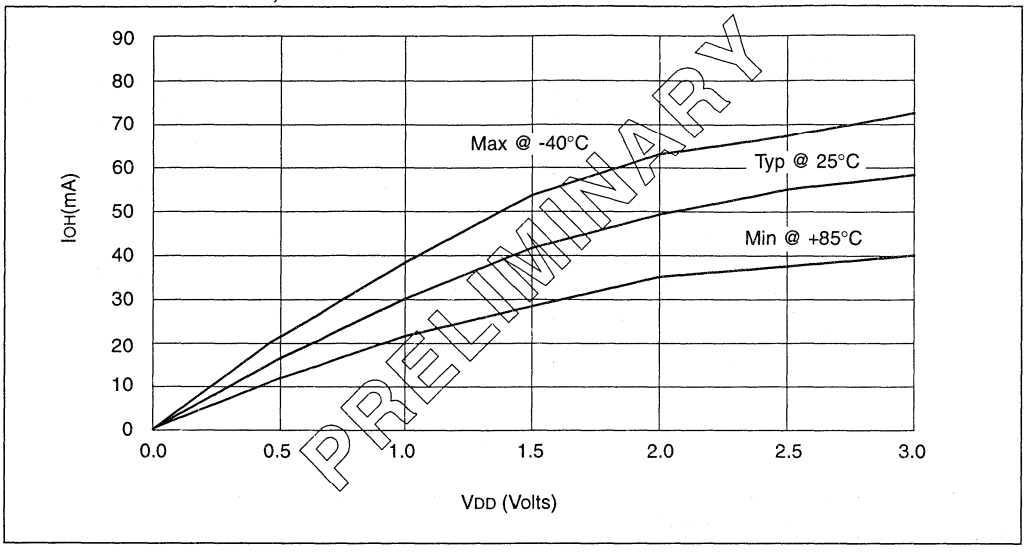


FIGURE 18-18: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS (TTL) vs. VDD

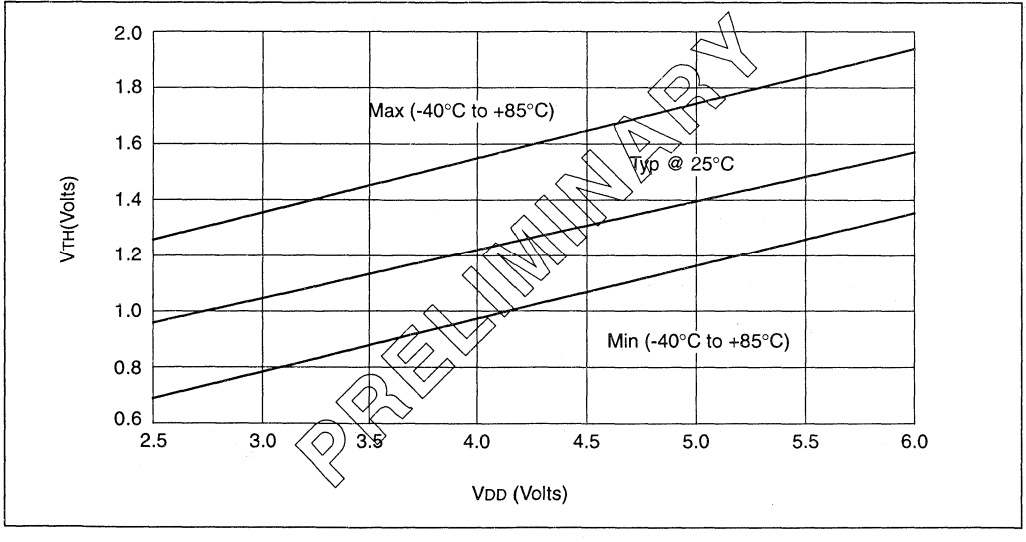


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FIGURE 18-19: VTH, VIL of I/O PINS (SCHMITT TRIGGER) vs. VDD

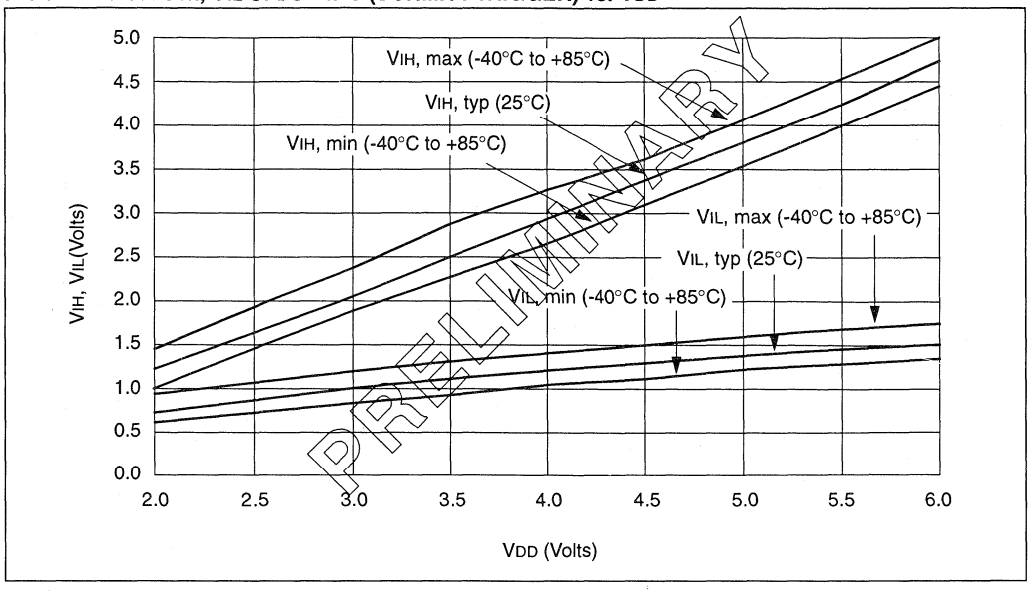
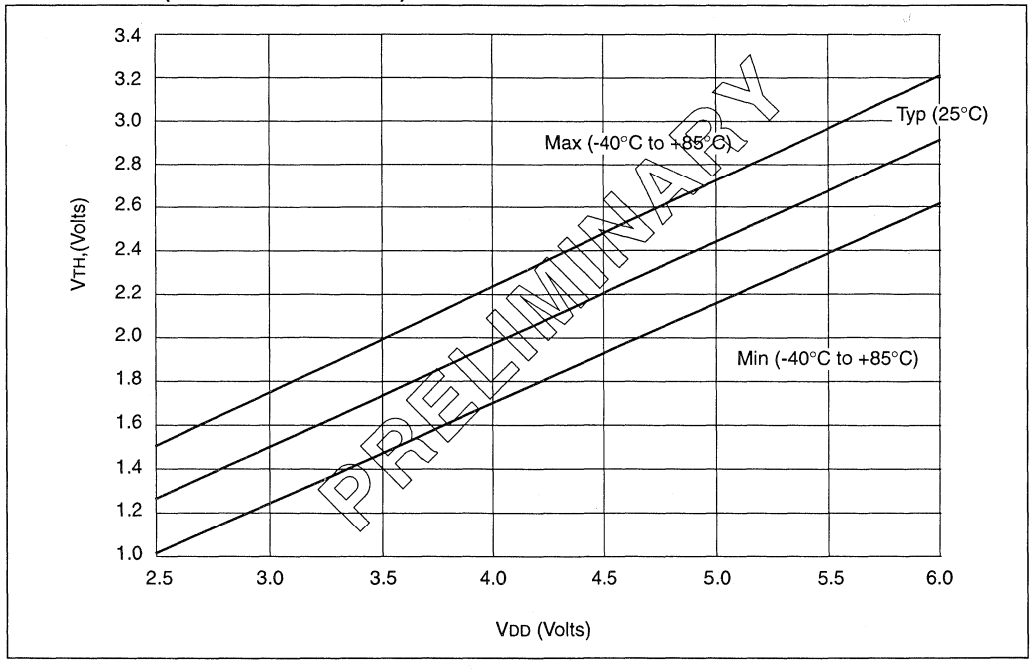


FIGURE 18-20: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT AND LF MODES) vs. VDD



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NOTES:

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APPENDIX A: MODIFICATIONS

The following is the list of modifications over the PIC16CXX microcontroller family:

1. Instruction word length is increased to 16-bit. This allows larger page sizes both in program memory (8 Kwords verses 2 Kwords) and register file (256 bytes versus 128 bytes).
2. Four modes of operation: microcontroller, protected microcontroller, extended microcontroller, and microprocessor.
3. 22 new instructions.
   The MOVF, TRIS and OPTION instructions have been removed.
4. 4 new instructions for transferring data between data memory and program memory. This can be used to "self program" the EPROM program memory.
5. Single cycle data memory to data memory transfers possible (MOVPF and MOVFP instructions). These instructions do not affect the Working register (WREG).
6. W register (WREG) is now directly addressable.
7. A PC high latch register (PCLATH) is extended to 8-bits. The PCLATCH register is now both readable and writable.
8. Data memory paging is redefined slightly.
9. DDR registers replaces function of TRIS registers.
10. Multiple Interrupt vectors added. This can decrease the latency for servicing the interrupt.
11. Stack size is increased to 16 deep.
12. BSR register for data memory paging.
13. Wake up from SLEEP operates slightly differently.
14. The Oscillator Start-Up Timer (OST) and Power-Up Timer (PWRT) operate in parallel and not in series.
15. PORTB interrupt on change feature works on all eight port pins.
16. TMR0 is 16-bit plus 8-bit prescaler.
17. Second indirect addressing register added (FSR1 and FSR2). Configuration bits can select the FSR registers to auto-increment, auto-decrement, remain unchanged after an indirect address.
18. Hardware multiplier added (8 x 8 → 16-bit) (PIC17C43 and PIC17C44 only).
19. Peripheral modules operate slightly differently.
20. Oscillator modes slightly redefined.
21. Control/Status bits and registers have been placed in different registers and the control bit for globally enabling interrupts has inverse polarity.
22. Addition of a test mode pin.
23. In-circuit serial programming is not implemented.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16CXX to PIC17CXX, the user should take the following steps:

1. Remove any TRIS and OPTION instructions, and implement the equivalent code.
2. Separate the interrupt service routine into its four vectors.
3. Replace:
   ```
   MOVF    REG1, W
   ```
   with:
   ```
   MOVFP   REG1, WREG
   ```
4. Replace:
   ```
   MOVF    REG1, W
   MOVWF   REG2
   ```
   with:
   ```
   MOVPF   REG1, REG2 ; Addr(REG1)<20h
   ```
   or
   ```
   MOVFP   REG1, REG2 ; Addr(REG2)<20h
   ```

   Note: If REG1 and REG2 are both at addresses greater then 20h, two instructions are required.
   ```
   MOVFP   REG1, WREG ;
   MOVPF   WREG, REG2 ;
   ```
5. Ensure that all bit names and register names are updated to new data memory map location.
6. Verify data memory banking.
7. Verify mode of operation for indirect addressing.
8. Verify peripheral routines for compatibility.
9. Weak pull-ups are enabled on reset.

To convert code from the PIC17C42 to all the other PIC17C4X devices, the user should take the following steps.

1. If the hardware multiply is to be used, ensure that any variables at address 18h and 19h are moved to another address.
2. Ensure that the upper nibble of the BSR was not written with a non-zero value. This may cause unexpected operation since the RAM bank is no longer 0.
3. The disabling of global interrupts has been enhanced so there is no additional testing of the GLINTD bit after a `BSF CPUSTA, GLINTD` instruction.

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APPENDIX C: WHAT'S NEW

The structure of the document has been made consistent with other data sheets. This ensures that important topics are covered across all PIC16/17 families. Here is an overview of new features.

Added the following devices:

PIC17CR42

PIC17C42A

PIC17CR43

A 33 MHz option is now available.

APPENDIX D: WHAT'S CHANGED

To make software more portable across the different PIC16/17 families, the name of several registers and control bits have been changed. This allows control bits that have the same function, to have the same name (regardless of processor family). Care must still be taken, since they may not be at the same special function register address. The following shows the register and bit names that have been changed:

Old Name	New Name
TX8/9	TX9
RC8/9	RX9
RCD8	RX9D
TXD8	TX9D

Instruction DECFSNZ corrected to DCFSNZ

Instruction INCFSNZ corrected to INFSNZ

Enhanced discussion on PWM to include equation for determining bits of PWM resolution.

Section 13.2.2 and 13.3.2 have had the description of updating the FERR and RX9 bits enhanced.

The location of configuration bit PM2 was changed (Figure 6-1 and Figure 14-1).

Enhanced description of the operation of the INTSTA register.

Added note to discussion of interrupt operation.

Tightened electrical spec D110.

Corrected steps for setting up USART Asynchronous Reception.

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APPENDIX E: ERRATA FOR PIC17C42 SILICON

The PIC17C42 devices that you have received have the following anomalies. At present there is no intention for future revisions to the present PIC17C42 silicon. If these cause issues for the application, it is recommended that you select the PIC17C42A device.

Note: New designs should use the PIC17C42A.

1. When the Oscillator Start-Up Timer (OST) is enabled (in LF or XT oscillator modes), any interrupt that wakes the processor may cause a WDT reset. This occurs when the WDT is greater than or equal to 50% time-out period when the SLEEP instruction is executed. This will not occur in either the EC or RC oscillator modes.

   Work-arounds

a) Always ensure that the CLRWDT instruction is executed before the WDT increments past 50% of the WDT period. This will keep the "false" WDT reset from occurring.

b) When using the WDT as a normal timer (WDT disabled), ensure that the WDT is less than or equal to 50% time-out period when the SLEEP instruction is executed. This can be done by monitoring the $\overline{TO}$ bit for changing state from set to clear. Example 1 shows putting the PIC17C42 to sleep.

EXAMPLE F-1: PIC17C42 TO SLEEP

```
      BTFSS   CPUSTA, TO   ; TO = 0?
      CLRWDT               ; YES, WDT = 0
LOOP  BTFSC   CPUSTA, TO   ; WDT rollover?
      GOTO    LOOP         ; NO, Wait
      SLEEP                ; YES, goto Sleep
```

2. When the clock source of Timer1 or Timer2 is selected to external clock, the overflow interrupt flag will be set twice, once when the timer equals the period, and again when the timer value is reset to 0h. If the latency to clear TMRxIF is greater than the time to the next clock pulse, no problems will be noticed. If the latency is less than the time to the next timer clock pulse, the interrupt will be serviced twice.

   Work-arounds

a) Ensure that the timer has rolled over to 0h before clearing the flag bit.

b) Clear the timer in software. Clearing the timer in software causes the period to be one count less than expected.

Design considerations

The device must not be operated outside of the specified voltage range. An external reset circuit must be used to ensure the device is in reset when a brown-out occurs or the V_{DD} rise time is too long. Failure to ensure that the device is in reset when device voltage is out of specification may cause the device to lock-up and ignore the $\overline{MCLR}$ pin.

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NOTES:

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PIC17C4X Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NO. – XX X /XX XXX

Pattern:	QTP, SQTP, ROM Code (factory specified) or Special Requirements. Blank for OTP and Windowed devices	
Package:	P	= PDIP
	JW	= Windowed CERDIP
	P	= PDIP (600 mil)
	PQ	= MQFP
	PT	= TQFP
	L	= PLCC
Temperature Range:	–	= 0°C to +70°C
	I	= –40°C to +85°C
Frequency Range:	08	= 8 MHz
	16	= 16 MHz
	25	= 25 Mhz
	33	= 33 Mhz
Device:	PIC17C44	: Standard Vdd range
	PIC17C44T	: (Tape and Reel)
	PIC17LC44	: Extended Vdd range

Examples

a) PIC17C42 – 16/P Commercial Temp., PDIP package, 16 MHZ, normal VDD limits

b) PIC17LC44 – 08/PT Commercial Temp., TQFP package, 8MHz, extended VDD limits

c) PIC17C43 – 25I/P Industrial Temp., PDIP package, 25 MHz, normal VDD limits

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Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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SECTION 14
PIC17C752/756 MICROCONTROLLER PRODUCT BRIEF

PIC17C752/756 64/68-Pin 8-Bit OTP High-Performance Microcontroller with 10-Bit A/D Product Brief 14-1

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PIC17C752/756

64/68-Pin 8-Bit OTP High-Performance Microcontroller with 10-Bit A/D
Product Brief

Device	Program Memory	Data Memory	Pins	HW Mult	10 bit A/D	16 bit Capture	10 bit PWM	No. of USARTs	I^2C Master
PIC17C752	8K x 16	454 x 8	64-68	Yes	12 ch	4 ch	3 ch	2	Yes
PIC17C756	16K x 16	902 x 8	64-68	Yes	12 ch	4 ch	3 ch	2	Yes

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Devices Included

- PIC17C752
- PIC17C756

High-Performance RISC CPU Features:

- Operating speed:
  - DC - 33 MHz clock input
  - DC - 120 ns instruction cycle
- ★ 120 ns 8 x 8 Hardware Multiplier
- ★ Up to **16K x 16** on-chip EPROM program memory
- ★ Up to **902 x 8** general purpose registers (SRAM)
- Multi-vector interrupt capability
- Sixteen levels deep hardware stack
- Direct, indirect and relative addressing modes
- Internal/External program memory execution

Peripheral Features:

- ★ Up to 50 I/O pins with individual direction control
- High current sink/source
- ★ **Four** pins that can be configured as capture input
- ★ **Three** pins can be configured as PWM output
- Capture is 16-bit, max resolution 120 ns
- PWM resolution is 1- to 10-bit. Maximum PWM frequency @: 8-bit resolution = 130 kHz 10-bit resolution = 32 kHz
- TMR0: 16-bit timer/counter with 8-bit programmable prescaler
- TMR1: 8-bit timer/counter
- TMR2: 8-bit timer/counter
- TMR3: 16-bit timer/counter
- ★ Two Serial Communications Interfaces (SCI/USART)
- Synchronous serial port (SSP) with two modes of operation:
  - 3-wire SPI™
  - ★ I^2C™ compatible including **master mode** support
- ★ **10-bit** 12-channel A/D:
  - High speed conversion rate (30 µs)
  - Can convert while in sleep mode

Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Brown-out Protection
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code Protection
- Power saving SLEEP mode
- Selectable oscillator options

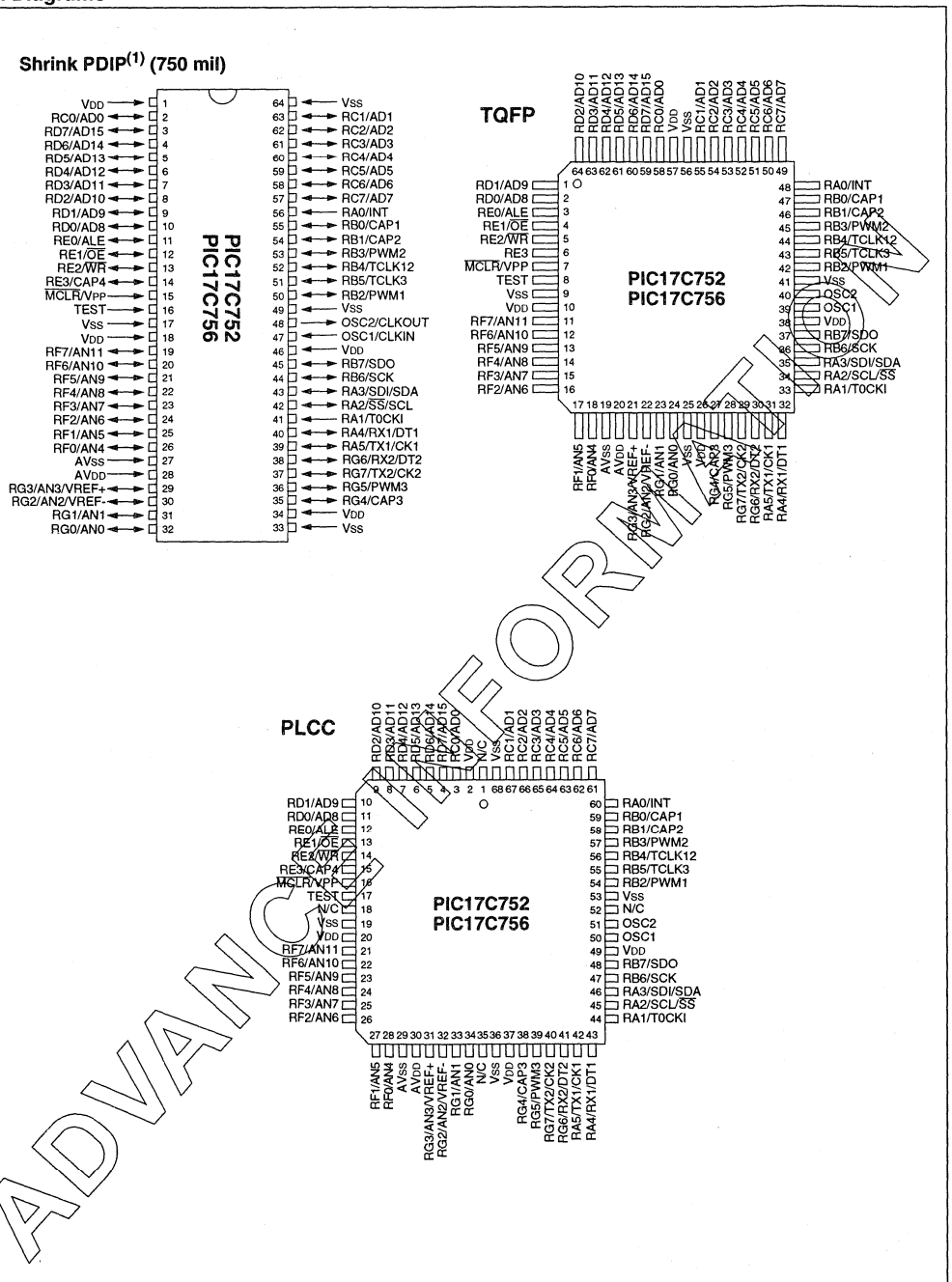
CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range (3.0V to 6.0V)
- Commercial and Industrial Temp. Range
- Low-power consumption
  - < 5.0 mA @ 5V, 4 MHz
  - 100µA typical @ 4.5V, 32 kHz
  - <1.0 µA typical standby current @ 5V

ADVANCE INFORMATION

I^2C is a trademark of Philips Corporation. SPI is a trademark of Motorola Corporaton.

Pin Diagrams



ADVANCE INFORMATION

Note 1: Please contact your local Microchip representative for availability of this package.

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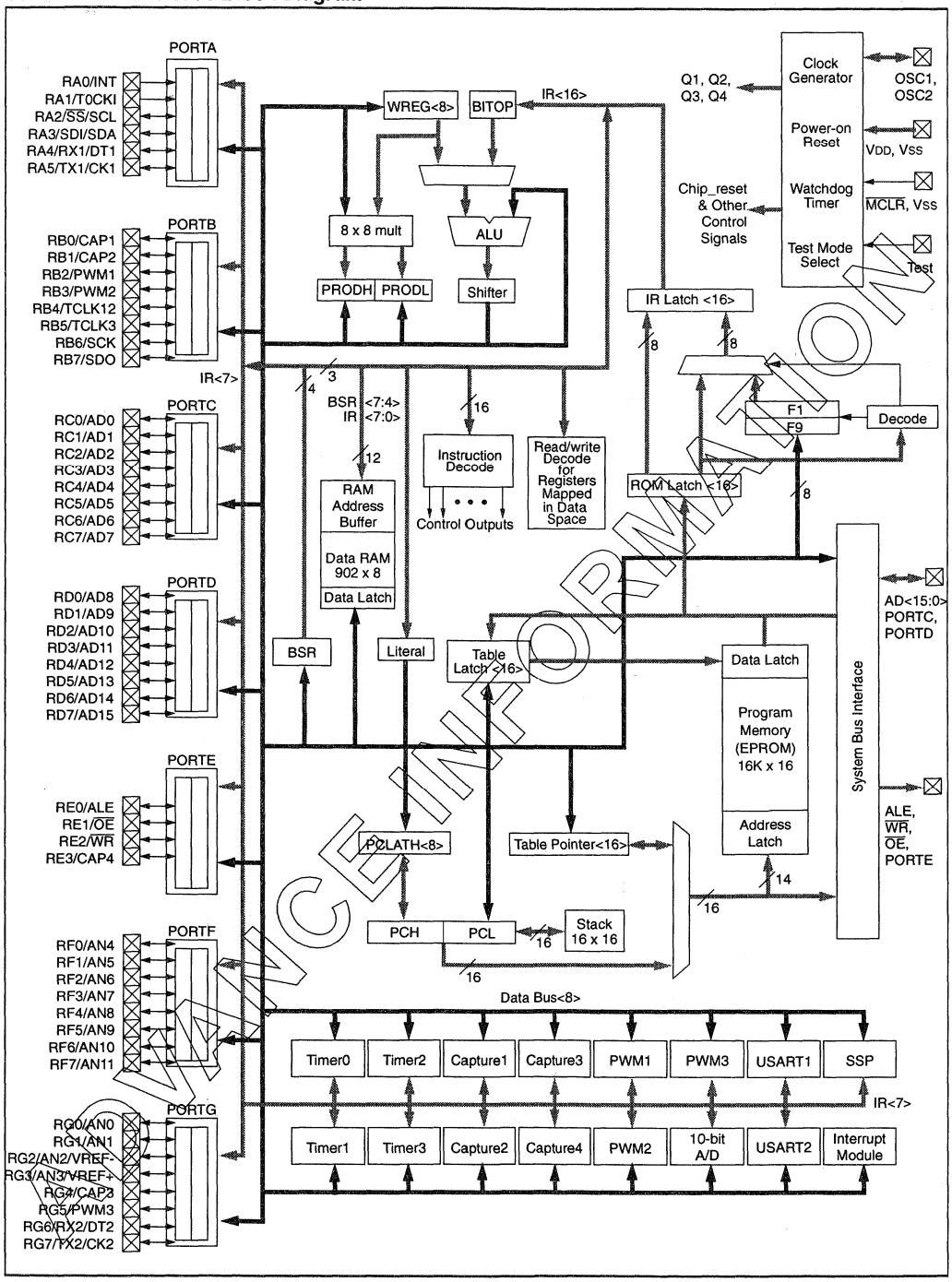
68-Pin PIC17C752/756 Block Diagram



ADVANCE INFORMATION

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SECTION 15
PIC16/17 MICROCONTROLLER INSTRUCTION SETS

PIC16C5X Instruction Set 15-1
PIC14000/PIC16CXXX Instruction Set 15-13
PIC17CXX Instruction Set 15-27

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PIC16C5X Instruction Set

1.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 1-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 1-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 1-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-Out bit
$\overline{PD}$	Power-Down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Figure 1-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 1-1: GENERAL FORMAT FOR INSTRUCTIONS

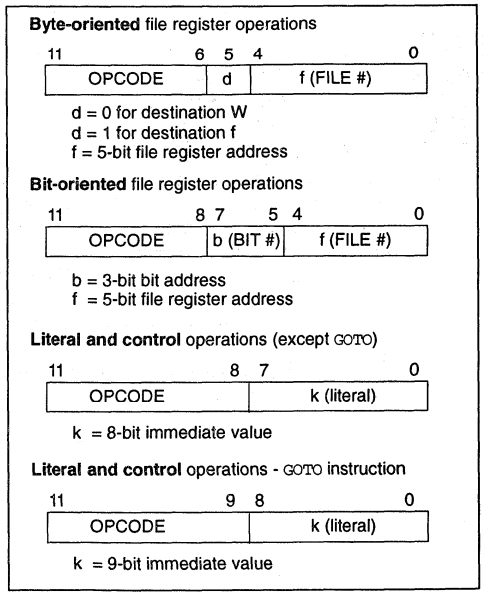

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TABLE 1-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode MSb		LSb	Status Affected	Notes
ADDWF	**f,d**	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF	**f,d**	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF	**f**	Clear f	1	0000	011f	ffff	Z	4
CLRW	**–**	Clear W	1	0000	0100	0000	Z	
COMF	**f, d**	Complement f	1	0010	01df	ffff	Z	
DECF	**f, d**	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ	**f, d**	Decrement f, Skip if 0	1(2)	0010	11df	ffff	None	2,4
INCF	**f, d**	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ	**f, d**	Increment f, Skip if 0	1(2)	0011	11df	ffff	None	2,4
IORWF	**f, d**	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF	**f, d**	Move f	1	0010	00df	ffff	Z	2,4
MOVWF	**f**	Move W to f	1	0000	001f	ffff	None	1,4
NOP	**–**	No Operation	1	0000	0000	0000	None	
RLF	**f, d**	Rotate left f through Carry	1	0011	01df	ffff	C	2,4
RRF	**f, d**	Rotate right f through Carry	1	0011	00df	ffff	C	2,4
SUBWF	**f, d**	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF	**f, d**	Swap f	1	0011	10df	ffff	None	2,4
XORWF	**f, d**	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	**f, b**	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF	**f, b**	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTFSC	**f, b**	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTFSS	**f, b**	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	**k**	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	**k**	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT	**k**	Clear Watchdog Timer	1	0000	0000	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	**k**	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	**k**	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	**k**	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	**k**	Load OPTION register	1	0000	0000	0010	None	
RETLW	**k**	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	**–**	Go into standby mode	1	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	
TRIS	**f**	Load TRIS register	1	0000	0000	0fff	None	3
XORLW	**k**	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. (See individual device data sheets, Memory Section/Indirect Data Addressing, INDF and FSR Registers)

2: When an I/O register is modified as a function of itself (e.g. `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction `TRIS f`, where f = 5, 6, or 7 causes the contents of the W register to be written to the tristate latches of PORTA, B or C, respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

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ADDWF **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0xD9
FSR = 0xC2

ANDWF **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

0001	01df	ffff

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR,    1
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0x17
FSR = 0x02

ANDLW **And literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

1110	kkkk	kkkk

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3
After Instruction
W = 0x03

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

0100	bbbf	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG,  7
```
Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

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BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: $1 \rightarrow (f<b>)$

Status Affected: None

Encoding:

0101	bbbf	ffff

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG,   7
```
Before Instruction
FLAG_REG = 0x0A

After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test f, Skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

0110	bbbf	ffff

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)

After Instruction
if FLAG<1> = 0,
PC = address (TRUE);
if FLAG<1> = 1,
PC = address (FALSE)

BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: $0 \le f \le 31$
$0 \le b < 7$

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

0111	bbbf	ffff

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)

After Instruction
If FLAG<1> = 0,
PC = address (FALSE);
if FLAG<1> = 1,
PC = address (TRUE)

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CALL **Subroutine Call**

Syntax: [*label*] CALL k

Operands: $0 \le k \le 255$

Operation: (PC) + 1→ Top of Stack;
k → PC<7:0>;
(STATUS<6:5>) → PC<10:9>;
0 → PC<8>

Status Affected: None

Encoding:

1001	kkkk	kkkk

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = address (HERE)
After Instruction
PC = address (THERE)
TOS = address (HERE + 1)

CLRF **Clear f**

Syntax: [*label*] CLRF f

Operands: $0 \le f \le 31$

Operation: 00h → (f);
1 → Z

Status Affected: Z

Encoding:

0000	011f	ffff

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W);
1 → Z

Status Affected: Z

Encoding:

0000	0100	0000

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler (if assigned);
1 → $\overline{TO}$;
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0100

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

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COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (dest)$

Status Affected: Z

Encoding:

0010	01df	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
COMF    REG1,0
```
Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - 1 \rightarrow (dest)$

Status Affected: Z

Encoding:

0000	11df	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
DECF    CNT,    1
```
Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - 1 \rightarrow d$; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    DECFSZ  CNT, 1
        GOTO    LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address (HERE)

After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 511$

Operation: $k \rightarrow PC<8:0>$;
$STATUS<6:5> \rightarrow PC<10:9>$

Status Affected: None

Encoding:

101k	kkkk	kkkk

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = address (THERE)

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INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

0010	10df	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example:
```
INCF    CNT,    1
```
Before Instruction
CNT = 0xFF
Z = 0

After Instruction
CNT = 0x00
Z = 1

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

0011	11df	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, then the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    INCFSZ    CNT,  1
        GOTO      LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address (HERE)

After Instruction
CNT = CNT + 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE +1)

IORLW **Inclusive OR literal with W**

Syntax: [*label*] IORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

1101	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW   0x35
```
Before Instruction
W = 0x9A

After Instruction
W = 0xBF
Z = 0

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (W).OR. (f) → (dest)

Status Affected: Z

Encoding:

0001	00df	ffff

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example:
```
IORWF           RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93
Z = 0

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MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

0010	00df	ffff

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR,    0
```
After Instruction
W = value in FSR register

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

1100	kkkk	kkkk

Description: The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 31$

Operation: (W) → (f)

Status Affected: None

Encoding:

0000	001f	ffff

Description: Move data from the W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVWF   TEMP_REG
```
Before Instruction
TEMP_REG = 0xFF
W = 0x4F

After Instruction
TEMP_REG = 0x4F
W = 0x4F

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

0000	0000	0000

Description: No operation.

Words: 1

Cycles: 1

Example:
```
NOP
```


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OPTION **Load OPTION Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

0000	0000	0010

Description: The content of the W register is loaded into the OPTION register.

Words: 1

Cycles: 1

Example

```
OPTION
```

Before Instruction
W = 0x07

After Instruction
OPTION = 0x07

RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

1000	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example:

```
CALL TABLE ;W contains
           ;table offset
           ;value.
•          ;W now has table
•          ;value.
•
TABLE      ADDWF PC   ;W = offset
           RETLW k1   ;Begin table
           RETLW k2   ;
           •
           •
           •
           RETLW kn   ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k8

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

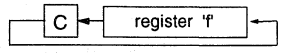
Operation: See description below

Status Affected: C

Encoding:

0011	01df	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

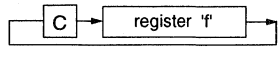
Operation: See description below

Status Affected: C

Encoding:

0011	00df	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RRF     REG1,0
```

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 0111 0011
C = 0

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SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler;
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0011

Description: Time-out status bit ($\overline{TO}$) is set. The power down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

0000	10df	ffff

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1:
```
SUBWF   REG1, 1
```
Before Instruction
REG1 = 3
W = 2
C = ?
After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:
Before Instruction
REG1 = 2
W = 2
C = ?
After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:
Before Instruction
REG1 = 1
W = 2
C = ?
After Instruction
REG1 = FF
W = 2
C = 0 ; result is negative

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SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

0011	10df	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example
```
SWAPF   REG1,   0
```
Before Instruction
REG1 = 0xA5
After Instruction
REG1 = 0xA5
W = 0X5A

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

0000	0000	0fff

Description: TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example
```
TRIS    PORTA
```
Before Instruction
W = 0XA5
After Instruction
TRISA = 0XA5

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

1111	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
XORLW   0xAF
```
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

0001	10df	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
XORWF   REG,1
```
Before Instruction
REG = 0xAF
W = 0xB5
After Instruction
REG = 0x1A
W = 0xB5

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NOTES:

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PIC14000/PIC16CXXX Instruction Set

1.0 INSTRUCTION SET SUMMARY

This instruction set is for all microcontroller devices with a 14-bit instruction word. This includes devices, such as, the PIC16C74, PIC14000, PIC16C924 and PIC16C554.

Each PIC16CXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 1-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 1-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 1-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

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The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Table 1-2 lists the instructions recognized by the MPASM assembler.

Figure 1-1 shows the three general formats that the instructions can have.

Note:	To maintain upward compatibility with future PIC16CXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 1-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

13	8	7	6	0
OPCODE		d	f (FILE #)	

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

13	10	9	7	6	0
OPCODE		b (BIT #)		f (FILE #)	

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General

13	8	7	0
OPCODE		k (literal)	

k = 8-bit immediate value

CALL and GOTO instructions only

13	11	10	0
OPCODE		k (literal)	

k = 11-bit immediate value

1.1 Special Function Registers as Source/Destination

The PIC14000/PIC16CXXX's orthogonal instruction set allows read and write of all file registers, including special function registers. There are some special situations the user should be aware of:

1.1.1 STATUS AS DESTINATION

If an instruction writes to STATUS, the Z, C and DC bits may be set or cleared as a result of the instruction and overwrite the original data bits written. For example, executing `CLRF STATUS` will clear register STATUS, and then set the Z bit leaving `0000 0100b` in the register.

1.1.2 PCL AS SOURCE OR DESTINATION

Read, write or read-modify-write on PCL may have the following results:

Read PC:	PCL → dest
Write PCL:	PCLATH → PCH; 8-bit destination value → PCL
Read-Modify-Write:	PCL→ ALU operand PCLATH → PCH; 8-bit result → PCL

Where PCH = program counter high byte (not an addressable register), PCLATH = Program counter high holding latch, dest = destination, WREG or f.

1.1.3 BIT MANIPULATION

All bit manipulation instructions are done by first reading the entire register, operating on the selected bit and writing the result back (read-modify-write). The user should keep this in mind when operating on special function registers, such as ports.

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TABLE 1-2: INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0000	0011	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

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1.2 Instruction Descriptions

ADDLW — **Add Literal and W**

Syntax: [*label*] ADDLW k

Operands: $0 \le k \le 255$

Operation: (W) + k → (W)

Status Affected: C, DC, Z

Encoding:

11	111x	kkkk	kkkk

Description: The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

Words: 1

Cycles: 1

Example
```
ADDLW   0x15
```
Before Instruction
W = 0x10
After Instruction
W = 0x25

ANDLW — **And Literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W) .AND. (k) → (W)

Status Affected: Z

Encoding:

11	1001	kkkk	kkkk

Description: The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3
After Instruction
W = 0x03

ADDWF — **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 127$, $d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0111	dfff	ffff

Description: Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0xD9
FSR = 0xC2

ANDWF — **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 127$, $d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

00	0101	dfff	ffff

Description: AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
ANDWF   FSR, 1
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0x17
FSR = 0x02

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BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

01	00bb	bfff	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example

```
BCF     FLAG_REG, 7
```

Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 1 → (f<b>)

Status Affected: None

Encoding:

01	01bb	bfff	ffff

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example

```
BSF     FLAG_REG,   7
```

Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test, Skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

01	10bb	bfff	ffff

Description: If bit 'b' in register 'f' is '0' then the next instruction is skipped.
If bit 'b' is '0' then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example

```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0,
PC = address TRUE
if FLAG<1>=1,
PC = address FALSE

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BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b < 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

01	11bb	bfff	ffff

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example

```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0,
PC = address FALSE
if FLAG<1> = 1,
PC = address TRUE

CALL **Call Subroutine**

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 2047

Operation: (PC)+ 1→ TOS,
k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

10	0kkk	kkkk	kkkk

Description: Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
HERE    CALL   THERE
```

Before Instruction
PC = Address HERE
After Instruction
PC = Address THERE
TOS = Address HERE+1

CLRF **Clear f**

Syntax: [*label*] CLRF f

Operands: 0 ≤ f ≤ 127

Operation: 00h → (f)
1 → Z

Status Affected: Z

Encoding:

00	0001	lfff	ffff

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example

```
CLRF    FLAG_REG
```

Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

00	0001	0000	0011

Description: W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example

```
CLRW
```

Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

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CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0100

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example

```
CLRWDT
```

Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: ($\bar{f}$) → (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example

```
COMF    REG1,0
```

Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) - 1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example

```
DECF    CNT,  1
```

Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) - 1 → (dest); skip if result = 0

Status Affected: None

Encoding:

00	1011	dfff	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example

```
HERE    DECFSZ  CNT, 1
        GOTO    LOOP
CONTINUE •
         •
         •
```

Before Instruction
PC = address HERE
After Instruction
CNT = CNT - 1
if CNT = 0,
PC = address CONTINUE
if CNT ≠ 0,
PC = address HERE+1

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GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: 0 ≤ k ≤ 2047

Operation: k → PC<10:0>
PCLATH<4:3> → PC<12:11>

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example
```
GOTO THERE
```
After Instruction
PC = Address THERE

INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

00	1010	dfff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example
```
INCF    CNT, 1
```
Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example
```
HERE    INCFSZ    CNT, 1
        GOTO      LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE
After Instruction
CNT = CNT + 1
if CNT= 0,
PC = address CONTINUE
if CNT≠ 0,
PC = address HERE +1

IORLW **Inclusive OR Literal with W**

Syntax: [*label*] IORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .OR. k → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
IORLW   0x35
```
Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 1

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IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .OR. (f) → (dest)

Status Affected: Z

Encoding:

00	0100	dfff	ffff

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example

```
IORWF          RESULT, 0
```

Before Instruction
RESULT = 0x13
W = 0x91
After Instruction
RESULT = 0x13
W = 0x93
Z = 1

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff

Description: The contents of register f is moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example

```
MOVF      FSR, 0
```

After Instruction
W = value in FSR register
Z = 1

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

11	00xx	kkkk	kkkk

Description: The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

Words: 1

Cycles: 1

Example

```
MOVLW     0x5A
```

After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 127$

Operation: (W) → (f)

Status Affected: None

Encoding:

00	0000	1fff	ffff

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example

```
MOVWF       OPTION
```

Before Instruction
OPTION = 0xFF
W = 0x4F
After Instruction
OPTION = 0x4F
W = 0x4F

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NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	00 | 0000 | 0xx0 | 0000
Description:	No operation.
Words:	1
Cycles:	1
Example	NOP

OPTION	Load Option Register
Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) → OPTION
Status Affected:	None
Encoding:	00 | 0000 | 0110 | 0010
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.
Words:	1
Cycles:	1
Example	**To maintain upward compatibility with future PIC16CXX products, do not use this instruction.**

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Encoding:	00 | 0000 | 0000 | 1001
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.
Words:	1
Cycles:	2
Example	RETFIE After Interrupt PC = TOS GIE = 1

RETLW	Return with Literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Encoding:	11 | 01xx | kkkk | kkkk
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.
Words:	1
Cycles:	2
Example	CALL TABLE ;W contains table ;offset value • ;W now has table value • • TABLE ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • RETLW kn ; End of table Before Instruction W = 0x07 After Instruction W = value of k8

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RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Encoding:

00	0000	0000	1000

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
RETURN
```

After Interrupt
PC = TOS

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

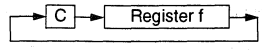
Operation: See description below

Status Affected: C

Encoding:

00	1100	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example

```
RRF             REG1,0
```

Before Instruction
REG1 = 1110 0110
C = 0
After Instruction
REG1 = 1110 0110
W = 0111 0011
C = 0

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

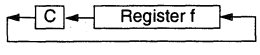
Operation: See description below

Status Affected: C

Encoding:

00	1101	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example

```
RLF             REG1,0
```

Before Instruction
REG1 = 1110 0110
C = 0
After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See Power-Down Mode (SLEEP) for more details.

Words: 1

Cycles: 1

Example:

```
SLEEP
```

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SUBLW **Subtract W from Literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

11	110x	kkkk	kkkk

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example 1:
```
SUBLW   0x02
```
Before Instruction
W = 1
C = ?
After Instruction
W = 1
C = 1; result is positive

Example 2: Before Instruction
W = 2
C = ?
After Instruction
W = 0
C = 1; result is zero

Example 3: Before Instruction
W = 3
C = ?
After Instruction
W = 0xFF
C = 0; result is negative

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0010	dfff	ffff

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1:
```
SUBWF   REG1,1
```
Before Instruction
REG1 = 3
W = 2
C = ?
After Instruction
REG1 = 1
W = 2
C = 1; result is positive

Example 2: Before Instruction
REG1 = 2
W = 2
C = ?
After Instruction
REG1 = 0
W = 2
C = 1; result is zero

Example 3: Before Instruction
REG1 = 1
W = 2
C = ?
After Instruction
REG1 = 0xFF
W = 2
C = 0; result is negative

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SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f<3:0>) → (dest<7:4>),
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example

```
SWAPF  REG,   0
```

Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0x5A

XORLW **Exclusive OR Literal with W**

Syntax: [*label*] XORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:

```
XORLW   0xAF
```

Before Instruction
W = 0xB5

After Instruction
W = 0x1A

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TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: 5 ≤ f ≤ 7

Operation: (W) → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example

```
XORWF   REG  1
```

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

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NOTES:

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PIC17CXX Instruction Set

1.0 INSTRUCTION SET SUMMARY

The PIC17CXX instruction set consists of 58 instructions. Each instruction is a 16-bit word divided into an OPCODE and one or more operands. The opcode specifies the instruction type, while the operand(s) further specify the operation of the instruction. The PIC17CXX instruction set can be grouped into three types:

- byte-oriented
- bit-oriented
- literal and control operations.

These formats are shown in Figure 1-1.

Table 1-1 shows the field descriptions for the opcodes. These descriptions are useful for understanding the opcodes in Table 1-2 and in each specific instruction descriptions.

byte-oriented instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' = '0', the result is placed in the WREG register. If 'd' = '1', the result is placed in the file register specified by the instruction.

bit-oriented instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

literal and control operations, 'k' represents an 8- or 11-bit constant or literal value.

The instruction set is highly orthogonal and is grouped into:

- byte-oriented operations
- bit-oriented operations
- literal and control operations

All instructions are executed within one single instruction cycle, unless:

- a conditional test is true
- the program counter is changed as a result of an instruction
- a table read or a table write instruction is executed (in this case, the execution takes two instruction cycles with the second cycle executed as a NOP)

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 25 MHz, the normal instruction execution time is 160 ns. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 320 ns.

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TABLE 1-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (00h to FFh)
p	Peripheral register file address (00h to 1Fh)
i	Table pointer control i = '0' (do not change) i = '1' (increment after instruction execution)
t	Table byte select t = '0' (perform operation on lower byte) t = '1' (perform operation on upper byte literal field, constant data)
WREG	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= '0' or '1') The assembler will generate code with x = '0'. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select 0 = store result in WREG 1 = store result in file register f Default is d = '1'
u	Unused, encoded as '0'
s	Destination select 0 = store result in file register f and in the WREG 1 = store result in file register f Default is s = '1'
label	Label name
C, DC, Z, OV	ALU status bits Carry, Digit Carry, Zero, Overflow
GLINTD	Global Interrupt Disable bit (CPUSTA<4>)
TBLPTR	Table Pointer (16-bit)
TBLAT	Table Latch (16-bit) consists of high byte (TBLATH) and low byte (TBLATL)
TBLATL	Table Latch low byte
TBLATH	Table Latch high byte
TOS	Top of Stack
PC	Program Counter
BSR	Bank Select Register
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination either the WREG register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

Table 1-2 lists the instructions recognized by the MPASM assembler.

Note 1: Any unused opcode is Reserved. Use of any reserved opcode may cause unexpected operation.

Note 2: The shaded instructions are not available in the PIC17C42

All instruction examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

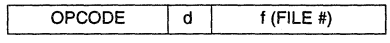
To represent a binary number:

0000 0100b

where b signifies a binary string.

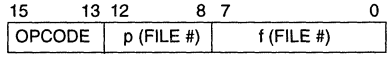
FIGURE 1-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations



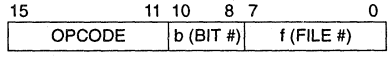
d = 0 for destination WREG
d = 1 for destination f
f = 8-bit file register address

Byte to Byte move operations



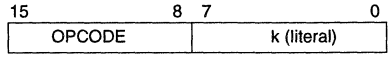
p = peripheral register file address
f = 8-bit file register address

Bit-oriented file register operations



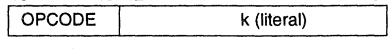
b = 3-bit address
f = 8-bit file register address

Literal and control operations



k = 8-bit immediate value

Call and GOTO operations



k = 13-bit immediate value

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1.1 Special Function Registers as Source/Destination

The PIC17CXX's orthogonal instruction set allows read and write of all file registers, including special function registers. There are some special situations the user should be aware of:

1.1.1 ALUSTA AS DESTINATION

If an instruction writes to ALUSTA, the Z, C, DC and OV bits may be set or cleared as a result of the instruction and overwrite the original data bits written. For example, executing `CLRF ALUSTA` will clear register ALUSTA, and then set the Z bit leaving `0000 0100b` in the register.

1.1.2 PCL AS SOURCE OR DESTINATION

Read, write or read-modify-write on PCL may have the following results:

Read PC:	PCH → PCLATH; PCL → dest
Write PCL:	PCLATH → PCH; 8-bit destination value → PCL
Read-Modify-Write:	PCL→ ALU operand PCLATH → PCH; 8-bit result → PCL

Where PCH = program counter high byte (not an addressable register), PCLATH = Program counter high holding latch, dest = destination, WREG or f.

1.1.3 BIT MANIPULATION

All bit manipulation instructions are done by first reading the entire register, operating on the selected bit and writing the result back (read-modify-write). The user should keep this in mind when operating on special function registers, such as ports.

1.2 Q Cycle Activity

Each instruction cycle (Tcy) is comprised of four Q cycles (Q1-Q4). The Q cycles provide the timing/designation for the Decode, Read, Execute, Write etc., of each instruction cycle. The following diagram shows the relationship of the Q cycles to the instruction cycle.

The 4 Q cycles that make up an instruction cycle (Tcy) can be generalized as:

Q1: Instruction Decode Cycle or forced NOP

Q2: Instruction Read Cycle or NOP

Q3: Instruction Execute

Q4: Instruction Write Cycle or NOP

Each instruction will show the detailed Q cycle operation for the instruction.

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FIGURE 1-2: Q CYCLE ACTIVITY

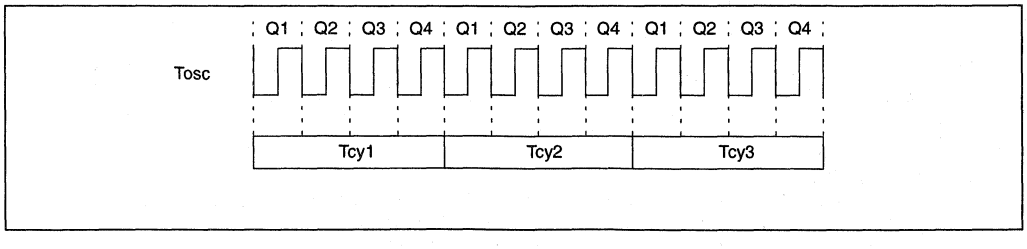

TABLE 1-2: PIC17CXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	16-bit Opcode MSb	LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	**f,d**	ADD WREG to f	1	0000 111d ffff ffff		OV,C,DC,Z	
ADDWFC	**f,d**	ADD WREG and Carry bit to f	1	0001 000d ffff ffff		OV,C,DC,Z	
ANDWF	**f,d**	AND WREG with f	1	0000 101d ffff ffff		Z	
CLRF	**f,s**	Clear f, or Clear f and Clear WREG	1	0010 100s ffff ffff		None	3
COMF	**f,d**	Complement f	1	0001 001d ffff ffff		Z	
CPFSEQ	**f**	Compare f with WREG, skip if f = WREG	1 (2)	0011 0001 ffff ffff		None	6,8
CPFSGT	**f**	Compare f with WREG, skip if f > WREG	1 (2)	0011 0010 ffff ffff		None	2,6,8
CPFSLT	**f**	Compare f with WREG, skip if f < WREG	1 (2)	0011 0000 ffff ffff		None	2,6,8
DAW	**f,s**	Decimal Adjust WREG Register	1	0010 111s ffff ffff		C	3
DECF	**f,d**	Decrement f	1	0000 011d ffff ffff		OV,C,DC,Z	
DECFSZ	**f,d**	Decrement f, skip if 0	1 (2)	0001 011d ffff ffff		None	6,8
DCFSNZ	**f,d**	Decrement f, skip if not 0	1 (2)	0010 011d ffff ffff		None	6,8
INCF	**f,d**	Increment f	1	0001 010d ffff ffff		OV,C,DC,Z	
INCFSZ	**f,d**	Increment f, skip if 0	1 (2)	0001 111d ffff ffff		None	6,8
INFSNZ	**f,d**	Increment f, skip if not 0	1 (2)	0010 010d ffff ffff		None	6,8
IORWF	**f,d**	Inclusive OR WREG with f	1	0000 100d ffff ffff		Z	
MOVFP	**f,p**	Move f to p	1	011p pppp ffff ffff		None	
MOVPF	**p,f**	Move p to f	1	010p pppp ffff ffff		Z	
MOVWF	**f**	Move WREG to f	1	0000 0001 ffff ffff		None	
MULWF	**f**	Multiply WREG with f	1	0011 0100 ffff ffff		None	9
NEGW	**f,s**	Negate WREG	1	0010 110s ffff ffff		OV,C,DC,Z	1,3
NOP	**—**	No Operation	1	0000 0000 0000 0000		None	
RLCF	**f,d**	Rotate left f through Carry	1	0001 101d ffff ffff		C	
RLNCF	**f,d**	Rotate left f (no carry)	1	0010 001d ffff ffff		None	
RRCF	**f,d**	Rotate right f through Carry	1	0001 100d ffff ffff		C	
RRNCF	**f,d**	Rotate right f (no carry)	1	0010 000d ffff ffff		None	
SETF	**f,s**	Set f	1	0010 101s ffff ffff		None	3
SUBWF	**f,d**	Subtract WREG from f	1	0000 010d ffff ffff		OV,C,DC,Z	1
SUBWFB	**f,d**	Subtract WREG from f with Borrow	1	0000 001d ffff ffff		OV,C,DC,Z	1
SWAPF	**f,d**	Swap f	1	0001 110d ffff ffff		None	
TABLRD	**t,i,f**	Table Read	2 (3)	1010 10ti ffff ffff		None	7

Legend: Refer to Table 1-1 for opcode field descriptions.

Note 1: 2's Complement method.

2: Unsigned arithmetic.

3: If s = '1', only the file is affected: If s = '0', both the WREG register and the file are affected; If only the Working register (WREG) is required to be affected, then f = WREG must be specified.

4: During an LCALL, the contents of PCLATH are loaded into the MSB of the PC and kkkk kkkk is loaded into the LSB of the PC (PCL)

5: Multiple cycle instruction for EPROM programming when table pointer selects internal EPROM. The instruction is terminated by an interrupt event. When writing to external program memory, it is a two-cycle instruction.

6: Two-cycle instruction when condition is true, else single cycle instruction.

7: Two-cycle instruction except for TABLRD to PCL (program counter low byte) in which case it takes 3 cycles.

8: A "skip" means that instruction fetched during execution of current instruction is not executed, instead an NOP is executed.

9: These instructions are not available on the PIC17C42.

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TABLE 1-2: PIC17CXX INSTRUCTION SET (Cont.'d)

Mnemonic, Operands		Description	Cycles	16-bit Opcode				Status Affected	Notes
				MSb			LSb		
TABLWT	**t,i,f**	Table Write	2	1010	11ti	ffff	ffff	None	5
TLRD	**t,f**	Table Latch Read	1	1010	00tx	ffff	ffff	None	
TLWT	**t,f**	Table Latch Write	1	1010	01tx	ffff	ffff	None	
TSTFSZ	**f**	Test f, skip if 0	1 (2)	0011	0011	ffff	ffff	None	6,8
XORWF	**f,d**	Exclusive OR WREG with f	1	0000	110d	ffff	ffff	Z	
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	**f,b**	Bit Clear f	1	1000	1bbb	ffff	ffff	None	
BSF	**f,b**	Bit Set f	1	1000	0bbb	ffff	ffff	None	
BTFSC	**f,b**	Bit test, skip if clear	1 (2)	1001	1bbb	ffff	ffff	None	6,8
BTFSS	**f,b**	Bit test, skip if set	1 (2)	1001	0bbb	ffff	ffff	None	6,8
BTG	**f,b**	Bit Toggle f	1	0011	1bbb	ffff	ffff	None	
LITERAL AND CONTROL OPERATIONS									
ADDLW	**k**	ADD literal to WREG	1	1011	0001	kkkk	kkkk	OV,C,DC,Z	
ANDLW	**k**	AND literal with WREG	1	1011	0101	kkkk	kkkk	Z	
CALL	**k**	Subroutine Call	2	111k	kkkk	kkkk	kkkk	None	7
CLRWDT	**—**	Clear Watchdog Timer	1	0000	0000	0000	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	**k**	Unconditional Branch	2	110k	kkkk	kkkk	kkkk	None	7
IORLW	**k**	Inclusive OR literal with WREG	1	1011	0011	kkkk	kkkk	Z	
LCALL	**k**	Long Call	2	1011	0111	kkkk	kkkk	None	4,7
MOVLB	**k**	Move literal to low nibble in BSR	1	1011	1000	uuuu	kkkk	None	
MOVLR	**k**	Move literal to high nibble in BSR	1	1011	101x	kkkk	uuuu	None	9
MOVLW	**k**	Move literal to WREG	1	1011	0000	kkkk	kkkk	None	
MULLW	**k**	Multiply literal with WREG	1	1011	1100	kkkk	kkkk	None	9
RETFIE	**—**	Return from interrupt (and enable interrupts)	2	0000	0000	0000	0101	GLINTD	7
RETLW	**k**	Return literal to WREG	2	1011	0110	kkkk	kkkk	None	7
RETURN	**—**	Return from subroutine	2	0000	0000	0000	0010	None	7
SLEEP	**—**	Enter SLEEP Mode	1	0000	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	**k**	Subtract WREG from literal	1	1011	0010	kkkk	kkkk	OV,C,DC,Z	
XORLW	**k**	Exclusive OR literal with WREG	1	1011	0100	kkkk	kkkk	Z	

Legend: Refer to Table 1-1 for opcode field descriptions.

Note 1: 2's Complement method.

2: Unsigned arithmetic.

3: If s = '1', only the file is affected: If s = '0', both the WREG register and the file are affected; If only the Working register (WREG) is required to be affected, then f = WREG must be specified.

4: During an LCALL, the contents of PCLATH are loaded into the MSB of the PC and kkkk kkkk is loaded into the LSB of the PC (PCL)

5: Multiple cycle instruction for EPROM programming when table pointer selects internal EPROM. The instruction is terminated by an interrupt event. When writing to external program memory, it is a two-cycle instruction.

6: Two-cycle instruction when condition is true, else single cycle instruction.

7: Two-cycle instruction except for TABLRD to PCL (program counter low byte) in which case it takes 3 cycles.

8: A "skip" means that instruction fetched during execution of current instruction is not executed, instead an NOP is executed.

9: These instructions are not available on the PIC17C42.

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ADDLW **ADD Literal to WREG**

Syntax: [*label*] ADDLW k

Operands: $0 \le k \le 255$

Operation: (WREG) + k → (WREG)

Status Affected: OV, C, DC, Z

Encoding:

1011	0001	kkkk	kkkk

Description: The contents of WREG are added to the 8-bit literal 'k' and the result is placed in WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write to WREG

Example: `ADDLW 0x15`

Before Instruction
WREG = 0x10

After Instruction
WREG = 0x25

ADDWF **ADD WREG to f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (WREG) + (f) → (dest)

Status Affected: OV, C, DC, Z

Encoding:

0000	111d	ffff	ffff

Description: Add WREG to register 'f'. If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: `ADDWF REG, 0`

Before Instruction
WREG = 0x17
REG = 0xC2

After Instruction
WREG = 0xD9
REG = 0xC2

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ADDWFC **ADD WREG and Carry bit to f**

Syntax: [*label*] ADDWFC f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (WREG) + (f) + C → (dest)

Status Affected: OV, C, DC, Z

Encoding:

0001	000d	ffff	ffff

Description: Add WREG, the Carry Flag and data memory location 'f'. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed in data memory location 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: ADDWFC REG 0

Before Instruction
Carry bit = 1
REG = 0x02
WREG = 0x4D

After Instruction
Carry bit = 0
REG = 0x02
WREG = 0x50

ANDLW **And Literal with WREG**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (WREG) .AND. (k) → (WREG)

Status Affected: Z

Encoding:

1011	0101	kkkk	kkkk

Description: The contents of WREG are AND'ed with the 8-bit literal 'k'. The result is placed in WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write to WREG

Example: ANDLW 0x5F

Before Instruction
WREG = 0xA3

After Instruction
WREG = 0x03

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ANDWF **AND WREG with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (WREG) .AND. (f) → (dest)

Status Affected: Z

Encoding:

0000	101d	ffff	ffff

Description: The contents of WREG are AND'ed with register 'f'. If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: `ANDWF REG, 1`

Before Instruction
WREG = 0x17
REG = 0xC2

After Instruction
WREG = 0x17
REG = 0x02

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \le f \le 255$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

1000	1bbb	ffff	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f'

Example: `BCF FLAG_REG, 7`

Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

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BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: $0 \le f \le 255$
$0 \le b \le 7$

Operation: $1 \rightarrow$ (f<b>)

Status Affected: None

Encoding:

1000	0bbb	ffff	ffff

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f'

Example: `BSF FLAG_REG, 7`

Before Instruction
FLAG_REG= 0x0A

After Instruction
FLAG_REG= 0x8A

BTFSC **Bit Test, skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: $0 \le f \le 255$
$0 \le b \le 7$

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

1001	1bbb	ffff	ffff

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and a `NOP` is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	NOP

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:
```
HERE    BTFSC   FLAG,1
FALSE   :
TRUE    :
```

Before Instruction
PC = address (HERE)

After Instruction
If FLAG<1> = 0;
PC = address (TRUE)
If FLAG<1> = 1;
PC = address (FALSE)

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BTFSS **Bit Test, skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: $0 \le f \le 127$
$0 \le b < 7$

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

1001	0bbb	ffff	ffff

Description: If bit 'b' in register 'f' is 1 then the next instruction is skipped.
If bit 'b' is 1, then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	NOP

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:
```
HERE    BTFSS   FLAG,1
FALSE   :
TRUE    :
```

Before Instruction
PC = address (HERE)

After Instruction
If FLAG<1> = 0;
PC = address (FALSE)
If FLAG<1> = 1;
PC = address (TRUE)

BTG **Bit Toggle f**

Syntax: [*label*] BTG f,b

Operands: $0 \le f \le 255$
$0 \le b < 7$

Operation: $(\overline{f<b>}) \rightarrow (f<b>)$

Status Affected: None

Encoding:

0011	1bbb	ffff	ffff

Description: Bit 'b' in data memory location 'f' is inverted.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f'

Example:
```
BTG     PORTC,  4
```

Before Instruction:
PORTC = 0111 0101 [0x75]

After Instruction:
PORTC = 0110 0101 [0x65]

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CALL **Subroutine Call**

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 4095

Operation: PC+ 1→ TOS, k → PC<12:0>, k<12:8> → PCLATH<4:0>; PC<15:13> → PCLATH<7:5>

Status Affected: None

Encoding:

111k	kkkk	kkkk	kkkk

Description: Subroutine call within 8K page. First, return address (PC+1) is pushed onto the stack. The 13-bit value is loaded into PC bits<12:0>. Then the upper-eight bits of the PC are copied into PCLATH. `Call` is a two-cycle instruction.

See `LCALL` for calls outside 8K memory space.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>	Execute	NOP
Forced NOP	NOP	Execute	NOP

Example: `HERE CALL THERE`

Before Instruction
PC = Address (`HERE`)

After Instruction
PC = Address (`THERE`)
TOS = Address (`HERE + 1`)

CLRF **Clear f**

Syntax: [*label*] CLRF f,s

Operands: 0 ≤ f ≤ 255

Operation: 00h → f, s ∈ [0,1]
00h → dest

Status Affected: None

Encoding:

0010	100s	ffff	ffff

Description: Clears the contents of the specified register(s).
s = 0: Data memory location 'f' and WREG are cleared.
s = 1: Data memory location 'f' is cleared.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f' and other specified register

Example: `CLRF FLAG_REG`

Before Instruction
FLAG_REG = 0x5A

After Instruction
FLAG_REG = 0x00

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CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT
0 → WDT postscaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0000	0100

Description: CLRWDT instruction resets the watchdog timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ALUSTA	Execute	NOP

Example: CLRWDT

Before Instruction
WDT counter = ?

After Instruction
WDT counter = 0x00
WDT Postscaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow$ (dest)

Status Affected: Z

Encoding:

0001	001d	ffff	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f'

Example: COMF REG1,0

Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
WREG = 0xEC

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CPFSEQ **Compare f with WREG, skip if f = WREG**

Syntax: [*label*] CPFSEQ f

Operands: $0 \le f \le 255$

Operation: (f) – (WREG), skip if (f) = (WREG) (unsigned comparison)

Status Affected: None

Encoding:

0011	0001	ffff	ffff

Description: Compares the contents of data memory location 'f' to the contents of WREG by performing an unsigned subtraction.

If 'f' = WREG then the fetched instruction is discarded and an NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	NOP

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:

```
HERE    CPFSEQ REG
NEQUAL  :
EQUAL   :
```

Before Instruction
PC Address = HERE
WREG = ?
REG = ?

After Instruction
If REG = WREG;
PC = Address (EQUAL)
If REG ≠ WREG;
PC = Address (NEQUAL)

CPFSGT **Compare f with WREG, skip if f > WREG**

Syntax: [*label*] CPFSGT f

Operands: $0 \le f \le 255$

Operation: (f) – (WREG), skip if (f) > (WREG) (unsigned comparison)

Status Affected: None

Encoding:

0011	0010	ffff	ffff

Description: Compares the contents of data memory location 'f' to the contents of the WREG by performing an unsigned subtraction.

If the contents of 'f' > the contents of WREG then the fetched instruction is discarded and an NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	NOP

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:

```
HERE      CPFSGT REG
NGREATER  :
GREATER   :
```

Before Instruction
PC = Address (HERE)
WREG = ?

After Instruction
If REG > WREG;
PC = Address (GREATER)
If REG ≤ WREG;
PC = Address (NGREATER)

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CPFSLT — **Compare f with WREG, skip if f < WREG**

Syntax: [*label*] CPFSLT f

Operands: $0 \le f \le 255$

Operation: (f) – (WREG), skip if (f) < (WREG) (unsigned comparison)

Status Affected: None

Encoding:

0011	0000	ffff	ffff

Description: Compares the contents of data memory location 'f' to the contents of WREG by performing an unsigned subtraction.

If the contents of 'f' < the contents of WREG, then the fetched instruction is discarded and an NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	NOP

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:

```
HERE    CPFSLT REG
NLESS   :
LESS    :
```

Before Instruction
PC = Address (HERE)
W = ?

After Instruction
If REG < WREG;
PC = Address (LESS)
If REG ≥ WREG;
PC = Address (NLESS)

DAW — **Decimal Adjust WREG Register**

Syntax: [*label*] DAW f,s

Operands: $0 \le f \le 255$
$s \in [0,1]$

Operation:
If [WREG<3:0> >9] .OR. [DC = 1] then
WREG<3:0> + 6 → f<3:0>, s<3:0>;
else
WREG<3:0> → f<3:0>, s<3:0>;

If [WREG<7:4> >9] .OR. [C = 1] then
WREG<7:4> + 6 → f<7:4>, s<7:4>
else
WREG<7:4> → f<7:4>, s<7:4>

Status Affected: C

Encoding:

0010	111s	ffff	ffff

Description: DAW adjusts the eight bit value in WREG resulting from the earlier addition of two variables (each in packed BCD format) and produces a correct packed BCD result.

s = 0: Result is placed in Data memory location 'f' and WREG.

s = 1: Result is placed in Data memory location 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f' and other specified register

Example1:

```
DAW   REG1, 0
```

Before Instruction
WREG = 0xA5
REG1 = ??
C = 0
DC = 0

After Instruction
WREG = 0x05
REG1 = 0x05
C = 1
DC = 0

Example 2:

Before Instruction
WREG = 0xCE
REG1 = ??
C = 0
DC = 0

After Instruction
WREG = 0x24
REG1 = 0x24
C = 1
DC = 0

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DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) – 1 → (dest)

Status Affected: OV, C, DC, Z

Encoding:

0000	011d	ffff	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: `DECF CNT, 1`

Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ **Decrement f, skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) – 1 → (dest);
skip if result = 0

Status Affected: None

Encoding:

0001	011d	ffff	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded, and an NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example:
```
HERE    DECFSZ  CNT, 1
        GOTO    LOOP
CONTINUE
```

Before Instruction
PC = Address (HERE)

After Instruction
CNT = CNT - 1
If CNT = 0;
PC = Address (CONTINUE)
If CNT ≠ 0;
PC = Address (HERE+1)

15

DCFSNZ **Decrement f, skip if not 0**

Syntax: [*label*] DCFSNZ f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) – 1 → (dest);
skip if not 0

Status Affected: None

Encoding:

0010	011d	ffff	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.
If the result is not 0, the next instruction, which is already fetched, is discarded, and an NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:
```
HERE    DCFSNZ  TEMP, 1
ZERO    :
NZERO   :
```

Before Instruction
TEMP_VALUE = ?

After Instruction
TEMP_VALUE = TEMP_VALUE - 1,
If TEMP_VALUE = 0;
PC = Address (ZERO)
If TEMP_VALUE ≠ 0;
PC = Address (NZERO)

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 8191$

Operation: k → PC<12:0>;
k<12:8> → PCLATH<4:0>,
PC<15:13> → PCLATH<7:5>

Status Affected: None

Encoding:

110k	kkkk	kkkk	kkkk

Description: GOTO allows an unconditional branch anywhere within an 8K page boundary. The thirteen bit immediate value is loaded into PC bits <12:0>. Then the upper eight bits of PC are loaded into PCLATH. GOTO is always a two-cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>	Execute	NOP
Forced NOP	NOP	Execute	NOP

Example:
```
GOTO THERE
```

After Instruction
PC = Address (THERE)

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INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: OV, C, DC, Z

Encoding:

0001	010d	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: `INCF CNT, 1`

Before Instruction
CNT = 0xFF
Z = 0
C = ?

After Instruction
CNT = 0x00
Z = 1
C = 1

INCFSZ **Increment f, skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) + 1 → (dest)
skip if result = 0

Status Affected: None

Encoding:

0001	111d	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded, and an NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:
```
HERE    INCFSZ  CNT, 1
NZERO   :
ZERO    :
```

Before Instruction
PC = Address (HERE)

After Instruction
CNT = CNT + 1
If CNT = 0;
PC = Address (ZERO)
If CNT ≠ 0;
PC = Address (NZERO)

15

INFSNZ **Increment f, skip if not 0**

Syntax: [*label*] INFSNZ f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if not 0

Status Affected: None

Encoding:

0010	010d	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.
If the result is not 0, the next instruction, which is already fetched, is discarded, and an NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:
```
HERE    INFSNZ  REG, 1
ZERO
NZERO
```
Before Instruction
REG = REG
After Instruction
REG = REG + 1
If REG = 1;
PC = Address (ZERO)
If REG = 0;
PC = Address (NZERO)

IORLW **Inclusive OR Literal with WREG**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (WREG) .OR. (k) → (WREG)

Status Affected: Z

Encoding:

1011	0011	kkkk	kkkk

Description: The contents of WREG are OR'ed with the eight bit literal 'k'. The result is placed in WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write to WREG

Example:
```
IORLW   0x35
```
Before Instruction
WREG = 0x9A
After Instruction
WREG = 0xBF

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IORWF **Inclusive OR WREG with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (WREG) .OR. (f) → (dest)

Status Affected: Z

Encoding:

0000	100d	ffff	ffff

Description: Inclusive OR WREG with register 'f'. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: `IORWF RESULT, 0`

Before Instruction
RESULT = 0x13
WREG = 0x91

After Instruction
RESULT = 0x13
WREG = 0x93

LCALL **Long Call**

Syntax: [*label*] LCALL k

Operands: $0 \le k \le 255$

Operation: PC + 1 → TOS;
k → PCL, (PCLATH) → PCH

Status Affected: None

Encoding:

1011	0111	kkkk	kkkk

Description: LCALL allows an unconditional subroutine call to anywhere within the 64k program memory space.

First, the return address (PC + 1) is pushed onto the stack. A 16-bit destination address is then loaded into the program counter. The lower 8-bits of the destination address is embedded in the instruction. The upper 8-bits of PC is loaded from PC high holding latch, PCLATH.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write register PCL
Forced NOP	NOP	Execute	NOP

Example:
```
MOVLW  HIGH(SUBROUTINE)
MOVPF  WREG, PCLATH
LCALL  LOW(SUBROUTINE)
```

Before Instruction
SUBROUTINE = 16-bit Address
PC = ?

After Instruction
PC = Address (SUBROUTINE)

15

MOVFP **Move f to p**

Syntax: [*label*] MOVFP f,p

Operands: $0 \le f \le 255$
$0 \le p \le 31$

Operation: (f) → (p)

Status Affected: None

Encoding:

011p	pppp	ffff	ffff

Description: Move data from data memory location 'f' to data memory location 'p'. Location 'f' can be anywhere in the 256 word data space (00h to FFh) while 'p' can be 00h to 1Fh.

Either 'p' or 'f' can be WREG (a useful special situation).

MOVFP is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port). Both 'f' and 'p' can be indirectly addressed.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'p'

Example: MOVFP REG1, REG2

Before Instruction
REG1 = 0x33,
REG2 = 0x11

After Instruction
REG1 = 0x33,
REG2 = 0x33

MOVLB **Move Literal to low nibble in BSR**

Syntax: [*label*] MOVLB k

Operands: $0 \le k \le 15$

Operation: k → (BSR<3:0>)

Status Affected: None

Encoding:

1011	1000	uuuu	kkkk

Description: The four bit literal 'k' is loaded in the Bank Select Register (BSR). Only the low 4-bits of the Bank Select Register are affected. The upper half of the BSR is unchanged. The assembler will encode the "u" fields as '0'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'u:k'	Execute	Write literal 'k' to BSR<3:0>

Example: MOVLB 0x5

Before Instruction
BSR register = 0x22

After Instruction
BSR register = 0x25

Note: For the PIC17C42, only the low four bits of the BSR register are physically implemented. The upper nibble is read as '0'.

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MOVLR **Move Literal to high nibble in BSR**

Syntax: [*label*] MOVLR k

Operands: $0 \le k \le 15$

Operation: k → (BSR<7:4>)

Status Affected: None

Encoding:

1011	101x	kkkk	uuuu

Description: The 4-bit literal 'k' is loaded into the most significant 4-bits of the Bank Select Register (BSR). Only the high 4-bits of the Bank Select Register are affected. The lower half of the BSR is unchanged. The assembler will encode the "u" fields as 0.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k:u'	Execute	Write literal 'k' to BSR<7:4>

Example: MOVLR 5

Before Instruction
BSR register = 0x22

After Instruction
BSR register = 0x52

Note: This instruction is not available in the PIC17C42 device.

MOVLW **Move Literal to WREG**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (WREG)

Status Affected: None

Encoding:

1011	0000	kkkk	kkkk

Description: The eight bit literal 'k' is loaded into WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write to WREG

Example: MOVLW 0x5A

After Instruction
WREG = 0x5A

15

MOVPF **Move p to f**

Syntax: [*label*] MOVPF p,f

Operands: $0 \le f \le 255$
$0 \le p \le 31$

Operation: (p) → (f)

Status Affected: Z

Encoding:

010p	pppp	ffff	ffff

Description: Move data from data memory location 'p' to data memory location 'f'. Location 'f' can be anywhere in the 256 byte data space (00h to FFh) while 'p' can be 00h to 1Fh.

Either 'p' or 'f' can be WREG (a useful special situation).

MOVPF is particularly useful for transferring a peripheral register (e.g. the timer or an I/O port) to a data memory location. Both 'f' and 'p' can be indirectly addressed.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'p'	Execute	Write register 'f'

Example: MOVPF REG1, REG2

Before Instruction
REG1 = 0x11
REG2 = 0x33

After Instruction
REG1 = 0x11
REG2 = 0x11

MOVWF **Move WREG to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 255$

Operation: (WREG) → (f)

Status Affected: None

Encoding:

0000	0001	ffff	ffff

Description: Move data from WREG to register 'f'. Location 'f' can be anywhere in the 256 word data space.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f'

Example: MOVWF REG

Before Instruction
WREG = 0x4F
REG = 0xFF

After Instruction
WREG = 0x4F
REG = 0x4F

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MULLW **Multiply Literal with WREG**

Syntax: [*label*] MULLW k

Operands: $0 \le k \le 255$

Operation: (k x WREG) → PRODH:PRODL

Status Affected: None

Encoding:

1011	1100	kkkk	kkkk

Description: An unsigned multiplication is carried out between the contents of WREG and the 8-bit literal 'k'. The 16-bit result is placed in PRODH:PRODL register pair. PRODH contains the high byte.

WREG is unchanged.

None of the status flags are affected.

Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write registers PRODH: PRODL

Example: `MULLW 0xC4`

Before Instruction
- WREG = 0xE2
- PRODH = ?
- PRODL = ?

After Instruction
- WREG = 0xC4
- PRODH = 0xAD
- PRODL = 0x08

Note: This instruction is not available in the PIC17C42 device.

MULWF **Multiply WREG with f**

Syntax: [*label*] MULWF f

Operands: $0 \le f \le 255$

Operation: (WREG x f) → PRODH:PRODL

Status Affected: None

Encoding:

0011	0100	ffff	ffff

Description: An unsigned multiplication is carried out between the contents of WREG and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte.

Both WREG and 'f' are unchanged.

None of the status flags are affected.

Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write registers PRODH: PRODL

Example: `MULWF REG`

Before Instruction
- WREG = 0xC4
- REG = 0xB5
- PRODH = ?
- PRODL = ?

After Instruction
- WREG = 0xC4
- REG = 0xB5
- PRODH = 0x8A
- PRODL = 0x94

Note: This instruction is not available in the PIC17C42 device.

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NEGW **Negate W**

Syntax: [*label*] NEGW f,s

Operands: $0 \le F \le 255$
$s \in [0,1]$

Operation: $\overline{WREG} + 1 \rightarrow (f)$;
$\overline{WREG} + 1 \rightarrow s$

Status Affected: OV, C, DC, Z

Encoding:

0010	110s	ffff	ffff

Description: WREG is negated using two's complement. If 's' is 0 the result is placed in WREG and data memory location 'f'. If 's' is 1 the result is placed only in data memory location 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f' and other specified register

Example: `NEGW REG, 0`

Before Instruction
WREG = 0011 1010 [0x3A],
REG = 1010 1011 [0xAB]

After Instruction
WREG = 1100 0111 [0xC6]
REG = 1100 0111 [0xC6]

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

0000	0000	0000	0000

Description: No operation.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	NOP	Execute	NOP

Example:

None.

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RETFIE **Return from Interrupt**

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → (PC);
0 → GLINTD;
PCLATH is unchanged.

Status Affected: GLINTD

Encoding:

0000	0000	0000	0101

Description: Return from Interrupt. Stack is POP'ed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by clearing the GLINTD bit. GLINTD is the global interrupt disable bit (CPUSTA<4>).

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register T0STA	Execute	NOP
Forced NOP	NOP	Execute	NOP

Example:

```
RETFIE
```

After Interrupt
PC = TOS
GLINTD = 0

RETLW **Return Literal to WREG**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (WREG); TOS → (PC);
PCLATH is unchanged

Status Affected: None

Encoding:

1011	0110	kkkk	kkkk

Description: WREG is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains unchanged.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write to WREG
Forced NOP	NOP	Execute	NOP

Example:

```
      CALL TABLE ; WREG contains table
                 ;  offset value
                 ;  WREG now has
                 ;  table value
        :
TABLE
      ADDWF PC   ; WREG = offset
      RETLW k0   ; Begin table
      RETLW k1   ;
        :
        :
      RETLW kn   ; End of table
```

Before Instruction
WREG = 0x07

After Instruction
WREG = value of k7

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RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC;

Status Affected: None

Encoding:

0000	0000	0000	0010

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register PCL*	Execute	NOP
Forced NOP	NOP	Execute	NOP

* Remember reading PCL causes PCLATH to be updated. This will be the high address of where the RETURN instruction is located.

Example: RETURN

After Interrupt
PC = TOS

RLCF **Rotate Left f through Carry**

Syntax: [*label*] RLCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

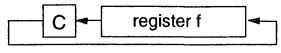
Operation: f<n> → d<n+1>;
f<7> → C;
C → d<0>

Status Affected: C

Encoding:

0001	101d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: RLCF REG,0

Before Instruction
REG = 1110 0110
C = 0

After Instruction
REG = 1110 0110
WREG = 1100 1100
C = 1

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RLNCF **Rotate Left f (no carry)**

Syntax: [*label*] RLNCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

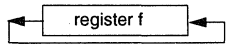
Operation: f<n> → d<n+1>;
f<7> → d<0>

Status Affected: None

Encoding:

0010	001d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: RLNCF REG, 1

Before Instruction
C = 0
REG = 1110 1011

After Instruction
C =
REG = 1101 0111

RRCF **Rotate Right f through Carry**

Syntax: [*label*] RRCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

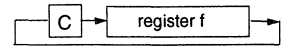
Operation: f<n> → d<n-1>;
f<0> → C;
C → d<7>

Status Affected: C

Encoding:

0001	100d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: RRCF REG1,0

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
WREG = 0111 0011
C = 0

15

RRNCF **Rotate Right f (no carry)**

Syntax: [*label*] RRNCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

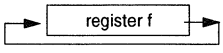
Operation: f<n> → d<n-1>;
f<0> → d<7>

Status Affected: None

Encoding:

0010	000d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example 1: `RRNCF REG, 1`

Before Instruction
WREG = ?
REG = 1101 0111

After Instruction
WREG = 0
REG = 1110 1011

Example 2: `RRNCF REG, 0`

Before Instruction
WREG = ?
REG = 1101 0111

After Instruction
WREG = 1110 1011
REG = 1101 0111

SETF **Set f**

Syntax: [*label*] SETF f,s

Operands: $0 \le f \le 255$
$s \in [0,1]$

Operation: FFh → f;
FFh → d

Status Affected: None

Encoding:

0010	101s	ffff	ffff

Description: If 's' is 0, both the data memory location 'f' and WREG are set to FFh. If 's' is 1 only the data memory location 'f' is set to FFh.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register 'f' and other specified register

Example1: `SETF REG, 0`

Before Instruction
REG = 0xDA
WREG = 0x05

After Instruction
REG = 0xFF
WREG = 0xFF

Example2: `SETF REG, 1`

Before Instruction
REG = 0xDA
WREG = 0x05

After Instruction
REG = 0xFF
WREG = 0x05

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SLEEP **Enter SLEEP mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT postscaler;
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0000	0011

Description: The power down status bit ($\overline{PD}$) is cleared. The time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register PCLATH	Execute	NOP

Example: SLEEP

Before Instruction
$\overline{TO}$ = ?
$\overline{PD}$ = ?

After Instruction
$\overline{TO}$ = 1 †
$\overline{PD}$ = 0

† If WDT causes wake-up, this bit is cleared

SUBLW **Subtract WREG from Literal**

Syntax: [*label*] SUBLW k

Operands: 0 ≤ k ≤ 255

Operation: k – (WREG) → (WREG)

Status Affected: OV, C, DC, Z

Encoding:

1011	0010	kkkk	kkkk

Description: WREG is subtracted from the eight bit literal 'k'. The result is placed in WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write to WREG

Example 1: SUBLW 0x02

Before Instruction
WREG = 1
C = ?

After Instruction
WREG = 1
C = 1 ; result is positive
Z = 0

Example 2:

Before Instruction
WREG = 2
C = ?

After Instruction
WREG = 0
C = 1 ; result is zero
Z = 1

Example 3:

Before Instruction
WREG = 3
C = ?

After Instruction
WREG = FF ; (2's complement)
C = 0 ; result is negative
Z = 1

15

SUBWF **Subtract WREG from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: OV, C, DC, Z

Encoding:

0000	010d	ffff	ffff

Description: Subtract WREG from register 'f' (2's complement method). If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example 1: `SUBWF REG1, 1`

Before Instruction
REG1 = 3
WREG = 2
C = ?

After Instruction
REG1 = 1
WREG = 2
C = 1 ; result is positive
Z = 0

Example 2:

Before Instruction
REG1 = 2
WREG = 2
C = ?

After Instruction
REG1 = 0
WREG = 2
C = 1 ; result is zero
Z = 1

Example 3:

Before Instruction
REG1 = 1
WREG = 2
C = ?

After Instruction
REG1 = FF
WREG = 2
C = 0 ; result is negative
Z = 0

SUBWFB **Subtract WREG from f with Borrow**

Syntax: [*label*] SUBWFB f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) – (W) – $\overline{C}$ → (dest)

Status Affected: OV, C, DC, Z

Encoding:

0000	001d	ffff	ffff

Description: Subtract WREG and the carry flag (borrow) from register 'f' (2's complement method). If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example 1: `SUBWFB REG1, 1`

Before Instruction
REG1 = 0x19 (0001 1001)
WREG = 0x0D (0000 1101)
C = 1

After Instruction
REG1 = 0x0C (0000 1011)
WREG = 0x0D (0000 1101)
C = 1 ; result is positive
Z = 0

Example2: `SUBWFB REG1,0`

Before Instruction
REG1 = 0x1B (0001 1011)
WREG = 0x1A (0001 1010)
C = 0

After Instruction
REG1 = 0x1B (0001 1011)
WREG = 0x00
C = 1 ; result is zero
Z = 1

Example3: `SUBWFB REG1,1`

Before Instruction
REG1 = 0x03 (0000 0011)
WREG = 0x0E (0000 1101)
C = 1

After Instruction
REG1 = 0xF5 (1111 0100) [2's comp]
WREG = 0x0E (0000 1101)
C = 0 ; result is negative
Z = 0

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SWAPF **Swap f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: f<3:0> → dest<7:4>;
f<7:4> → dest<3:0>

Status Affected: None

Encoding:

0001	110d	ffff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in WREG. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: SWAPF REG, 0

Before Instruction
REG = 0x53

After Instruction
REG = 0x35

TABLRD **Table Read**

Syntax: [*label*] TABLRD t,i,f

Operands: $0 \le f \le 255$
$i \in [0,1]$
$t \in [0,1]$

Operation: If t = 1,
TBLATH → f;
If t = 0,
TBLATL → f;
Prog Mem (TBLPTR) → TBLAT;
If i = 1,
TBLPTR + 1 → TBLPTR

Status Affected: None

Encoding:

1010	10ti	ffff	ffff

Description:
1. A byte of the table latch (TBLAT) is moved to register file 'f'.
If t = 0: the high byte is moved;
If t = 1: the low byte is moved
2. Then the contents of the program memory location pointed to by the 16-bit Table Pointer (TBLPTR) is loaded into the 16-bit Table Latch (TBLAT).
3. If i = 1: TBLPTR is incremented;
If i = 0: TBLPTR is not incremented

Words: 1

Cycles: 2 (3 cycle if f = PCL)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register TBLATH or TBLATL	Execute	Write register 'f'

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TABLRD **Table Read**

Example1: `TABLRD 1, 1, REG ;`

Before Instruction

REG	=	0x53
TBLATH	=	0xAA
TBLATL	=	0x55
TBLPTR	=	0xA356
MEMORY(TBLPTR)	=	0x1234

After Instruction (table write completion)

REG	=	0xAA
TBLATH	=	0x12
TBLATL	=	0x34
TBLPTR	=	0xA357
MEMORY(TBLPTR)	=	0x5678

Example2: `TABLRD 0, 0, REG ;`

Before Instruction

REG	=	0x53
TBLATH	=	0xAA
TBLATL	=	0x55
TBLPTR	=	0xA356
MEMORY(TBLPTR)	=	0x1234

After Instruction (table write completion)

REG	=	0x55
TBLATH	=	0x12
TBLATL	=	0x34
TBLPTR	=	0xA356
MEMORY(TBLPTR)	=	0x1234

TABLWT **Table Write**

Syntax: [*label*] TABLWT t,i,f

Operands: $0 \le f \le 255$
$i \in [0,1]$
$t \in [0,1]$

Operation: If t = 0,
f → TBLATL;
If t = 1,
f → TBLATH;
TBLAT → Prog Mem (TBLPTR);
If i = 1,
TBLPTR + 1 → TBLPTR

Status Affected: None

Encoding:

1010	11ti	ffff	ffff

Description:

1. Load value in 'f' into 16-bit table latch (TBLAT)
   If t = 0: load into low byte;
   If t = 1: load into high byte
2. The contents of TBLAT is written to the program memory location pointed to by TBLPTR
   If TBLPTR points to external program memory location, then the instruction takes two-cycle
   If TBLPTR points to an internal EPROM location, then the instruction is terminated when an interrupt is received.

Note: The $\overline{MCLR}/V_{PP}$ pin must be at the programming voltage for successful programming of internal memory.
If $\overline{MCLR}/V_{PP} = V_{DD}$
the programming sequence of internal memory will be executed, but will not be successful (although the internal memory location may be disturbed)

3. The TBLPTR can be automatically incremented
   If i = 0; TBLPTR is not incremented
   If i = 1; TBLPTR is incremented

Words: 1

Cycles: 2 (many if write is to on-chip EPROM program memory)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register TBLATH or TBLATL

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TABLWT **Table Write**

Example1: `TABLWT 0, 1, REG`

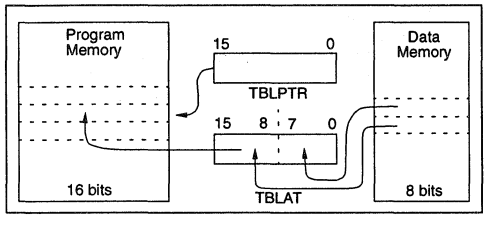
Before Instruction
- REG = 0x53
- TBLATH = 0xAA
- TBLATL = 0x55
- TBLPTR = 0xA356
- MEMORY(TBLPTR) = 0xFFFF

After Instruction (table write completion)
- REG = 0x53
- TBLATH = 0x53
- TBLATL = 0x55
- TBLPTR = 0xA357
- MEMORY(TBLPTR - 1) = 0x5355

Example 2: `TABLWT 1, 0, REG`

Before Instruction
- REG = 0x53
- TBLATH = 0xAA
- TBLATL = 0x55
- TBLPTR = 0xA356
- MEMORY(TBLPTR) = 0xFFFF

After Instruction (table write completion)
- REG = 0x53
- TBLATH = 0xAA
- TBLATL = 0x53
- TBLPTR = 0xA356
- MEMORY(TBLPTR) = 0xAA53



TLRD **Table Latch Read**

Syntax: [*label*] TLRD t,f

Operands: $0 \le f \le 255$
$t \in [0,1]$

Operation: If t = 0,
TBLATL → f;
If t = 1,
TBLATH → f

Status Affected: None

Encoding:

1010	00tx	ffff	ffff

Description: Read data from 16-bit table latch (TBLAT) into file register 'f'. Table Latch is unaffected.
If t = 1; high byte is read
If t = 0; low byte is read
This instruction is used in conjunction with `TABLRD` to transfer data from program memory to data memory.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register TBLATH or TBLATL	Execute	Write register 'f'

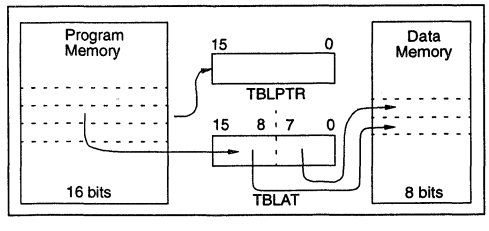
Example: `TLRD t, RAM`

Before Instruction
- t = 0
- RAM = ?
- TBLAT = 0x00AF (TBLATH = 0x00) (TBLATL = 0xAF)

After Instruction
- RAM = 0xAF
- TBLAT = 0x00AF (TBLATH = 0x00) (TBLATL = 0xAF)

Before Instruction
- t = 1
- RAM = ?
- TBLAT = 0x00AF (TBLATH = 0x00) (TBLATL = 0xAF)

After Instruction
- RAM = 0x00
- TBLAT = 0x00AF (TBLATH = 0x00) (TBLATL = 0xAF)



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TLWT **Table Latch Write**

Syntax: [*label*] TLWT t,f

Operands: $0 \le f \le 255$
$t \in [0,1]$

Operation: If t = 0,
f → TBLATL;
If t = 1,
f → TBLATH

Status Affected: None

Encoding:

1010	01tx	ffff	ffff

Description: Data from file register 'f' is written into the 16-bit table latch (TBLAT).
If t = 1; high byte is written
If t = 0; low byte is written
This instruction is used in conjunction with TABLWT to transfer data from data memory to program memory.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write register TBLATH or TBLATL

Example: TLWT t, RAM

Before Instruction
t = 0
RAM = 0xB7
TBLAT = 0x0000 (TBLATH = 0x00)
(TBLATL = 0x00)

After Instruction
RAM = 0xB7
TBLAT = 0x00B7 (TBLATH = 0x00)
(TBLATL = 0xB7)

Before Instruction
t = 1
RAM = 0xB7
TBLAT = 0x0000 (TBLATH = 0x00)
(TBLATL = 0x00)

After Instruction
RAM = 0xB7
TBLAT = 0xB700 (TBLATH = 0xB7)
(TBLATL = 0x00)

TSTFSZ **Test f, skip if 0**

Syntax: [*label*] TSTFSZ f

Operands: $0 \le f \le 255$

Operation: skip if f = 0

Status Affected: None

Encoding:

0011	0011	ffff	ffff

Description: If 'f' = 0, the next instruction, fetched during the current instruction execution, is discarded and an NOP is executed making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	NOP

If skip:

Q1	Q2	Q3	Q4
Forced NOP	NOP	Execute	NOP

Example:
```
HERE    TSTFSZ  CNT
NZERO   :
ZERO    :
```

Before Instruction
PC = Address(HERE)

After Instruction
If CNT = 0x00,
PC = Address (ZERO)
If CNT ≠ 0x00,
PC = Address (NZERO)

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XORLW **Exclusive OR Literal with WREG**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (WREG) .XOR. k → (WREG)

Status Affected: Z

Encoding:

1011	0100	kkkk	kkkk

Description: The contents of WREG are XOR'ed with the 8-bit literal 'k'. The result is placed in WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Execute	Write to WREG

Example: XORLW 0xAF

Before Instruction
WREG = 0xB5

After Instruction
WREG = 0x1A

XORWF **Exclusive OR WREG with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (WREG) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

0000	110d	ffff	ffff

Description: Exclusive OR the contents of WREG with register 'f'. If 'd' is 0 the result is stored in WREG. If 'd' is 1 the result is stored back in the register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Execute	Write to destination

Example: XORWF REG, 1

Before Instruction
REG = 0xAF
WREG = 0xB5

After Instruction
REG = 0x1A
WREG = 0xB5

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NOTES:

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MICROCHIP

SECTION 16
DEVELOPMENT SYSTEMS AND SOFTWARE SUPPORT PRODUCT SPECIFICATIONS

System Support 16-1
On-Line Support 16-3
MPLAB™ 16-5
MPASM Universal Assembler 16-7
MPLAB™ SIM 16-9
MPLAB™ C 16-11
MP-DRIVEWAY™ 16-13
*fuzzy*TECH® MP 16-15
PICMASTER® CE 16-17
ICEPIC™ 16-19
PRO MATE™ II 16-21
PICSTART® PLUS 16-23
PICSTART® LITE 16-25
KEELOQ™ Programming System 16-27
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Development Tools Selection Chart

Product	(1) MPLAB™ Integrated Development Environment	MPLAB™ C Compiler	MP-DriveWay Application Code Generator	fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	(2) PICMASTER®/ PICMASTER-CE In-Circuit Emulator	ICEPIC Low-Cost In-Circuit Emulator	(3) PRO MATE™II Universal Microchip Programmer	PICSTART® Lite Ultra Low-Cost Dev. Kit	PICSTART® Plus Low-Cost Universal Dev. Kit
PIC12C508, 509	SW007002	SW006005	—	—	EM167015/ EM167101	—	DV007003	—	DV003001
PIC14000	SW007002	SW006005	—	—	EM147001/ EM147101	—	DV007003	—	DV003001
PIC16C52, 54, 54A, 55, 56, 57, 58A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167015/ EM167101	EM167201	DV007003	DV162003	DV003001
PIC16C554, 556, 558	SW007002	SW006005	—	DV005001/ DV005002	EM167033/ EM167113	—	DV007003	—	DV003001
PIC16C61	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167021/ N/A	EM167205	DV007003	DV162003	DV003001
PIC16C62, 62A, 64, 64A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167025/ EM167103	EM167203	DV007003	DV162002	DV003001
PIC16C620, 621, 622	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167023/ EM167109	EM167202	DV007003	DV162003	DV003001
PIC16C63, 65, 65A, 73, 73A, 74, 74A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167025/ EM167103	EM167204	DV007003	DV162002	DV003001
PIC16C642, 662*	SW007002	SW006005	—	—	EM167035/ EM167105	—	DV007003	DV162002	DV003001
PIC16C71	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167027/ EM167105	EM167205	DV007003	DV162003	DV003001
PIC16C710, 711	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167027/ EM167105	—	DV007003	DV162003	DV003001
PIC16C72	SW007002	SW006005	SW006006	—	EM167025/ EM167103	—	DV007003	DV162002	DV003001
PIC16F83	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	—	DV007003	DV162003	DV003001
PIC16C84	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	EM167206	DV007003	DV162003	DV003001
PIC16F84	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	—	DV007003	DV162003	DV003001
PIC16C923, 924*	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167031/ EM167111	—	DV007003	—	DV003001
PIC17C42, 42A, 43, 44	SW007002	SW006005	SW006006	DV005001/ DV005002	EM177007/ EM177107	—	DV007003	—	DV003001

*Contact Microchip Technology for availability date

(1) MPLAB Integrated Development Environment includes MPLAB-SIM Simulator and MPASM Assembler

(2) All PICMASTER and PICMASTER-CE ordering part numbers above include PRO MATE II programmer

(3) PRO MATE socket modules are ordered separately. See development systems ordering guide for specific ordering part numbers

Product	TRUEGAUGE® Development Kit	SEEVAL® Designers Kit	Hopping Code Security Programmer Kit	Hopping Code Security Eval/ Demo Kit
All 2 wire and 3 wire Serial EEPROM's	N/A	DV243001	N/A	N/A
MTA11200B	DV114001	N/A	N/A	N/A
HCS200, 300, 301 *	N/A	N/A	PG306001	DM303001

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ON-LINE SUPPORT

Microchip BBS and Internet Connections

ON-LINE SUPPORT

Microchip provides two methods of on-line support. These are the Microchip BBS and the Microchip World Wide Web (WWW) site.

Use Microchip's Bulletin Board Service (BBS) to get current information and help about Microchip products. Microchip provides the BBS communication channel for you to use in extending your technical staff with microcontroller and memory experts.

To provide you with the most responsive service possible, the Microchip systems team monitors the BBS, posts the latest component data and software tool updates, provides technical help and embedded systems insights, and discusses how Microchip products provide project solutions.

The web site, like the BBS, is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp.mchip.com/biz/mchip

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products

Connecting to the Microchip BBS

Connect worldwide to the Microchip BBS using either the Internet or the CompuServe® communications network.

Internet:

You can telnet or ftp to the Microchip BBS at the address:

mchipbbs.microchip.com

CompuServe Communications Network:

When using the BBS via the Compuserve Network, in most cases, a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore you do not need CompuServe membership to join Microchip's BBS. There is no charge for connecting to the Microchip BBS.

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe service allow multiple users various baud rates depending on the local point of access.

The following connect procedure applies in most locations.

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe access number.
3. Depress the **<Enter>** key and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type **+**, depress the **<Enter>** key and "`Host Name:`" will appear.
5. Type MCHIPBBS, depress the <Enter> key and you will be connected to the Microchip BBS.

In the United States, to find the CompuServe phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600-14400 baud connection. After the system responds with "`Host Name:`", type `NETWORK`, depress the **<Enter>** key and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 723-1550 for your local CompuServe number.

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Microchip regularly uses the Microchip BBS to distribute technical information, application notes, source code, errata sheets, bug reports, and interim patches for Microchip systems software products. For each SIG, a moderator monitors, scans, and approves or disapproves files submitted to the SIG. No executable files are accepted from the user community in general to limit the spread of computer viruses.

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits.The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-602-786-7302 for the rest of the world.

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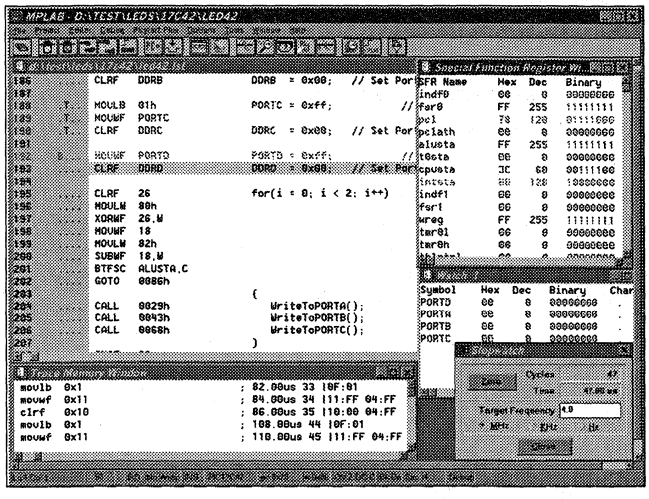
MICROCHIP

MPLAB™

Integrated Development Environment Product Brief



MPLAB gives PIC16/17 microcontroller users the flexibility to edit, compile and debug from a single user interface.

MPLAB is a Windows®-based development platform for the Microchip Technology PIC16/17 one-time-programmable (OTP) microcontroller families. MPLAB Integrated Development Environment (IDE) offers a project manager and program text editor, a user-configurable toolbar containing four pre-defined sets and a status bar which communicates editing and debugging information.

MPLAB is the common user interface for Microchip development systems tools including MPLAB Editor, MPASM Assembler, MPLAB-SIM Software Simulator, PICMASTER® In-Circuit Emulator and PICSTART® Plus Development Programmer. Additional products may become available as add-on tools in the future.

The MPLAB desktop provides the development environment and tools for developing and debugging your application as a project, allowing you to quickly move between different development and debugging modes. With the MPLAB environment, you can debug your source code, automatically locate errors in source files for editing, debug with breakpoints based on internal register values, watch the program flow with MPLAB-SIM (software simulator) or PICMASTER, make timing measurements with a "stop watch," view variables in watch windows and find quick answers to questions from the MPLAB on-line help.

Features:

MPLAB Project Manager

- Organizes the different files that comprise your application firmware under one "Project"
- Allows you to create a project; add, edit or debug a source code file in a project; and build object files

MPLAB Editor

- Full-featured programmer's editor lets you write and edit firmware source files or other text files for PIC16/17 MCUs
- Creates re-usable source file templates for quick creation of new source files

MPASM Universal Assembler

- Has full-featured macro capabilities, conditional assembly and several source and listing formats
- Generates various object code formats to support Microchip development tools and third-party programmers without exiting MPLAB

MPLAB-SIM Software Simulator

- Discrete-event simulator integrated into the MPLAB IDE features debug capabilities including unlimited breakpoints, trace, examine/modify registers, watch variables and time-stamp
- Simulates the core functions as well as most peripherals of the PIC16/17 MCUs

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MPLAB IDE

Ordering Information:

Model Name:

MPLAB

Ordering Part Number:

SW007002

Tools Supported:

PICMASTER In-Circuit Emulator

PICSTART Plus Low-cost Programmer

Host System Requirements:

PC with 386 or higher processor. Pentium™ recommended

4 MB Memory, 16 MB recommended

8 MB hard disk space, 20 MB recommended

VGA or Super VGA Monitor

Microsoft Windows 3.1 or greater

System Description:

MPLAB allows you to write, debug, and optimize the PIC16/17 microcontroller applications for firmware product designs.

MPLAB IDE software package includes the following:

- MPLAB Project Manager
- MPLAB Editor
- MPASM Universal Macro Assembler for the PIC16/17 MCUs and other language products supporting the Common Object Description file format
- MPLAB-SIM Software Simulator

MPLAB currently supports the following systems:

- PICMASTER In-Circuit Emulator
- PICSTART Plus Development Programmer

To order or obtain more information about MPLAB IDE, contact the Microchip sales office nearest you. MPLAB software may also be downloaded from Microchip's Bulletin Board System. User's can connect to the BBS through the CompuServe® communications network.

Customer Support:

Microchip maintains a worldwide network of distributors, representatives, local sales offices, Field Application Engineers and Corporate Application Engineers as well as a multifaceted Bulletin Board System. Microchip's Internet home page can be reached at: http://www.microchip.com

"The Microchip Advantage"	
MPLAB™	Integrated Development Environment (IDE)
MPASM	Universal PIC16/17 macro-assembler
MPLAB-SIM	Software Simulator
MPLAB-C	C compiler for PIC16/17 microcontrollers
PICMASTER®	Full-featured modular in-circuit emulator
ICEPIC	Low-cost modular in-circuit emulator
PRO MATE™ II	Full-featured, modular device programmer
PICSTART® Plus	Entry-level development kit with programmer
PICSTART® Lite	Low-cost entry level development kit
fuzzyTECH®-MP	Fuzzy Logic development software
MP-DriveWay™	Application Code Generator
KEELOQ®	Code Hopping Devices

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MPASM Universal Assembler

Universal PIC16/17 Microcontroller Assembler Software

This product brief describes the technical aspects of the PIC16/17 Assembler. The MPASM Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series, including the PIC16C5X, PIC16CXX and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER™).

MPASM REQUIREMENTS

MPASM will run on any IBM PC/AT® or compatible computer running DOS 5.0 or later.

MPASM ASSEMBLER FEATURES

MPASM supports the 12-bit PIC16C5X, the 14-bit PIC16CXX, and the 16-bit PIC17CXX cores.

All instructions are single-word and single-cycle, except for branches, which execute in two cycles. Most instructions operate on one or more operands.

MPASM have the following features to assist in developing software for specific user applications:

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.
- Output formats: INHX8S, INHX8M, INHX32 and relocatable objects.

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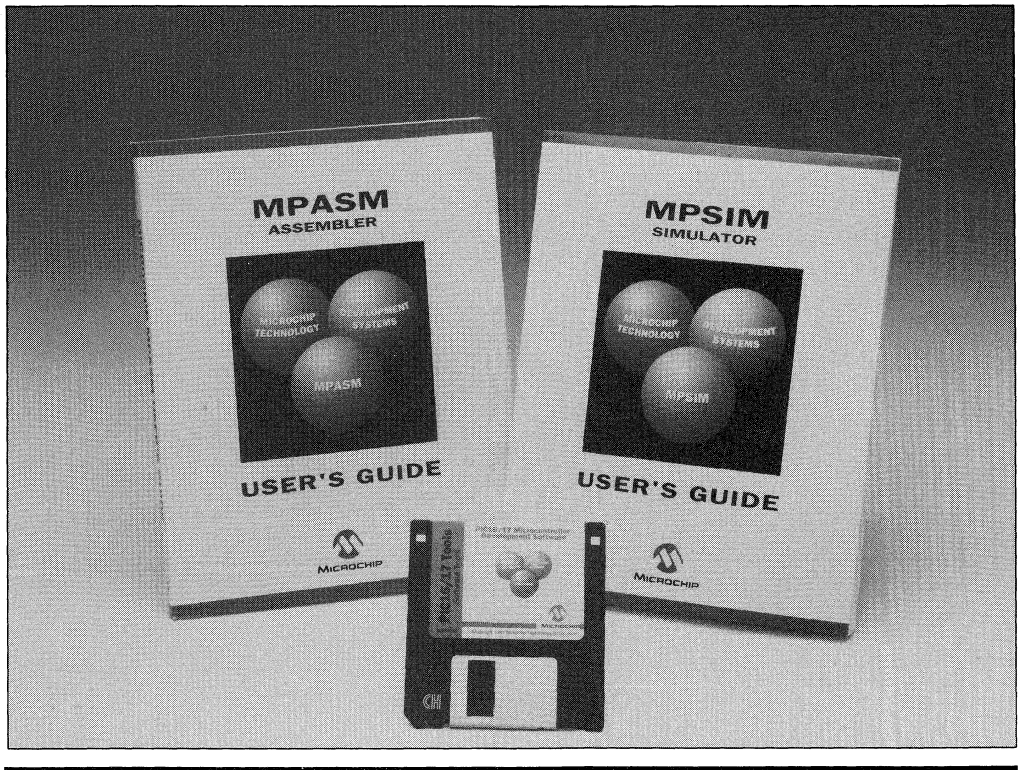

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MPASM DIRECTIVE LANGUAGE

MPASM provides a full featured directive language represented by four basic classes of directives:

- Data Directives are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- Listing Directives control the MPASM listing display. They allow the specification of titles and subtitles, page ejects and other listing control.
- Control Directives permit sections of conditionally assembled code.
- Macro Directives control the execution and data allocation within macro body definitions.

MPASM INSTRUCTION SET

MPASM supports the entire instruction set of the PIC16C5X, PIC16CXX and PIC17CXX microcontrollers, as represented in the following four classes of instructions:

- Data Move Operations
- Arithmetic and Logical Operations
- Bit Manipulation Operations
- Special Control Operations

The Microchip microcontroller set is used to operate on data located in any of the file registers, including the I/O registers. There are:

- Data Transfer Operations
- Logical Operations
- Rotate Operations

MPASM provides bit level file register operations to manipulate and test individual bits in any addressable register, literal and control operations permitting operations on literals and branches to subroutines in program memory.

The Microchip microcontroller instruction sets allow read and write of special function registers such as the PC and status registers.

SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
SW165002	MPSIM/MPASM Simulator and Assembler Software and Documentation

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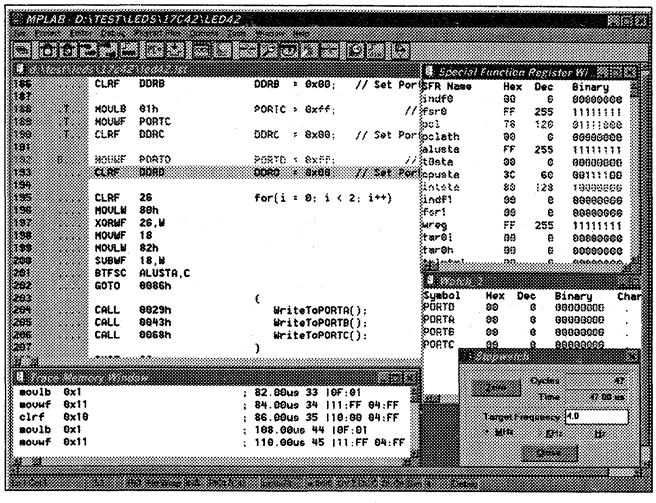
MICROCHIP

MPLAB™SIM

Software Simulator Product Brief



MPLAB-SIM takes advantage of the power of MPLAB to provide an extremely powerful and cost effective debugging solution.

The MPLAB-SIM software simulator allows the user to isolate code problems and debug firmware designs on PIC16/17 devices. It simulates the core functions as well as most of the peripherals of the PIC16/17 microcontroller families. It is particularly suitable for optimizing algorithms where real-time emulation is not required.

MPLAB is a Windows®-based development platform for the Microchip Technology PIC16/17 one-time-programmable (OTP) microcontroller families. MPLAB Integrated Development Environment (IDE) offers a project manager and program text editor, a user-configurable toolbar containing four pre-defined sets and a status bar which communicates editing and debugging information.

The MPLAB desktop provides the development environment and tools for developing and debugging your application as a project, allowing you to quickly move between different development and debugging modes. With the MPLAB environment, you can debug your source code, automatically locate errors in source files for editing, debug with breakpoints based on internal register values, watch the program flow with MPLAB-SIM (software simulator) or PICMASTER, make timing measurements with a "stop watch," view variables in watch windows and find quick answers to questions from the MPLAB on-line help.

Features:

MPLAB-SIM Software Simulator

- Discrete-event simulator integrated into the MPLAB IDE features debug capabilities including unlimited breakpoints, trace, examine/modify registers, watch variables and time-stamp
- Simulates the core functions as well as most peripherals of the PIC16/17 MCUs

MPLAB Project Manager

- Organizes the different files that comprise your application firmware under one "Project"
- Allows you to create a project; add, edit or debug a source code file in a project; and build object files

MPLAB Editor

- Full-featured programmer's editor lets you write and edit firmware source files or other text files for PIC16/17 MCUs
- Creates re-usable source file templates for quick creation of new source files

MPASM Universal Assembler

- Has full-featured macro capabilities, conditional assembly and several source and listing formats
- Generates various object code formats to support Microchip development tools and third-party programmers without exiting MPLAB

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MPLAB-SIM

Ordering Information:

Model Name:

MPLAB

Ordering Part Number:

SW007002

Tools Supported:

MPLAB-SIM Software Simulator

PICMASTER In-Circuit Emulator

PICSTART Plus Low-cost Programmer

Host System Requirements:

PC with 386 or higher processor. Pentium™ recommended

4 MB Memory, 16 MB recommended

8 MB hard disk space, 20 MB recommended

VGA or Super VGA Monitor

Microsoft Windows 3.1 or greater

System Description:

MPLAB-SIM is a discrete event simulator software application designed to imitate operation of the PIC16/17 microcontrollers. It allows the user to debug software that will use any of these microcontrollers.

At any instruction boundary, you may examine and/or modify any data area within the processor, or provide external stimulus to any of the pins. MPLAB-SIM gives you a solid, low cost, source-level debug tool to help you through the early design verification stages of your project.

MPLAB-SIM runs under MPLAB. This allows you to write, debug, and optimize the PIC16/17 microcontroller applications for firmware product designs.

MPLAB IDE software package includes the following:

- MPLAB Project Manager
- MPLAB Editor
- MPASM Universal Macro Assembler for the PIC16/17 MCUs and other language products supporting the Common Object Description file format

To order or obtain more information about MPLAB-SIM, contact the Microchip sales office nearest you. MPLAB-SIM software may also be downloaded from Microchip's Bulletin Board System. User's can connect to the BBS through the CompuServe® communications network.

Customer Support:

Microchip maintains a worldwide network of distributors, representatives, local sales offices, Field Application Engineers and Corporate Application Engineers as well as a multifaceted Bulletin Board System. Microchip's Internet home page can be reached at: http://www.microchip.com

"The Microchip Advantage"	
MPLAB™	Integrated Development Environment (IDE)
MPASM	Universal PIC16/17 macro-assembler
MPLAB-SIM	Software Simulator
MPLAB-C	C compiler for PIC16/17 microcontrollers
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ICEPIC	Low-cost modular in-circuit emulator
PRO MATE™ II	Full-featured, modular device programmer
PICSTART® Plus	Entry-level development kit with programmer
PICSTART® Lite	Low-cost entry level development kit
fuzzyTECH®-MP	Fuzzy Logic development software
MP-DriveWay™	Application Code Generator
KEELOQ®	Code Hopping Devices

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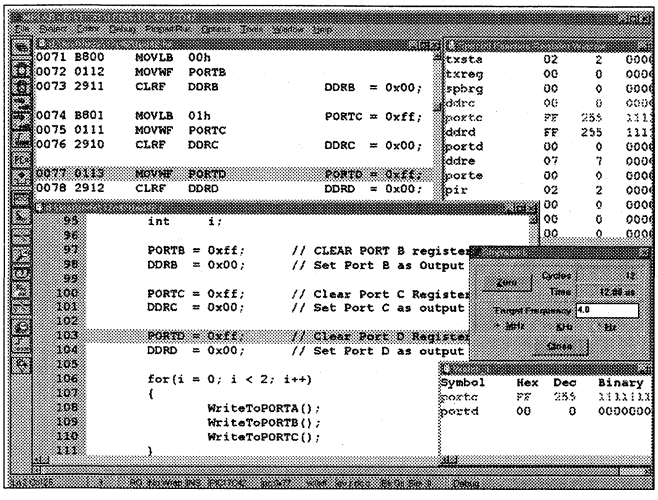
MICROCHIP

MPLAB™C

Universal C Compiler for PIC16/17 MCUs Product Brief



Features:

- MPLAB-compatible for source level debugging in an easy-to-use project environment
- Provides Object, Listing, Symbol and special files for debugging with MPLAB
- Supports interrupt routines
- Compares source code to target hardware definitions
- Header file register definitions compatible with MPASM Assembler
- Generates tight, efficient code
- Output formats: INHX8S, INHX8M and INHX32
- Has ability to embed assembly

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MPLAB-C provides powerful integration capabilities and ease of use not found with other compilers.

The **MPLAB-C** Universal C Compiler is a complete high-level language compiler for the Microchip Technology PIC16/17 families of 8-bit one-time-programmable (OTP) microcontrollers. Since MPLAB-C is compatible with Microchip's MPLAB Integrated Development Environment (IDE), it functions with the PICMASTER® in-circuit emulator and the MPLAB-SIM simulator. When using MPLAB-C with MPLAB, you get full source level debugging in an easy-to-use project environment which helps you reduce development time.

The MPLAB-C C compiler generates executable code directly from the compile process. There is no need for an extra step to assemble code generated by the compiler.

MPLAB-C allows you to write code for PIC16/17 microcontroller applications in a high level language. The detailed operation of the target processor is mostly hidden which means less time is devoted to considering the details of the processors's architecture. This feature also permits easy code portability between different PIC16/17 devices – often as simple as changing one line of source code.

MPLAB-C will run on any IBM PC/AT® or compatible computer running DOS 5.0 or later, and it supports the 12-bit, 14-bit and 16-bit Microchip microcontroller cores. MPLAB-C is a rule based compiler with expert systems tailored to each of these platforms for optimal efficiency.

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Ordering Information:

Model Name:

MPLAB-C

Ordering Part Number:

SW006005

Devices Supported:

All PIC16/17 microcontrollers

Model Name:

MPLAB-C with MP-DriveWay™

Ordering Part Number:

SW006008

Devices Supported:

MPLAB-C supports all PIC16/17 microcontrollers.

MP-DriveWay supports: PIC16C54, PIC16C54A, PIC16C55, PIC16C56, PIC16C57, PIC16C58A, PIC16CR54, PIC16CR57A, PIC16CR58A, PIC16C64, PIC16C71, PIC16C74, PIC16C84, PIC17C42, PIC17C42A, PIC17C43, PIC17C44

System Requirements:

IBM PC/AT® or compatible computer

DOS 5.0 or later operating system

System Description:

The MPLAB-C Universal C Compiler comes complete with the MPLAB IDE. The IDE allows you to quickly move between different development and debugging modes, for example, you can quickly advance from software debugging with MPLAB-SIM to hardware debugging with PICMASTER.

MPLAB-C has implemented extensions to the C language to provide specific support for microcontroller environments, including:

- I/O Ports (read only, write only and read/write)
- Read only access to the processor status register
- Read/write access to the processor index register
- Read/write access to the processor working (W) register
- Interrupt vectors
- Fix variables and functions in memory

To order or obtain more information about MPLAB-C or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

Microchip maintains a worldwide network of distributors, representatives, local sales offices, Field Application Engineers and Corporate Application Engineers as well as a multifaceted Bulletin Board System. Microchip's Internet home page can be reached at: http://www.microchip.com

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PRO MATE™ II	Full-featured, modular device programmer
PICSTART® Plus	Entry-level development kit with programmer
PICSTART® Lite	Low-cost entry level development kit
fuzzyTECH®-MP	Fuzzy Logic development software
MP-DriveWay™	Application Code Generator
KEELOQ®	Code Hopping Devices

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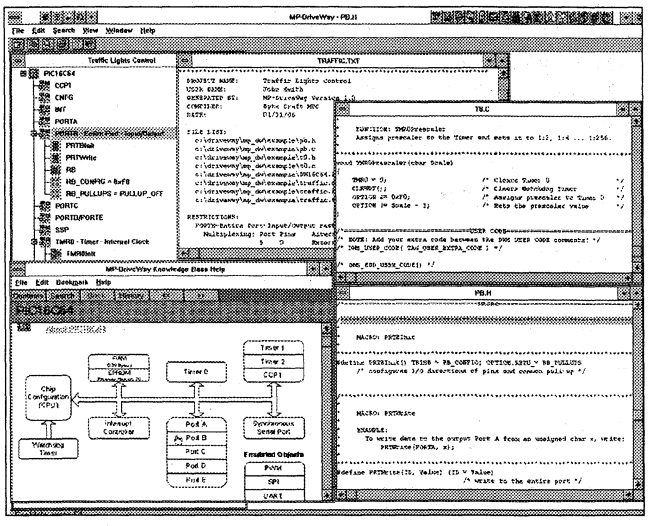
MP-DRIVEWAY™

Application Code Generator Product Brief



MP-DriveWay generates 'C' code for PIC16/17 microcontrollers.

MP-DriveWay is an easy to use Windows®-based Application Code Generator for Microchip Technology's 8-bit, one-time-programmable (OTP) PIC16/17 microcontrollers. With MP-DriveWay you can visually configure all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language.

The output of MP-DriveWay is fully compatible with Microchip's MPLAB-C compiler. The code produced is highly modular and allows easy integration of your own code. In fact, MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

MP-DriveWay derives code output from an extensive knowledge base. For each peripheral, the knowledge base contains an array of driver routines. For example, the USART module can be configured to be full duplex or half duplex, 8- or 9-bit, interrupt driven or polled and so on. MP-DriveWay, further allows you to specify desired operating parameters, such as baud rate. This information is used to generate all the appropriate control register values which are then plugged into the initialization code.

MP-DriveWay also generates "emulated" or "virtual" peripherals. Peripheral functions such as USART or PWM that may not exist on a selected PIC16/17 microcontroller are implemented entirely in software.

Features:

- Application Code Generator for PIC16/17 microcontrollers
- Windows-based intuitive user interface
- Describe peripheral operation at a high level
- Generates initialization and functional code
- Generates C code, compatible with Microchip's MPLAB-C
- Built in knowledge base for all peripherals
- Code generated is fully tested and documented reducing your debug time
- Specify operating parameters (such as baud rate)
- Emulated Peripherals
- IDS: Interactive Data Sheet, is an innovative on-line help
- Reduce your learning curve on a new device
- Use DriveWay to prototype quickly

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MP-DriveWay

Ordering Information:

Model Name:

MP-DriveWay

Ordering Part Number:

SW006006

Devices Supported:

PIC16C54, PIC16C54A,

PIC16C55, PIC16C56,

PIC16C57, PIC16C58A,

PIC16CR54, PIC16CR57A, PIC16CR58A

PIC16C64

PIC16C71, PIC16C74

PIC16C84

PIC17C42A, PIC17C43, PIC17C44

Model Name:

MP-DriveWay with MPLAB-C

Ordering Part Number:

SW006008

Devices Supported:

See device listing above for

MP-DriveWay support.

MPLAB-C supports all PIC16/17 microcontrollers.

Host System Requirements:

386 based PC or greater

Microsoft Windows 3.1 or higher

4 MB RAM, 5 MB free disk space

3.5 inch diskette drive

MP-DriveWay has an extensive and unique on-line interactive help called Integrated Data Sheet (IDS). It is geared towards engineers developing code. With IDS you can find all the information you need for any peripheral all in one place.

MP-DriveWay generates fully tested and documented code, reducing your debug time. Use of pre-developed code segments from the knowledge base results in highly efficient code output.

MP-DriveWay enhances your productivity. As a new user, you can reduce your learning curve. As an expert user, it allows you to prototype applications faster.

MP-DriveWay is a result of partnership effort between by AISYS Intelligent Systems Ltd. of Israel and Microchip.

To order or obtain more information about MP-DriveWay or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

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PICSTART® Plus	Entry-level development kit with programmer
PICSTART® Lite	Low-cost entry level development kit
fuzzyTECH®-MP	Fuzzy Logic development software
MP-DriveWay™	Application Code Generator
KEELOQ®	Code Hopping Devices

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MICROCHIP

*fuzzy*TECH®MP

Fuzzy Logic Development System for PIC16/17

*fuzzy*TECH-MP FOR MICROCHIP PIC16/17

This product brief describes the technical aspects of the *fuzzy*TECH-MP Fuzzy Logic Development System for PIC16/17 microcontrollers developed by INFORM Software Corporation specifically for Microchip.

The *fuzzy*TECH-MP Development System comes in two versions. The first, the Explorer, contains everything you need to gain a comprehensive working knowledge about fuzzy-logic system design. It is easy-to-use, all graphic editors and tools guide you step-by-step through the development phases of fuzzy systems. The Explorer supports two input variables and one output variable.

The full-featured *fuzzy*TECH-MP Edition offers all of the capabilities of the Explorer, plus it has the additional flexibility of eight input variables and four output variables for designing more complex systems. The full features are enabled with a hardware key lock attached to the parallel port of the PC.

Included in both versions is *fuzzy*LAB™, a fully functional demonstration board, to give customers hand-on experience with fuzzy logic systems implementation. *fuzzy*LAB is a simple heating thermostat consisting of a PWM-controlled resistor configured to heat a thermistor to a preset temperature. Using the two fuzzy algorithms provided, a designer can set a target temperature and observe the thermostat response to the set point.

Both systems generate assembly code compatible with the MPASM, Microchip's Universal Assembler, that can be integrated into your application. Examining this code provides you with further insights into the fabrics of fuzzy logic systems.

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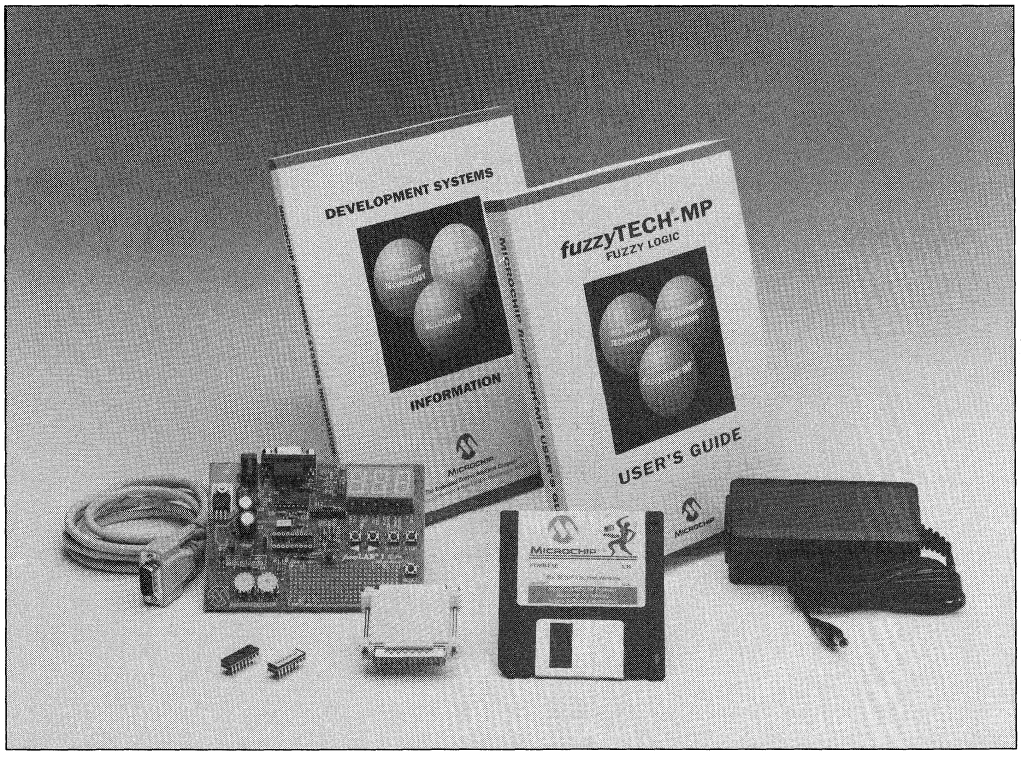

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*fuzzy*TECH-MP System Requirements

*fuzzy*TECH-MP will run on any IBM PC® (386 or higher) or compatible computer, running DOS 4.1 or later, and Microsof®t Windows® 3.0 or later. Because *fuzzy*TECH-MP makes extensive use of graphics, a color graphic monitor (VGA) is required, and higher resolutions of 800 x 600 or 1024 x 768 are recommended.

What is Fuzzy Logic?

Fuzzy logic is a technology that enhances mode-based system designs using both intuition and engineering heuristics. Fuzzy logic uses elements of everyday language to represent desired system behavior, thus circumventing the need for rigorous mathematical modeling.

It is an efficient way of designing, optimizing and maintaining highly complex systems transparently.

Fuzzy Logic Applications

Fuzzy logic finds its home in unique applications:

- When no adequate mathematical model for a given problem is readily apparent.
- When non-linearities, time constraints or multiple parameters exist.
- When engineering know-how about the given problem is available or can be acquired during the design process.

The *fuzzy*TECH-MP Implementation

*fuzzy*TECH-MP provides the following standard features:

- Windows Compatible with full graphical user interface
- 8-Input variables (2 for the Explorer version)
- 4-Output variables (1 for the Explorer version)
- 8-Bit resolution on input and output variables
- 16-Bit computation resolution for the PIC16CXX and PIC17CXX microcontrollers
- No theoretical limit on rules, antecedents and linguistic conjunctions (chip limitations will place a practical limit on these)
- MAX-MIN and MAX-DOT inference methods
- CoM and MoM defuzzification methods
- MPASM Compatible
- PICMASTER™ Compatible

*fuzzy*TECH-MP

*fuzzy*TECH-MP is available directly from Microchip Technology and its authorized distributors. Contact your local sales office for more information.

SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DV005001	*fuzzy*TECH-MP EXPLORER
DV005002	*fuzzy*TECH-MP EDITION

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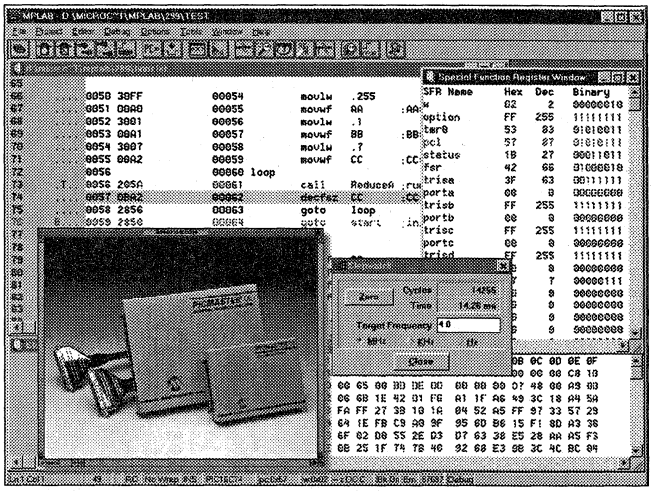
PICMASTER®CE

CE Compliant In-Circuit Emulator Product Brief



CE compliant PICMASTER offers design engineers maximum power, flexibility and rapid design turn-around!

The PICMASTER-CE in-circuit emulator systems from Microchip Technology provide a high-quality, universal platform for emulating the entire line of Microchip 8-bit, one-time-programmable (OTP) microcontrollers. PICMASTER-CE is identical in user functionality with the popular PICMASTER emulators, but features additional enhancements.

PICMASTER-CE is a high-performance, real-time in-circuit emulator. Included in the complete system are the emulator, MPLAB™ integrated development environment, MPASM full-featured macro assembler, and MPLAB-SIM, an unusually sophisticated simulator program. Systems may be purchased that also include a device programmer (see ordering information on reverse side). Sample programs are provided to help quickly familiarize the user with the development system and the PIC16/17 8-bit OTP microcontroller families. The MPLAB IDE user interface features a built-in text editor, project management, and full integration with MPASM and high level languages that support the Common Object Description format (i.e. MPLAB-C and MPC).

PICMASTER-CE meets or exceeds the stringent Electromagnetic Compatibility requirements known as CE compliance directives established by the European Union (EU) countries. These include limiting radiated emission, improving susceptibility to radiated emission and improving susceptibility to Electrostatic Discharge (ESD).

Features:

- High-performance PC-based development system for PIC16/17 microcontrollers
- Real-time in-circuit emulation
- Program memory emulation and memory mapping capability up to 64k words
- Real-time trace
- Unlimited hardware breakpoints
- External break with AND/OR capability with identical breakpoints
- Trigger out
- Multi-processor emulation
- Highly shielded cable to connect pod and prober
- Supported by MPLAB IDE for Windows
- Assembly and C source level debugging
- Includes MPLAB Project Manager
- Includes MPLAB Editor
- Includes MPASM Universal Assembler
- Includes MPLAB-SIM Simulator

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PICMASTER-CE

Ordering Information:

Complete Systems with PRO MATE II programmer:

Ordering Part #:	Devices Supported:
EM147101	PIC14000
EM167101	PIC16C52, 54, 54A, 55, 56, 57, 58A
EM167103	PIC16C62, 63, 64, 65, 72, 73, 74
EM167105	PIC16C71, 710, 711
EM167107	PIC16F83, 84
EM167109	PIC16C620, 621, 622
EM177107	PIC17C42A, 43, 44

Complete Systems without PRO MATE II programmer:

Ordering Part #:	Devices Supported:
EM147102	PIC14000
EM167102	PIC16C52, 54, 54A, 55, 56, 57, 58A,
EM167104	PIC16C62, 63, 64, 65, 72, 73, 74
EM167106	PIC16C71, 710, 711
EM167108	PIC16F83, 84
EM167110	PIC16C620, 621, 622
EM177108	PIC17C42A, 43, 44

Host System Requirements:

- PC-compatible computer: 386DX, 486 or PENTIUM™ based with ISA or EISA bus
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended)
- MS-DOS®/PC-DOS® v. 5.0 or greater
- Microsoft Windows 3.1 or greater in 386 enhanced mode
- 4 MB RAM, 4 MB free disk space
- 3.5 inch diskette drive
- One 8-bit PC/AT (ISA) I/O expansion slot (half size)

System Description:

The PICMASTER-CE emulator systems feature real-time instruction emulation with program memory emulation and memory mapping capability up to 64K words. Instruction execution can be mapped into either emulation memory or user prototype memory. An unlimited number of hardware breakpoints can be set anywhere in the program memory.

The multiprocessor emulation capability allows for up to four PICMASTER-CE emulators to be synchronized on a single PC. PICMASTER-CE is capable of full symbolic debugging with symbolic display and alter of all register files, special purpose registers, stack registers and bank registers.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. PIC16C5X probes operate to 20 MHz, PIC17CXX to 16 MHz and PIC16CXX to 10 MHz. The universal architecture of the PICMASTER-CE allows expansion to support all new microcontroller architectures with data and program memory paths to 16 bits.

To order or obtain more information about PICMASTER-CE or any other Microchip product, contact the Microchip sales office nearest.

Customer Support:

Microchip maintains a worldwide network of distributors, representatives, local sales offices, Field Application Engineers and Corporate Application Engineers as well as a multifaceted Bulletin Board System. Microchip's Internet home page can be reached at: http://www.microchip.com

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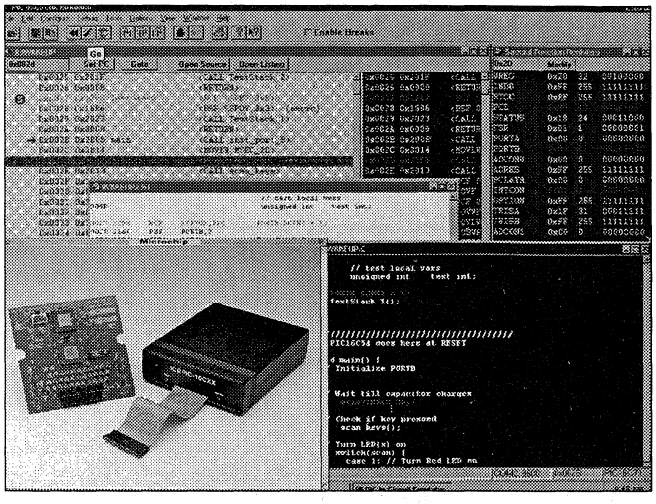
ICEPIC™

Low-Cost PIC16CXXX In-Circuit Emulator Product Brief



ICEPIC: Affordable PIC16CXXX In-Circuit Emulation Solution.

ICEPIC is a low-cost in-circuit emulation solution for the Microchip Technology PIC16C5X and PIC16CXXX families of 8-bit one-time-programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules or daughter boards. The emulator is capable of emulating without target application circuitry being present.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT® systems through the new Pentium™ based machines. The ICEPIC development software runs under Microsoft Windows® 3.X environment, allowing the operator access to a wide range of supporting software accessories.

The ICEPIC development software provides a user-friendly operating environment with an easy-to-use toolbar; unlimited number of breakpoints; single, multiple and procedure step; ability to display and modify any register; user-selectable processor speeds via an oscillator module; full context-sensitive help and an RS-232 serial port.

ICEPIC is fully compatible with Microchip's MPASM Universal Assembler and MPLAB-C Compiler. ICEPIC is CE compliant, meaning it meets or exceeds all the directives for safety, emissions, ESD and susceptibility (to radiated emission) requirements set forth by the European Union (EU) countries.

Features:

- Real time, non-intrusive emulation of PIC16C5X and PIC16CXXX microcontrollers
- 8K words of emulation memory
- Full speed, real time emulation to 20 MHz for PIC16C5X family
- Up to 10 MHz real time emulation for PIC16CXXX family
- Microsoft Windows® compatible
- Source level debug capability in assembly or C
- Symbolic debug capability
- 8K hardware breakpoints
- Custom watch points
- PC communication via serial interface at speeds up to 57K baud
- Display and modify any register (Program or Data)
- User selectable processor speeds (via oscillator module)

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Ordering Information:

Model Name	Ordering Part Number	Devices Supported
Complete Emulator Systems:		
ICEPIC5X	EM167201	16C54/54A, 55, 56, 57, 58A
ICEPIC62X	EM167202	16C620, 621, 622
ICEPIC64	EM167203	16C64, 62
ICEPIC74	EM167204	16C74, 73, 65, 63
ICEPIC71	EM167205	16C71, 61
ICEPIC84	EM167206	16C84
Daughter Boards:		
ICEPICDB5X	AC165201	16C54/54A, 55, 56, 57, 58A
ICEPICDB62X	AC165202	16C620, 621, 622
ICEPICDB64	AC165203	16C64, 62
ICEPICDB74	AC165204	16C74, 73, 65, 63
ICEPICDB71	AC165205	16C71, 61
ICEPICDB84	AC165206	16C84
Base Unit Only Without Daughter Board:		
ICEPIC POD	EM167200	All

System Description:

The low-cost PC-based ICEPIC In-Circuit Emulator system comes with an emulator unit (mother board), power supply, RS-232 cable, probe header cable(s) to connect to the application circuit, and one device-specific personality daughter board.

These interchangeable personality modules or daughter boards are contained with the mother board within one housing, connecting to the target application via a connector cable that extends from the housing. The mother board incorporates the common emulation logic while the daughter board is for device-specific emulator logic. This economical system allows the user to purchase a new daughter board for a new processor group as needed, at approximately 30% of the full system cost.

ICEPIC was designed by NEOSOFT Inc. and is manufactured under license by RF Solutions Ltd. To order or obtain more information about ICEPIC or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

Microchip maintains a worldwide network of distributors, representatives, local sales offices, Field Application Engineers and Corporate Application Engineers as well as a multifaceted Bulletin Board System. Microchip's Internet home page can be reached at: http://www.microchip.com

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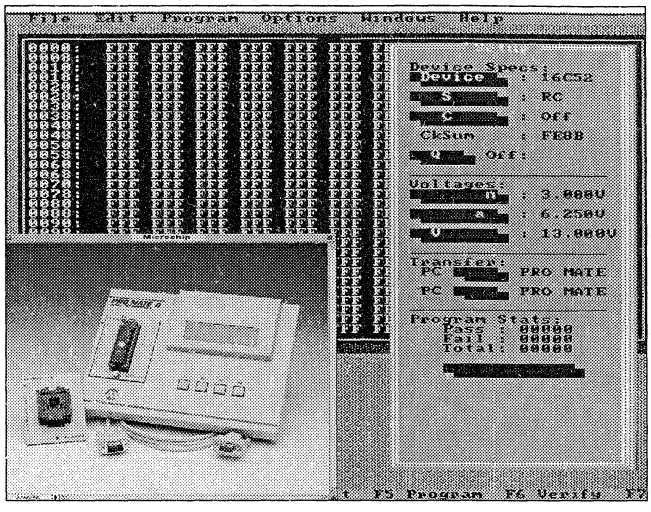
PRO MATE®II

Universal Device Programmer Product Brief



CE Compliant PRO MATE II makes programming easy.

The PRO MATE II device programmer tool allows development engineers to program user software into Microchip Technology's entire line of PIC16/17 8-bit one-time-programmable (OTP) microcontrollers. PRO MATE II is CE compliant, meaning it meets or exceeds all the directives for safety, emissions, ESD and susceptibility (to radiated emission) requirements set forth by the European Union (EU) countries.

The PRO MATE II device programmer is designed to be robust and reliable with: enhanced socket module alignment with four auto alignment pins; three levels of over-current protection and superior electrostatic discharge immunity for rugged environments; a small and compact univeral IEC power supply and improved LCD display and buttons.

The PRO MATE II device programmer is easy to use and operates either as a stand-alone unit or in conjunction with a PC-compatible host system. This time-saving tool comes complete with all the accessories needed to connect to a host system including interface cables and a universal input power supply.

In addition to the programmer unit, the PRO MATE II system contains Microchip's popular discrete event software simulator (MPLAB-SIM), a universal PIC16/17 macro assembler (MPASM), and host operating software which offers file display and editing and transfer to and from the programming unit.

Features:

- Programs EPROM and/or EEPROM program and data memory for all Microchip PIC16/17 microcontrollers
- Operates as stand-alone or with PC-host system
- Three operating modes:
  - Host Mode
  - Safe Mode
  - Stand-Alone Mode
- Complete line of interchangeable socket modules supports all package options (sold separately)
- Universal platform can quickly and easily support future Microchip products
- SQTP^{SM} serialization adds a unique serial number to each device programmed (in PC host mode)
- Safe Mode prevents accidental corruption of master code
- Saves and restores "environment" including all device settings, object file and more
- Indexed on-line help
- Complete documentation including all User's Guides

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PRO MATE II

Ordering Information:

Model Name:

PRO MATE II

Ordering Part Number:

DV007003

Devices Supported:

PIC14000

PIC16C52, PIC16C54, PIC16C54A, PIC16C54B, PIC16C55, PIC16C56, PIC16C57, PIC16C58A

PIC16C61, PIC16C62, PIC16C620, PIC16C621, PIC16C622, PIC16C62A, PIC16C63, PIC16C64, PIC16C64A, PIC16C65, PIC16C65A

PIC16C71, PIC16C710, PIC16C711, PIC16C72, PIC16C73, PIC16C74, PIC16C74A

PIC16F83, PIC16C84, PIC16F84

PIC17C42A, PIC17C43, PIC17C44

Socket Modules are sold separately. For a complete list, please contact Microchip or refer to the Development Systems Ordering Guide (DS30177).

System Description:

Microchip's PRO MATE II makes it easy to program the company's entire line of 8-bit OTP RISC microcontrollers, operating either as a stand-alone unit or in conjunction with a PC-compatible host system. When connected to a host system, PRO MATE II provides an exceptionally user-friendly interface to give the developer complete control over the programming session.

The new PRO MATE II software provides many user interface features. These include a "safe mode" targeting production environments where accidental corruption of master code is prevented; the ability to save and restore "environment," including all device settings, object file and more; and complete indexed on-line help. The PRO MATE II system also contains Microchip's popular discrete event software simulator (MPLAB-SIM) and a universal PIC16/17 macro assembler (MPASM).

To order or obtain more information about PRO MATE II or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

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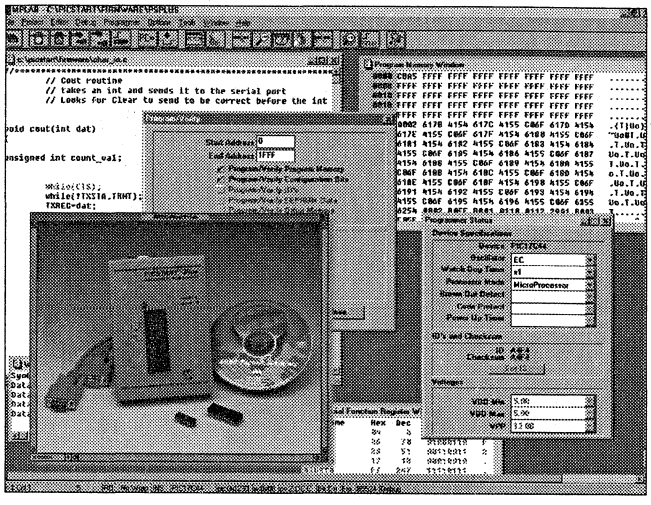
PICSTART®PLUS

Low Cost Development Kit Product Brief



PICSTART Plus makes designing with Microchip MCUs simple and affordable.

The **PICSTART Plus** development system from Microchip Technology provides the product development engineer with a highly-flexible low-cost microcontroller design tool set for all PIC14000, PIC16C5X, PIC16CXX and PIC17CXX 8-bit one-time-programmable (OTP) devices (DIP packages up to 40 pins).

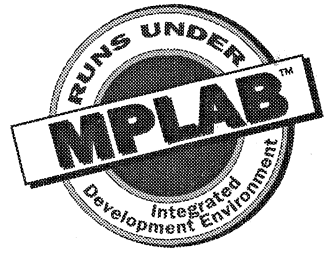
The PICSTART Plus development system operates on any PC-compatible machine running under the Windows® 3.1 operating system. PICSTART Plus is easy-to-use and features Microchip's highly acclaimed MPLAB™ Integrated Development Environment, with its built-in editor, assembler and Windows-based MPLAB-SIM simulator. The PICSTART Plus development system includes full documentation, software, development programmer and a device sample.

The CE compliant PICSTART Plus development programmer features a molded plastic enclosure and special circuit design techniques to enhance ESD protection. PICSTART Plus is a development programmer and is not recommended for use in a production environment.

Sample software programs are provided to help the developer quickly become familiar with the PICSTART Plus development system and with Microchip's microcontroller families. The PICSTART Plus system also includes Microchip's new CD-ROM containing a complete databook and Embedded Control Handbook (Application notes).

Features:

- Operates with PC-compatible host system running Windows under MPLAB™ environment
- Reads, programs, verifies EPROM and EEPROM program and data memory
- Reads, programs, verifies all configuration bits
- Programs and verifies an address range
- Displays, edits, and transfers device contents to and from programmer unit
- MPLAB Project support to automatically download object file to PICSTART Plus
- MPASM Assembler translates assembler source code to object code for all PIC16/17 devices
- MPLAB-SIM Windows-based simulator designed to model operation of all PIC16/17 microcontrollers
- Complete with RS-232 cable, 9 volt universal IEC power supply and power cable
- PIC16/17 MCU device sample
- Complete documentation, User's Guides and CD-ROM



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PICSTART Plus

Ordering Information:

Model Name:

PICSTART Plus

Ordering Part Number:

DV003001

Devices Supported:

PIC14000

PIC16C52, PIC16C54, PIC16C54A, PIC16C54B, PIC16C55, PIC16C56, PIC16C57, PIC16C58A

PIC16C61, PIC16C62, PIC16C620, PIC16C621, PIC16C622, PIC16C62A, PIC16C63, PIC16C64, PIC16C64A, PIC16C65, PIC16C65A

PIC16C71, PIC16C710, PIC16C711, PIC16C72, PIC16C73, PIC16C74, PIC16C74A

PIC16F83, PIC16C84, PIC16F84

PIC17C42A, PIC17C43, PIC17C44

System Description:

The PICSTART Plus development system includes the PICSTART Plus development programmer and the MPLAB IDE.

The PICSTART Plus programmer gives the product developer the ability to program user software into any of the supported microcontrollers. The PICSTART Plus software running under MPLAB provides for full interactive control over the programmer.

The MPASM macro assembler provides programmable memory data files, listing files and special files required for symbolic debug. The MPLAB-SIM software simulator allows the user to isolate code problems and debug firmware designs on PIC16/17 devices. It simulates the core functions as well as most of the peripherals of the PIC16/17 microcontroller families. It is particularly suitable for optimizing algorithms where real-time emulation is not required.

To order or obtain more information about PICSTART Plus or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

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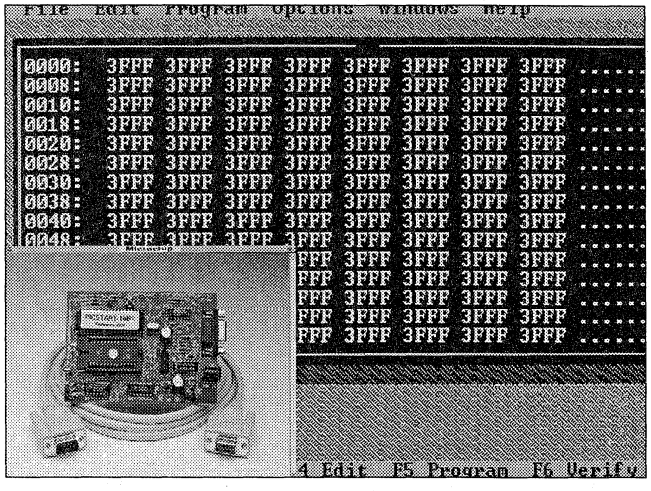
PICSTART®LITE

Ultra Low Cost Development Kit Product Brief



PICSTART Lite makes designing with PIC16CXXX MCUs simple and affordable.

The PICSTART Lite development systems from Microchip Technology provide the product development engineer with a fast, easy and very low-cost way to begin evaluation and code development for base-line PIC16C5X and mid-range PIC16CXXX 8-bit one-time-programmable (OTP) microcontroller products where full real-time emulation is not required. PICSTART Lite is available in two versions, the PICSTART Lite-16B1 (28-pin DIP socket) and the PICSTART Lite-16C (40-pin DIP socket).

The PICSTART Lite development systems operate on any PC-compatible machine running the DOS operating system. Each development system includes an MS-DOS®-based software simulator (MPSIM), a macro assembler (MPASM), a microcontroller EPROM programmer board and a product sample. All supporting documentation and user's guides are supplied on 3-1/2" disks.

Sample software programs to run on the simulator are provided to help the development engineer quickly become familiar with the PICSTART Lite development system and PIC16C5X and PIC16CXX microcontroller families. A user need only provide his or her own preferred text editor and the system is ready for development of end products using one of Microchip's base-line or mid-range MCUs. PICSTART Lite is designed as a development programmer and is not recommended for use in a production environment.

Features:

- Very low-cost introductory microcontroller design tool set
- DOS-based
- Operates with a PC-compatible host system
- Reads, programs and verifies EPROM Memories of PIC16C5X and PIC16CXXX microcontrollers
- PC Host Software provides file display, editing, and transfer device contents to and from programmer unit
- RS-232 interface cable
- Programmer unit connects to standard PC serial port
- MPASM Assembler for translation of assembler source code to object code for all PIC16/17 devices
- MPSIM, an MS-DOS based discrete-event simulator, is designed to model operation of all PIC16C5X and PIC16CXXX microcontrollers and debug
- PIC16C5X or PIC16CXXX device sample

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PICSTART Lite

Ordering Information:

Model Name:

PICSTART Lite-16B1

Ordering Part Number:

DV162003

Devices Supported:

PIC16C54, PIC16C54A, PIC16C55, PIC16C56, PIC16C57, PIC16C58A, PIC16C61, PIC16C62X, PIC16C71, PIC16C710, PIC16C711, PIC16C84

Model Name:

PICSTART Lite-16C

Ordering Part Number:

DV162002

Devices Supported:

PIC16C62, PIC16C62A, PIC16C63, PIC16C64, PIC16C64A, PIC16C65, PIC16C65A, PIC16C72, PIC16C73, PIC16C73A, PIC16C74

System Description:

The PICSTART Lite Development Programmer operates from a user supplied 9 volt power supply and connects with the supplied RS-232 (9 pin-D connector) cable to a serial port on the host PC. A full screen, user-friendly software program is provided for full interactive control over the programmer. Parts may be read, programmed, blank checked and verified. Configuration bits and ID locations may be specified.

The MPASM macro assembler provides translation of Assembler source code to object code with INHX8S, INHX8M and INHX32 output formats. The MPSIM discrete event software simulator models operation of PIC16/17 MCUs and allows the user to debug software that will use any of these devices. MPSIM features include program load and save, disassembler, symbolic debug, execution trace and breakpoints.

To order or obtain more information about PICSTART Lite or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

Microchip maintains a worldwide network of distributors, representatives, local sales offices, Field Application Engineers and Corporate Application Engineers as well as a multifaceted Bulletin Board System. Microchip's Internet home page can be reached at: http://www.microchip.com

"The Microchip Advantage"	
MPLAB™	Integrated Development Environment (IDE)
MPASM	Universal PIC16/17 macro-assembler
MPLAB-SIM	Software Simulator
MPLAB-C	C compiler for PIC16/17 microcontrollers
PICMASTER®	Full-featured modular in-circuit emulator
ICEPIC	Low-cost modular in-circuit emulator
PRO MATE® II	Full-featured, modular device programmer
PICSTART® Plus	Entry-level development kit with programmer
PICSTART® Lite	Low-cost entry level development kit
fuzzyTECH®-MP	Fuzzy Logic development software
MP-DriveWay™	Application Code Generator
KEELOQ®	Code Hopping Devices

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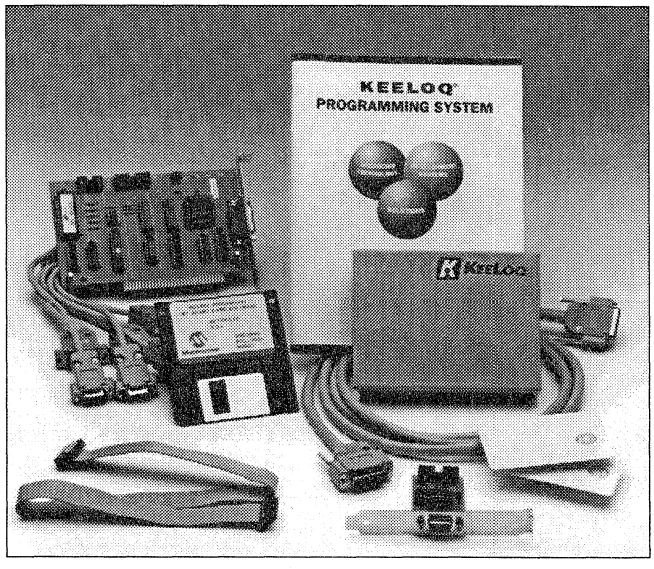
KEELOQ® Programming System

KEELOQ HCSXXX Device Programmers



Programs KEELOQ Encoders and Decoders in manufacturing environment

The **KEELOQ® Programmer** provides manufacturing with the capability to program large quantities of HCS200, HCS300, HCS301, HCS360, HCS361 encoders and HCS509 and HCS512 decoders. The Code Hopping Encoder devices are used in the transmitter portion and the decoder devices in the receiver portion of secure RKE systems. The devices use the KEELOQ code hopping algorithm which combines high security, a small package outline and a very low cost to make this an ideal solution for unidirectional RKE systems.

Primary applications for the KEELOQ devices include automobile keyless entry and security systems, garage door openers, home security systems, central locking systems, gate openers, transaction cards, pre-paid telephone cards, vehicle immobilizers, identity tokens, electronic tagging, passive (batteryless) transponders, point-of-sale readers/adaptors and a growing list of other applications.

The KEELOQ Programmer is supplied with software to automate the programming of HCSXXX devices in the customer's factory production environment, and comes complete with accessories to be used with a host PC computer system. The KEELOQ Programmer includes an interface PCB, Smartcard reader, Smartcards and set of probes.

The versatility and security of the hardware-based key generation allow product range protection.

Features:

- Set up HCSXXX encoder/decoder programming options
- Multiple algorithms for key generation
- Smartcard protection of manufacturer's keys
- Automatic serialization of encoders
- Logging to disk for factory record keeping
- Interface to automated test equipment
- Menu-driven user-friendly software includes:
  - Smartcard initialization program
  - Setup program to configure the various encoder/decoder programming options
  - Transmitter programming software
  - Receiver programming software
- Comprehensive User's Guide with easy-to-follow, step-by-step *Getting Started*

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KEELOQ Programming System

Ordering Information:

Model Name:

KEELOQ Programmer

Ordering Part Number:

PG306001

Devices Supported:

HCS200	Encoder
HCS300	Encoder
HCS301	Encoder
HCS360	Encoder
HCS361	Encoder
HCS509	Decoder
HCS512	Decoder

Host System Requirements:

- PC-compatible computer: 386DX, 486 or PENTIUM™ based with ISA or EISA bus
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended)
- MS-DOS®/PC-DOS® v. 5.0 or greater
- Microsoft Windows 3.1 or greater in 386 enhanced mode
- 4 MB RAM, 4 MB free disk space
- 3.5 inch diskette drive
- One 8-bit PC/AT (ISA) I/O expansion slot (half size)

System Description:

The KEELOQ Programming System Hardware consists of a Key generation card used to securely generate encryption and decryption keys. The card may be plugged into a standard ISA bus slot on a PC. Also included is a Smartcard used to securely store the Manufacturer's Key, which is further protected by a PIN. A Smartcard reader and a set of spring-probes for connection to the transmitter PCB to be programmed complete the programming station hardware.

The accompanying user-friendly menu-driven Software, is supplied on 3.5" diskette and includes all the necessary software for programming large quantities of HCSXXX code hopping devices.

To order or obtain more information about KEELOQ or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

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MPASM	Universal PIC16/17 macro-assembler
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PICMASTER®	Full-featured modular in-circuit emulator
ICEPIC	Low-cost modular in-circuit emulator
PRO MATE® II	Full-featured, modular device programmer
PICSTART® Plus	Entry-level development kit with programmer
PICSTART® Lite	Low-cost entry level development kit
fuzzyTECH®-MP	Fuzzy Logic development software
MP-DriveWay™	Application Code Generator
KEELOQ®	Code Hopping Device Tools

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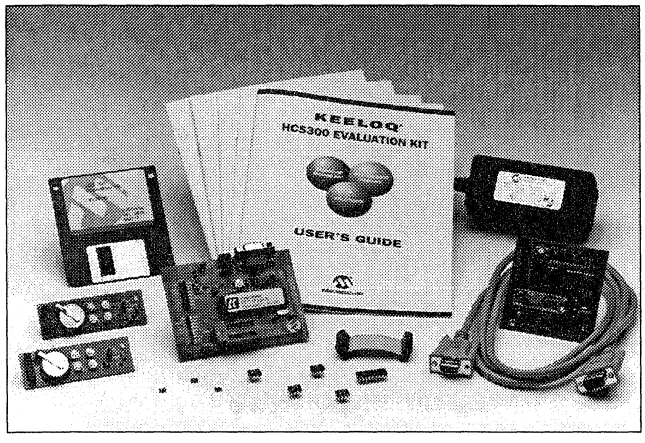
MICROCHIP

KEELOQ® Evaluation Kit

KEELOQ HCSXXX Evaluation Kit Product Brief



Features:

- Transmit hopping code messages using HCSXXX encoders
- Display the fixed and changing parts of hopping code messages on a PC
- Receive and decode hopping code transmissions using a PIC16C56 decoder and 93C46 EEPROM
- Learn new HCSXXX encoders onto the PIC16C56/93C46 decoder
- Program HCSXXX encoders
- Comprehensive User's Guide
- Schematics for transmitter and receiver

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Let's you evaluate the capabilities of Microchip's code hopping devices

The KEELOQ Evaluation Kit demonstrates the capabilities of Microchip Technology's code hopping technology. The Code Hopping Encoder devices are designed to be the transmitter portion and the Decoder devices the receiver portion, of secure RKE* systems. The devices use the KEELOQ code hopping algorithm which combines high security, a small package outline and a very low cost to make this an ideal solution for unidirectional RKE systems.

Primary applications for the KEELOQ HCSXXX devices include automobile keyless entry and security systems, garage door openers, home security systems, central locking systems, gate openers, transaction cards, pre-paid telephone cards, vehicle immobilizers, identity tokens, electronic tagging, passive (batteryless) transponders, point-of-sale readers/adaptors and a growing list of other applications.

The KEELOQ Demonstration Kit includes all the necessary hardware to evaluate a code hopping system, as well as a basic demonstration software program, which is supplied on a PC-compatible 3.5" diskette.

*Remote Keyless Entry

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KEELOQ Evaluation Kit

Ordering Information:

Model Name:

KEELOQ Evaluation Kit

Ordering Part Number:

DM303001

Devices Supported:

HCS300

HCS301

PIC16C56 Decoder

Host System Requirements:

- PC-compatible computer: 386DX, 486 or PENTIUM™ based with ISA or EISA bus
- Serial Port
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended)
- MS-DOS®/PC-DOS® v. 5.0 or greater
- Microsoft Windows 3.1 or greater in 386 enhanced mode
- 4 MB RAM, 4 MB free disk space
- 3.5 inch diskette drive
- One 8-bit PC/AT (ISA) I/O expansion slot (half size)

System Description:

Hardware

- PIC16C56/93C46 EEPROM-based decoder
- RF Receiver module
- On-board +5V regulator and filtered rectifier for direct input from 9V AC/DC wall adapter
- Multiple radio frequency transmitters using HCS300 hopping code encoders
- RS232 socket and associated hardware for direct connection to RS232 interface
- Six bright LEDs connected to decoder outputs

Also includes all necessary software to program transmitters and to display codes or messages.

To order or obtain more information about KEELOQ or any other Microchip product, contact the Microchip sales office nearest you.

Customer Support:

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PICSTART® Lite	Low-cost entry level development kit
fuzzyTECH®-MP	Fuzzy Logic development software
MP-DriveWay™	Application Code Generator
KEELOQ®	Code Hopping Device Tools

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MICROCHIP

PICDEM-1

Low-Cost PIC16/17 Demonstration Board

PRODUCT INFORMATION

The PICDEM-1 is a simple board which demonstrates the capabilities of several Microchip microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58), PIC16C62X, PIC16C61, PIC16C62X, PIC16C71, PIC16C84, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5" disk. The users can program the samples (one each of PIC17C42, PIC16C71 and PIC16C55) provided with the PICDEM-1, on a PRO MATE™or PICSTART™ programmer and easily debug/test the sample code, or the user can connect the PICDEM-1 with the PICMASTER™ emulator and download the sample code to the emulator and debug/test the code. Additionally, a generous 200-hole prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s).

FEATURES:

Hardware:

- 40-pin, 28-pin and 18-pin Precision sockets for all supported microcontrollers.
- On board +5V regulator and filter rectifier for direct input from 9V AC/DC wall adapter.
- RS-232 socket and associated hardware for direct connection to RS-232 interface.
- 5K pot to simulate analog input for PIC16C71.
- Three push button Key for external stimulus and RESET.
- Eight bright LEDs connect to PORTB, help in displaying 8-bit binary values on PORTB.
- Socket for "canned" crystal Oscillator.
- Unpopulated holes provided for Xtal connection
- Jumper to disconnect on board RC Oscillator.
- 200-hole prototype area for user's hardware.

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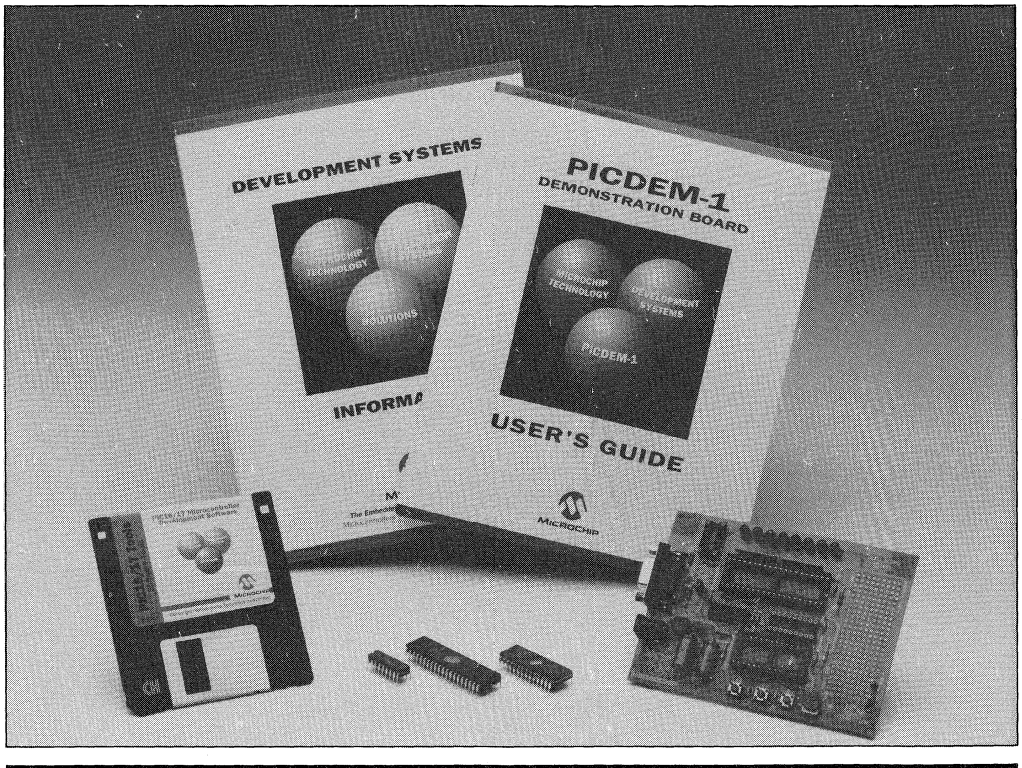

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Software:

- Program for PIC16C71 to demonstrate on-chip A/D features.
- Program for PIC16C84 to demonstrate on-chip EEPROM.
- Program for PIC17C42 to demonstrate on-chip USART.
- Program for PIC16C5X to demonstrate key input capability.
- All demo programs supplied on 3.5" disk,
- Additional programs available on Microchip's BBS.

DOCUMENTATION

- A comprehensive User's Guide with easy to follow step-by-step Getting Started and a Tutorial.
- Schematics for the entire circuit.

SAMPLES

Several UV erasable devices supplied are included. The device types may change from time to time. The supplied devices are typically:

- PIC17C42
- PIC16C71
- PIC16C55

SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DM163001	Low-cost Demonstration Board for PIC16C5X, PIC16C61, PIC16C62X, PIC16C71, PIC16C84, PIC17C42, PIC17C43 and PIC17C44.

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MICROCHIP

PICDEM-2

Low-Cost PIC16CXX Demonstration Board

PRODUCT INFORMATION

The PICDEM-2 is a simple board which demonstrates the capabilities of several Microchip microcontrollers, including PIC16C62, PIC16C63, PIC16C64, PIC16C65, PIC16C73 and the PIC16C74. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5" disk. A programmed sample is included, and the user may erase it and program it with the other sample programs using the PRO MATE™ or PICSTART™ programmer and easily debug and test the sample code. The PICDEM-2 is also usable with the PICMASTER™ emulator, and all of the sample programs can be run and modified using the PICMASTER. Additionally, a generous prototype area is available for user hardware.

FEATURES:

Hardware:

- 40- and 28-pin DIP sockets
- On board +5V regulator for direct input from 9V AC/DC wall adapter or 9V battery.
- RS-232C socket and associated hardware for direct connection to RS-232C interface.
- 5K pot for analog inputs for the PIC16C73/74
- Three push button keys for external stimulus and RESET.
- Eight bright LEDs connected to PORTB for displaying 8-bit binary values.
- Socket for "canned" crystal oscillator.
- Unpopulated holes provided for crystal connection
- 128 x 8 Serial EEPROM.
- LCD module header.
- Keyboard header.
- Unpopulated holes for ACCESS.bus™ connector.

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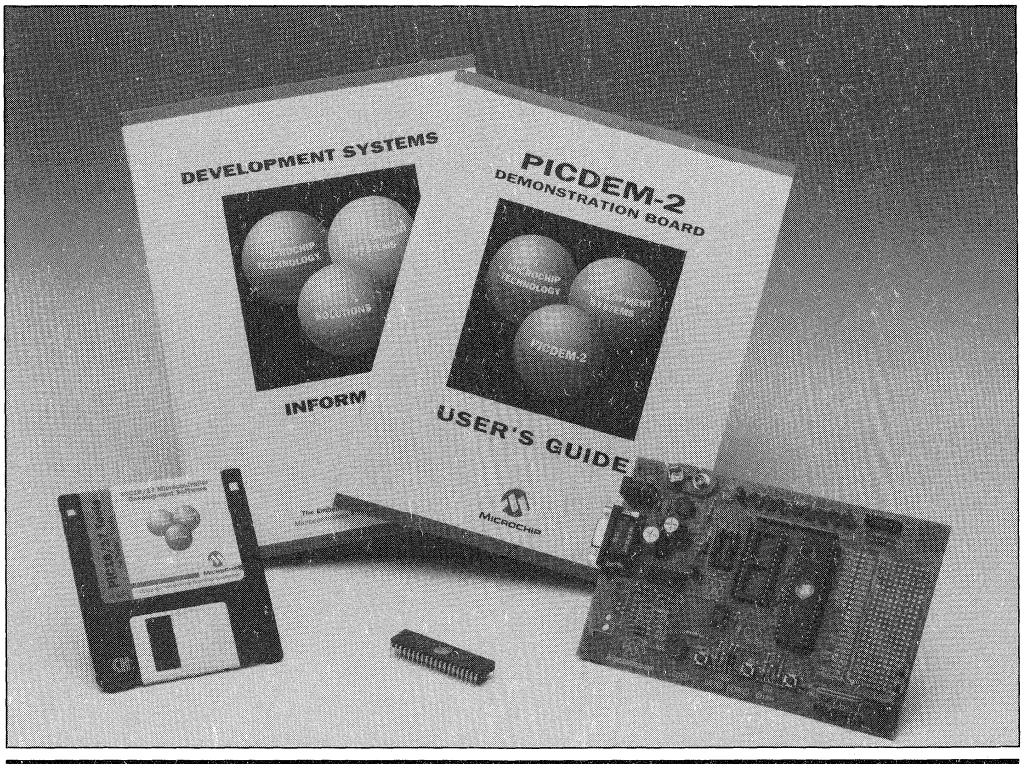

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Hardware (continued):

- Jacks for connection of 9V battery.
- Jumper to disconnect on-board RC oscillator.
- Prototype area for user hardware.

Software:

- Program for PIC16C74 to demonstrate on-chip A/D feature.
- Program for PIC16C64 to demonstrate I^2C™ Serial EEPROM usage.
- All demo programs supplied on 3.5" disk.
- Additional programs available on Microchip's BBS.

DOCUMENTATION:

- A comprehensive User's Guide with easy to follow, step-by-step Getting Started and Tutorial.
- Full schematics.

Samples:

Several UV erasable devices supplied are included. The device types may change from time to time. The supplied devices are typically:

- PIC16C64
- PIC16C74

SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DM163002	Low-cost Demonstration Board for PIC16C64, PIC16C65, PIC16C73 AND PIC17C74

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MICROCHIP

PICDEM-3

Low-Cost PIC16C9XX Demonstration Board

PRODUCT INFORMATION

The PICDEM-3 is a simple board which demonstrates the capabilities of Microchip's microcontroller LCD family. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5" disk. A programmed sample is included, and the user may erase it and program it with the other sample programs using the PRO MATE® or PICSTART®Plus programmer. The PICSTART Plus requires a 68- to 40-pin converter socket.

The PICDEM-3 is also usable with the PICMASTER® emulator, and all of the sample programs can be run and modified using the PICMASTER. Additionally, a generous prototype area is available for user hardware.

All software is written in C using the MPLAB-C/demo version.

FEATURES:

Hardware:

- 68-pin PLCC sockets
- Unpopulated 44-pin PLCC socket for future 44-pin versions
- On board +5V regulator for direct input from 9V AC/DC wall adapter or 9V battery
- RS-232C socket and associated hardware for direct connection to RS-232C interface
- 5K pot for analog input to the PIC16C9XX
- Thermistor for use with A/D converter
- Three push button keys for external stimulus and RESET
- LCD Panel with 4 backplanes and 12 segments
- On-board LCD charge pump circuit with "unpopulated" external resistor ladder supported
- Socket for "canned" crystal oscillator
- Unpopulated holes provided for crystal or ceramic resonator connection
- Supports custom LCD Panel connection (up to 4 common, up to 28 segment) with common/segment header
- LCD pixel data converted to a digital result. Requires external hardware with SPI interface
- Serial port to communicate LCD pixel data to PC for display
- Keyboard header
- Jacks for connection of 9V battery
- Jumper to disconnect on-board RC oscillator
- Prototype area for user hardware

Software:

- MPLAB-C demo for PIC16CXX
- Sample programs which demonstrate:
  - real-time clock and display
  - temperature sensor and display
  - volt meter
  - USART using the SPI port
  - PC software to display LCD pixel information
- All demo programs supplied on 3.5" disk.
- Additional programs available on Microchip's BBS.

DOCUMENTATION:

- A comprehensive User's Guide with easy to follow, step-by-step Getting Started and Tutorial.
- Full schematics.

A UV erasable device is supplied. The device type may vary depending upon availability. The supplied devices are either:

- PIC16C924
- PIC16C923

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SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DM163003	Low-cost Demonstration Board for PIC16C923 and PIC16C924

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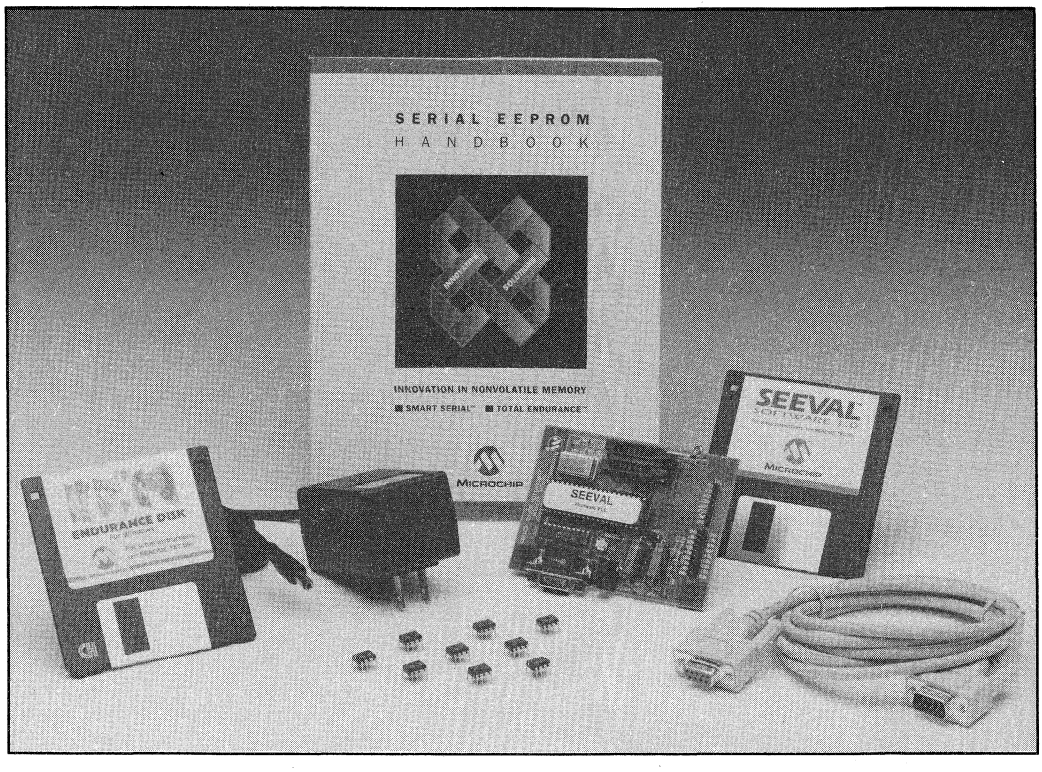
SEEVAL® DESIGNER'S KIT

Microchip Serial EEPROM Designer's Kit



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FEATURES

- Includes everything necessary to begin developing Serial EEPROM-based applications
- Microchip *Total Endurance*™ software model
- Microchip *SEEVAL* evaluation and programming board
- Microchip *SEEVAL* software
- Microchip Serial EEPROM handbook
- Microchip Serial EEPROM sample pack
- RS-232 serial cable
- Power supply

SYSTEM REQUIREMENTS

- DOS 3.1 or higher
- Windows® 3.1
- VGA monitor
- 386 or 486 processor recommended
- Math coprocessor recommended

DEVICE SUPPORT

- Microchip 2-wire 24CXX/24LCXXB/85CXX
- Microchip *Smart Serial*™ 24XX65
- Microchip 3-wire 93CXX/93LCXX series
- Microchip 4-wire 59C11

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Designer's Kit

DESCRIPTION

Now designers of Serial EEPROM-based applications can enjoy the increased productivity, reduced time to market, and the ability to create a rock-solid design that only a well-thought-out development system can provide. Microchip's new Serial EEPROM Designer's Kit includes everything necessary to quickly develop a robust and reliable Serial EEPROM-based design and greatly reduce the time required for system integration and hardware/software debug.

The **Total Endurance software model** enables designers to quickly choose the best Serial EEPROM for the specific application and perform trade-off analysis with voltage, temperature, write cycle and other system parameters in order to achieve the desired Erase/Write endurance (specific ppm rate) or product lifetime. Total Endurance is the new standard of excellence in understanding and predicting the Erase/Write endurance of Serial EEPROMs. An on-line endurance tutorial is included, along with hypertext help files.

Microchip's **SEEVAL Serial EEPROM evaluation and programming system** will accept any Microchip Serial EEPROM in DIP package and enable the designer or system integrator to read, write, or erase any byte or the entire array. SEEVAL also provides the following advanced features to aid in system integration and debug:

- Program special user functions like *Smart Serial* configurations
- Hexadecimal display of array contents
- Pre-set or user-defined repeating patterns
- User-configurable functions like continuous read/write, programmable delay, etc.
- Upload/download files between the Serial EEPROM and disk

Another industry first, the **Microchip Serial EEPROM Handbook** provides a plethora of information crucial to the designers of Serial EEPROM-based systems. Along with data sheets on Microchip Serial EEPROMs, this resource provides application notes regarding Erase/Write endurance, interfacing with different protocols and many, many others. A cross-reference and selector guide are also included, plus article reprints and qualification reports on Microchip Serial EEPROMs.

USING SEEVAL AND TOTAL ENDURANCE

Both software packages can be loaded from Windows by choosing FILE RUN and entering SETUP.EXE from the Program Manager. The applications will install themselves; then a double mouse-click will start either application. The first step in either program is to select a device from the device list.

In Total Endurance, the user has simply to choose a Microchip Serial EEPROM device from the device-list menu and begin entering the application parameters. The entire process can take literally seconds to complete, and the model will output the PPM level and FIT rate of the device vs. the number of Erase/Write cycles. If the user has specified an application lifetime, the model will output PPM and FIT rates at that point in time. Alternately, the user may input a desired PPM level and the model will calculate the application lifetime which will result in that survival rate. The user may then trade-off any of the parameters (device type, voltage, application life, temperature, # of bytes per cycle, # of cycles per day etc.) to arrive at an optimal solution for the intended application.

Whenever a parameter is changed, calculation of the ppm/application life is automatic. An "update" box will appear inside the graph to indicate that new data has been entered and the graph should be redrawn. A single click in the "draw" box will redraw the plot of ppm vs. cycles; a click in the "Resize" box will take the plot to full-screen display for a closer view. The plot data can be saved to a file or the plot itself can be copied to the clipboard to be pasted into another application.

In **SEEVAL**, the user may choose to load a file from disk to program the Serial EEPROM, or read data from the EEPROM and save it to disk. The screen displays the contents of a software buffer. The buffer may be manipulated before programming data to the Serial EEPROM, or data can be written to the Serial EEPROM directly on-line. An area of memory can be highlighted (selected) and programmed with a predefined pattern or user-specified pattern. Alternately, the entire device can be programmed with any repeating pattern.

Both SEEVAL and Total Endurance allow the user to save any configuration as default. This configuration (device and application settings) will then automatically load at boot time.

Order Information:

Description	Part Number
Serial EEPROM Designer's Kit	DV243001

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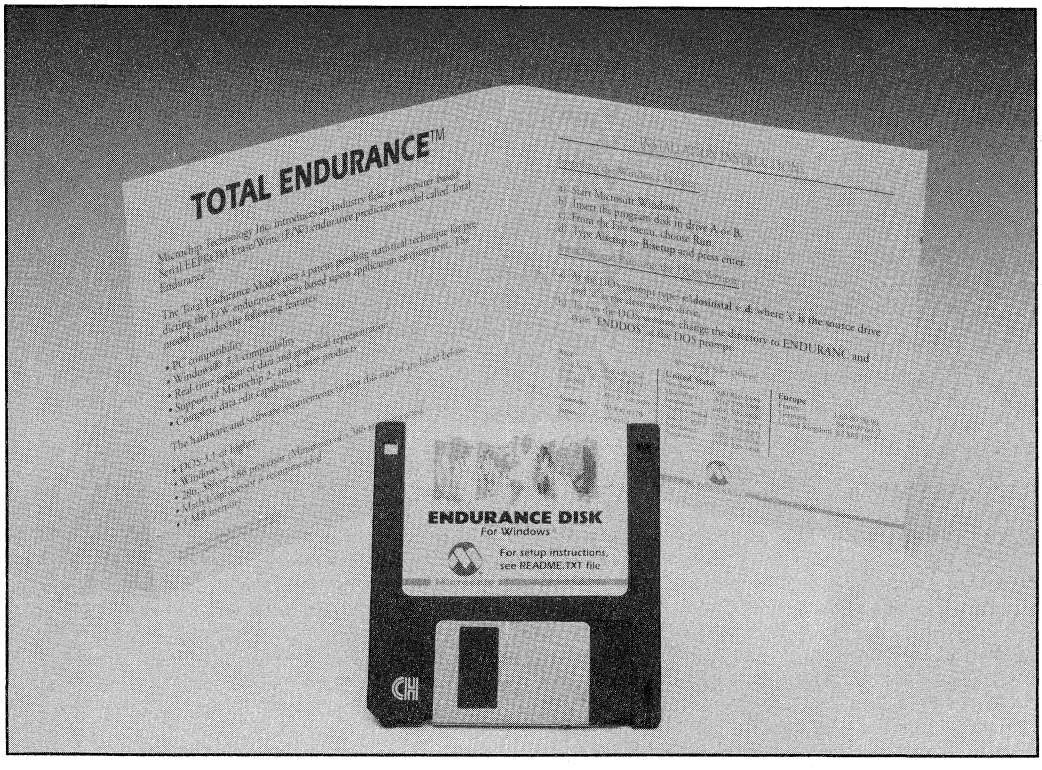
TOTAL ENDURANCE™

Microchip Serial EEPROM Endurance Model



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FEATURES

- IBM® PC compatibility
- Windows® 3.1 or DOS 3.1 compatibility
- Automatic or manual recalculation
- Real-time update of data
- Full-screen or windowed graphical view
- Hypertext on-screen help
- Key or slide-bar entry of parameters
- On-screen editing of parameters
- Single-click copy of plot to clipboard
- Numeric export to delimited text file
- On-disk Endurance Tutorial

SYSTEM REQUIREMENTS

- DOS 3.1 or higher
- Windows 3.1
- 1MB memory
- 386 or 486 processor recommended
- Math coprocessor recommended

DEVICE SUPPORT

- Microchip 2-wire 24CXX/24LCXXB/24AAXX/ 85CXX
- Microchip 3-wire 93CXX/93LCXX/93AAXX Series
- Microchip 4-wire 59C11

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Total Endurance™

DESCRIPTION

Microchip's revolutionary Total Endurance Model provides electronic systems designers with unprecedented visibility into Serial EEPROM-based applications. This advanced software model (with a very friendly user interface) eliminates time and guesswork from Serial EEPROM-based designs by accurately predicting the device's performance and reliability within a user-defined application environment. Design trade-off analysis which formerly consumed days or weeks can now be performed in minutes...with a level of accuracy that delivers a truly robust design.

Users may input the following application parameters:

- Serial EEPROM device type
- Bytes to be written per cycle
- Cycling mode - byte or page
- Data pattern type - random or worst-case
- Temperature in °C
- Erase/Write cycles per day
- Application lifetime or target PPM level

The model will respond with FIT rate, PPM level, application life and a plot of the PPM level vs. number of cycles. The model is available in both DOS and Windows versions.

BACKGROUND

Microchip's research into the Erase/Write endurance of Serial EEPROMs has resulted in the conclusion that endurance depends upon three primary effects: the physical properties of the EEPROM cell, the internal error-correction technology employed, and the application environment. EEPROM endurance specified as a "typical" value in device data sheets must therefore be evaluated on a case-by-case basis, taking into account the manner in which the device will be used in the application. The Microchip Total Endurance™ software applies the user-defined application parameters to a complex mathematical model in order to emulate the EEPROM's performance and reliability in the system.

USING THE MODEL

The user has simply to choose a Microchip Serial EEPROM device from the device-list menu and begin entering the application parameters. The entire process can take literally seconds to complete, and the model will output the PPM level and FIT rate of the device vs. the number of Erase/Write cycles. If the user has specified an application lifetime, the model will output PPM and FIT rates at that point in time. Alternately, the user may input a desired PPM level and the model will calculate the application lifetime which will result in that survival rate. The user may then trade-off any of the parameters (device type, voltage, application life, temperature, # of bytes per cycle, # of cycles per day etc.) to arrive at an optimal solution for the intended application.

Whenever a parameter is changed, calculation of the ppm/application life is automatic. An "update" box will appear inside the graph to indicate that new data has been entered and the graph should be redrawn. A single click in the "draw" box will redraw the plot of ppm vs. cycles; a click in the "Resize" box will take the plot to full-screen display for a closer view. The plot data can be saved to a file or the plot itself can be copied to the clipboard to be pasted into another application.

ACCURACY OF THE MODEL

The accuracy of the Microchip Total Endurance model has been verified against test data to within ten percent of the actual values. However, Microchip makes no warranty as to its accuracy or applicability of the information to any given application. It is intended to be used as a guide to aid designers of Serial EEPROM-based systems in performing trade-off analysis and developing robust and reliable designs.

Order Information:

Description	Part Number
Total Endurance Software Disk	SW242001

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Third Party Support Cross Reference Charts

Microchip Technology Inc. has positioned itself to play a dominant role as a supplier of high-performance, field-programmable microcontrollers and associated memory and logic products for embedded control applications.

The following reference charts represent many of the third party development products and services available for Microchip PIC16/17 Microcontrollers, ASSP and Memory products.

The listings include emulators, programmers, development boards, assemblers, simulators, linkers, compilers, development software, and accessories. New products and services are continually being developed. For the most current listing of Third Party development products as well as an up-to-date listing of independent Microchip consultants, refer to Microchip's website at: www.microchip.com.

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Emulators

	PIC14000	PIC16C52	PIC16C54	PIC16C54A	PIC16C55	PIC16C56	PIC16C58A	PIC16C58B	PIC16C554	PIC16C558	PIC16C57	PIC16C574	PIC16C58A	PIC16C58B	PIC16C61	PIC16C62	PIC16C62A	PIC16C63	PIC16C64	PIC16C64A	PIC16C65	PIC16C65A	PIC16C620	PIC16C621	PIC16C622	PIC16C71	PIC16C710	PIC16C711	PIC16C712	PIC16C713	PIC16C72	PIC16C72A	PIC16C73	PIC16C73A	PIC16C74	PIC16C74A	PIC16F83	PIC16CR83	PIC16F84	PIC16CR84	PIC16C923	PIC17C42A	PIC17C43	MTAXXXXXXX	Ex. Algorithm
Advanced Transdata Corporation																																													
ICE-16C5X and ICE-16C71		●	●		●	●			●						●									●																				
RICE16		●			●	●			●						●									●																				
RICE17																																													
Axiom Manufacturing																																													
ICE-PIC															●	●																													
CEIBO																																													
CEIBO DS-M8	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Dr. Krohn & Stiller																																													
Emulator E8/E16/E32	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Emulation Technology, Inc.																																													
ETiC16 & ETiCRT		●	●		●	●			●						●									●																				
Farsoft Computers cc																																													
PIXIE		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Goldenchip Electronics Ltd.																																													
PICMATE		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Goldenchip Institute																																													
PICRICE		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
ISYSTEM GmbH																																													
iC2000	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
iC181 Power Emulator	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
MicroSystems Development, Inc.																																													
PicEm-14															●	●								●																						
MICROTIME Computer Inc.																																													
WINICE PIC16/17	●	●		●	●			●			●					●				●					●						●				●						●			
Micropet 16C5X	●	●		●	●			●			●					●				●					●						●				●						●			
Parallax Inc.																																													
ClearView Mathias		●	●		●	●			●						●									●						●				●						●			
ClearView '5x Hobbyist Pack		●	●		●	●			●						●									●						●				●						●			
Pinnacle Technologies																																													
PICE		●	●	●	●	●			●						●									●						●				●						●			
PIC-ICE II	●	●	●	●	●	●			●						●									●						●				●						●			
PHYTON Ltd.																																													
picACE		●	●	●	●	●	●	●																																					
PROCHIPS																																													
PRO STATION-5X	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
PRO STATION-X2																																													
RF Solutions & Neosoft, Inc.																																													
The ICEPIC16CXX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●

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Emulators/Programmers

Emulators continued...

	PIC14000	PIC16C92	PIC16C54	PIC16C54A	PIC16C54B	PIC16CR54	PIC16C54A	PIC16C55	PIC16C56	PIC16C56B	PIC16C57	PIC16CR57B	PIC16C58A	PIC16C58B	PIC16CR58A	PIC16C58A	PIC16C62	PIC16C62A	PIC16C63	PIC16C64A	PIC16C65	PIC16C65A	PIC16C620	PIC16C621	PIC16C622	PIC16C71	PIC16C710	PIC16C711	PIC16C712	PIC16C715	PIC16C72A	PIC16C74	PIC16C74A	PIC16F83	PIC16CR83	PIC16C84	PIC16F84	PIC16CR84	PIC16C92X	PIC17C42A	PIC17C43	PIC17C44	MTAXXXXXX	Ex. Algorithm
Softaid, Inc.																																												
UEM	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
SofTec Microsystems																																											
DSE1657	●			●		●		●																																			
DSE1671													●																															
DSE16822																						●	●																					
DSE1674														●			●	●		●																								
Programmers																																											
Abitec Products																																											
PIC-DATS and PIC-DATS-PG	●			●		●		●																																			
Advanced Transdata Corporation																																											
PGM16N	●	●		●		●		●																																		
PGM17													●									●	●																					
PGM810														●			●	●		●																								
Advantech Equipment Corp.																																											
LabTool-48	●	●		●		●		●																																		
Advin Systems, Inc.																																											
PILOT-U84	●	●				●		●																																			
PILOT-145	●	●				●		●																																			
Application Solutions, Ltd.																																											
ASL PROGRAMMER	●	●				●		●																																			
AS Entwicklungsbüro für Industrieelektronik																																											
Factory Programmer and Tester																																											
Baradine Products Ltd.																																											
MICRO-BURNER System 512	●	●		●		●		●																																			
BP Microsystems, Inc.																																											
BP-1200 Universal Device Pgm.	●			●		●		●																																			
BP-4100 Automated Pgm. System	●			●		●		●																																			
Citadel Products Ltd.																																											
PC82 Univ. Pgm. & Tester	●			●		●		●																																			
Data I/O®																																											
2700 Programming System	●	●		●		●		●																																			
3900 Programming System	●	●		●		●		●																																			
ProMaster 2500	●	●		●		●		●																																			
UniSite™	●	●		●		●		●																																			

Programmers

	PIC14000	PIC16C52	PIC16C54	PIC16C54A	PIC16C54B	PIC16CR54A	PIC16C55	PIC16C56	PIC16C57B	PIC16C58B	PIC16CR57B	PIC16C58A	PIC16C58B	PIC16CR58A	PIC16C61	PIC16C62	PIC16C62A	PIC16C63	PIC16C64A	PIC16C65	PIC16C65A	PIC16C620	PIC16C621	PIC16C622	PIC16C71	PIC16C710	PIC16C711	PIC16C72	PIC16C73	PIC16C73A	PIC16C74	PIC16C74A	PIC16C83	PIC16C84	PIC16F84	PIC16CR84	PIC16C923	PIC16C924	PIC17C42A	PIC17C43	MAXXXXXXX	Ex. Algorithm
Dataman Programmers Ltd.																																											
Dataman-48	●		●	●			●	●		●					●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●			●			●	●			
Dataman Softy 4			●	●			●	●		●					●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●			●			●	●			
Deus Ex Machina Engineering, Inc.																																										
XPGM™ (Note 1)																																											
EBLabs																																										
EBP-1000	●															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●									
E D Technical Publications																																										
EDTP PIC17C42 Programmer																																							●				
Elan Digital Systems Ltd.																																										
Model 5000		●	●			●	●											●	●					●	●				●	●												
Model 6000		●	●			●	●											●	●					●	●				●	●												
Electro-Kenetics																																										
Micro-bRISC	●															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●									
E.E. TOOLS, INC.																																										
AllMax, AllMax+		●	●			●	●			●					●	●		●	●					●	●	●			●	●												
MegaMax, MegaMax-4G		●	●			●	●			●					●	●		●	●					●	●	●			●	●												
Emulation Technology, Inc.																																										
ET-PIC1000				●			●			●					●	●		●						●			●			●				●									
ET-PIC4000/48				●			●			●					●	●		●						●			●			●				●									
ET-PIC5000				●			●											●						●						●													
ET-PIC16				●			●			●					●	●		●						●																			
ET-PIC17																																							●				
Goldenchip Electronics Ltd.																																										
PICKIT	●	●	●				●	●							●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●								
Goldenchip Institute																																										
PICPGM-ALL	●	●	●				●	●							●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●					●			
Hamis																																										
AllProg-44		●	●				●	●															●											●								
ICE Technology Ltd.																																										
LV40 Portable		●	●				●	●							●	●		●						●			●			●				●								
MICROMASTER LV		●	●				●	●							●	●		●						●			●			●				●								
INTER Mühendilik																																										
PICPR16																																										
iSYSTEM GmbH																																										
SEPROG		●	●			●	●			●																																
ITU Technologies																																										
PIC-la Programmer																●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●								

Note 1: Supports 37LV36, 37LV65, 37LV128 only

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Programmers

	PIC14000	PIC16C92	PIC16C924	PIC16C64	PIC16C642	PIC16C64A	PIC16C65B	PIC16CR64	PIC16C642A	PIC16C65	PIC16C65A	PIC16C84	PIC16C620	PIC16C621	PIC16C622	PIC16C71	PIC16C710	PIC16C72	PIC16C73	PIC16C73A	PIC16C74	PIC16C74A	PIC16F83	PIC16CR83	PIC16C84	PIC16F84	PIC16CR84	PIC16C92X	PIC17C42A	PIC17C43	PIC17C44	MAXXXXXX	Ex. Algorithm
J&M Microtek, Inc.																																	
JM-PICE	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
K.E.M. Electronics Japan Ltd.																																	
KEM-901dash8 and KEM-905A		●	●		●	●		●		●		●			●				●				●										
LEAP Electronic Co., Ltd.																																	
LEAPER 10		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
LP-U4		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
LEAPER-6																																	
Link Instruments, Inc.																																	
CLK-3100		●	●	●		●	●		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
Logical Devices, Inc.																																	
Allpro-88 and 88XR		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
XPRO Family		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
Chipmaster 3000		●	●		●	●	●		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
MEMEC BALTIC Ltd.																																	
UNIPIC	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
microEngineering Labs																																	
EPIC Pocket PIC Programmer													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
MicroPross																																	
The ROM 5000B and ROM 3000B		●			●		●																										
MSI Electronics																																	
MSI In Circuit Programmer		●			●		●			●					●				●				●										
MQP Electronics																																	
MQP System 2000		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
MQP Model 200		●		●	●		●		●			●			●																		
PIN-MASTER 48		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
Needham's Electronics Inc.																																	
EMP-20		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
Newfound Electronics																																	
WARP-3	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
WARP-17		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
ORMIX, Ltd.																																	
COMPIC-PRO	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
COMPIC-1	●												●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
COMPIC-5X	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
OWEN electronic GmbH																																	
AP-II+		●			●		●						●																				
Parallax, Inc.																																	
PIC16CXX Programmer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						

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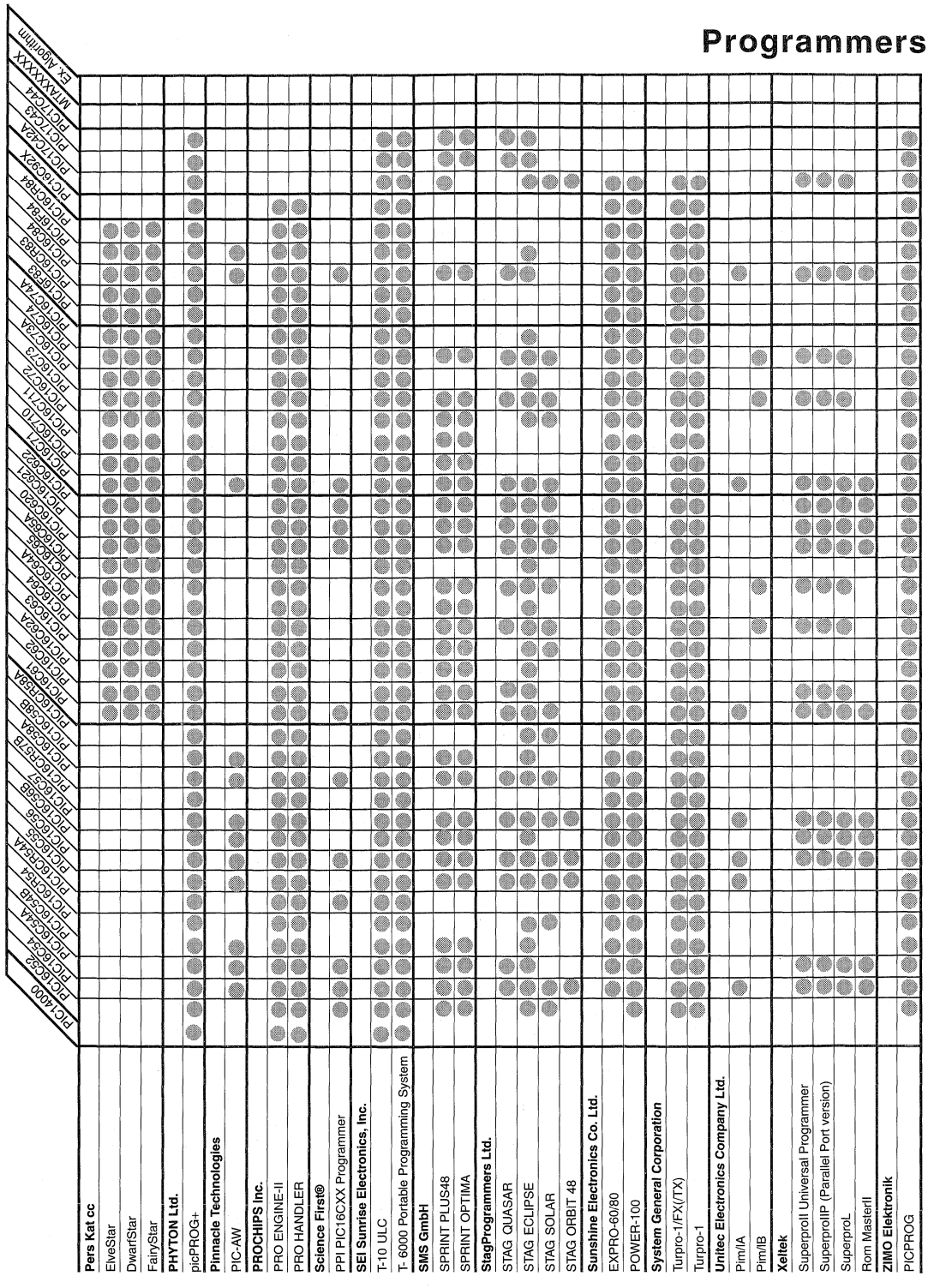
Programmers



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Gang Programmers

	PIC14000	PIC16C62	PIC16C64	PIC16C642	PIC16C65A	PIC16C65B	PIC16C74	PIC16C74A	PIC16C76	PIC16C77	PIC16C554	PIC16C554A	PIC16C556	PIC16C556A	PIC16C558	PIC16C558A	PIC16CR57B	PIC16C57	PIC16C58B	PIC16C58A	PIC16CR58A	PIC16C61	PIC16C62A	PIC16C63	PIC16C64A	PIC16C65A	PIC16C65B	PIC16C620	PIC16C621	PIC16C622	PIC16C620A	PIC16C621A	PIC16C622A	PIC16C71	PIC16C710	PIC16C711	PIC16C72	PIC16C73	PIC16C73A	PIC16C74	PIC16C74A	PIC16F83	PIC16CR83	PIC16C84	PIC16F84	PIC16CR84	PIC16C92X	PIC17C42A	PIC17C43	PIC17C44	MTAXXXXXXX	Ex: Algorithm
Advanced Transdata Corporation																																																					
PGM16G		●			●		●																																														
PGM17G																																																					
PGM40G																																																					
PGM47G																																																					
BP Microsystems, Inc.																																																					
BP-2100 Concurrent Pgm. System™		●			●		●																																													
BP-2200 Concurrent Pgm. System™		●			●		●																																													
BYTEK Corporation																																																					
MULTITRK Gang & Set		●			●		●																																													
Emulation Technology, Inc.																																																					
ET-PIC16G		●		●			●																																													
ET-PIC17G																																																					
ET-PIC47G																																																					
ET-PIC12000		●		●			●																																													
HI-LO Systems Research Co. Ltd.																																																				
ALL-07		●		●			●																																													
Lloyd Research Ltd.																																																					
L9OOO		●		●			●																																													
MicroLabs																																																					
Octopussy		●		●			●																																													
Pinnacle Technologies																																																					
PAW2		●		●			●																																													
PAW3		●		●			●																																													
SEI Sunrise Electronics, Inc.																																																				
T- 2000		●		●			●																																													
T- 4000		●		●			●																																													
T- 5000		●		●			●																																													
T- 8000		●		●			●																																													
SMS GmbH																																																				
SPRINT MULTISYTE		●		●			●																																												
PP-Parallel-Programming-Handler		●		●			●																																												
System General Corporation																																																				
Multi-APRO		●		●			●																																												
Triba Microsystems, Inc.																																																				
Flex-700		●		●			●																																												
Unitec Electronics Company Ltd.																																																				
Pim/10A		●		●			●																																												
Pim/10B																																																			

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Software Tools

	PIC14000	PIC16C52	PIC16C54	PIC16C54A	PIC16C55	PIC16C56	PIC16C57	PIC16C58A	PIC16C58B	PIC16C554	PIC16C554A	PIC16C558	PIC16C558A	PIC16C61	PIC16C62	PIC16C62A	PIC16C63	PIC16C64	PIC16C64A	PIC16C65	PIC16C65A	PIC16C620	PIC16C621	PIC16C622	PIC16C62A	PIC16C62B	PIC16C63A	PIC16C642	PIC16C65B	PIC16C66	PIC16C67	PIC16C71	PIC16C710	PIC16C711	PIC16C712	PIC16C715	PIC16C72	PIC16C72A	PIC16C73	PIC16C73A	PIC16C74	PIC16C74A	PIC16C76	PIC16C83	PIC16C84	PIC16C923	PIC16C924	PIC17C42	PIC17C42A	PIC17C43	PIC17C44	MTAXXXXXX	Ex. Algorithm
2500AD Software, Inc.																																																					
PIC Macro Cross Assembler		●						●																																														
Actum Solutions																																																				
The Realizer®		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Avocet Systems, Inc.																																																				
PIC-Tools	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Butterfly Signal Processing Inc.																																																				
B.LO.C™	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Butterfly Signal Processing Inc. and M&M Embedded Systems																																																				
B.LO.C ReSource™	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Byte Craft Limited																																																				
MP-C Code Development System	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Custom Computer Services, INC.																																																				
C Compilers	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Electronic Emulation cc																																																				
ICEPIC		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
PICASM	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Hamis																																																				
P-As V2.0		●				●	●			●	●																																									
P-Sim V2.0		●				●	●			●	●																																									
HI-TECH Software																																																				
HI-TECH C Cross Compiler	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
ICOMS Communications																																																				
MicroPix-C		●				●	●			●	●																																									
microEngineering Labs																																																				
PicBasic Compiler																																																				
MicroLabs																																																				
PS-PIC16C5X Simulator Tools		●				●	●			●	●																																								
Mikrocomputer-Verlag Jürgen Ortmann																																																			
SIMPIC and EMUPIC		●				●	●			●	●																																								
Momentum Microsystems																																																				
ACCESS. abl® Development Kit																																																			
NITPIC cc																																																			
NITPIC™		●				●	●			●	●																																								
OEMA																																																			
ECAL		●				●	●			●	●																																								
PHYTON, Ltd.																																																			
picDESIGNER	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●

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Software Tools/Development Boards & Accessories

	PIC14000	PIC16C92	PIC16C54	PIC16C54A	PIC16C55A	PIC16C56A	PIC16C58B	PIC16C57	PIC16C58A	PIC16CR57B	PIC16C58A	PIC16C58B	PIC16C61	PIC16C62B	PIC16C62	PIC16C63A	PIC16C64A	PIC16C65B	PIC16C66	PIC16C620	PIC16C621	PIC16C622	PIC16C71	PIC16C710	PIC16C711	PIC16C712	PIC16C715	PIC16C72A	PIC16C73B	PIC16C74A	PIC16C76	PIC16C83	PIC16C84	PIC16F83	PIC16F84	PIC16F84A	PIC16F87	PIC16F872	PIC16C923	PIC16C924	PIC17C42A	PIC17C43	MTAXXXXXX	Ex. Algorithm
PROCHIPS, Inc.																																												
PRO LAB		●				●		●						●		●				●				●				●				●													
STYX																																												
PICNIC		●				●		●						●		●				●				●				●				●													
Universal Cross-Assemblers																																												
Cross-32 Meta-Assembler		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Development Boards & Accessories																																												
Application Solutions, Ltd.																																												
PIC16C71 Evaluation Board																																												
Arcox Engineering																																												
PIC16C5X Single Board Computer Kit																																											
Axiom Manufacturing																																											
Development Board																																											
Bluebird Electronics																																												
PIC16/17 Support Products		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
P. Caritato & Associates S.A.																																												
PICBOARD																						●																							
PICLAB													●									●																							
Cooper Ridge Systems																																												
PIC16CXX Proto boards		●				●								●		●				●				●				●				●													
Custom Computer Services, Inc.																																												
Software Prototyping Board		●	●	●	●	●		●				●		●		●				●				●				●				●													
E D Technical Publications																																												
EDTP PIC-PERF		●				●		●				●										●										●													
Emulation Technology, Inc.																																												
Adapt-A-Socket®		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
SMT Adapters and Accessories		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
E-LAB Digital Engineering, Inc.																																												
PICPLUS™																																												
FARSOFT Computers cc																																													
PROTO-1		●				●		●														●																							
HEWLETT-PACKARD																																												
HP54620A/C Logic Analyzer		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
HP54645D Mixed Signal Oscilloscope		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●

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Development Boards & Accessories

	PIC14000	PIC16C52	PIC16C54	PIC16C54A	PIC16C54B	PIC16CR54	PIC16C55A	PIC16C56	PIC16C58B	PIC16C57	PIC16CR57B	PIC16C58A	PIC16C58B	PIC16F83A	PIC16C61	PIC16C62	PIC16C62A	PIC16C63	PIC16C64A	PIC16C65B	PIC16C65A	PIC16C620	PIC16C621	PIC16C622	PIC16C70	PIC16C71	PIC16C72	PIC16C73	PIC16C73A	PIC16C74A	PIC16C74	PIC16C83	PIC16CR83	PIC16C84	PIC16F84	PIC16C923	PIC16C92X	PIC17C42A	PIC17C43	PIC17C44	MTAXXXXXX	Ex. Algorithm
Hitachi-Denshi America, Ltd.																																										
Logic Analyzers VC-3120 and VC-3130																																									
Logical Systems Corporation																																									
Programming and Prototyping Adapters	●	●	●			●		●		●						●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				
Macraigor Systems Inc.																																									
P57 Mustang Board™		●				●		●		●																															
Micro Application Laboratory Corp.																																									
PRO-KIT Evaluation Board	●	●	●			●		●		●												●	●											●	●							
microEngineeringLabs																																									
PICProto prototyping boards	●	●	●			●		●		●		●				●			●			●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				
MICROMINT, Inc.																																									
PicStic™ Modules																																									
Micropower Electronics, Inc.																																									
PIC Micro-Proto		●		●				●								●			●			●	●											●	●							
MICRO software																																									
28-pin DIP to SOIC Converter		●	●	●		●		●		●		●				●			●			●	●			●								●	●							
MQP Electronics																																									
Package converters		●				●		●								●																			●							
P&S Electronics Co. Ltd																																									
PS1008 Microcontroller/PS1008-Kit										●																															
Parallax Inc.																																									
BASIC Stamp version D																																									
BASIC Stamp I Module (BS1-IC)																																									
BASIC Stamp II Module (BS2-IC)																																									
Pers Kat cc																																									
BrightStar																																									
PROCHIPS, Inc.																																									
PRO TRAINER	●	●	●	●		●		●		●		●				●			●			●	●			●								●	●							
Southwest Microelectronics, Inc.																																									
SMI-1014-TG																																									
Sparks																																									
PIC16C55/PIC16C57 Product Platform	●			●		●																																			
TR Engineering, Inc.																																									
PIC14000 Mixed Signal Controller	●																																								
Unified Microsystems																																									
SXT-55																																									
VersaTech Electronics																																									
FBASIC TICkit								●																																●	
Winslow International Ltd.																																									
Winslow Adaptics™	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●

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MICROCHIP

SECTION 17
PIC16/17 MICROCONTROLLER PROGRAMMING SPECIFICATIONS

PIC12C5XX EPROM Memory Programming Specification 17-1
PIC14000 EPROM Memory Programming Specification 17-13
PIC16C5X EPROM/ROM Memory Programming/Verify Specification 17-25
PIC16C55X EPROM Memory Programming Specification 17-37
PIC16C6X/7X/9XX EPROM Memory Programming Specification 17-49
PIC16C84 EEPROM Memory Programming Specification 17-69
PIC16F8X EEPROM Memory Programming Specification 17-81
PIC17CXX EPROM Memory Programming Specification 17-95
SQTP Specification for PIC16/17 17-109

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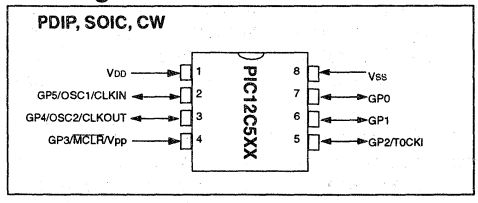
PIC12C5XX

EPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC12C508
- PIC12C509

Pin Diagram



1.0 PROGRAMMING THE PIC12C5XX

The PIC12C5XX can be programmed using a serial method. Due to this serial programming, the PIC12C5XX can be programmed while in the user's system increasing design flexibility. This programming specification applies to PIC12C5XX devices in all packages.

1.1 Hardware Requirements

The PIC12C5XX requires two programmable power supplies, one for VDD (2.0V to 6.5V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

The programming mode for the PIC12C5XX allows programming of user program memory, special locations used for ID, and the configuration word for the PIC12C5XX.

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PIN DESCRIPTIONS (DURING PROGRAMMING): PIC12C508/509

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
GP1	CLOCK	I	Clock input
GP0	DATA	I/O	Data input/output
GP3/MCLR/VPP	VPP	P	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = input, O = Output, P = Power

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2.0 PROGRAM MODE ENTRY

The program/verify test mode is entered by holding pins DB0 and DB1 low while raising $\overline{MCLR}$ pin from VIL to VIHH. Once in this test mode the user program memory and the test program memory can be accessed and programmed in a serial fashion. The first selected memory location is the fuses. **GP0 and GP1 are Schmitt trigger inputs in this mode.**

Incrementing the PC once (using the increment address command) selects location 0x000 of the regular program memory. Afterwards all other memory locations from 0x001-01FF (PIC12C5[illegible]), 0x001-03FF (PIC12C509) can be addressed by incrementing the PC.

If the program counter has reached the last user program location and is incremented again, the on-chip special EPROM area will be addressed. (See Figure 2-2 to determine where the special EPROM area is located for the various PIC12C5XX devices).

2.1 Programming Method

The programming technique is described in the following section. It is designed to guarantee good programming margins. It does, however, require a variable power supply for VCC.

2.1.1 PROGRAMMING METHOD DETAILS

Essentially, this technique includes the following steps:

1. Perform blank check at VDD = VDDmin. Report failure. The device may not be properly erased.
2. Program location with pulses and verify after each pulse at VDD = VDDP:
   where VDDP = VDD range required during programming (4.5V - 5.5V).

a) Programming condition:

VPP = 13.0V to 13.25V

VDD = VDDP = 4.5V to 5.5V

VPP must be ≥ VDD + 7.25V to keep "programming mode" active.

b) Verify condition:

VDD = VDDP

VPP ≥ VDD + 7.5V but not to exceed 13.25V

If location fails to program after "N" pulses, (suggested maximum program pulses of 25) then report error as a programming failure.

Note:	Device must be verified at minimum and maximum specified operating voltages as specified in the data sheet.

3. Once location passes "Step 2", apply 3X over-programming, i.e., apply three times the number of pulses that were required to program the location. This will guarantee a solid programming margin. The overprogramming should be made "software programmable" for easy updates.
4. Program all locations.
5. Verify all locations (using speed verify mode) at VDD = VDDmin
6. Verify all locations at VDD = VDDmax

   VDDmin is the minimum operating voltage spec. for the part. VDDmax is the maximum operating voltage spec. for the part.

2.1.2 SYSTEM REQUIREMENTS

Clearly, to implement this technique, the most stringent requirements will be that of the power supplies:

VPP: VPP can be a fixed 13.0V to 13.25V supply. It must not exceed 14.0V to avoid damage to the pin and should be current limited to approximately 100mA.

VDD: 2.0V to 6.5V with 0.25V granularity. Since this method calls for verification at different VDD values, a programmable VDD power supply is needed.

Current Requirement: 40mA maximum

Microchip may release devices in the future with different VDD ranges which make it necessary to have a programmable VDD.

It is important to verify an EPROM at the voltages specified in this method to remain consistent with Microchip's test screening. For example, a PIC12C5XX specified for 4.5V to 5.5V should be tested for proper programming from 4.5V to 5.5V.

Note:	Any programmer not meeting the programmable VDD requirement and the verify at VDDmax and VDDmin requirement may only be classified as "prototype" or "development" programmer but not a production programmer.

2.1.3 SOFTWARE REQUIREMENTS

Certain parameters should be programmable (and therefore easily modified) for easy upgrade.

a) Pulse width

b) Maximum number of pulses, present limit 25.

c) Number of over-programming pulses: should be = (A • N) + B, where N = number of pulses required in regular programming. In our current algorithm A = 3, B = 0.

2.2 Programming Pulse Width

Program Memory Cells: When programming one word of EPROM, a programming pulse width (TPW) of 100µs is recommended.

The maximum number of programming attempts should be limited to 25 per word.

After the first successful verify, the same location should be over-programmed with 3X over-programming.

Configuration Word: The configuration word for oscillator selection, WDT (watchdog timer) disable and code protection, and MCLR enable, requires a programming pulse width (TPWF) of 10ms. A series of 100µs pulses is preferred over a single 10ms pulse.

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FIGURE 2-1: PROGRAMMING METHOD FLOWCHART

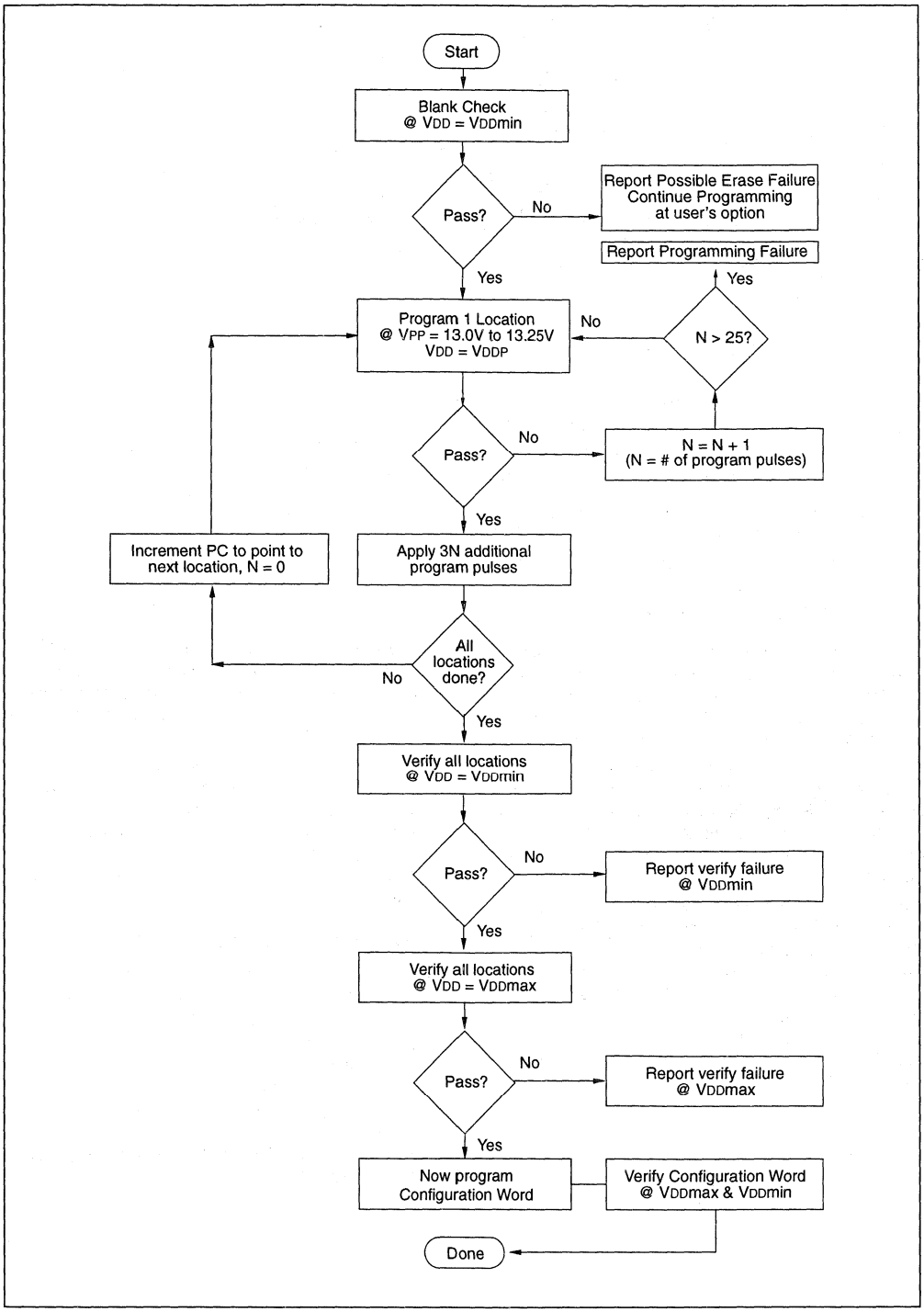

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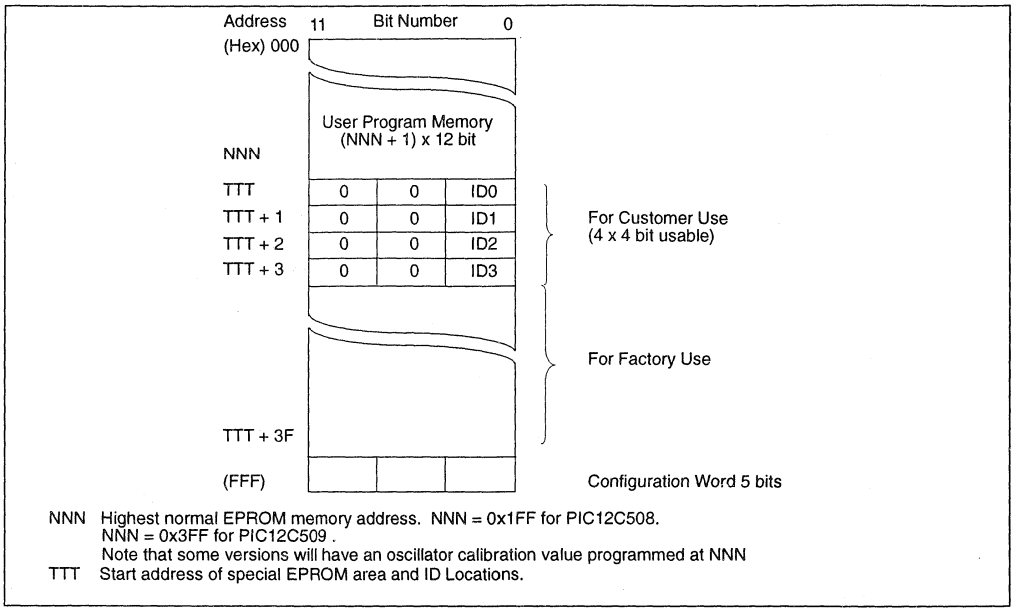
FIGURE 2-2: PIC12C5XX SERIES PROGRAM MEMORY MAP IN PROGRAM/VERIFY MODE



NNN Highest normal EPROM memory address. NNN = 0x1FF for PIC12C508.
NNN = 0x3FF for PIC12C509 .
Note that some versions will have an oscillator calibration value programmed at NNN
TTT Start address of special EPROM area and ID Locations.

2.3 Special Memory Locations

The highest address of program memory space is reserved for the internal RC oscillator calibration value. This location should not be overwritten except when this location is blank, and it should be verified, when programmed, that it is a `MOVLW XX` instruction.

The ID Locations area is only enabled if the device is in a test or programming/verify mode. Thus, in normal operation mode only the memory location 0x000 to 0xNNN will be accessed and the Program Counter will just roll over from address 0xNNN to 0x000 when incremented.

The configuration word can only be accessed immediately after $\overline{MCLR}$ going from V_{IL} to V_{HH}. The Program Counter will be set to all '1's upon $\overline{MCLR} = V_{IL}$. Thus, it has the value "0xFFF" when accessing the configuration EPROM. Incrementing the Program Counter once causes the Program Counter to roll over to all '0's. Incrementing the Program Counter 4K times after reset ($\overline{MCLR} = V_{IL}$) does not allow access to the configuration EPROM.

2.3.1 CUSTOMER ID CODE LOCATIONS

Per definition, the first four words (address TTT to TTT + 3) are reserved for customer use. It is recommended that the customer use only the four lower order bits (bits 0 through 3) of each word and filling the eight higher order bits with '0's.

A user may want to store an identification code (ID) in the ID locations and still be able to read this code after the code protection bit was programmed. This is possible if the ID code is only four bits long per memory location, is located in the least significant nibble boundary of the 12-bit word, and the remaining eight bits are all '0's.

EXAMPLE 2-1:CUSTOMER CODE 0xD1E2

The Customer ID code "0xD1E2" should be stored in the ID locations 200-203 like this:

```
200:   0000 0000 1101
201:   0000 0000 0001
202:   0000 0000 1110
203:   0000 0000 0010
```

Reading these four memory locations, even with the code protection bit programmed would still output on Port A the bit sequence "1101", "0001", "1110", "0010" which is "0xD1E2".

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2.4 Program/Verify Mode

The program/verify mode is entered by holding pins GP1 and GP0 low while raising $\overline{MCLR}$ pin from VIL to VIHH (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. GP1 is a Schmitt Trigger input in this mode.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the MCLR pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

Note: The $\overline{MCLR}$ pin should be raised from VIL to VIHH within 9 ms of VDD rise. This is to ensure that the device does not have the PC incremented while in valid operation range.

2.4.1 PROGRAM/VERIFY OPERATION

The GP1 pin is used as a clock input pin, and the GP0 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (GP1) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSB) of the command being input first. The data on pin GP0 is required to have a minimum setup and hold time (see AC/DC specs) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1µs between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output LSB first. Therefore, during a read operation the LSB will be transmitted onto pin GP0 on the rising edge of the second cycle, and during a load operation the LSB will be latched on the falling edge of the second cycle. A minimum 1µs delay is also specified between consecutive commands.

All commands are transmitted LSB first. Data words are also transmitted LSB first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1µs is required between a command and a data word (or another command).

The commands that are available are listed in Table 2-1.

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TABLE 2-1: COMMAND MAPPING

Command	Mapping (MSB ... LSB)						Data
Load Data	0	0	0	0	1	0	0, data(14), 0
Read Data	0	0	0	1	0	0	0, data(14), 0
Increment Address	0	0	0	1	1	0	
Begin programming	0	0	1	0	0	0	
End Programming	0	0	1	1	1	0	

Note: The clock must be disabled during in-circuit programming.

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2.4.1.1 LOAD DATA

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. Because this is a 12 bit core, the two msb's of the data word are ignored. A timing diagram for the load data command is shown in Figure 5-1.

2.4.1.2 READ DATA

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The GP0 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.4.1.3 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.4.1.4 BEGIN PROGRAMMING

A load data command must be given before every begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100µs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

2.4.1.5 END PROGRAMMING

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

2.5 Programming Algorithm Requires Variable VDD

The PIC12C5XX uses an intelligent algorithm. The algorithm calls for program verification at VDDmin as well as VDDmax. Verification at VDDmin guarantees good "erase margin". Verification at VDDmax guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (4.75 - 5.25V).

VDDP = VCC range required during programming.

VDD min. = minimum operating VDD spec for the part.

VDDmax = maximum operating VDD spec for the part.

Programmers must verify the PIC12C5XX at its specified VDDmax and VDDmin levels. Since Microchip may introduce future versions of the PIC12C5XX with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

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3.0 CONFIGURATION WORD

The PIC12C5XX family members have several configuration bits. These bits can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. Figure 3-1 provides an overview of configuration bits.

FIGURE 3-1: CONFIGURATION WORD BIT MAP

Bit Number:	11	10	9	8	7	6	5	4	3	2	1	0
PIC12C5XX	—	—	—	—	—	—	—	MCLRE	CP	WDTE	FOSC1	FOSC0

bit 11-5:**Reserved**, '–' write as '0' for PIC12C5XX

bit 4: **MCLRE**, Master Clear pin Enable Bit
0 = MCLR internally connected to Vdd
1 = MCLR pin enabled

bit 3: **CP**, Code Protect Enable Bit
1 = Code Memory Unprotected
0 = Code Memory Protected

bit 2: **WDTE**, WDT Enable Bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC<1:0>**, Oscillator Selection Bit
11: ExtRC oscillator
10: IntRC oscillator
01: XT oscillator
00: LP oscillator

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4.0 CODE PROTECTION

The program code written into the EPROM can be protected by writing to the CP0 bit of the configuration word.

In PIC12C5XX it is still possible to program and read locations 0x000 through 0x03F, after code protection. Once code protection is enabled, all protected segments read '0's (or "garbage values") and are prevented from further programming. All unprotected segments, including ID locations and configuration word, read normally. These locations can be programmed.

4.1 Embedding Configuration Word and ID Information in the Hex File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, configuration word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 4-1: CODE PROTECTION

PIC12C508

To code protect:

- (CP enable pattern: XXXXXXXX0XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read enabled, Write Enabled	Read enabled, Write Enabled
[0x00:0x3F]	Read enabled, Write Enabled	Read enabled, Write Enabled
[0x40:0x1FF]	Read disabled (all 0's), Write Disabled	Read enabled, Write Enabled
ID Locations (0x200 : 0x203)	Read enabled, Write Enabled	Read enabled, Write Enabled

PIC12C509

To code protect:

- (CP enable pattern: XXXXXXXX0XXX))

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read enabled, Write Enabled	Read enabled, Write Enabled
[0x00:0x3F]	Read enabled, Write Enabled	Read enabled, Write Enabled
[0x40:0x3FF]	Read disabled (all 0's), Write Disabled	Read enabled, Write Enabled
ID Locations (0x400 : 0x403)	Read enabled, Write Enabled	Read enabled, Write Enabled

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4.2 Checksum

4.2.1 CHECKSUM CALCULATIONS

Checksum is calculated by reading the contents of the PIC12C5XX memory locations and adding up the opcodes up to the maximum user addressable location, (not including the last location which is reserved for the oscillator calibration value) e.g., 0x1FE for the PIC12C508. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC12C50X family is shown in Table 4-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x723 at 0 and max address
PIC12C508	OFF	SUM[0x000:0x1FE] + CFGW & 0x001F	EE20	DC68
	ON	SUM[0x000:0x03F] + CFGW & 0x001F	EDF7	D363
PIC12C509	OFF	SUM[0x000:0x3FE] + CFGW & 0x001F	EC20	DA68
	ON	SUM[0x000:0x03F] + CFGW & 0x001F	EBF7	D163

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a through b inclusive]
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nibble.
For example,
ID0 = 0x12, ID1 = 0x37, ID2 = 0x4, ID3 = 0x26, then SUM_ID = 0x2746.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

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5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions
Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (20°C recommended)
Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.

Parameter No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
General							
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	IDDP	Supply current (from VDD) during programming			20	mA	
PD3	VDDV	Supply voltage during verify	VDDmin		VDDmax	V	Note 1
PD4	VIHH1	Voltage on $\overline{MCLR}$/VPP during programming	12.75		13.25	V	Note 2
PD5	VIHH2	Voltage on $\overline{MCLR}$/VPP during verify	VDD + 4.0		13.5		
PD6	IPP	Programming supply current (from VPP)			50	mA	
PD9	VIH1	(GP1, GP0) input high level	0.8 VDD			V	Schmitt Trigger input
PD8	VIL1	(GP1, GP0) input low level	0.2 VDD			V	Schmitt Trigger input
Serial Program Verify							
P1	TR	$\overline{MCLR}$/VPP rise time (VSS to VHH) for test mode entry			8.0	µs	
P2	Tf	$\overline{MCLR}$ Fall time			8.0	µs	
P3	Tset1	Data in setup time before clock ↓	100			ns	
P4	Thld1	Data in hold time after clock ↓	100			ns	
P5	Tdly1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0			µs	
P6	Tdly2	Delay between clock ↓ to clock ↑ of next command or data	1.0			µs	
P7	Tdly3	Clock ↑ to date out valid (during read data)	200			ns	
P8	Thld0	Hold time after $\overline{MCLR}$ ↑	2			µs	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be greater than VDD + 4.5V to stay in programming/verify mode.

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FIGURE 5-1: LOAD DATA COMMAND (PROGRAM/VERIFY)

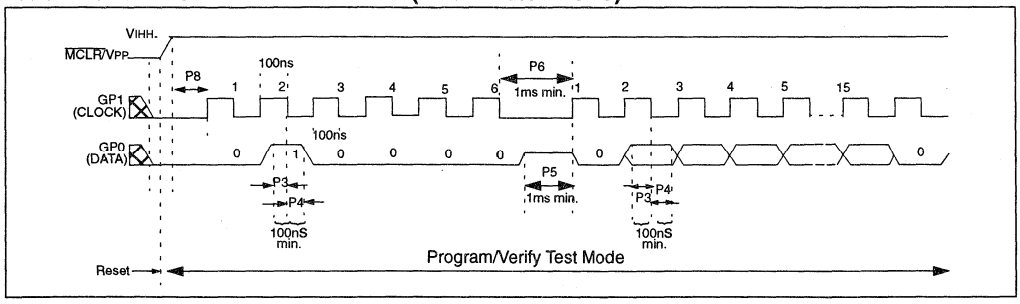


FIGURE 5-2: READ DATA COMMAND (PROGRAM/VERIFY)

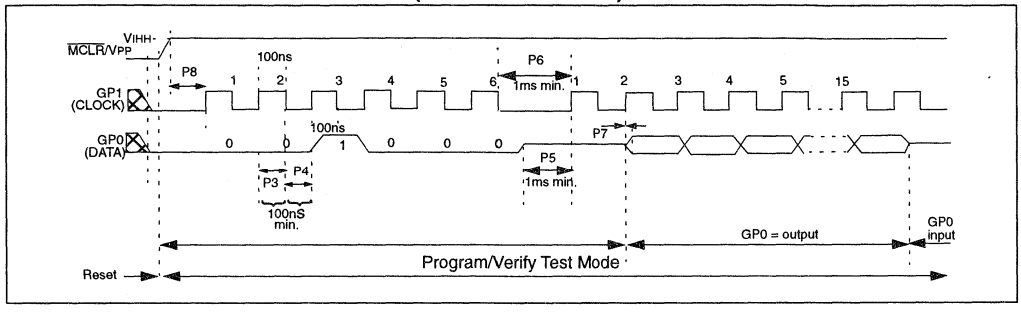
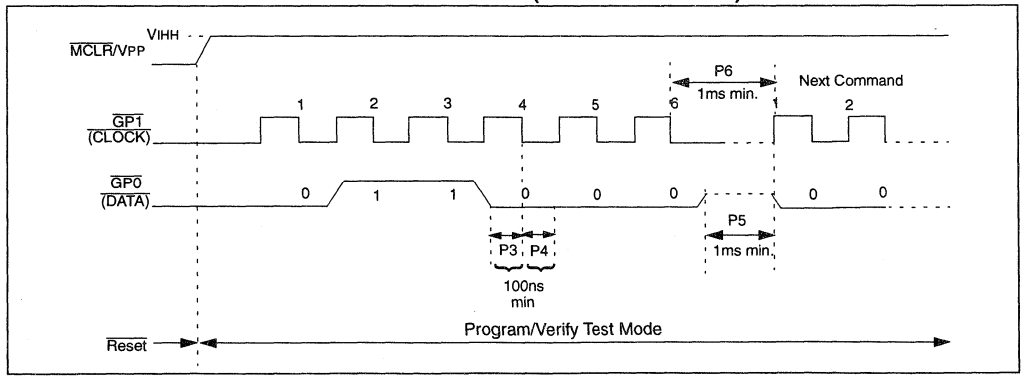


FIGURE 5-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)



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NOTES:

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MICROCHIP

PIC14000

EPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC14000

1.0 PROGRAMMING THE PIC14000

The PIC14000 can be programmed using a serial method. In serial mode the PIC14000 can be programmed while in the users system. This allows for increased design flexibility. This programming specification applies to PIC14000 devices in all packages.

1.1 Hardware Requirements

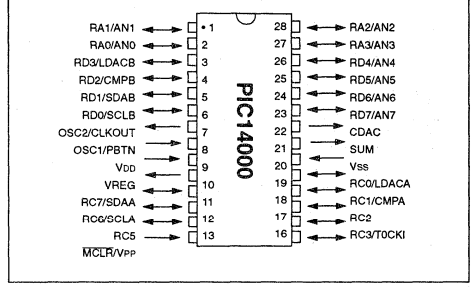
The PIC14000 requires two programmable power supplies, one for VDD (2.0V to 6.5V recommended) and one for VPP (12V to 14V).

1.2 Programming Mode

The programming mode for the PIC14000 allows programming of user program memory, configuration word, and calibration memory.

Pin Diagram

PDIP, SOIC, SSOP, Windowed CERDIP



Note: Peripheral pinout functions are not shown (see data sheets for full pinout information).

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PIN DESCRIPTIONS (DURING PROGRAMMING): PIC14000

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RC6	CLOCK	I	Clock input
RC7	DATA	I/O	Data input/output
MCLR/VPP	VPP	P	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

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2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The program and calibration memory space extends from 0x000 to 0xFFF (4096 words). Table 2-1 shows actual implementation of program memory in the PIC14000.

TABLE 2-1: IMPLEMENTATION OF PROGRAM AND CALIBRATION MEMORY IN THE PIC14000

Area	Memory Space	Access to Memory
Program	0x000-0xFBF	PC<12:0>
Calibration	0xFC0 -0xFFF	PC<12:0>

When the PC reaches address 0xFFF, it will wrap around and address a location within the physically implemented memory (see Figure 2-1).

In programming mode the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x0000, or 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode, as described in Section 2.2.

In the configuration memory space, 0x2000-0x20FF are utilized. When in configuration memory, as in the user memory, the 0x2000-0x2XFF segment is repeatedly accessed as PC exceeds 0x2XFF (see Figure 2-1).

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000 : 0x2003]. All other locations are reserved and should not be programmed.

The ID locations read out normally, even after code protection. To understand how the devices behave, refer to Table 4-1.

To understand the scrambling mechanism after code protection, refer to Section 4.1.

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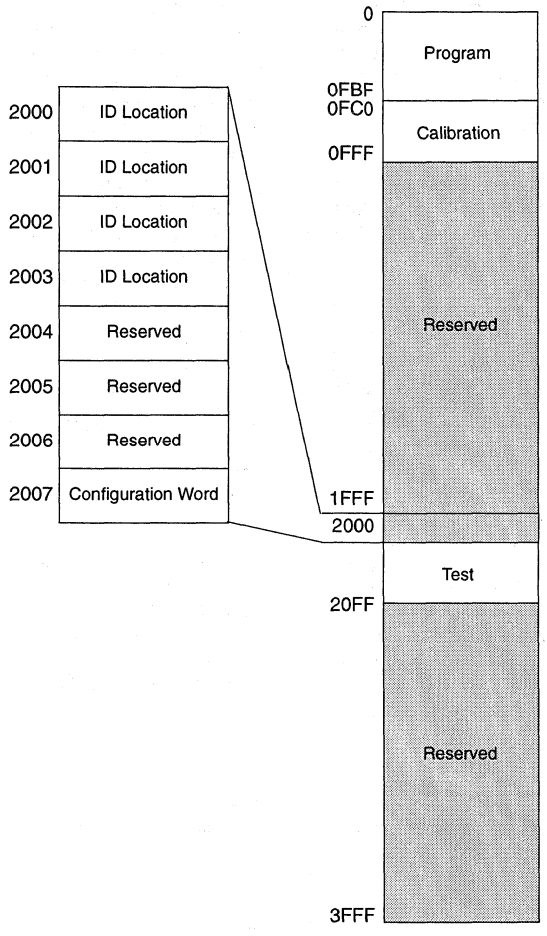
FIGURE 2-1: PROGRAM MEMORY MAPPING



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2.2 Program/Verify Mode

The program/verify mode is entered by holding pins RC6 and RC7 low while raising $\overline{MCLR}$ pin from VIL to VIHH (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. RC6 and RC7 are both Schmitt Trigger inputs in this mode.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the $\overline{MCLR}$ pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

Note: The $\overline{MCLR}$ pin should be raised as quickly as possible from VIL to VIHH. This is to ensure that the device does not have the PC incremented while in valid operation range.

2.2.1 PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RC6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSB) of the command being input first. The data on pin RC7 is required to have a minimum setup and hold time (see AC/DC specs) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1µs between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output LSB first. Therefore, during a read operation the LSB will be transmitted onto pin RC7 on the rising edge of the second cycle, and during a load operation the LSB will be latched on the falling edge of the second cycle. A minimum 1µs delay is also specified between consecutive commands.

All commands are transmitted LSB first. Data words are also transmitted LSB first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1µs is required between a command and a data word (or another command).

The commands that are available are listed in Table 2-2.

2.2.1.1 LOAD CONFIGURATION

After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits a "data word" as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking $\overline{MCLR}$ low (VIL).

TABLE 2-2: COMMAND MAPPING

Command	Mapping (MSB ... LSB)						Data
Load Configuration	0	0	0	0	0	0	0, data(14), 0
Load Data	0	0	0	0	1	0	0, data(14), 0
Read Data	0	0	0	1	0	0	0, data(14), 0
Increment Address	0	0	0	1	1	0	
Begin programming	0	0	1	0	0	0	
End Programming	0	0	1	1	1	0	

Note: The CPU clock must be disabled during in-circuit programming (to avoid incrementing the PC).

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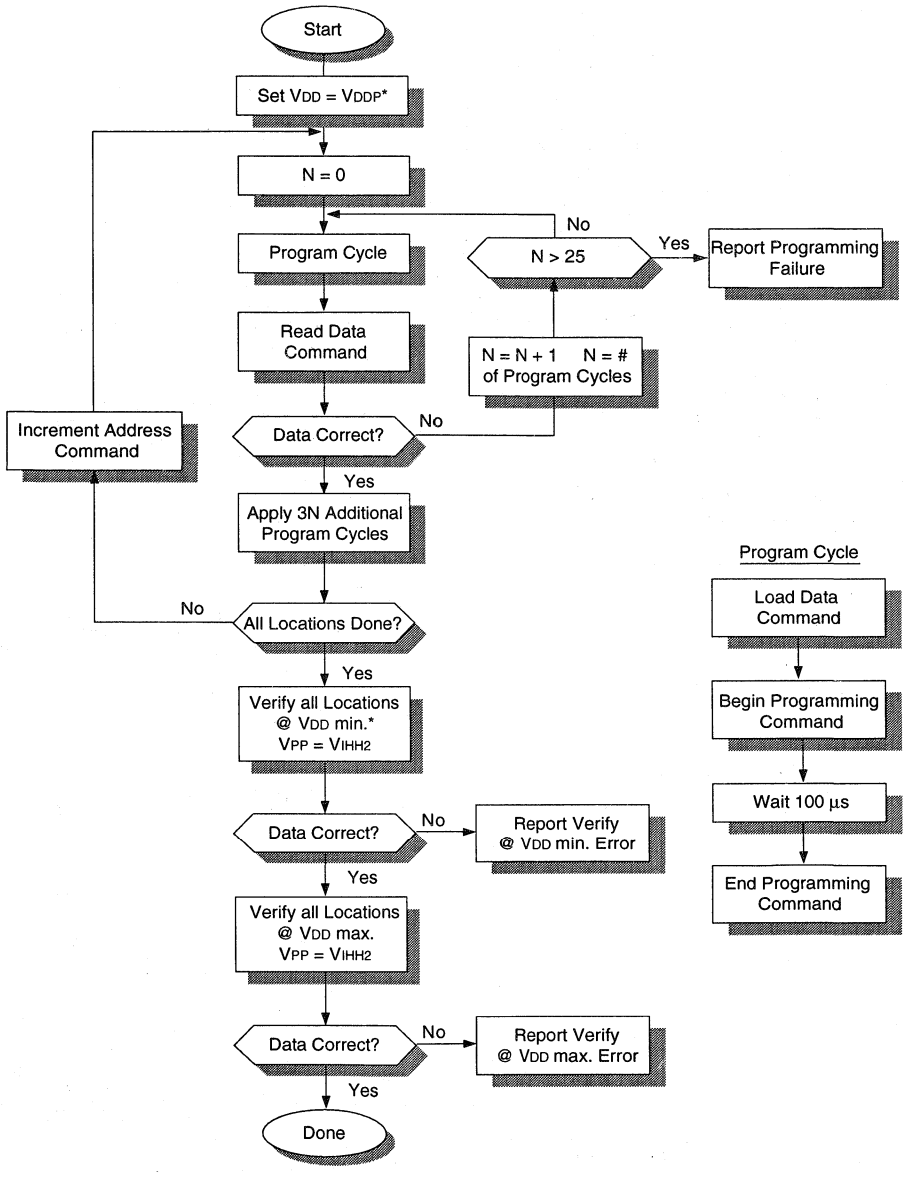
FIGURE 2-2: PROGRAM FLOW CHART - PIC14000 PROGRAM MEMORY AND CALIBRATION



* VDDP = VDD range for programming (typically 4.75V - 5.25V).
VDDmin = Minimum VDD for device operation.
VDDmax = Maximum VDD for device operation.

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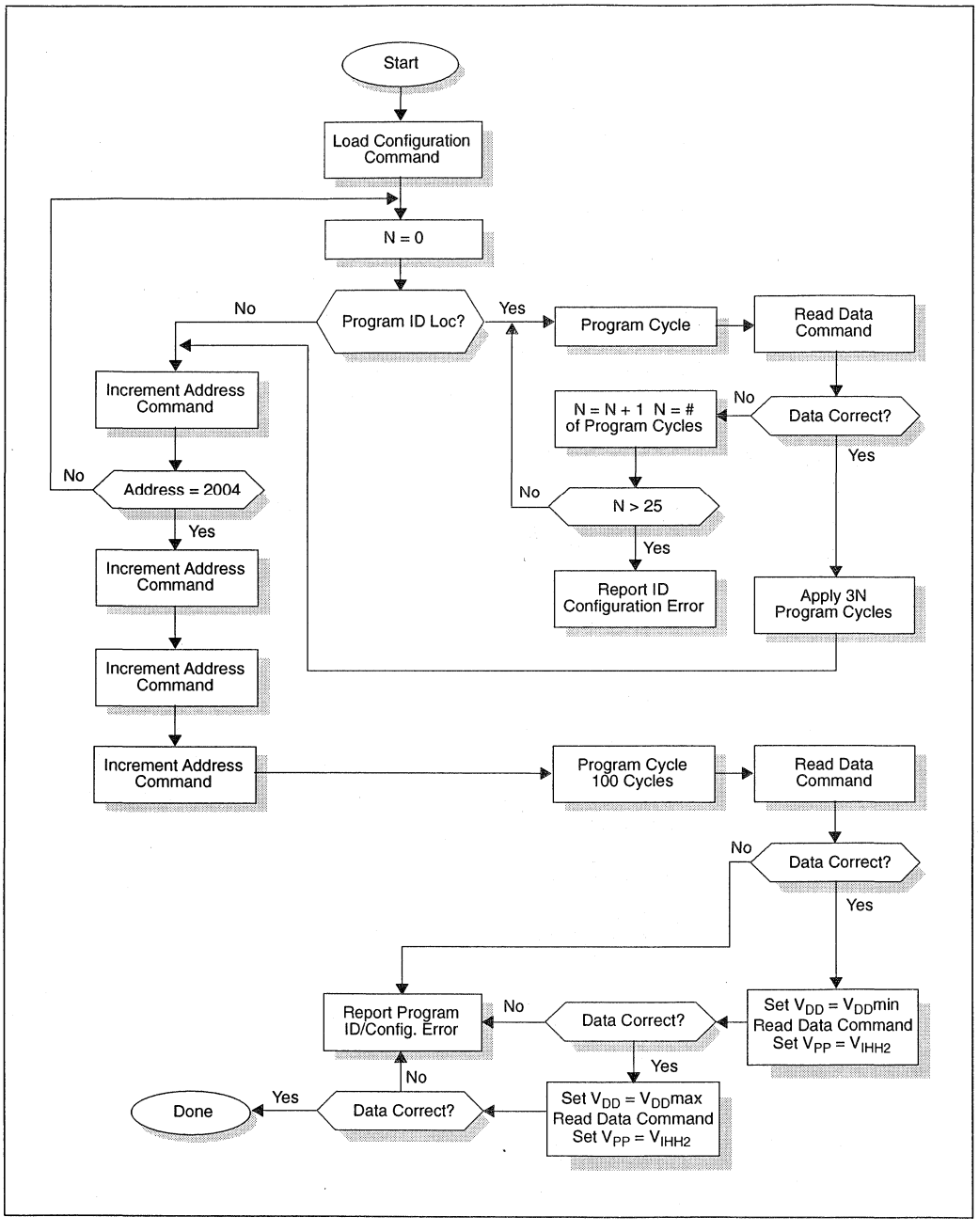
FIGURE 2-3: PROGRAM FLOW CHART - PIC14000 CONFIGURATION WORD & ID LOCATIONS



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2.2.1.2 LOAD DATA

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 5-1.

2.2.1.3 READ DATA

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RC7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.2.1.4 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.2.1.5 BEGIN PROGRAMMING

A load command (load configuration or load data) must be given before every begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100µs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

2.2.1.6 END PROGRAMMING

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

2.3 Programming Algorithm Requires Variable VDD

The PIC14000 uses an intelligent algorithm. The algorithm calls for program verification at VDDmin as well as VDDmax. Verification at VDDmin guarantees good "erase margin". Verification at VDDmax guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (4.75 - 5.25V).

VDDP = VCC range required during programming.

VDDmin = minimum operating VDD spec for the part.

VDDmax = maximum operating VDD spec for the part.

Programmers must verify the PIC14000 at its specified VDDmax and VDDmin levels. Since Microchip may introduce future versions of the PIC14000 with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

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3.0 CONFIGURATION WORD

The PIC14000 has several configuration bits. These bits can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. Figure 3-1 provides an overview of configuration bits.

FIGURE 3-1: CONFIGURATION WORD BIT MAP

Bit Number:	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIC14000	CPC	CPP1	CPP0	CPP0	CPP1	CPC	CPC	F	CPP1	CPP0	$\overline{\text{PWRTE}}$	WDTE	F	FOSC

CPP<1:0>
- 11: All Unprotected
- 10: N/A
- 01: N/A
- 00: All Protected

bit 1,6: **F** Internal trim, factory programmed. DO NOT CHANGE! Program as '1'. Note 1.

bit 3: **$\overline{\text{PWRTE}}$**, Power Up Timer Enable Bit
- 0 = Power up timer enabled
- 1 = Power up timer disabled (unprogrammed)

bit 2: **WDTE**, WDT Enable Bit
- 0 = WDT disabled
- 1 = WDT enabled (unprogrammed)

bit 0: **FOSC<1:0>**, Oscillator Selection Bit
- 0: HS oscillator (crystal/resonator)
- 1: Internal RC oscillator (unprogrammed)

Note 1: See Section 4.1.2 for cautions.

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4.0 CODE PROTECTION

The memory space in the PIC14000 is divided into two areas: program space (0-0xFBF) and calibration space (0xFC0-0xFFF).

For program space or user space, once code protection is enabled, all protected segments read '0's (or "garbage values") and are prevented from further programming. All unprotected segments, including ID locations and configuration word, read normally. These locations can be programmed.

4.1 Calibration Space

The calibration space can contain factory-generated and programmed values. For non-JW devices, the CPC bits in the configuration word are set to '0' at the factory, and the calibration data values are write-protected; they may still be read out, but not programmed. JW devices contain the factory values, but DO NOT have the CPC bits set.

Microchip does not recommend setting code protect bits in windowed devices to '0'. Once code-protected, the device cannot be reprogrammed.

4.1.1 CALIBRATION SPACE CHECKSUM

The data in the calibration space has its own checksum. When properly programmed, the calibration memory will always checksum to 0x0000. When this checksum is 0x0000, and the checksum of memory [0x0000:0xFBF] is 0x2FBF, the part is effectively blank, and the programmer should indicate such.

If the CPC bits are set to '1', but the checksum of the calibration memory is 0x0000, the programmer should NOT program locations in the calibration memory space, even if requested to do so by the operator. This would be the case for a new JW device.

If the CPC bits are set to '1', and the checksum of the calibration memory is NOT 0x0000, the programmer is allowed to program the calibration space as directed by the operator.

The calibration space contains specially coded data values used for device parameter calibration. The programmer may wish to read these values and display them for the operator's convenience. For further information on these values and their coding, refer to AN621 (DS00621B).

4.1.2 REPROGRAMMING CALIBRATION SPACE

The operator should be allowed to read and store the data in the calibration space, for future reprogramming of the device. This procedure is necessary for reprogramming a windowed device, since the calibration data will be erased along with the rest of the memory. When saving this data, Configuration Word <1,6> must also be saved, and restored when the calibration data is reloaded.

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4.2 Embedding Configuration Word and ID Information in the Hex File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, configuration word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 4-1: CODE PROTECT OPTIONS

- Protect calibration memory `0XXXX00XXXXXXX`
- Protect program memory `X0000XXX00XXXX`
- No code protection `1111111X11XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
Protected calibration memory	Read Unscrambled, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

Legend: X = Don't care

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4.3 Checksum

4.3.1 CHECKSUM CALCULATIONS

Checksum is calculated by reading the contents of the PIC14000 memory locations and adding up the opcodes up to the maximum user addressable location, 0xFBF. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for the PIC14000 device is shown in Table 4-2:

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
OFF	SUM[0000:0FBF] + CFGW & 0x3FBD	0x2FFD	0xFBCB
OFF OTP	SUM[0000:0FBF] + CFGW & 0x3FBD	0x0E7D	0xDA4B
ON	CFGW & 0x3FBD + SUM(IDs)	0x300A	0xFBD8

Legend: CFGW = Configuration Word
SUM[A:B] = [Sum of locations a through b inclusive]
SUM(ID) = ID locations masked by 0x7F then made into a 28-bit value with ID0 as the most significant byte
*Checksum = [Sum of all the individual expressions] MODULO [0xFFFF]
+ = Addition
& = Bitwise AND

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5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS
AC/DC Timing Requirements for Program/Verify Mode

Standard Operating Conditions Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (25°C recommended) Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.							
Parameter No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
General							
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	IDDP	Supply current (from VDD) during programming	–	–	20	mA	
PD3	VDDV	Supply voltage during verify	VDDmin		VDDmax	V	Note 1
PD4	VIHH1	Voltage on $\overline{MCLR}$/VPP during programming	12.75	–	13.25	V	Note 2
PD5	VIHH2	Voltage on $\overline{MCLR}$/VPP during verify	VDD + 4.0		13.5		
PD6	IPP	Programming supply current (from VPP)	–	–	50	mA	
PD9	VIH1	(RC6, RC7) input high level	0.8 VDD	–	–	V	Schmitt Trigger input
PD8	VIL1	(RC6, RC7) input low level	0.2 VDD	–	–	V	Schmitt Trigger input
Serial Program Verify							
P1	TR	$\overline{MCLR}$/VPP rise time (VSS to VHH) for test mode entry	–	–	8.0	µs	
P2	Tf	$\overline{MCLR}$ Fall time	–	–	8.0	µs	
P3	Tset1	Data in setup time before clock ↓	100	–	–	ns	
P4	Thld1	Data in hold time after clock ↓	100	–	–	ns	
P5	Tdly1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	–	–	µs	
P6	Tdly2	Delay between clock ↓ to clock ↑ of next command or data	1.0	–	–	µs	
P7	Tdly3	Clock ↑ to date out valid (during read data)	200	–	–	ns	
P8	Thld0	Hold time after $\overline{MCLR}$ ↑	2	–	–	µs	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be greater than VDD + 4.5V to stay in programming/verify mode.

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FIGURE 5-1: LOAD DATA COMMAND (PROGRAM/VERIFY)

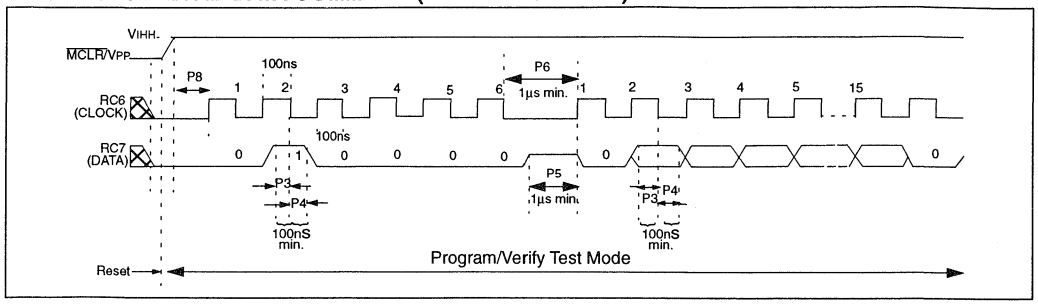


FIGURE 5-2: READ DATA COMMAND (PROGRAM/VERIFY)

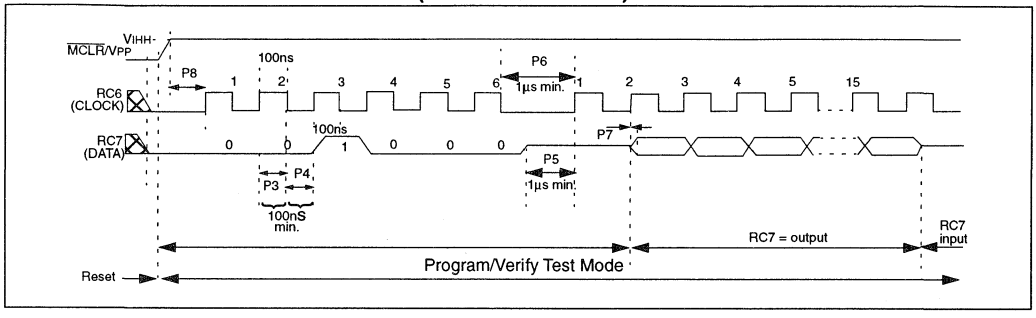
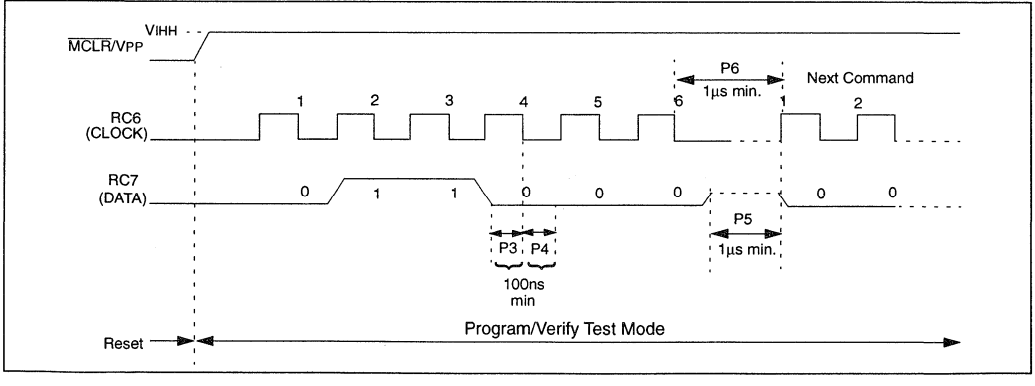


FIGURE 5-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)



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MICROCHIP

PIC16C5X

EPROM/ROM Memory Programming/Verify Specification

This document includes the programming specifications for the following devices:

- PIC16C52
- PIC16C54
- PIC16C54A
- PIC16CR54A
- PIC16C55
- PIC16C56
- PIC16C57
- PIC16CR57B
- PIC16C58A
- PIC16CR58A

INTRODUCTION

Overview

The PIC16C5X Series is a family of single-chip CMOS microcontrollers with on-chip EPROM for program storage. The programming specification also applies to ROM products for verification only.

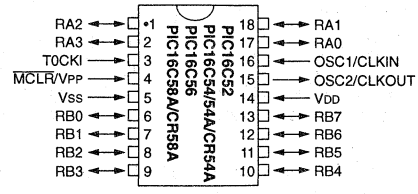
Due to the special architecture of these microcontrollers (12-bit wide instruction word) and the low pin counts (starting at 18 pins), the EPROM programming methodology is different from that of standard (byte-wide) EPROMs (e.g., 27C256).

The PIC16C5X Series can be programmed by applying the 12-bit wide data word to the 12 available I/O pins while the address is generated by the on-chip Program Counter. The $\overline{MCLR}$/VPP pin provides the programming supply voltage (VPP). Programming/verify chip enable is controlled by the T0CKI pin while the OSC1 pin controls the Program Counter.

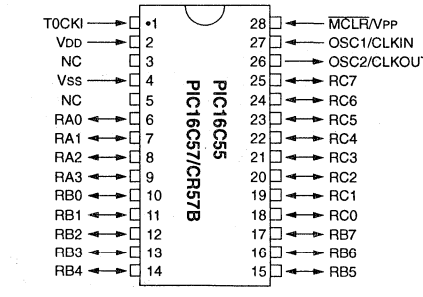
This document describes all the programming details of the PIC16C5X Series and the requirements for programming equipment to be used from programming prototypes in the engineering lab up to high volume programming on the factory floor.

Pin Configurations

PDIP, SOIC, Windowed CERDIP



PDIP, SOIC, Windowed CERDIP



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PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16C52/54/54A/55/56/57/58A

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
T0CKI	$\overline{PROG}$/VER	I	Program pulse input/verify pulse input
RA0 - RA3	D0 - D3	I/O	Data input/output
RB0 - RB7	D4 - D11	I/O	Data input/output
OSC1	INCPC	I	Increment Program Counter input
$\overline{MCLR}$/VPP	VPP	P	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

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1.0 PROGRAM/VERIFY MODES

The PIC16C5X Series uses the internal Program Counter (PC) to generate the EPROM address. VPP is supplied through the $\overline{MCLR}$ pin.

The T0CKI pin acts as chip enable, alternating between programming and verifying.

The OSC1 pin is used for incrementing the PC.

Data is applied to, or can be read on PORTA and PORTB (MSB on RB7, LSB on RA0).

The programming/verify mode is entered by raising the level on the $\overline{MCLR}$ pin from VIL to VHH (= VPP) while the T0CKI pin is held at VIH and the OSC1 pin is held at VIL.

The Program Counter now has the value "0xFFF", because $\overline{MCLR}$ was at VIL before. This condition selects the configuration word as the very first EPROM location to be accessed after entering the program/verify mode.

Since the $\overline{MCLR}$ pin was initially at VIL, the device is in the reset state (the I/O pins are in the reset state).

Incrementing the PC once (by pulsing the OSC1 pin) selects location "0x000" of the user program memory. Afterwards all other memory locations from 001h through end of memory can be addressed by incrementing the PC.

If the Program Counter has reached the last address of the user memory area (e.g. "0x1FF" for the PIC16C54), and is incremented again, the on-chip special EPROM area will be addressed. (See Figure 1-2 to determine where the special EPROM area is located for the various PIC16C5X devices).

1.1 Program/Verify without PC Increment

After entering the program/verify mode, pulsing the T0CKI pin LOW programs the data present on PORTA and PORTB into the memory location selected by the Program Counter. The duration of the T0CKI LOW time determines the length of the programming pulse.

Pulsing the T0CKI pin LOW again without changing the signals on $\overline{MCLR}$ and OSC1 puts the contents of the selected memory location out on PORTA and PORTB for verification of a successful programming cycle. This verification pulse on T0CKI can be much shorter than the programming pulse. If the programming was not successful, T0CKI can be pulsed LOW again to apply another programming pulse, followed again by a shorter T0CKI LOW pulse for another verification cycle.

This sequence can be repeated as many times as required until the programming is successful.

1.2 Verify with PC Increment

If a verification cycle shows that programming was successful, the Program Counter can be incremented by keeping the T0CKI input at a HIGH level while pulsing the OSC1 input HIGH. When both T0CKI and OSC1 are HIGH, the contents of the selected memory location is put out on Ports A and B (= Verify). The falling edge of OSC1 will increment the Program Counter.

A fast VERIFY- ONLY with automatic increment of the PC can be performed by entering the program/verify mode as described above and then clocking the OSC1 input. If OSC1 is HIGH, the selected memory location is output on Ports A and B, while the falling edge of OSC1 will increment the Program Counter. Thus, the first memory location to be verified after entering the program/verify mode, is the configuration word. The next location is 000h followed by 001h and so on. The program memory location "N" can be reached by generating "N + 1" falling edges on OSC1. When OSC1 is brought HIGH again, the contents of address "N" are output on Ports A and B as long as OSC1 stays HIGH.

1.3 Programming/Verifying Configuration Word

The configuration word is logically mapped at program memory location "0xFFF". The PC points to the configuration word after $\overline{MCLR}$ pin goes from LOW to VHH (HIGH). The configuration word can be programmed or verified using the techniques described in Section 1.1 and Section 1.2.

If PC is incremented, the next location it will point to is "0x000" in user memory. Incrementing PC 4096 times will not allow the user to point to the configuration word. The only way to point to it again is to reset and re-enter program mode.

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1.4 Programming Method

The programming technique is described in the following section. It is designed to guarantee good programming margins. It does, however, require a variable power supply for VCC.

1.4.1 PROGRAMMING METHOD DETAILS

Essentially, this technique includes the following steps:

1. Perform blank check at VDD = VDDmin. Report failure. The device may not be properly erased.
2. Program location with pulses and verify after each pulse at VDD = VDDP:
   where VDDP = VDD range required during programming (4.5V - 5.5V).

a) Programming condition:

VPP = 13.0V to 13.25V

VDD = VDDP = 4.5V to 5.5V

VPP must be ≥ VDD + 7.25V to keep "programming mode" active.

b) Verify condition:

VDD = VDDP

VPP ≥ VDD + 7.5V but not to exceed 13.25V

If location fails to program after "N" pulses, (suggested maximum program pulses of 25) then report error as a programming failure.

Note:	Device must be verified at minimum and maximum specified operating voltages as specified in the data sheet.

3. Once location passes "Step 2", apply 3X over-programming, i.e., apply three times the number of pulses that were required to program the location. This will guarantee a solid programming margin. The overprogramming should be made "software programmable" for easy updates.
4. Program all locations.
5. Verify all locations (using speed verify mode) at VDD = VDDmin
6. Verify all locations at VDD = VDDmax

   VDDmin is the minimum operating voltage spec. for the part. VDDmax is the maximum operating voltage spec. for the part.

1.4.2 SYSTEM REQUIREMENTS

Clearly, to implement this technique, the most stringent requirements will be that of the power supplies:

VPP: VPP can be a fixed 13.0V to 13.25V supply. It must not exceed 14.0V to avoid damage to the pin and should be current limited to approximately 100mA.

VDD: 2.0V to 6.5V with 0.25V granularity. Since this method calls for verification at different VDD values, a programmable VDD power supply is needed.

Current Requirement: 40mA maximum

Microchip may release PIC16C5Xs in the future with different VDD ranges which make it necessary to have a programmable VDD.

It is important to verify an EPROM at the voltages specified in this method to remain consistent with Microchip's test screening. For example, a PIC16C5X specified for 4.5V to 5.5V should be tested for proper programming from 4.5V to 5.5V.

Note:	Any programmer not meeting the programmable VDD requirement and the verify at VDDmax and VDDmin requirement may only be classified as "prototype" or "development" programmer but not a production programmer.

1.4.3 SOFTWARE REQUIREMENTS

Certain parameters should be programmable (and therefore easily modified) for easy upgrade.

a) Pulse width

b) Maximum number of pulses, current limit 25.

c) Number of over-programming pulses: should be = (A • N) + B, where N = number of pulses required in regular programming. In our current algorithm A = 3, B = 0.

1.5 Programming Pulse Width

Program Memory Cells: When programming one word of EPROM, a programming pulse width (TPW) of 100µs is recommended.

The maximum number of programming attempts should be limited to 25 per word.

After the first successful verify, the same location should be over-programmed with 3X over-programming.

Configuration Word: The configuration word for oscillator selection, WDT (watchdog timer) disable and code protection, requires a programming pulse width (TPWF) of 10ms. A series of 100µs pulses is preferred over a single 10ms pulse.

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FIGURE 1-1: PROGRAMMING METHOD FLOWCHART

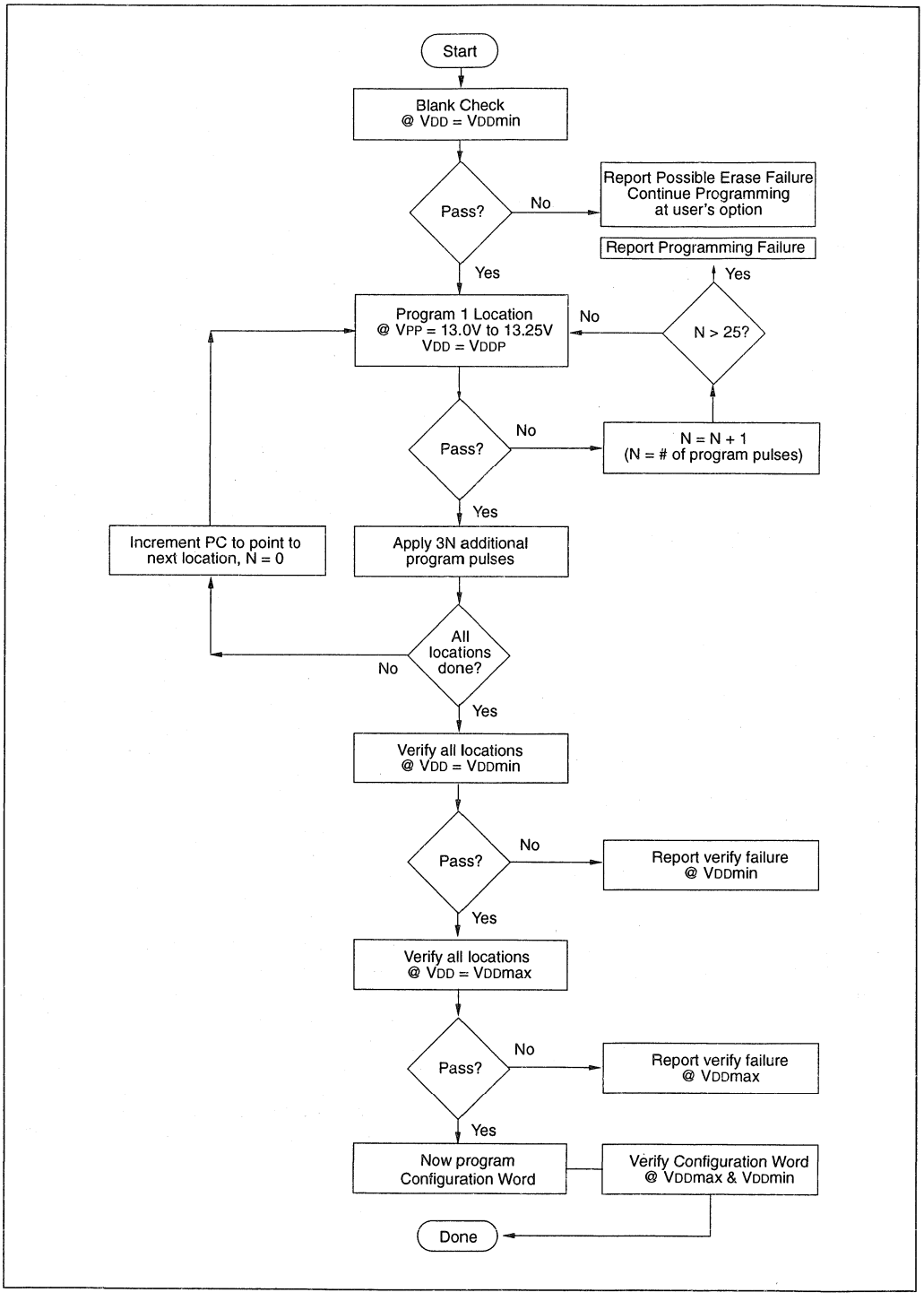

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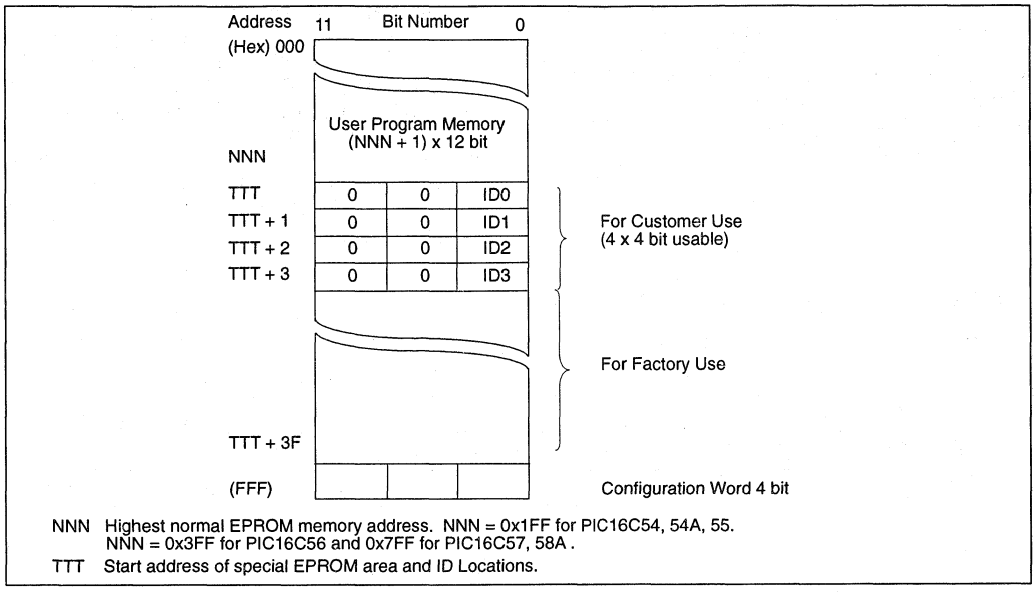
FIGURE 1-2: PIC16C5X SERIES PROGRAM MEMORY MAP IN PROGRAM/VERIFY MODE



NNN Highest normal EPROM memory address. NNN = 0x1FF for PIC16C54, 54A, 55.
NNN = 0x3FF for PIC16C56 and 0x7FF for PIC16C57, 58A.

TTT Start address of special EPROM area and ID Locations.

1.6 Special Memory Locations

The ID Locations area is only enabled if the device is in a test or programming/verify mode. Thus, in normal operation mode only the memory location 0x000 to 0xNNN will be accessed and the Program Counter will just roll over from address 0xNNN to 0x000 when incremented.

The configuration word can only be accessed immediately after $\overline{MCLR}$ going from V_{IL} to V_{HH}. The Program Counter will be set to all '1's upon $\overline{MCLR} = V_{IL}$. Thus, it has the value "0xFFF" when accessing the configuration EPROM. Incrementing the Program Counter once by pulsing OSC1 causes the Program Counter to roll over to all '0's. Incrementing the Program Counter 4K times after reset ($\overline{MCLR} = V_{IL}$) does not allow access to the configuration EPROM.

1.6.1 CUSTOMER ID CODE LOCATIONS

Per definition, the first four words (address TTT to TTT + 3) are reserved for customer use. It is recommended that the customer use only the four lower order bits (bits 0 through 3) of each word and filling the eight higher order bits with '0's.

A user may want to store an identification code (ID) in the ID locations and still be able to read this code after the code protection bit was programmed. This is possible if the ID code is only four bits long per memory location, is located in the least significant nibble boundary of the 12-bit word, and the remaining eight bits are all '0's.

EXAMPLE 1: CUSTOMER CODE 0xD1E2

The Customer ID code "0xD1E2" should be stored in the ID locations 200-203 like this:

```
200:  0000 0000 1101
201:  0000 0000 0001
202:  0000 0000 1110
203:  0000 0000 0010
```

Reading these four memory locations, even with the code protection bit programmed would still output on Port A the bit sequence "1101", "0001", "1110", "0010" which is "0xD1E2".

Note:	Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

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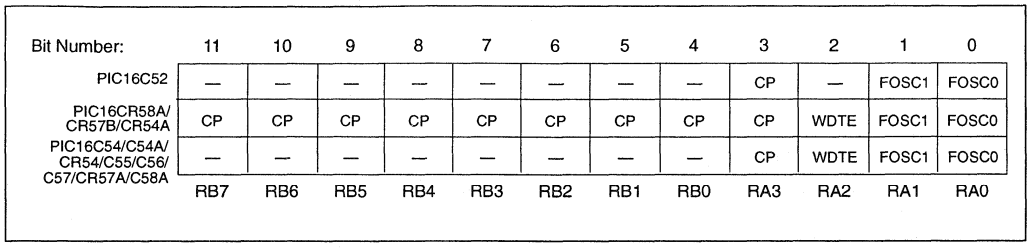
2.0 CONFIGURATION WORD

The configuration word is the very first memory location which is accessed after entering the program/verify mode of the PIC16C5X. It contains the two bits for the selection of the oscillator type, the watchdog timer enable bit, and the code protection bit. All other bits (4 through 11) are read as '1's.

One-Time-Programmable (OTP) devices may have the oscillator configuration bits "FOSC0" and "FOSC1" set by the factory and are tested accordingly. The packages are marked "PIC16C5XHS", "PIC16C5XXT", "PIC16C5XLP", or "PIC16C5XRC". Therefore, it is essential that the inputs RA0 and RA1 are held at '1's when programming the "WDTE" and/or the "CP" bit of the configuration word. Otherwise, the factory tested and selected oscillator configuration could be overwritten and the functionality of the device is not guaranteed any more.

FIGURE 2-1: CONFIGURATION WORD BIT MAP



Bit Number:	11	10	9	8	7	6	5	4	3	2	1	0
PIC16C52	—	—	—	—	—	—	—	—	CP	—	FOSC1	FOSC0
PIC16CR58A/ CR57B/CR54A	CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
PIC16C54/C54A/ CR54/C55/C56/ C57/CR57A/C58A	—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	RA3	RA2	RA1	RA0

TABLE 2-1: CONFIGURATION BIT FUNCTIONALITY (PIC16C54/C55/C56/C57/C54A/C58A/CR57B/CR58A)

RA3-RA11 CP	RA2 WDTE	RA1 FOSC1	RA0 FOSC2	Function	Remarks
1	x	x	x	Memory unprotected	Default
0	x	x	x	Memory protected	
x	1	x	x	Watchdog Timer enabled	Default
x	0	x	x	Watchdog Timer disabled	
x	x	1	1	RC - Oscillator	Default
x	x	1	0	HS - High Speed Crystal	
x	x	0	1	XT - Standard Crystal	
x	x	0	0	LP - Low Frequency Crystal	

Legend: 1= Erased (apply HIGH Level to I/O pin during program)
0 = Written (apply LOW Level to I/O pin during program)
x = Don't Care

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3.0 CODE PROTECTION

The program code written into the EPROM can be protected by writing to the "CP" bit of the configuration word. All memory locations starting at 0x40 and above are protected against programming. It is still possible to program locations 0x00 through 0x3F, the ID locations, and the configuration word.

Note: Locations [0x000 : 0x03F] are not secure after code protection.

3.1 Programming Locations 0x000 to 0x03F after Code Protection

In a code protected part, these locations will program with the exception of the PIC16CRXX devices. They will read back scrambled data, with the exception of PIC16CR54A and PIC16CR58A. In any event, the programmer cannot verify the device once it is code protected.

In code protected parts, specifically PIC16C54/C54A/C55/C56/C57 devices, the contents of the program memory cannot be read out in a way that the program code can be reconstructed. A location when read out will read as: 0000 0000 xxxx where xxxx is the XOR of the three nibbles.

For example, if the memory location contains 0xC04 (movlw 4), after code protection the output will be 0x008.

In addition, all memory locations starting at 0x40 and above are protected against programming. It is still possible to program locations 0x000 through 0x03F and the configuration word. However, performing a verify with activated code protection logic puts a 4-bit wide "checksum" on PORTA while the 8-bits of PORTB are read as '0's. The checksum is computed as follows:

The four high order bits of an instruction word are "XOR'ed" with the four middle and the four low order bits, and the result is transferred to PORTA. All memory locations are affected.

To program location 0x000 to 0x03F in a code protected part, the programmer should program one nibble at a time and verify the result through the XOR'ed output. For example, to program a location with 0xA93, first program the location with 0xFF3, verify checksum to be 0x003; then program the location with 0xF93 and verify the XOR'ed output to be 0x00C and finally program the location with 0xA93 and verify the read-out to be 0x006.

3.2 Embedding Configuration Word and ID Information in the Hex File

To allow portability of code, a PIC16C5X programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, all configuration word and ID information must be included. Configuration word should have the address of 0xFFF. ID locations are mapped at addresses described in Section 1.6.1 and Table 2-2 . An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 3-1: CONFIGURATION WORD

PIC16C52 (CP enable pattern: XXXXXXXX0XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
ID Words [0x200 : 0x203]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
[0x040 : 0x17F]	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
[0x000 : 0x03F]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C54 (CP enable pattern: XXXXXXXX0XXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
ID Words [0x200 : 0x203]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
[0x040 : 0x1FF]	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
[0x000 : 0x03F]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

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PIC16C54A (CP enable pattern: XXXXXXXX0XXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
ID Words [0x200 : 0x203]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
[0x040 : 0x1FF]	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
[0x000 : 0x03F]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16CR54A (CP enable pattern: 000000000XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Unscrambled	Read Unscrambled
ID Words [0x800 : 0x803]	Read Unscrambled	Read Unscrambled
[0x040 : 0x7FF]	Read Disabled	Read Unscrambled
[0x000 : 0x03F]	Read Unscrambled	Read Unscrambled

PIC16C55 (CP enable pattern: XXXXXXXX0XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
ID Words [0x200 : 0x203]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
[0x040 : 0x1FF]	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
[0x000 : 0x03F]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C56 (CP enable pattern: XXXXXXXX0XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
ID Words [0x400 : 0x403]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
[0x040 : 0x3FF]	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
[0x000 : 0x03F]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C57 (CP enable pattern: XXXXXXXX0XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
ID Words [0x800 : 0x803]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
[0x040 : 0x7FF]	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
[0x000 : 0x03F]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16CR57B (CP enable pattern: 000000000XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Unscrambled	Read Unscrambled
ID Words [0x800 : 0x803]	Read Unscrambled	Read Unscrambled
[0x040 : 0x7FF]	Read All 0's	Read Unscrambled
[0x000 : 0x03F]	Read Unscrambled	Read Unscrambled

PIC16C58A (CP enable pattern: XXXXXXXX0XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
ID Words [0x800 : 0x803]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
[0x040 : 0x7FF]	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
[0x000 : 0x03F]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

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PIC16CR58A (CP enable pattern: 000000000XXX)

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFFF)	Read Unscrambled	Read Unscrambled
ID Words [0x800 : 0x803]	Read Unscrambled	Read Unscrambled
[0x040 : 0x7FF]	Read Disabled	Read Unscrambled
[0x000 : 0x03F]	Read Unscrambled	Read Unscrambled

Legend: X = Don't care

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3.3 Checksum

3.3.1 CHECKSUM CALCULATIONS

Checksum is calculated by reading the contents of the PIC16C5X memory locations and adding up the opcodes up to the maximum user addressable location, e.g., 0x1FF for the PIC16C54/55. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16C5X devices is shown in Table 3-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 3-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x723 at 0 and max address
PIC16C52	OFF ON	SUM[0x000:0x17F] + CFGW & 0x00B SUM_XOR4[0x000:0x17F] + CFGW & 0x00B	0xFE8B 0x1683	0xECD3 0x1671
PIC16C54	OFF ON	SUM[0x000:0x1FF] + CFGW & 0x00F + 0x0FF0 SUM_XOR4[0x000:0x1FF] + CFGW & 0x00F	0x0DFF 0x1E07	0xFC47 0x1DF5
PIC16C54A	OFF ON	SUM[0x000:0x1FF] + CFGW & 0xFFF SUM_XOR4[0x000:0x1FF] + CFGW & 0x00F	0x0DFF 0x1E07	0xFC47 0x1DF5
PIC16CR54A	OFF ON	SUM[0x000:0x1FF] + CFGW & 0xFFF SUM[0x00:0x3F] + CFGW & 0xFFF + SUM_1D	0x0DFF 0x0DC6	0xFC47 0xF332
PIC16C55	OFF ON	SUM[0x000:0x1FF] + CFGW & 0x00F + 0x0FF0 SUM_XOR4[0x000:0x1FF] + CFGW & 0x00F	0x0DFF 0x1E07	0xFC47 0x1DF5
PIC16C56	OFF ON	SUM[0x000:0x3FF] + CFGW & 0x00F + 0x0FF0 SUM_XOR4[0x000:0x3FF] + CFGW & 0x00F	0x0BFF 0x3C07	0xFA47 0x3BF5
PIC16C57	OFF ON	SUM[0x000:0x7FF] + CFGW & 0x00F + 0x0FF0 SUM_XOR4[0x000:0x7FF] + CFGW & 0x00F	0x07FF 0x7807	0xF647 0x77F5
PIC16CR57B	OFF ON	SUM[0x000:0x7FF] + CFGW & 0xFFF SUM[0x00x:0x3F] + CFGW & 0xFFF + SUM_ID	0x07FF 0x07C6	0xF647 0xED32
PIC16C58A	OFF ON	SUM[0x000:0x7FF] + CFGW & 0x00F + 0x0FF0 SUM_XOR4[0x000:0x7FF] + CFGW & 0x00F	0x07FF 0x7807	0xF647 0x77F5
PIC16CR58A	OFF ON	SUM[0x000:0x7FF] + CFGW & 0xFFF SUM[0x000:0x3F] + CFGW & 0xFFF + SUM_ID	0x07FF 0x07C6	0xF647 0xED32

Legend: CFGW = Configuration Word
SUM[a:b] = Sum of locations a through b inclusive
SUM_XOR4[a:b] = XOR of the four high order bits with the four middle and the four low of memory location order bits summed over the locations a through b inclusive. For example, location_a = 0x123 and location_b = 0x456, then SUM_XOR [location_a : location_b] = 0x0007.
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nibble. For example, ID0 = 0x1, ID1 = 0x2, ID3 = 0x3, ID4 = 0x4, then SUM_ID = 0x1234.
*Checksum = Sum of all individual expressions **modulo** [0xFFFF]
+ = Addition
& = Bitwise AND

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4.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

4.1 DC Program Characteristics

TABLE 4-1: DC CHARACTERISTICS (TA = +10°C TO +40°C) (25°C IS RECOMMENDED)

Parameter No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	Note 1
PD2	IDDP	Supply Current (from VDD)			25.0	mA	VDD = 5.0V, Fosc1 = 5MHz
PD3	VDDV	Supply Voltage during verify	VDDmin		VDDmax		
PD4	VHH1	Voltage on $\overline{MCLR}$ to stay in Program/Verify Modes	VDD + 3		VDD+7.25	V	
PD5	VHH2	Voltage on $\overline{MCLR}$ during programming	12.5		13.5	V	
PD6	IHH	Supply current from programming voltage source			100	mA	
PD7	IHH2	Current into $\overline{MCLR}$ pin during programming (T0CKI=0)		10.0	25.0	mA	VHH = 13.5V, VDD = 6.0V
PD8	VIL	Input Low Voltage	VSS		0.15VDD	V	
PD9	VIH	Input High Voltage	0.85VDD	5.0	VDD	V	

Note 1: Device must be verified at minimum and maximum operating voltages specified in the data sheet.

4.2 AC Program and Test Mode Characteristics

TABLE 4-2: AC CHARACTERISTICS (TA = +10°C TO +40°C, VDD = 5.0V ± 5%) (25°C IS RECOMMENDED)

Parameter No.	Symbol	Characteristics	Min	Typ	Max	Units	Conditions
P1	TR	$\overline{MCLR}$ Rise Time	0.15	1.0	8	µs	
P2	TF	$\overline{MCLR}$ Fall Time	0.5	2.0	8	µs	
P3	TPS	Program Mode Setup Time	1.0			µs	
P4	TACC	Data Access Time			250	ns	
P5	TDS	Data Setup Time	1.0			µs	
P6	TDH	Data Hold Time	1.0			µs	
P7	TOE	Output Enable Time	0		100	ns	
P8	TOZ	Output Disable Time	0		100	ns	
P9	TPW	Programming Pulse Width	10.0	100		µs	
P10	TPWF	Programming Pulse Width		10,000		µs	Configuration Word only
P11	TRC	Recovery Time	10.0			µs	
P12	FOSC	Frequency on OSC1	DC		5	MHz	For incrementing of the PC

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FIGURE 4-1: PROGRAMMING AND VERIFY TIMING WAVEFORM

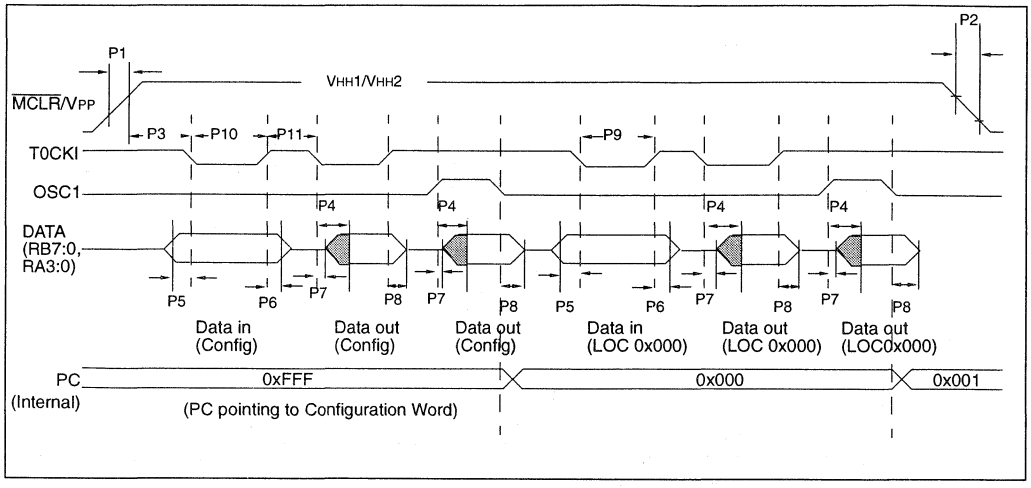
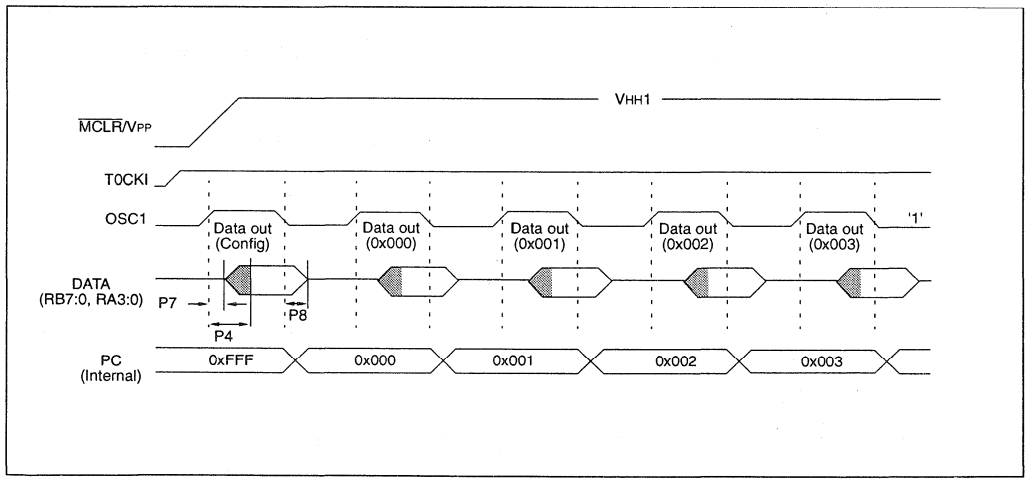


FIGURE 4-2: SPEED VERIFY TIMING WAVEFORM



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PIC16C55X

EPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16C554
- PIC16C556
- PIC16C558

1.0 PROGRAMMING THE PIC16C55X

The PIC16C55X can be programmed using a serial method. In serial mode the PIC16C55X can be programmed while in the users system. This allows for increased design flexibility.

1.1 Hardware Requirements

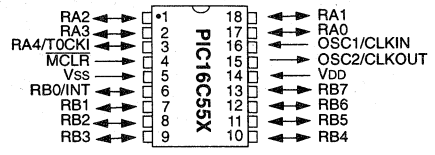
The PIC16C55X requires two programmable power supplies, one for VDD (2.0V to 6.5V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

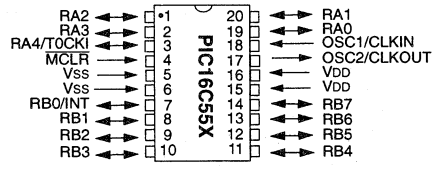
The programming mode for the PIC16C55X allows programming of user program memory, special locations used for ID, and the configuration word for the PIC16C55X.

Pin Diagrams

PDIP, SOIC, Windowed CERDIP



SSOP



Note: Peripheral pinout functions are not shown (see data sheets for full pinout information).

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PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16C554/556/558

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RB6	CLOCK	I	Clock input
RB7	DATA	I/O	Data input/output
MCLR/VPP	VPP	P	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

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2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K). Table 2-1 shows actual implementation of program memory in the PIC16C55X family.

TABLE 2-1: IMPLEMENTATION OF PROGRAM MEMORY IN THE PIC16C55X

Device	Program Memory Size	Access to Program Memory
PIC16C554	0x000 - 0x1FF (0.5K)	PC<8:0>
PIC16C556	0x000 - 0x3FF (1K)	PC<9:0>
PIC16C558	0x000 - 0x7FF (2K)	PC<10:0>

When the PC reaches the last location of the implemented program memory, it will wrap around and address a location within the physically implemented memory (see Figure 2-1).

In programming mode the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x000 or 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode, as described in Section 2.2.

In the configuration memory space, 0x2000-0x20FF are utilized. When in a configuration memory, as in the user memory, the 0x2000-0x2XFF segment is repeatedly accessed as the PC exceeds 0x2XFF (see Figure 2-1).

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000 : 0x2003]. It is recommended that the user use only the four least significant bits of each ID location. In some devices, the ID locations read-out in a scrambled fashion after code protection is enabled. For these devices, it is recommended that ID location is written as "11 1111 1000 bbbb" where 'bbbb' is ID information.

Note: All other locations are reserved and should not be programmed.

In other devices, the ID locations read out normally, even after code protection. To understand how the devices behave, refer to Table 4-1.

To understand the scrambling mechanism after code protection, refer to Section 4.1.

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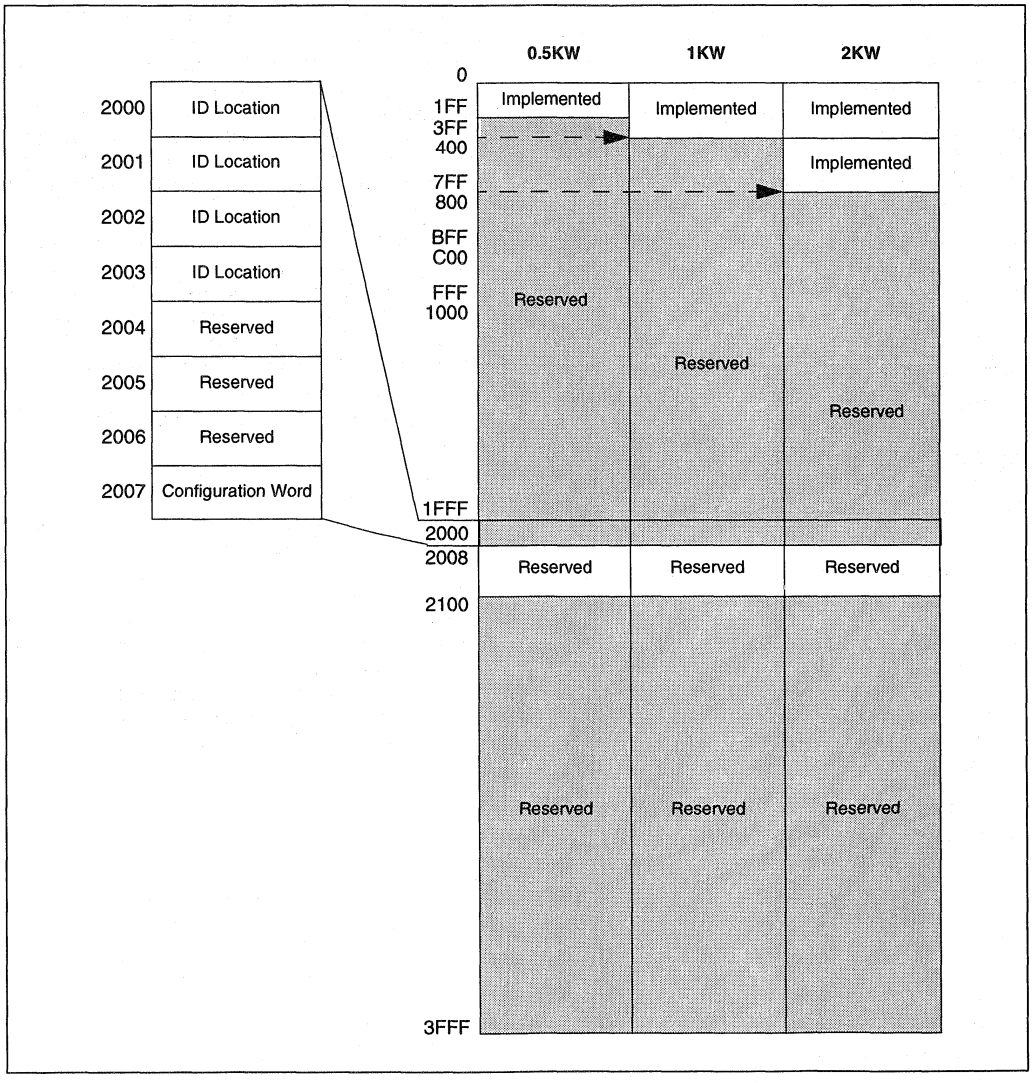
FIGURE 2-1: PROGRAM MEMORY MAPPING



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2.2 Program/Verify Mode

The program/verify mode is entered by holding pins RB6 and RB7 low while raising $\overline{MCLR}$ pin from VIL to VIHH (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. RB6 is a Schmitt Trigger input in this mode.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the $\overline{MCLR}$ pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

Note: The $\overline{MCLR}$ pin should be raised as quickly as possible from VIL to VIHH. this is to ensure that the device does not have the PC incremented while in valid operation range.

2.2.1 PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSB) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specs) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1µs between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output LSB first. Therefore, during a read operation the LSB will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the LSB will be latched on the falling edge of the second cycle. A minimum 1µs delay is also specified between consecutive commands.

All commands are transmitted LSB first. Data words are also transmitted LSB first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1µs is required between a command and a data word (or another command).

The commands that are available are listed in Table 2-2.

2.2.1.1 LOAD CONFIGURATION

After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits a "data word" as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking $\overline{MCLR}$ low (VIL).

TABLE 2-2: COMMAND MAPPING

Command	Mapping (MSB ... LSB)						Data
Load Configuration	0	0	0	0	0	0	0, data(14), 0
Load Data	0	0	0	0	1	0	0, data(14), 0
Read Data	0	0	0	1	0	0	0, data(14), 0
Increment Address	0	0	0	1	1	0	
Begin programming	0	0	1	0	0	0	
End Programming	0	0	1	1	1	0	

Note: The CPU clock must be disabled during in-circuit programming.

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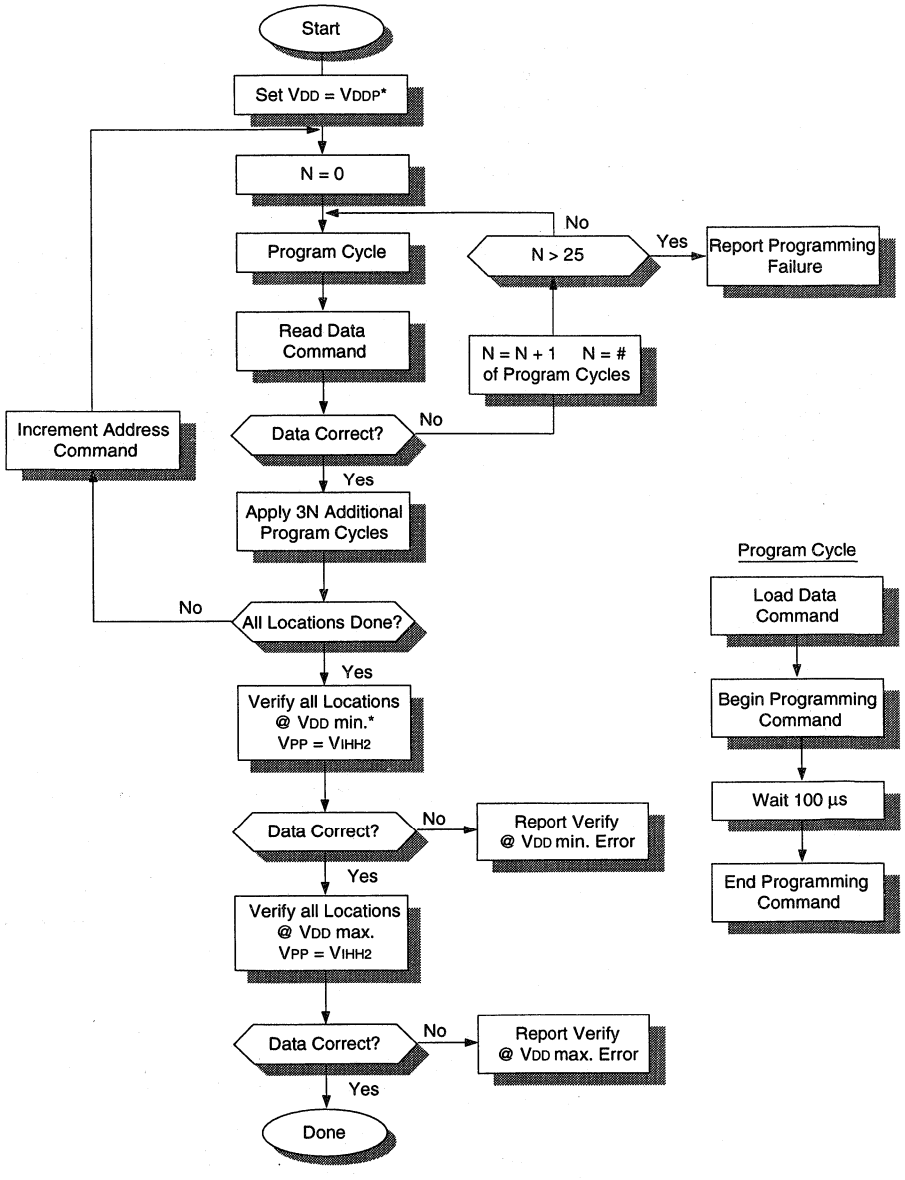
FIGURE 2-2: PROGRAM FLOW CHART - PIC16C55X PROGRAM MEMORY



* VDDP = VDD range for programming (typically 4.75V - 5.25V).
VDDmin = Minimum VDD for device operation.
VDDmax = Maximum VDD for device operation.

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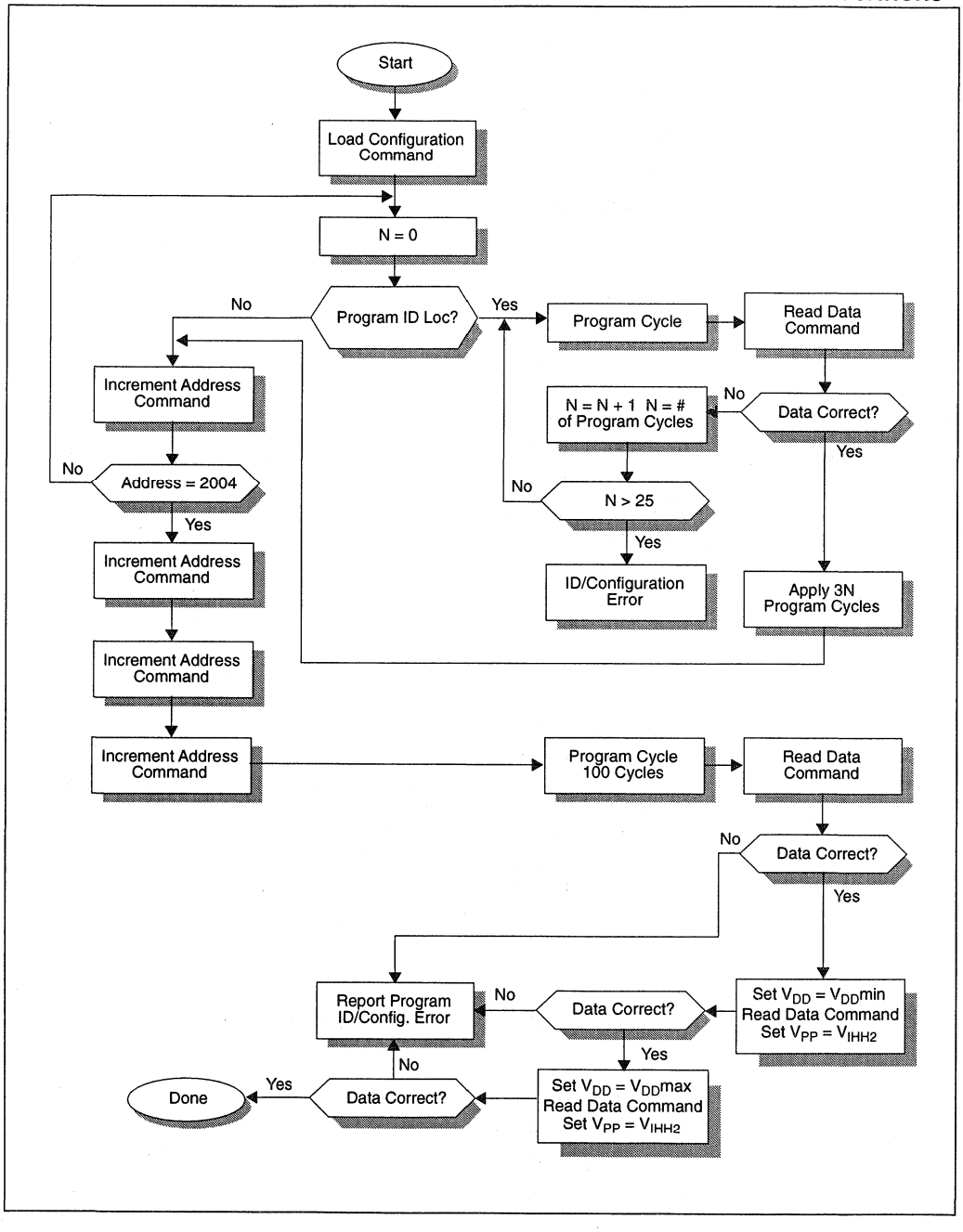
FIGURE 2-3: PROGRAM FLOW CHART - PIC16C55X CONFIGURATION WORD & ID LOCATIONS



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2.2.1.2 LOAD DATA

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 5-1.

2.2.1.3 READ DATA

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.2.1.4 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.2.1.5 BEGIN PROGRAMMING

A load command (load configuration or load data) must be given before every begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100μs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

2.2.1.6 END PROGRAMMING

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

2.3 Programming Algorithm Requires Variable VDD

The PIC16C55X uses an intelligent algorithm. The algorithm calls for program verification at VDDmin as well as VDDmax. Verification at VDDmin guarantees good "erase margin". Verification at VDDmax guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (4.75 - 5.25V).

VDDP = VCC range required during programming.

VDD min. = minimum operating VDD spec for the part.

VDD max.= maximum operating VDD spec for the part.

Programmers must verify the PIC16C55X at its specified VDDmax and VDDmin levels. Since Microchip may introduce future versions of the PIC16C55X with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

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3.0 CONFIGURATION WORD

The PIC16C55X family members have several configuration bits. These bits can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. Figure 3-1 provides an overview of configuration bits.

FIGURE 3-1: CONFIGURATION WORD BIT MAP

Bit Number:	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIC16C554/556/558	CP1	CP0	CP1	CP0	CP1	CP0	—	—	CP1	CP0	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0

bit 6-7:**Reserved for future use**

bit 5-4: **CP1:CP0**, Code Protect

bit 8-13

Device	CP1	CP0	Code Protection
PIC16C554	0	0	All memory protected
	0	1	Do not use
	1	0	Do not use
	1	1	Code protection off
PIC16C556	0	0	All memory protected
	0	1	Upper 1/2 memory protected
	1	0	Do not use
	1	1	Code protection off
PIC16C558	0	0	All memory protected
	0	1	Upper 3/4 memory protected
	1	0	Upper 1/2 memory protected
	1	1	Code protection off

bit 3: **$\overline{\text{PWRTE}}$**, Power Up Timer Enable Bit
PIC16C554/556/558:
0 = Power up timer enabled
1 = Power up timer disabled

bit 2: **WDTE**, WDT Enable Bit
1 = WDT enabled
0 = WDT disabled

bit 1-0:**FOSC<1:0>**, Oscillator Selection Bit
11: RC oscillator
10: HS oscillator
01: XT oscillator
00: LP oscillator

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4.0 CODE PROTECTION

The program code written into the EPROM can be protected by writing to the CP0 & CP1 bits of the configuration word.

4.1 Programming Locations 0x0000 to 0x03F after Code Protection

For PIC16C55X devices, once code protection is enabled, all protected segments read '0's (or "garbage values") and are prevented from further programming. All unprotected segments, including ID locations and configuration word, read normally. These locations can be programmed.

4.2 Embedding Configuration Word and ID Information in the Hex File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, configuration word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 4-1: CONFIGURATION WORD

PIC16C554

To code protect:

- Protect all memory `0000001X00XXXX`
- No code protection `1111111X11XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C556

To code protect:

- Protect all memory `0000001X00XXXX`
- Protect upper 1/2 memory `0101011X01XXXX`
- No code protection `1111111X11XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C558

To code protect:

- Protect all memory `0000001X00XXXX`
- Protect upper 3/4 memory `0101011X01XXXX`
- Protect upper 1/2 memory `1010101X10XXXX`
- No code protection `1111111X11XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

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4.3 Checksum

4.3.1 CHECKSUM CALCULATIONS

Checksum is calculated by reading the contents of the PIC16C55X memory locations and adding up the opcodes up to the maximum user addressable location, e.g., 0x1FF for the PIC16C74. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16C55X devices is shown in Table 4-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
PIC16C554	OFF	SUM[0x000:0x1FF] + CFGW & 0x3F3F	3D3F	090D
	ALL	SUM_ID + CFGW & 0x3F3F	3D4E	091C
PIC16C556	OFF	SUM[0x000:0x3FF] + CFGW & 0x3F3F	3B3F	070D
	1/2	SUM[0x000:0x1FF] + CFGW & 0x3F3F + SUM_ID	4E5E	0013
	ALL	CFGW & 0x3F3F + SUM_ID	3B4E	071C
PIC16C558	OFF	SUM[0x000:0x7FF] + CFGW & 0x3F3F	373F	030D
	1/2	SUM[0x000:0x3FF] + CFGW & 0x3F3F + SUM_ID	5D6E	0F23
	3/4	SUM[0x000:0x1FF] + CFGW & 0x3F3F + SUM_ID	4A5E	FC13
	ALL	CFGW & 0x3F3F + SUM_ID	374E	031C

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a through b inclusive]
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nibble.
For example,
ID0 = 0x12, ID1 = 0x37, ID2 = 0x4, ID3 = 0x26, then SUM_ID = 0x2746.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

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5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (25°C is recommended) Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.							
Parameter No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
General							
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	IDDP	Supply current (from VDD) during programming			20	mA	
PD3	VDDV	Supply voltage during verify	VDDmin		VDDmax	V	Note 1
PD4	VIHH1	Voltage on $\overline{MCLR}$/VPP during programming	12.75		13.25	V	Note 2
PD5	VIHH2	Voltage on $\overline{MCLR}$/VPP during verify	VDD + 4.0		13.5		
PD6	IPP	Programming supply current (from VPP)			50	mA	
PD9	VIH1	(RB6, RB7) input high level	0.8 VDD			V	Schmitt Trigger input
PD8	VIL1	(RB6, RB7) input low level	0.2 VDD			V	Schmitt Trigger input
Serial Program Verify							
P1	TR	$\overline{MCLR}$/VPP rise time (VSS to VHH) for test mode entry			8.0	µs	
P2	Tf	$\overline{MCLR}$ Fall time			8.0	µs	
P3	Tset1	Data in setup time before clock ↓	100			ns	
P4	Thld1	Data in hold time after clock ↓	100			ns	
P5	Tdly1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0			µs	
P6	Tdly2	Delay between clock ↓ to clock ↑ of next command or data	1.0			µs	
P7	Tdly3	Clock ↑ to date out valid (during read data)	200			ns	
P8	Thld0	Hold time after $\overline{MCLR}$ ↑	2			µs	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be greater than VDD + 4.5V to stay in programming/verify mode.

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FIGURE 5-1: LOAD DATA COMMAND (PROGRAM/VERIFY)

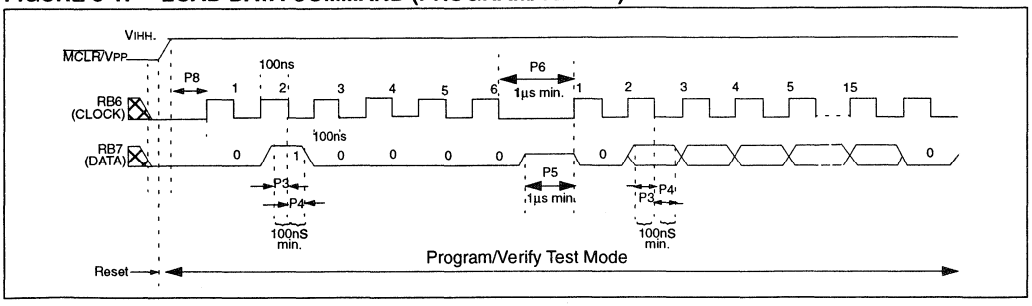


FIGURE 5-2: READ DATA COMMAND (PROGRAM/VERIFY)

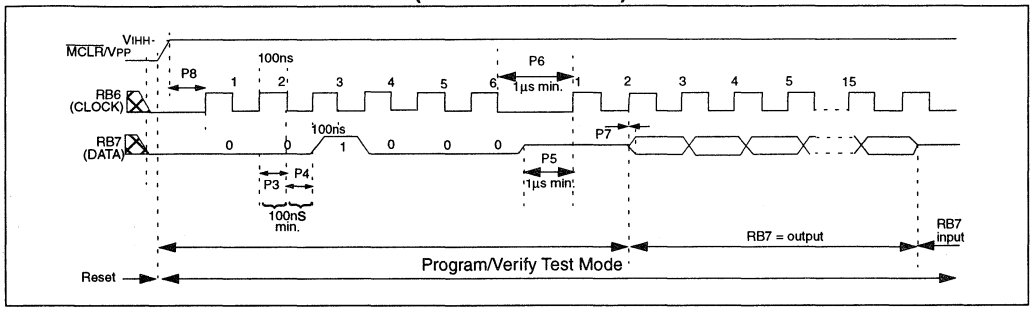
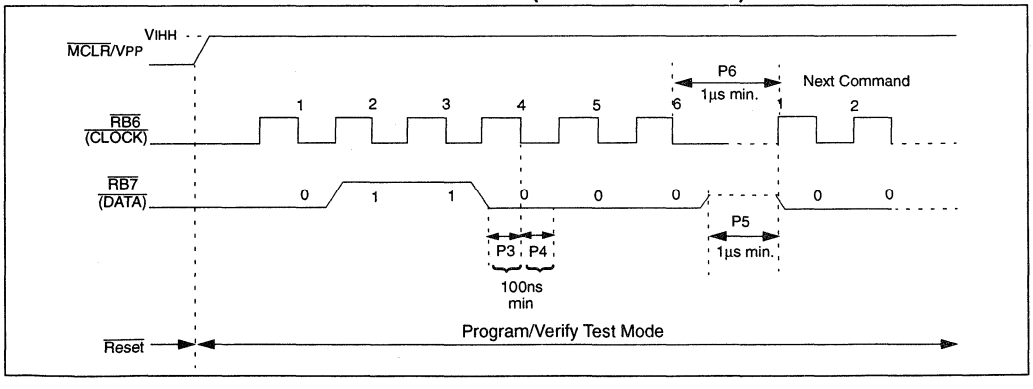


FIGURE 5-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)



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PIC16C6X/7X/9XX

EPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16C61
- PIC16C62
- PIC16C62A
- PIC16C63
- PIC16C64
- PIC16C64A
- PIC16C65
- PIC16C65A
- PIC16C71
- PIC16C710
- PIC16C711
- PIC16C72
- PIC16C73
- PIC16C73A
- PIC16C74
- PIC16C74A
- PIC16C620
- PIC16C621
- PIC16C622
- PIC16C923
- PIC16C924

1.0 PROGRAMMING THE PIC16C6X/7X/9XX

The PIC16C6X/7X/9XX can be programmed using a serial method. In serial mode the PIC16C6X/7X/9XX can be programmed while in the users system. This allows for increased design flexibility. This programming specification applies to PIC16C6X/7X/9XX devices in all packages.

1.1 Hardware Requirements

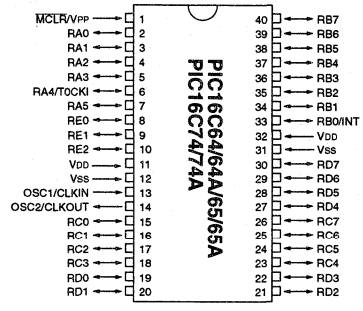
The PIC16C6X/7X/9XX requires two programmable power supplies, one for VDD (2.0V to 6.5V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

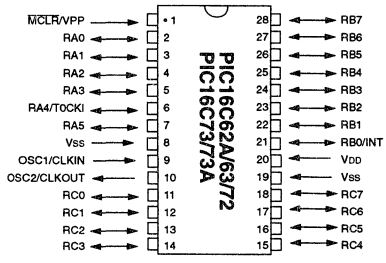
The programming mode for the PIC16C6X/7X/9XX allows programming of user program memory, special locations used for ID, and the configuration word for the PIC16C6X/7X/9XX.

Pin Diagrams

PDIP, Windowed CERDIP



PDIP, SOIC, Windowed CERDIP (300 mil)



Note: Peripheral pinout functions are not shown (see data sheets for full pinout information).

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PIN DESCRIPTIONS (DURING PROGRAMMING):
PIC16C61/620/621/622/62/62A/63/64/64A/65/65A/71/73/73A/74/74A/710/711/923/924

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RB6	CLOCK	I	Clock input
RB7	DATA	I/O	Data input/output
MCLR/VPP	VPP	P	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = input, O = Output, P = Power

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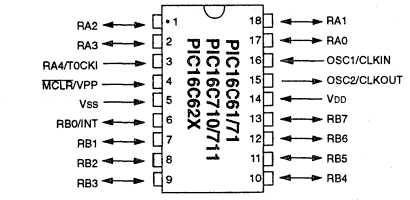
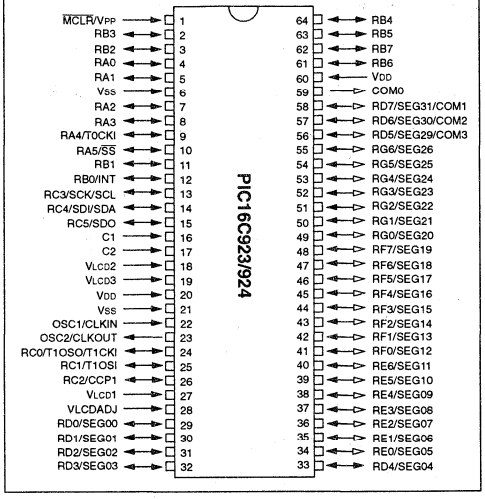
Pin Diagrams (Con't)

PDIP, SOIC, Windowed CERDIP



Shrink PDIP (750 mil)



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2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K). Table 2-1 shows actual implementation of program memory in the PIC16C6X/7X/9XX family.

TABLE 2-1: IMPLEMENTATION OF PROGRAM MEMORY IN THE PIC16C6X/7X/9XX

Device	Program Memory Size	Access to Program Memory
PIC16C61	0x000-0x3FF (1K)	PC<9:0>
PIC16C620	0x000 -0x1FF (0.5K)	PC<8:0>
PIC16C621	0x000 - 0x3FF (1K)	PC<9:0>
PIC16C622	0x000 -0x7FF (2K)	PC<10:0>
PIC16C62/62A	0x000 - 0x7FF (2K)	PC <10:0>
PIC16C63	0x000 - 0xFFF (4K)	PC<11:0>
PIC16C64/64A	0x000 - 0x7FF (2K)	PC<10:0>
PIC16C65	0x000 - 0xFFF (4K)	PC<11:0>
PIC16C71	0x000 - 0x3FF (1K)	PC<9:0>
PIC16C710	0x000 - 0x1FF (0.5K)	PC<8:0>
PIC16C711	0x000 - 0x3FF (1K)	PC<9:0>
PIC16C72	0x000 - 0x7FF (2K)	PC<10:0>
PIC16C73/73A	0x000 - 0xFFF (4K)	PC<11:0>
PIC16C74/74A	0x000 - 0xFFF (4K)	PC<11:0>
PIC16C923/924	0x000 - 0xFFF (4K)	PC<11:0>

When the PC reaches the last location of the implemented program memory, it will wrap around and address a location within the physically implemented memory (see Figure 2-1).

In programming mode the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x000 or 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode, as described in Section 2.2.

In the configuration memory space, 0x2000-0x207F or 0x2000-0x20FF are utilized. When in a configuration memory, as in the user memory, the 0x2000-0x2XFF segment is repeatedly accessed as PC exceeds 0x2XFF (see Figure 2-1).

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000 : 0x2003]. It is recommended that the user use only the four least significant bits of each ID location. In some devices, the ID locations read-out in a scrambled fashion after code protection is enabled. For these devices, it is recommended that ID location is written as "11 1111 1000 bbbb" where 'bbbb' is ID information.

Note: All other locations are reserved and should not be programmed.

In other devices, the ID locations read out normally, even after code protection. To understand how the devices behave, refer to Table 4-1.

To understand the scrambling mechanism after code protection, refer to Section 4.1.

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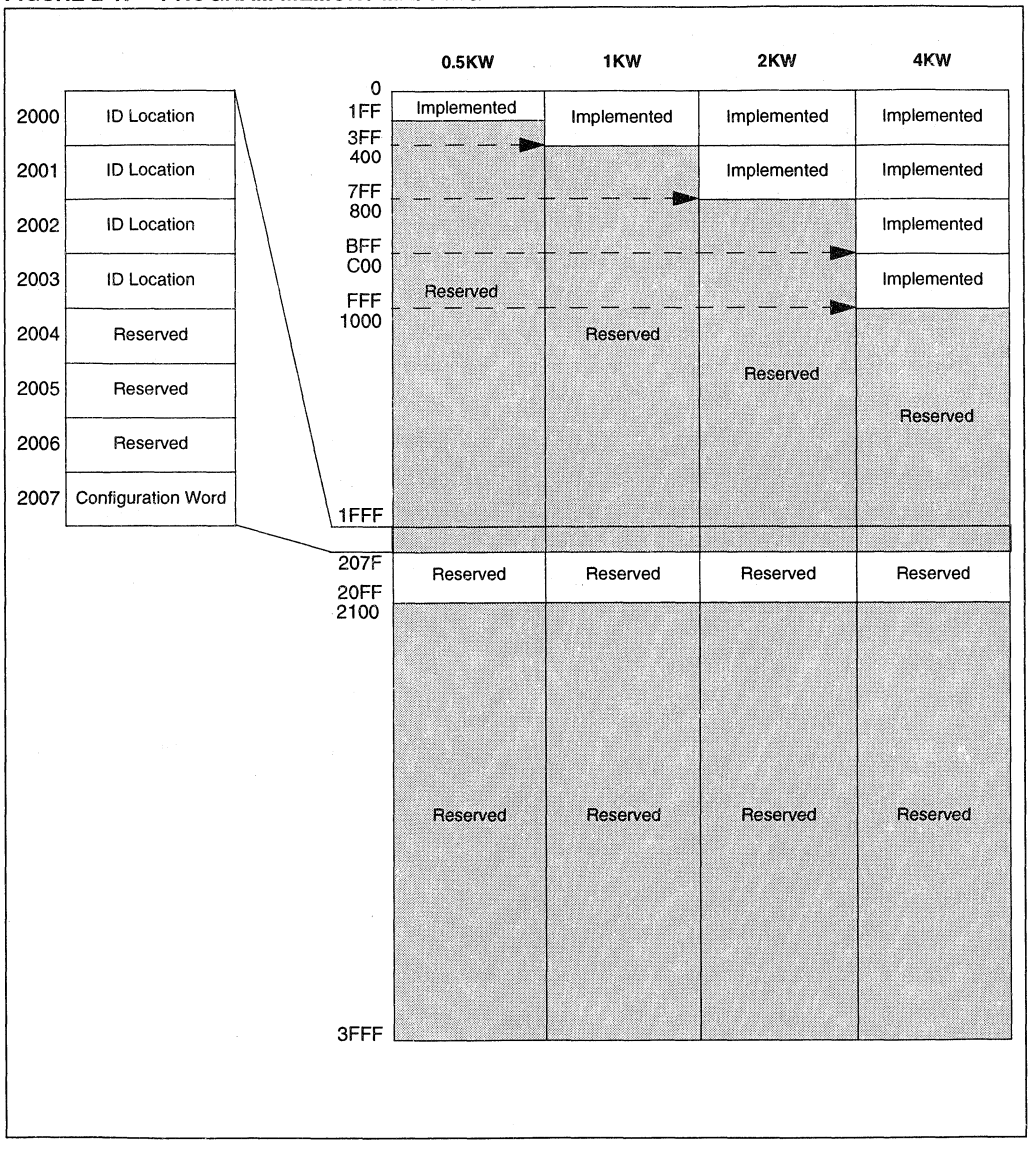
FIGURE 2-1: PROGRAM MEMORY MAPPING



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2.2 Program/Verify Mode

The program/verify mode is entered by holding pins RB6 and RB7 low while raising $\overline{MCLR}$ pin from VIL to VIHH (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. RB6 is a Schmitt Trigger input in this mode.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the MCLR pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

Note: The $\overline{MCLR}$ pin should be raised as quickly as possible from VIL to VIHH. this is to ensure that the device does not have the PC incremented while in valid operation range.

2.2.1 PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSB) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specs) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1µs between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output LSB first. Therefore, during a read operation the LSB will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the LSB will be latched on the falling edge of the second cycle. A minimum 1µs delay is also specified between consecutive commands.

All commands are transmitted LSB first. Data words are also transmitted LSB first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1µs is required between a command and a data word (or another command).

The commands that are available are listed in Table 2-2.

2.2.1.1 LOAD CONFIGURATION

After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits a "data word" as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking $\overline{MCLR}$ low (VIL).

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TABLE 2-2: COMMAND MAPPING

Command	Mapping (MSB ... LSB)						Data
Load Configuration	0	0	0	0	0	0	0, data(14), 0
Load Data	0	0	0	0	1	0	0, data(14), 0
Read Data	0	0	0	1	0	0	0, data(14), 0
Increment Address	0	0	0	1	1	0	
Begin programming	0	0	1	0	0	0	
End Programming	0	0	1	1	1	0	

Note: The clock must be disabled during in-circuit programming.

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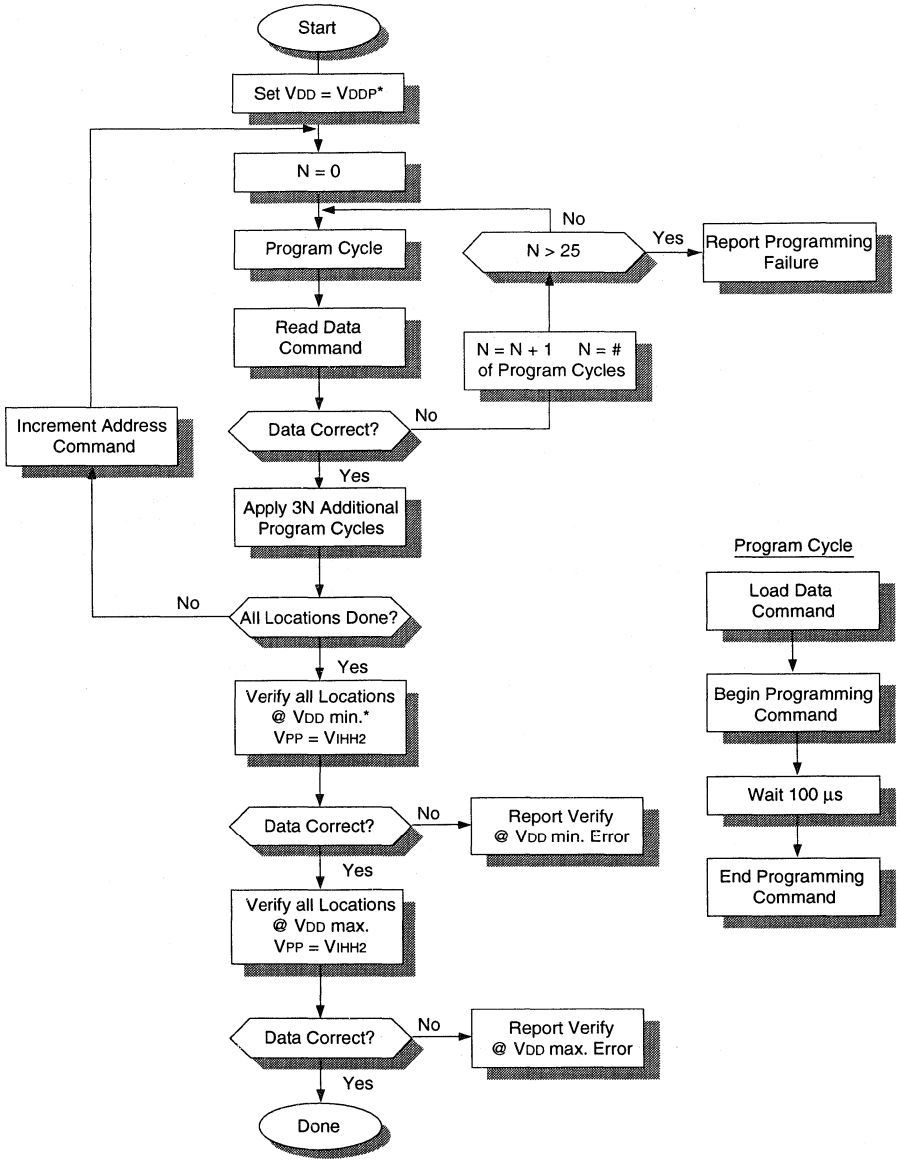
FIGURE 2-2: PROGRAM FLOW CHART - PIC16C6X/7X/9XX PROGRAM MEMORY



* VDDP = VDD range for programming (typically 4.75V - 5.25V).
VDDmin = Minimum VDD for device operation.
VDDmax = Maximum VDD for device operation.

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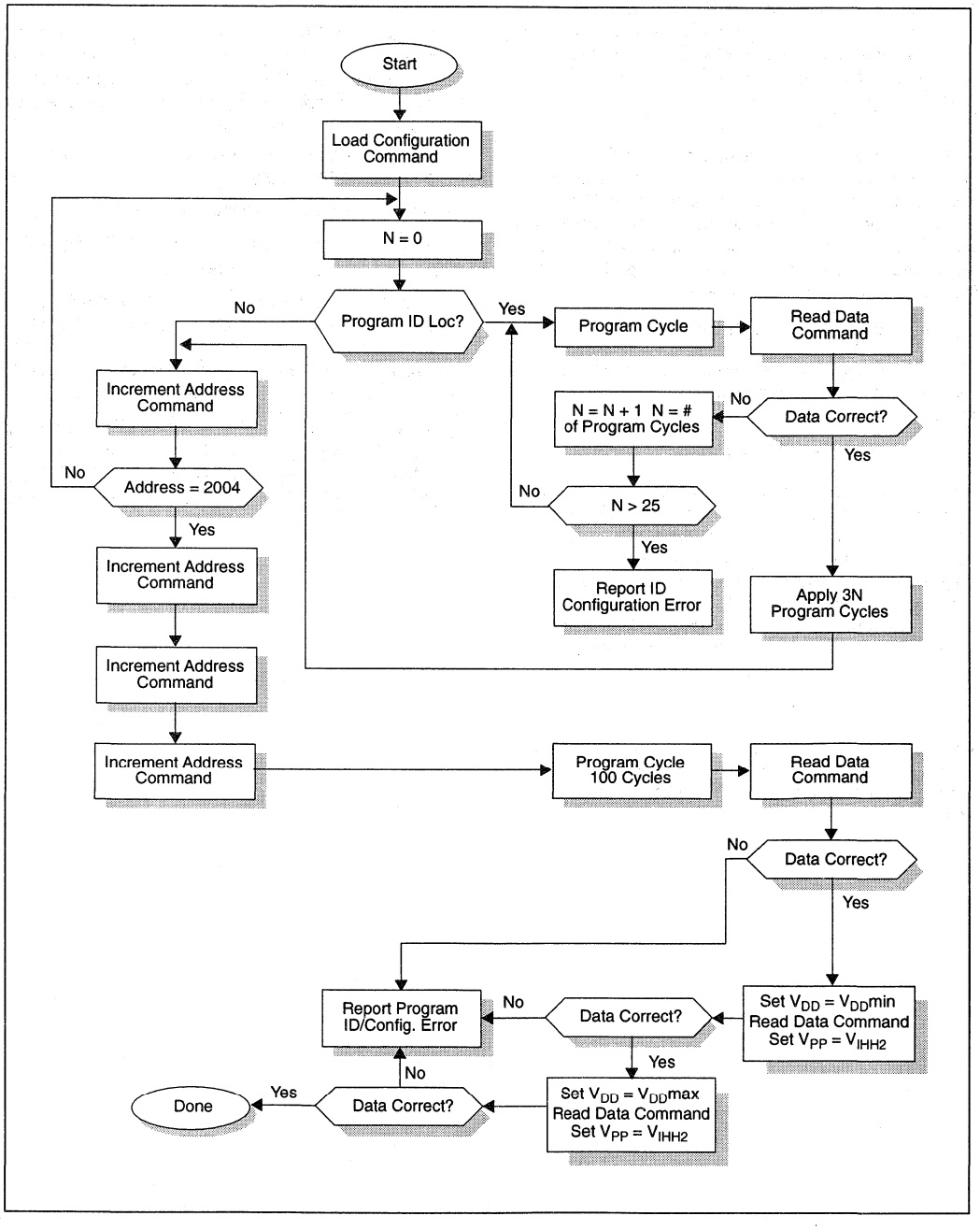
FIGURE 2-3: PROGRAM FLOW CHART - PIC16C6X/7X/9XX CONFIGURATION WORD & ID LOCATIONS



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2.2.1.2 LOAD DATA

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 5-1.

2.2.1.3 READ DATA

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.2.1.4 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.2.1.5 BEGIN PROGRAMMING

A load command (load configuration or load data) must be given before every begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100μs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

2.2.1.6 END PROGRAMMING

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

2.3 Programming Algorithm Requires Variable VDD

The PIC16C6X/7X/9XX uses an intelligent algorithm. The algorithm calls for program verification at VDDmin as well as VDDmax. Verification at VDDmin guarantees good "erase margin". Verification at VDDmax guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (4.75 - 5.25V).

VDDP = VCC range required during programming.

VDD min. = minimum operating VDD spec for the part.

VDDmax = maximum operating VDD spec for the part.

Programmers must verify the PIC16C6X/7X/9XX at its specified VDDmax and VDDmin levels. Since Microchip may introduce future versions of the PIC16C6X/7X/9XX with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

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3.0 CONFIGURATION WORD

The PIC16C6X/7X/9XX family members have several configuration bits. These bits can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. Figure 3-1 provides an overview of configuration bits.

FIGURE 3-1: CONFIGURATION WORD BIT MAP

Bit Number:	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIC16C61/71	—	—	—	—	—	—	—	—	—	CP0	PWRTE	WDTE	FOSC1	FOSC0
PIC16C62/64/65/73/74	—	—	—	—	—	—	—	0	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
PIC16C710/711	CP0	CP0	CP0	CP0	CP0	CP0	CP0	BODEN	CP0	CP0	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
PIC16C62A/CR62/63/64A/CR64/65A/72/73A/74A/620/621/622	CP1	CP0	CP1	CP0	CP1	CP0	—	BODEN	CP1	CP0	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
PIC16C9XX	CP1	CP0	CP1	CP0	CP1	CP0	—	—	CP1	CP0	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0

bit 6: **Reserved**, '–' write as '1' for PIC16C6X/7X/9XX

bit 5-4: **CP1:CP0**, Code Protect

Device	CP1	CP0	Code Protection
PIC16C62/62A/63 PIC16C64/64A	0	0	All memory protected
PIC16C65/65A PIC16C72 PIC16C73/73A	0	1	Upper 3/4 memory protected
PIC16C74/74A PIC16C9XX	1	0	Upper 1/2 memory protected
	1	1	Code protection off
PIC16C61 PIC16C71 PIC16C710 PIC16C711	—	0	On
	—	1	Off
	0	0	All memory protected
PIC16C620	0	1	Do not use
	1	0	Do not use
	1	1	Code protection off
PIC16C621	0	0	All memory protected
	0	1	Upper 1/2 memory protected
	1	0	Do not use
	1	1	Code protection off
PIC16C622	0	0	All memory protected
	0	1	Upper 3/4 memory protected
	1	0	Upper 1/2 memory protected
	1	1	Code protection off

bit 6: **BODEN**, Brown Out Enable Bit

bit 4: **$\overline{\text{PWRTE}}$/PWRTE**, Power Up Timer Enable Bit
PIC16C61/62/64/65/71/73/74:
1 = Power up timer enabled
0 = Power up timer disabled
PIC16C620/621/622/62A/63/65A/72/73A/74A:
0 = Power up timer enabled
1 = Power up timer disabled

bit 3-2: **WDTE**, WDT Enable Bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC<1:0>**, Oscillator Selection Bit
11: RC oscillator
10: HS oscillator
01: XT oscillator
00: LP oscillator

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4.0 CODE PROTECTION

The program code written into the EPROM can be protected by writing to the CP0 & CP1 bits of the configuration word.

In PIC16C61/71 it is still possible to program locations 0x000 through 0x03F, after code protection. For all other devices, writing to all protected memory is disabled.

4.1 Programming Locations 0x0000 to 0x03F after Code Protection

For PIC16C61/71 devices, once code protection is enabled, all program memory locations read out in a scrambled fashion. The ID locations and the configuration word also read out in a scrambled fashion. Further programming is disabled for locations 0x040 and above. It is possible to program the ID locations and the configuration word.

For PIC16C61/71 devices, program memory locations 0x000 through 0x03F are essentially unprotected, i.e., these locations can be further programmed after code protection is enabled. However, since the data reads out in a scrambled fashion, to correctly overprogram these locations, the programmer must program seven bits at a time. For example, to program 0x3AD2 ("11 1010 1101 0010") in a blank location, first program the location with "11 1111 1101 0010" and verify scrambled output to be "xx xxxx x101 0010". Next, program the location with "11 1010 1101 0010" and verify scrambled output to be "xx xxxx x101 1000".

For all other PIC16C6X/7X/9XX devices, once code protection is enabled, all protected segments read '0's (or "garbage values") and are prevented from further programming. All unprotected segments, including ID locations and configuration word, read normally. These locations can be programmed.

4.2 Embedding Configuration Word and ID Information in the Hex File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, configuration word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 4-1: CONFIGURATION WORD

PIC16C61

To code protect:

- Protect all memory `1111111110XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C620

To code protect:

- Protect all memory `0000001X00XXXX`
- No code protection `1111111X11XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

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PIC16C621

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 1/2 memory 0101011X01XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C622

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C62

To code protect:

- Protect all memory 1111111000XXXX
- Protect upper 3/4 memory 1111111001XXXX
- Protect upper 1/2 memory 1111111010XXXX
- No code protection 1111111011XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C62A

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

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PIC16C63

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C64

To code protect:

- Protect all memory 1111111000XXXX
- Protect upper 3/4 memory 1111111001XXXX
- Protect upper 1/2 memory 1111111010XXXX
- No code protection 1111111011XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C64A

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C65

To code protect:

- Protect all memory 1111111000XXXX
- Protect upper 3/4 memory 1111111001XXXX
- Protect upper 1/2 memory 1111111010XXXX
- No code protection 1111111011XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

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PIC16C65A

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C710

To code protect:

- Protect all memory 0000000X00XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C71

To code protect:

- Protect all memory 1111111110XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C711

To code protect:

- Protect all memory 0000000X00XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C72

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

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PIC16C73

To code protect:

- Protect all memory 1111111000XXXX
- Protect upper 3/4 memory 1111111001XXXX
- Protect upper 1/2 memory 1111111010XXXX
- No code protection 1111111011XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C73A

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C74

To code protect:

- Protect all memory 1111111000XXXX
- Protect upper 3/4 memory 1111111001XXXX
- Protect upper 1/2 memory 1111111010XXXX
- No code protection 1111111011XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C74A

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

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PIC16C923

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C924

To code protect:

- Protect all memory 0000001X00XXXX
- Protect upper 3/4 memory 0101011X01XXXX
- Protect upper 1/2 memory 1010101X10XXXX
- No code protection 1111111X11XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

Legend: X = Don't care

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4.3 Checksum

4.3.1 CHECKSUM CALCULATIONS

Checksum is calculated by reading the contents of the PIC16C6X/7X/9XX memory locations and adding up the opcodes up to the maximum user addressable location, e.g., 0x1FF for the PIC16C74. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16C8X devices is shown in Table 4-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
PIC16C61	OFF	SUM[0x000:0x3FF] + CFGW & 0x001F + 0x3FE0	0x3BFF	0x07CD
	ON	SUM_XNOR7[0x000:0x3FF] + (CFGW & 0x001F | 0x0060)	0xFC6F	0xFC15
PIC16C620	OFF	SUM[0x000:0x1FF] + CFGW & 0x3F7F	0x3D7F	0x094D
	ON	SUM_ID + CFGW & 0x3F7F	0x3DCE	0x099C
PIC16C621	OFF	SUM[0x000:0x3FF] + CFGW & 0x3F7F	0x3B7F	0x074D
	1/2	SUM[0x000:0x1FF] + CFGW & 0x3F7F + SUM_ID	0x4EDE	0x0093
	ALL	CFGW & 0x3F7F + SUM_ID	0x3BCE	0x079C
PIC16C622	OFF	SUM[0x000:0x7FF] + CFGW & 0x3F7F	0x377F	0x034D
	1/2	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x5DEE	0x0FA3
	3/4	SUM[0x000:0x1FF] + CFGW & 0x3F7F + SUM_ID	0x4ADE	0xFC93
	ALL	CFGW & 0x3F7F + SUM_ID	0x37CE	0x039C
PIC16C62	OFF	SUM[0x000:0x7FF] + CFGW & 0x003F + 0x3F80	0x37BF	0x038D
	1/2	SUM[0x000:0x3FF] + SUM_XNOR7[0x400:0x7FF] + CFGW & 0x003F + 0x3F80	0x37AF	0x1D69
	3/4	SUM[0x000:0x1FF] + SUM_XNOR7[0x200:0x7FF] + CFGW & 0x003F + 0x3F80	0x379F	0x1D59
	ALL	SUM_XNOR7[0x000:0x7FF] + CFGW & 0x003F + 0x3F80	0x378F	0x3735
PIC16C62A	OFF	SUM[0x000:0x7FF] + CFGW & 0x3F7F	0x377F	0x034D
	1/2	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x5DEE	0x0FA3
	3/4	SUM[0x000:0x1FF] + CFGW & 0x3F7F + SUM_ID	0x4ADE	0xFC93
	ALL	CFGW & 0x3F7F + SUM_ID	0x37CE	0x039C
PIC16C63	OFF	SUM[0x000:0xFFF] + CFGW & 0x3F7F	0x2F7F	0xFB4D
	1/2	SUM[0x000:0x7FF] + CFGW & 0x3F7F + SUM_ID	0x51EE	0x03A3
	3/4	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x40DE	0xF293
	ALL	CFGW & 0x3F7F + SUM_ID	0x2FCE	0xFB9C
PIC16C64	OFF	SUM[0x000:0x7FF] + CFGW & 0x003F + 0x3F80	0x37BF	0x038D
	1/2	SUM[0x000:0x3FF] + SUM_XNOR7[0x400:0x7FF] + CFGW & 0x003F + 0x3F80	0x37AF	0x1D69
	3/4	SUM[0x000:0x1FF] + SUM_XNOR7[0x200:0x7FF] + CFGW & 0x003F + 0x3F80	0x379F	0x1D59
	ALL	SUM_XNOR7[0x000:0x7FF] + CFGW & 0x003F + 0x3F80	0x378F	0x3735

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a through b inclusive]
SUM_XNOR7[a:b] = XNOR of the seven high order bits of memory location with the seven low order bits summed over locations a through b inclusive. For example, location_a = 0x123 and location_b = 0x456, then SUM_XNOR7 [location_a : location_b] = 0x001F.
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nibble. For example, ID0 = 0x12, ID1 = 0x37, ID2 = 0x4, ID3 = 0x26, then SUM_ID = 0x2746.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

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TABLE 4-2: CHECKSUM COMPUTATION (CONTINUED)

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
PIC16C64A	OFF	SUM[0x000:0x7FF] + CFGW & 0x3F7F	0x377F	0x034D
	1/2	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x5DEE	0x0FA3
	3/4	SUM[0x000:0x1FF] + CFGW & 0x3F7F + SUM_ID	0x4ADE	0xFC93
	ALL	CFGW & 0x3F7F + SUM_ID	0x37CE	0x039C
PIC16C65	OFF	SUM[0x000:0xFFF] + CFGW & 0x003F + 0x3F80	0x2FBF	0xFB8D
	1/2	SUM[0x000:0x7FF] + SUM_XNOR7[0x800:FFF] + CFGW & 0x003F + 0x3F80	0x2FAF	0x1569
	3/4	SUM[0x000:0x3FF] + SUM_XNOR7[0x400:FFF] + CFGW & 0x003F + 0x3F80	0x2F9F	0x1559
	ALL	SUM_XNOR7[0x000:0xFFF] + CFGW & 0x003F + 0x3F80	0x2F8F	0x2F35
PIC16C65A	OFF	SUM[0x000:0xFFF] + CFGW & 0x3F7F	0x2F7F	0xFB4D
	1/2	SUM[0x000:0x7FF] + CFGW & 0x3F7F + SUM_ID	0x51EE	0x03A3
	3/4	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x40DE	0xF293
	ALL	CFGW & 0x3F7F + SUM_ID	0x2FCE	0xFB9C
PIC16C710	OFF	SUM[0x000:0x1FF] + CFGW & 0x3FFF	0x3DFF	0x09CD
	ON	SUM[0x00:0x3F] + CFGW & 0x3FFF + SUM_ID	0x3E0E	0xEFC3
PIC16C71	OFF	SUM[0x000:0x3FF] + CFGW & 0x001F + 0x3FE0	0x3BFF	0x07CD
	ON	SUM_XNOR7[0x000:0x3FF] + (CFGW & 0x001F I 0x0060)	0xFC6F	0xFC15
PIC16C711	OFF	SUM[0x000:0x3FF] + CFGW & 0x3FFF	0x3BFF	0x07CD
	ON	SUM[0x00:0x3F] + CFGW & 0x3FFF + SUM_ID	0x3C0E	0xEDC3
PIC16C72	OFF	SUM[0x000:0x7FF] + CFGW & 0x3F7F	0x377F	0x034D
	1/2	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x5DEE	0x0FA3
	3/4	SUM[0x000:0x1FF] + CFGW & 0x3F7F + SUM_ID	0x4ADE	0xFC93
	ALL	CFGW & 0x3F7F + SUM_ID	0x37CE	0x039C
PIC16C73	OFF	SUM[0x000:0xFFF] + CFGW & 0x003F + 0x3F80	0x2FBF	0xFB8D
	1/2	SUM[0x000:0x7FF] + SUM_XNOR7[0x800:FFF] + CFGW & 0x003F + 0x3F80	0x2FAF	0x1569
	3/4	SUM[0x000:0x3FF] + SUM_XNOR7[0x400:FFF] + CFGW & 0x003F + 0x3F80	0x2F9F	0x1559
	ALL	SUM_XNOR7[0x000:0xFFF] + CFGW & 0x003F + 0x3F80	0x2F8F	0x2F35
PIC16C73A	OFF	SUM[0x000:0xFFF] + CFGW & 0x3F7F	0x2F7F	0xFB4D
	1/2	SUM[0x000:0x7FF] + CFGW & 0x3F7F + SUM_ID	0x51EE	0x03A3
	3/4	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x40DE	0xF293
	ALL	CFGW & 0x3F7F + SUM_ID	0x2FCE	0xFB9C
PIC16C74	OFF	SUM[0x000:0xFFF] + CFGW & 0x003F + 0x3F80	0x2FBF	0xFB8D
	1/2	SUM[0x000:0x7FF] + SUM_XNOR7[0x800:FFF] + CFGW & 0x003F + 0x3F80	0x2FAF	0x1569
	3/4	SUM[0x000:0x3FF] + SUM_XNOR7[0x400:FFF] + CFGW & 0x003F + 0x3F80	0x2F9F	0x1559
	ALL	SUM_XNOR7[0x000:0xFFF] + CFGW & 0x003F + 0x3F80	0x2F8F	0x2F35
PIC16C74A	OFF	SUM[0x000:0xFFF] + CFGW & 0x3F7F	0x2F7F	0xFB4D
	1/2	SUM[0x000:0x7FF] + CFGW & 0x3F7F + SUM_ID	0x51EE	0x03A3
	3/4	SUM[0x000:0x3FF] + CFGW & 0x3F7F + SUM_ID	0x40DE	0xF293
	ALL	CFGW & 0x3F7F + SUM_ID	0x2FCE	0xFB9C
PIC16C923	OFF	SUM[0x000:0xFFF] + CFGW & 0x3F3F	0x2F3F	0xFB0D
	1/2	SUM[0x000:0x7FF] + CFGW & 0x3F3F + SUM_ID	0x516E	0x0323
	3/4	SUM[0x000:0x3FF] + CFGW & 0x3F3F + SUM_ID	0x405E	0xF213
	ALL	CFGW & 0x3F3F + SUM_ID	0x2F4E	0xFB1C
PIC16C924	OFF	SUM[0x000:0xFFF] + CFGW & 0x3F3F	0x2F3F	0xFB0D
	1/2	SUM[0x000:0x7FF] + CFGW & 0x3F3F + SUM_ID	0x516E	0x0323
	3/4	SUM[0x000:0x3FF] + CFGW & 0x3F3F + SUM_ID	0x405E	0xF213
	ALL	CFGW & 0x3F3F + SUM_ID	0x2F4E	0xFB1C

Legend: CFGW = Configuration Word

SUM[a:b] = [Sum of locations a through b inclusive]

SUM_XNOR7[a:b] = XNOR of the seven high order bits of memory location with the seven low order bits summed over locations a through b inclusive. For example, location_a = 0x123 and location_b = 0x456, then SUM_XNOR7 [location_a : location_b] = 0x001F.

SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nibble. For example, ID0 = 0x12, ID1 = 0x37, ID2 = 0x4, ID3 = 0x26, then SUM_ID = 0x2746.

*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]

+ = Addition

& = Bitwise AND

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5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions
Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (20°C recommended)
Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.

Parameter No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
General							
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	IDDP	Supply current (from VDD) during programming			20	mA	
PD3	VDDV	Supply voltage during verify	VDDmin		VDDmax	V	Note 1
PD4	VIHH1	Voltage on $\overline{MCLR}$/VPP during programming	12.75		13.25	V	Note 2
PD5	VIHH2	Voltage on $\overline{MCLR}$/VPP during verify	VDD + 4.0		13.5		
PD6	IPP	Programming supply current (from VPP)			50	mA	
PD9	VIH1	(RB6, RB7) input high level	0.8 VDD			V	Schmitt Trigger input
PD8	VIL1	(RB6, RB7) input low level	0.2 VDD			V	Schmitt Trigger input
Serial Program Verify							
P1	TR	$\overline{MCLR}$/VPP rise time (VSS to VHH) for test mode entry			8.0	µs	
P2	Tf	$\overline{MCLR}$ Fall time			8.0	µs	
P3	Tset1	Data in setup time before clock ↓	100			ns	
P4	Thld1	Data in hold time after clock ↓	100			ns	
P5	Tdly1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0			µs	
P6	Tdly2	Delay between clock ↓ to clock ↑ of next command or data	1.0			µs	
P7	Tdly3	Clock ↑ to date out valid (during read data)	200			ns	
P8	Thld0	Hold time after $\overline{MCLR}$ ↑	2			µs	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be greater than VDD + 4.5V to stay in programming/verify mode.

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FIGURE 5-1: LOAD DATA COMMAND (PROGRAM/VERIFY)

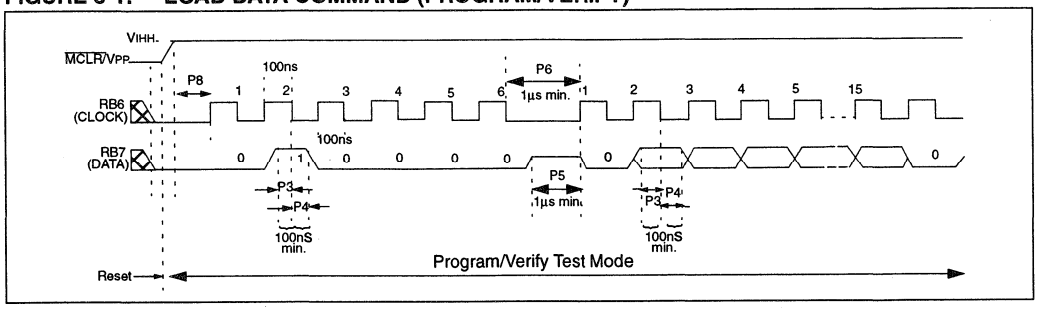


FIGURE 5-2: READ DATA COMMAND (PROGRAM/VERIFY)

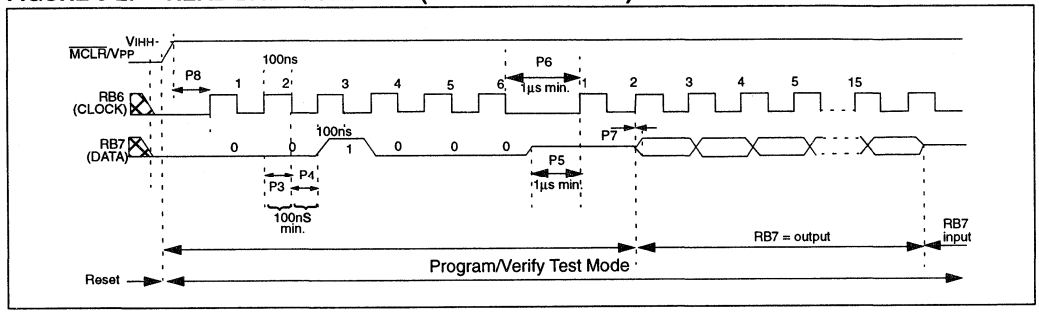
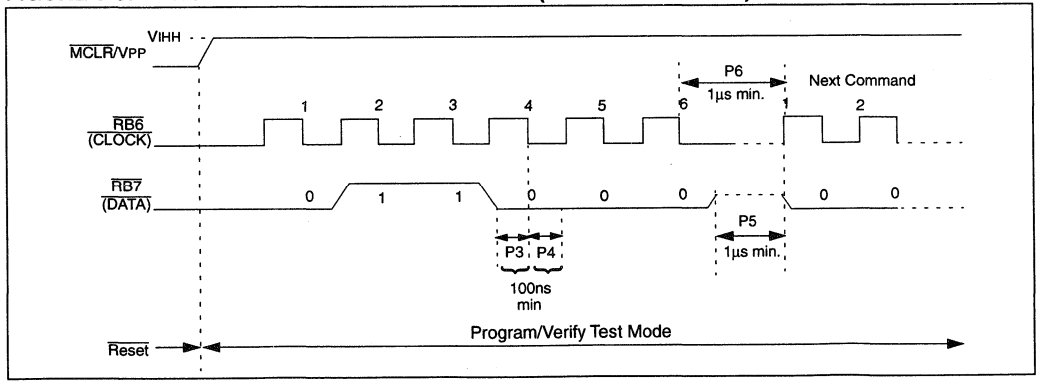


FIGURE 5-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)



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NOTES:

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PIC16C84

EEPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16C84

1.0 PROGRAMMING THE PIC16C84

The PIC16C84 is programmed using the serial method. The serial mode will allow the PIC16C84 to be programmed while in the users system. This allows for increased design flexibility.

1.1 Hardware Requirements

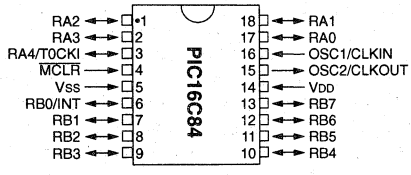
The PIC16C84 requires one programmable power supply for VDD (4.5V to 5.5V) and a VPP of 12V to 14V. Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

The programming mode for the PIC16C84 allows programming of user program memory, data memory, special locations used for ID, and the configuration word.

Pin Diagram

PDIP, SOIC



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PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16C84

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RB6	CLOCK	I	Clock input
RB7	DATA	I/O	Data input/output
$\overline{MCLR}$	VTEST MODE	P*	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I =Input, O = Output, P = Power

*In PIC16C84, programming high voltage is internally generated. To activate the programming mode, high voltage needs to be applied to $\overline{MCLR}$ input. This means that $\overline{MCLR}$ does not draw any significant current.

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2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K), of which 1K (0x0000 - 0x03FF) is physically implemented. In actual implementation the on-chip user program memory is accessed by the lower 10-bits of the PC, with the upper 3-bits of the PC ignored. Therefore if the PC is greater than 0x3FF, it will wrap around and address a location within the physically implemented memory. (See Figure 2-1).

In programming mode the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF to 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode as described in Section 2.3.

In the configuration memory space, 0x2000-0x200F are physically implemented. Locations beyond 0x200F will physically access user memory. (See Figure 2-1).

2.2 ID Locations

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000 : 0x2003]. It is recommended that the user use only the four least significant bits of each ID location. In some devices, the ID locations read-out in a scrambled fashion after code protection is enabled. For these devices, it is recommended that ID location is written as "11 1111 1000 bbbb" where 'bbbb' is ID information.

In other devices, the ID locations read out normally, even after code protection. To understand how the devices behave, refer to Table 4.3.

To understand the scrambling mechanism after code protection, refer to Section 4.0.

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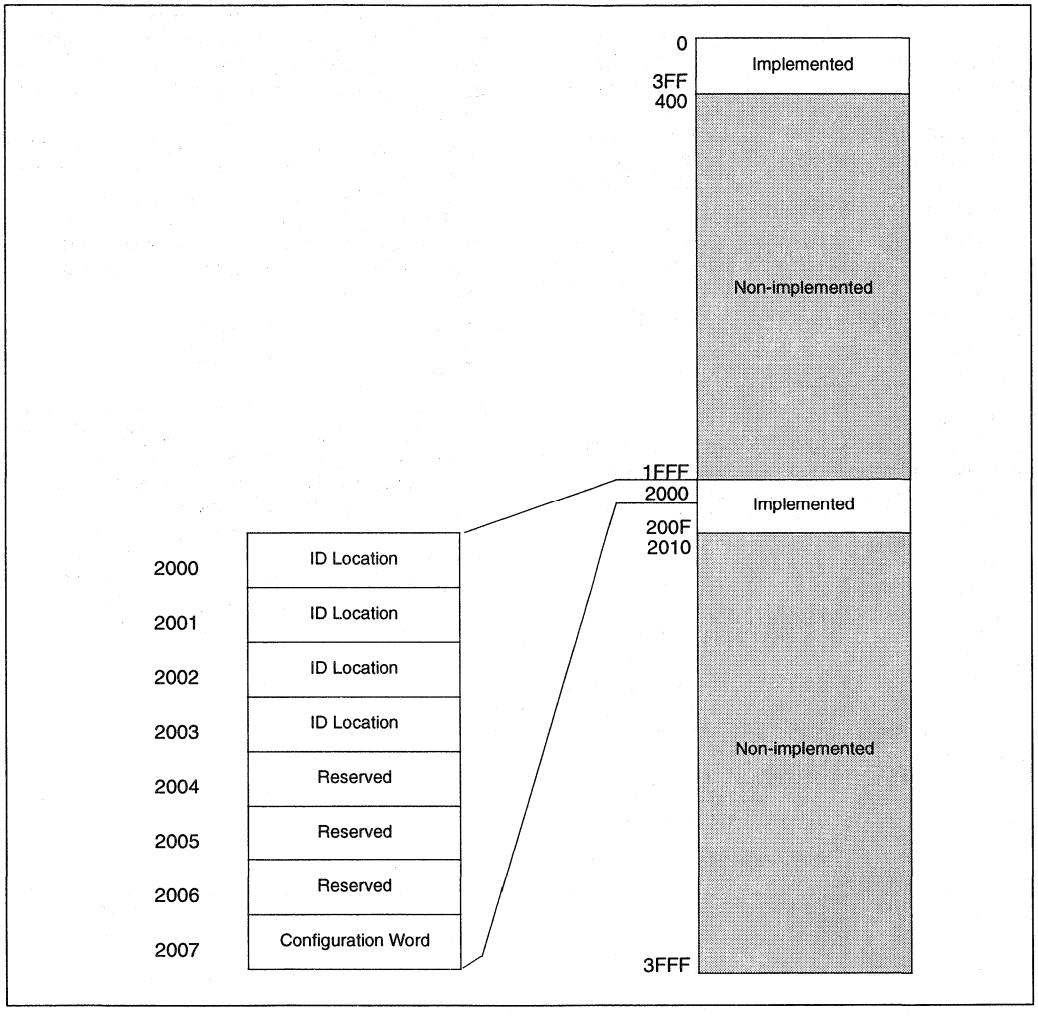
FIGURE 2-1: PROGRAM MEMORY MAPPING



2.3 Program/Verify Mode

The program/verify mode is entered by holding pins RB6 and RB7 low while raising $\overline{MCLR}$ pin from VIL to VIHH (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. RB6 and RB7 are Schmitt Trigger inputs in this mode.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the $\overline{MCLR}$ pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

2.3.1 SERIAL PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (lsb) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specifications) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output lsb first.

Therefore, during a read operation the lsb will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the lsb will be latched on the falling edge of the second cycle. A minimum 1µs delay is also specified between consecutive commands.

All commands are transmitted lsb first. Data words are also transmitted lsb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1 µs is required between a command and a data word (or another command).

The commands that are available are:

2.3.1.1 LOAD CONFIGURATION

After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits in a "data word", as described above, to be programmed into the configuration memory. A description of the memory mapping schemes of the program memory for normal operation and configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking $\overline{MCLR}$ low (VIL).

TABLE 2-1: COMMAND MAPPING (SERIAL OPERATION)

Command	Mapping (MSB ... LSB)						Data
Load Configuration	0	0	0	0	0	0	0, data (14), 0
Load Data for Program Memory	0	0	0	0	1	0	0, data (14), 0
Read Data from Program Memory	0	0	0	1	0	0	0, data (14), 0
Increment Address	0	0	0	1	1	0	
Begin Programming	0	0	1	0	0	0	
Load Data for Data Memory	0	0	0	0	1	1	0, data (14), 0
Read Data from Data Memory	0	0	0	1	0	1	0, data (14), 0
Bulk Erase Program Memory	0	0	1	0	0	1	
Bulk Erase Data Memory	0	0	1	0	1	1	

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FIGURE 2-2: PROGRAM FLOW CHART - PIC16C84 PROGRAM MEMORY

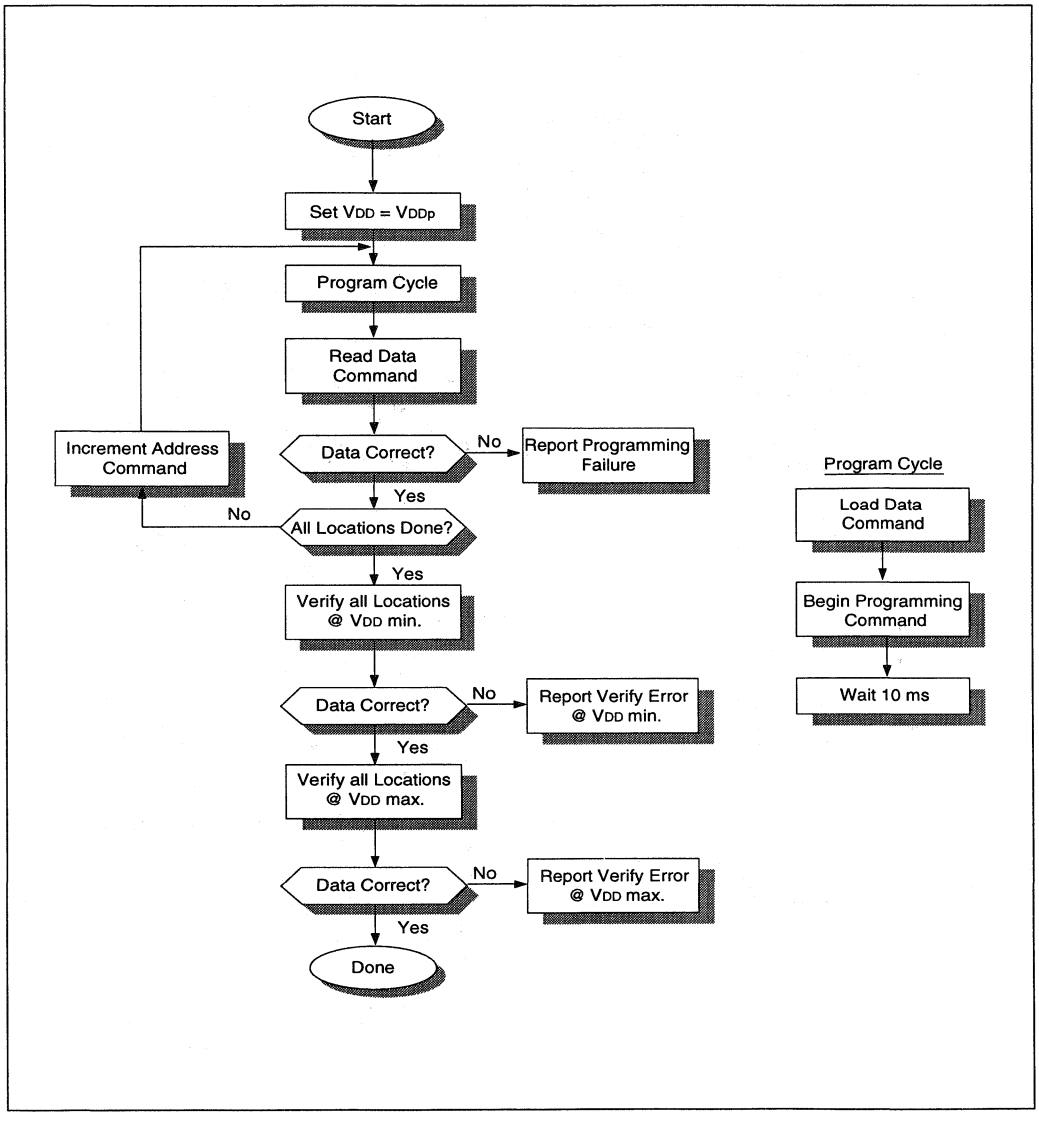

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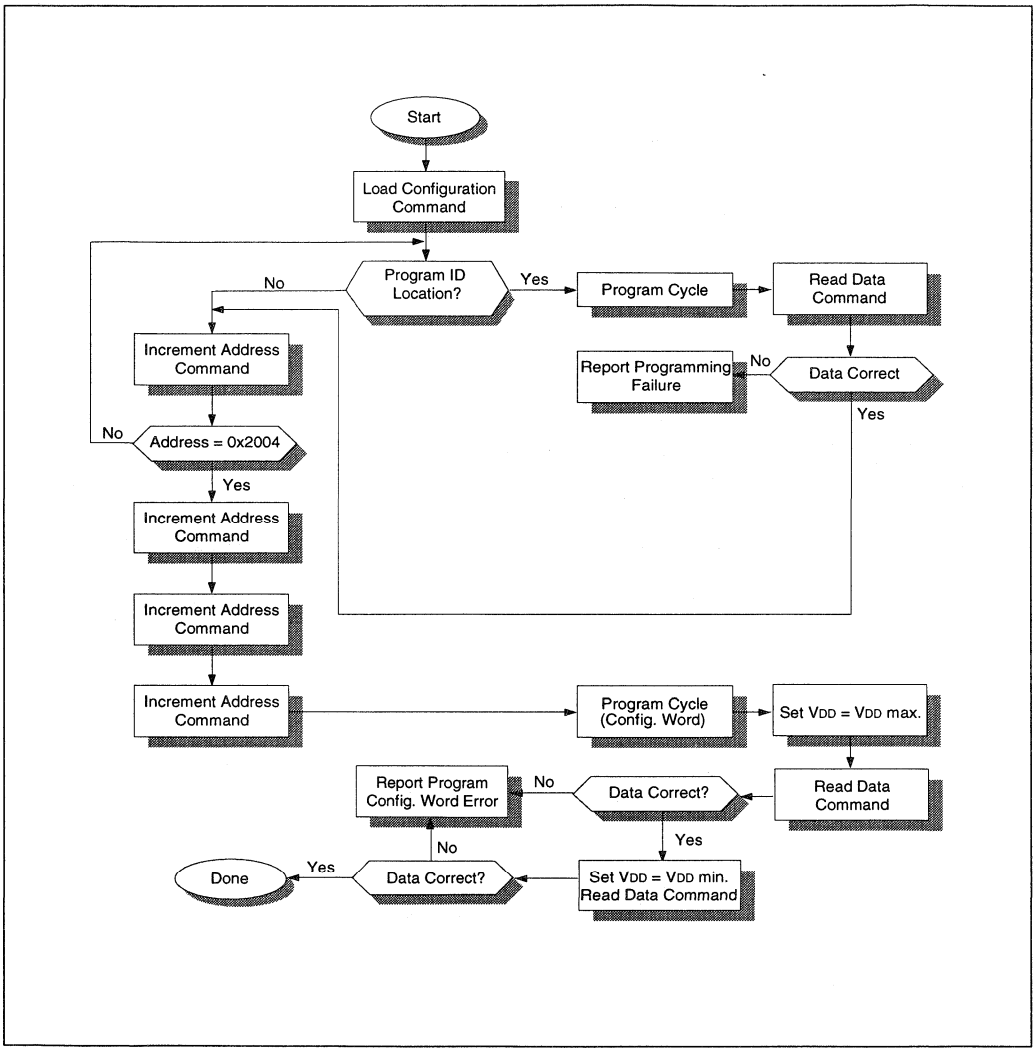
FIGURE 2-3: PROGRAM FLOW CHART - PIC16C84 CONFIGURATION MEMORY



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2.3.1.2 LOAD DATA FOR PROGRAM MEMORY

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 5-1.

2.3.1.3 LOAD DATA FOR DATA MEMORY

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied. However, the data memory is only 8-bits wide, and thus only the first 8-bits of data after the start bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly. The data memory contains 64 words. Only the lower 8-bits of the PC are decoded by the data memory, and therefore if the PC is greater than 0x3F, it will wrap around and address a location within the physically implemented memory.

2.3.1.4 READ DATA FROM PROGRAM MEMORY

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.3.1.5 READ DATA FROM DATA MEMORY

After receiving this command, the chip will transmit data bits out of the data memory starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. As previously stated, the data memory is 8-bits wide, and therefore, only the first 8-bits that are output are actual data.

2.3.1.6 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.3.1.7 BEGIN PROGRAMMING

A load command must be given before every begin programming command. Programming of the appropriate memory (test program memory, user program memory or data memory) will begin after this command is received and decoded. An internal timing mechanism executes an erase before write. The user must allow 10ms for programming to complete. No "end programming" command is required.

2.3.1.8 BULK ERASE PROGRAM MEMORY

To perform a bulk erase of the program memory, the following sequence must be performed.

1. Do a "Load Data All 1's" command.
2. Do a "Bulk Erase User Memory" command.
3. Do a "Begin Programming" command.
4. Wait 10 ms to complete bulk erase.

If the address is pointing to the test program memory (0x2000 - 0x200F), then both the user memory and the test memory will be erased. The configuration word will not be erased, even if the address is pointing to location 0x2007.

If the address is pointing to the test program memory (0x2000 - 0x200F), then both the user memory and the test memory will be erased. The configuration word will not be erased, even if the address is pointing to location 0x2007.

2.3.1.9 BULK ERASE DATA MEMORY

To perform a bulk erase of the data memory, the following sequence must be performed.

1. Do a "Load Data All 1's" command.
2. Do a "Bulk Erase Data Memory" command.
3. Do a "Begin Programming" command.
4. Wait 10 ms to complete bulk erase.

2.4 Programming Algorithm Requires Variable VDD

The PIC16C84 uses an intelligent algorithm. The algorithm calls for program verification at VDD (min.) as well as VDD (max.). Verification at VDD (min.) guarantees good "erase margin". Verification at VDD (max) guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (4.5 - 5.5V).

VDDP = VCC range required during programming.

VDD min. = minimum operating VDD spec for the part.

VDD max.= maximum operating VDD spec for the part.

Programmers must verify the PIC16C84 at its specified VDD max. and VDD min. levels. Since Microchip may introduce future versions of the PIC16C84 with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

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3.0 CONFIGURATION WORD

The PIC16C84 has five configuration bits. These bits can be set (reads '0') or left unchanged (reads '1') to select various device configurations.

FIGURE 3-1: CONFIGURATION WORD BIT MAP

Bit Number:	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CP	PWRTE	WDTE	FOSC1	FOSC0

bit 4: **CP**, Code Protection Configuration Bit
1 = code protection off
0 = code protection on

bit 3: **PWRTE**, Power Up Timer Enable Configuration Bit
1 = Power up timer enabled
0 = Power up timer disabled

bit 3-2: **WDTE**, WDT Enable Configuration Bits
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>**, Oscillator Selection Configuration Bits
11: RC oscillator
10: HS oscillator
01: XT oscillator
00: LP oscillator

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4.0 CODE PROTECTION

For PIC16C84 devices, once code protection is enabled, all program memory locations read out in a scrambled fashion. The ID locations and the configuration word also read out in a scrambled fashion. Further programming is disabled for the entire program memory as well as data memory. It is possible to program the ID locations and the configuration word.

4.1 Disabling Code-Protection

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off (code protect bit = 1) using this procedure; however, ***all data within the program memory and the data memory will be erased when this procedure is executed, and thus, the security of the data or code is not compromised.***

Procedure to disable code protect:

a) Execute load configuration (with a '1' in bit 4, code protect).
b) Increment to configuration word location (0x2007)
c) Execute command (000001)
d) Execute command (000111)
e) Execute 'Begin Programming' (001000)
f) Wait 10ms
g) Execute command (000001)
h) Execute command (000111)

4.2 Embedding Configuration Word and ID Information in the Hex File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, all configuration word and ID information must be included. An option to not include this information may be provided.

Specifically for the PIC16C84, the EEPROM data memory should also be embedded in the hex file (see Section 5.1).

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

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TABLE 4-1: CONFIGURATION WORD

PIC16C84

To code protect: XXXXXXXX0XXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory.	Read Scrambled, Write Disabled	Read Unscrambled, Write Enabled
ID Locations [0x2000 : 0x2003]	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled

Legend: X = Don't care

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4.3 Checksum

4.3.1 CHECKSUM CALCULATIONS

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
PIC16C84	OFF	SUM[0x000:0x3FF] + CFGW & 0x1F + 0x3FE0	0x3BFF	0x07CD
	ON	SUM_XNOR7[0x000:0x3FF] + (CFGW & 0x1F I 0x60)	0xFC6F	0xFC15

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_XNOR7[a:b] = XNOR of the seven high order bits of memory location with the seven low order bits summed over locations a through b inclusive. For example, location_a = 0x123 and location_b = 0x456, then SUM_XNOR7 [location_a : location_b] = 0x001F.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]

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5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

5.1 Embedding Data EEPROM Contents in Hex File

The programmer should be able to read data EEPROM information from a hex file and conversely (as an option) write data EEPROM contents to a hex file along with program memory information and fuse information.

The 64 data memory locations are logically mapped starting at address 0x2100. The format for data memory storage is one data byte per address location, lsb aligned.

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions						
Operating Temperature	+10°C ≤ TA ≤ +40°C, unless otherwise stated, (25°C is recommended)					
Operating Voltage	4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.					
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Supply voltage during programming	VDDP	4.5	5.0	5.5	V	
Supply voltage during verify	VDDV	VDD min.		VDD max.	V	Note 1
High voltage on $\overline{MCLR}$ for test mode entry	VIHH	12		14.0	V	Note 2
Supply current (from VDD) during program/verify	IDDP			50	mA	
Supply current from VIHH (on $\overline{MCLR}$)	IHH			200	µA	
$\overline{MCLR}$ rise time (VSS to VHH) for test mode entry	tVHHR			1.0	µs	
(RB6, RB7) input high level	VIH1	0.8 VDD			V	Schmitt Trigger input
(RB6, RB7) input low level $\overline{MCLR}$ (test mode selection	VIL1	0.2 VDD			V	Schmitt Trigger input
RB6, RB7 setup time (before pattern setup time)	tset0	100			ns	
Data in setup time before clock ↓	tset1	100			ns	
Data in hold time after clock ↓	thld1	100			ns	
Data input not driven to next clock input (delay required between command/data or command/command)	tdly1	1.0			µs	
Delay between clock ↓ to clock ↑ of next command or data	tdly2	1.0			µs	
Clock to data out valid (during read data)	tdly3	80			ns	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be higher than VDD + 4.5V to stay in programming/verify mode.

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FIGURE 5-1: LOAD DATA FOR PROGRAM MEMORY COMMAND (SERIAL PROGRAM/VERIFY)

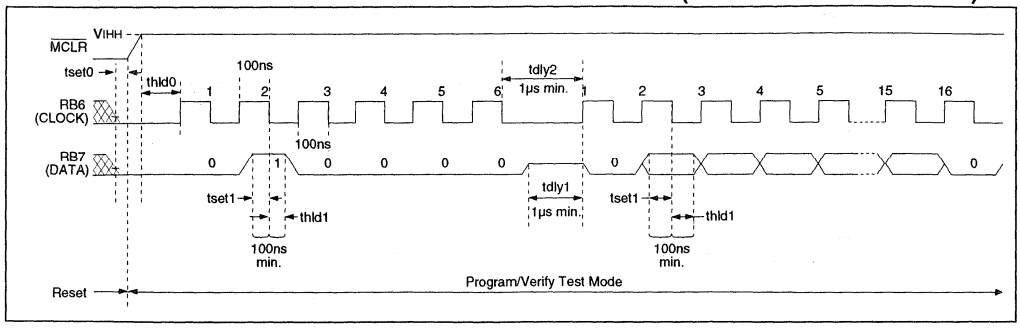


FIGURE 5-2: READ DATA FROM PROGRAM MEMORY COMMAND (SERIAL PROGRAM/VERIFY)

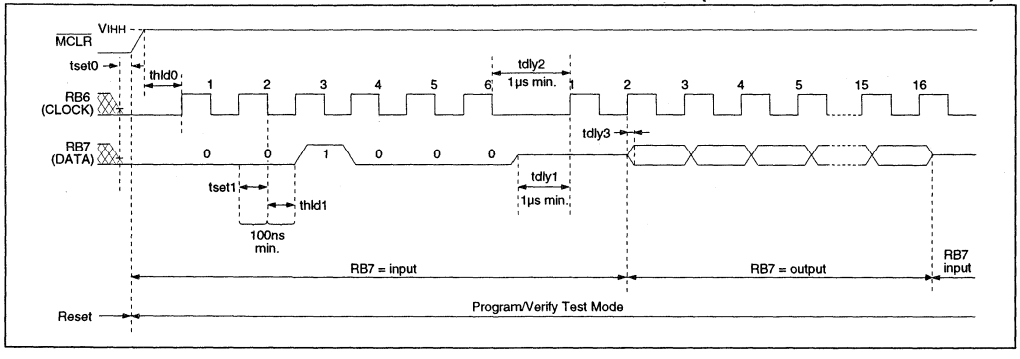
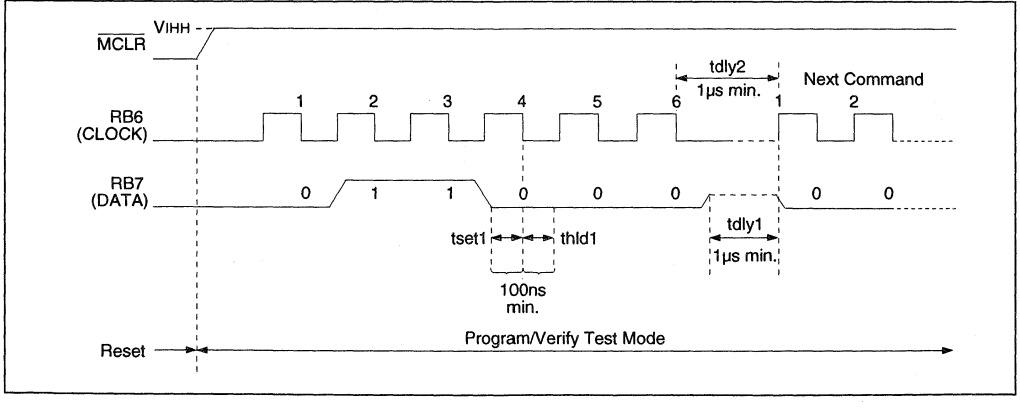


FIGURE 5-3: INCREMENT ADDRESS COMMAND (SERIAL PROGRAM/VERIFY)



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EEPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84

1.0 PROGRAMMING THE PIC16F8X

The PIC16F8X is programmed using a serial method. The serial mode will allow the PIC16F8X to be programmed while in the users system. This allows for increased design flexibility. This programming specification applies to PIC16F8X devices in all packages.

1.1 Hardware Requirements

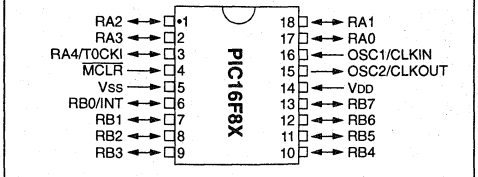
The PIC16F8X requires one programmable power supply for VDD (4.5V to 5.5V) and a VPP of 12V to 14V. Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

The programming mode for the PIC16F8X allows programming of user program memory, data memory, special locations used for ID, and the configuration word.

Pin Diagram

PDIP, SOIC



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PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16F8X

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RB6	CLOCK	I	Clock input
RB7	DATA	I/O	Data input/output
MCLR	VTEST MODE	P*	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

*In the PIC16F8X, the programming high voltage is internally generated. To activate the programming mode, high voltage needs to be applied to MCLR input. Since the MCLR is used for a level source, this means that MCLR does not draw any significant current.

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2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K), of which 1K (0x0000 - 0x03FF) is physically implemented. In actual implementation the on-chip user program memory is accessed by the lower 10-bits of the PC, with the upper 3-bits of the PC ignored. Therefore if the PC is greater than 0x3FF, it will wrap around and address a location within the physically implemented memory. (See Figure 2-1).

In programming mode the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x000 or 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode as described in Section 2.3.

In the configuration memory space, 0x2000-0x200F are physically implemented. However, only locations 0x2000 through 0x2007 are available. Other locations are reserved. Locations beyond 0x200F will physically access user memory. (See Figure 2-1).

2.2 ID Locations

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000 : 0x2003]. It is recommended that the user use only the four least significant bits of each ID location. In some devices, the ID locations read-out in an unscrambled fashion after code protection is enabled. For these devices, it is recommended that ID location is written as "11 1111 1000 bbbb" where 'bbbb' is ID information.

In other devices, the ID locations read out normally, even after code protection. To understand how the devices behave, refer to Table 4-2.

To understand the scrambling mechanism after code protection, refer to Section 4.0.

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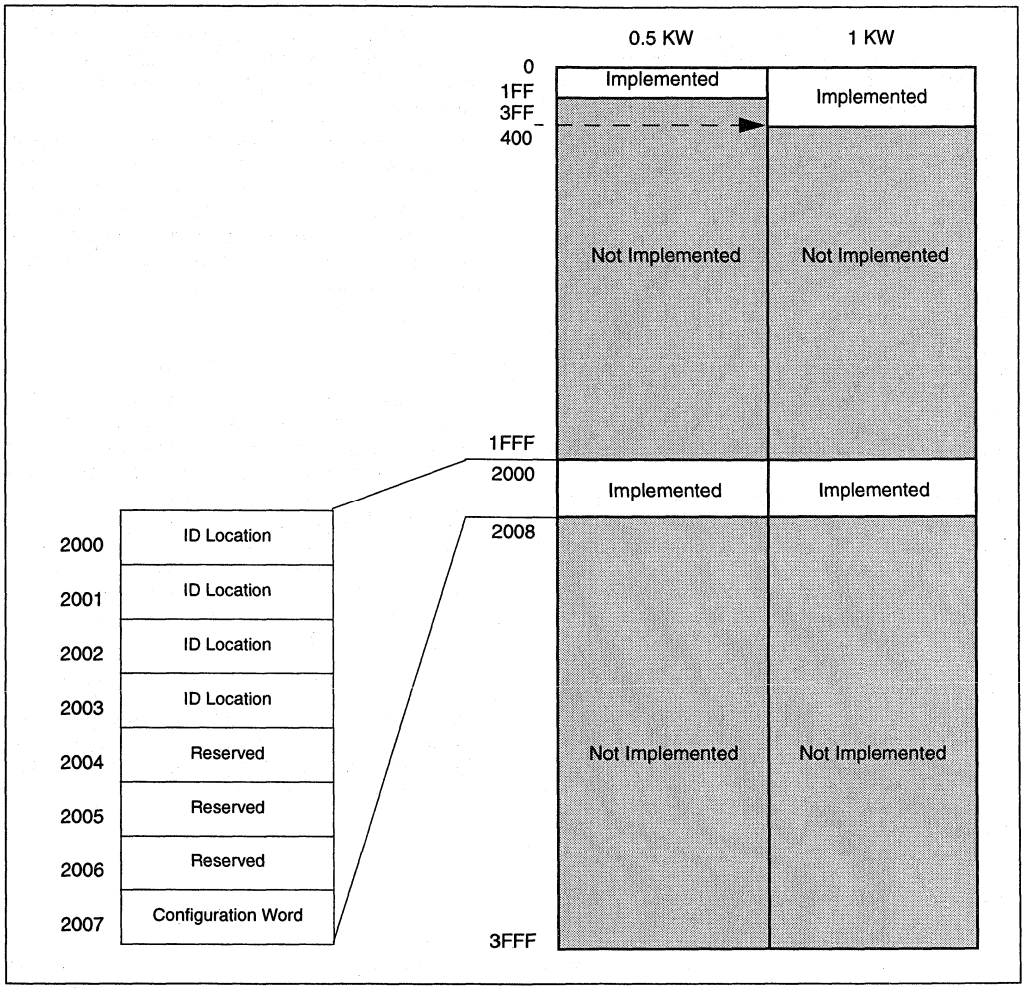
FIGURE 2-1: PROGRAM MEMORY MAPPING



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2.3 Program/Verify Mode

The program/verify mode is entered by holding pins RB6 and RB7 low while raising $\overline{MCLR}$ pin from VIL to VIHH (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. RB6 and RB7 are Schmitt Trigger Inputs in this mode.

Note: The OSC must not have 72 osc clocks while the device $\overline{MCLR}$ is between VIL and VIHH.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the $\overline{MCLR}$ pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

2.3.1 SERIAL PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSB) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specifications) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output LSB first.

Therefore, during a read operation the LSB will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the LSB will be latched on the falling edge of the second cycle. A minimum 1µs delay is also specified between consecutive commands.

All commands are transmitted LSB first. Data words are also transmitted LSB first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1 µs is required between a command and a data word (or another command).

The commands that are available are:

2.3.1.1 LOAD CONFIGURATION

After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits in a "data word", as described above, to be programmed into the configuration memory. A description of the memory mapping schemes of the program memory for normal operation and configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking $\overline{MCLR}$ low (VIL).

2.3.1.2 LOAD DATA FOR PROGRAM MEMORY

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 5-1.

TABLE 2-1: COMMAND MAPPING

Command	Mapping (MSB ... LSB)						Data
Load Configuration	0	0	0	0	0	0	0, data (14), 0
Load Data for Program Memory	0	0	0	0	1	0	0, data (14), 0
Read Data from Program Memory	0	0	0	1	0	0	0, data (14), 0
Increment Address	0	0	0	1	1	0	
Begin Programming	0	0	1	0	0	0	
Load Data for Data Memory	0	0	0	0	1	1	0, data (14), 0
Read Data from Data Memory	0	0	0	1	0	1	0, data (14), 0
Bulk Erase Program Memory	0	0	1	0	0	1	
Bulk Erase Data Memory	0	0	1	0	1	1	

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FIGURE 2-2: PROGRAM FLOW CHART - PIC16F8X PROGRAM MEMORY

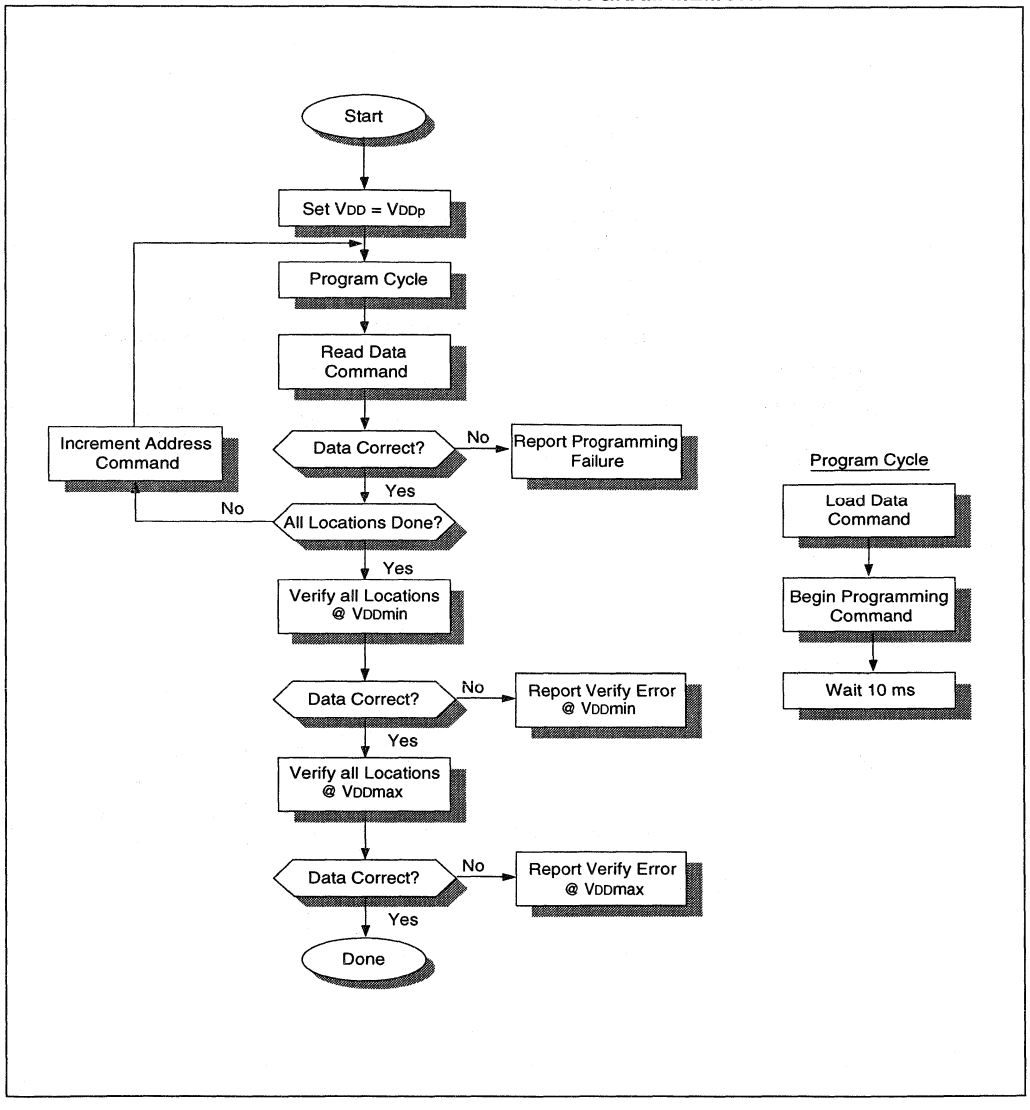
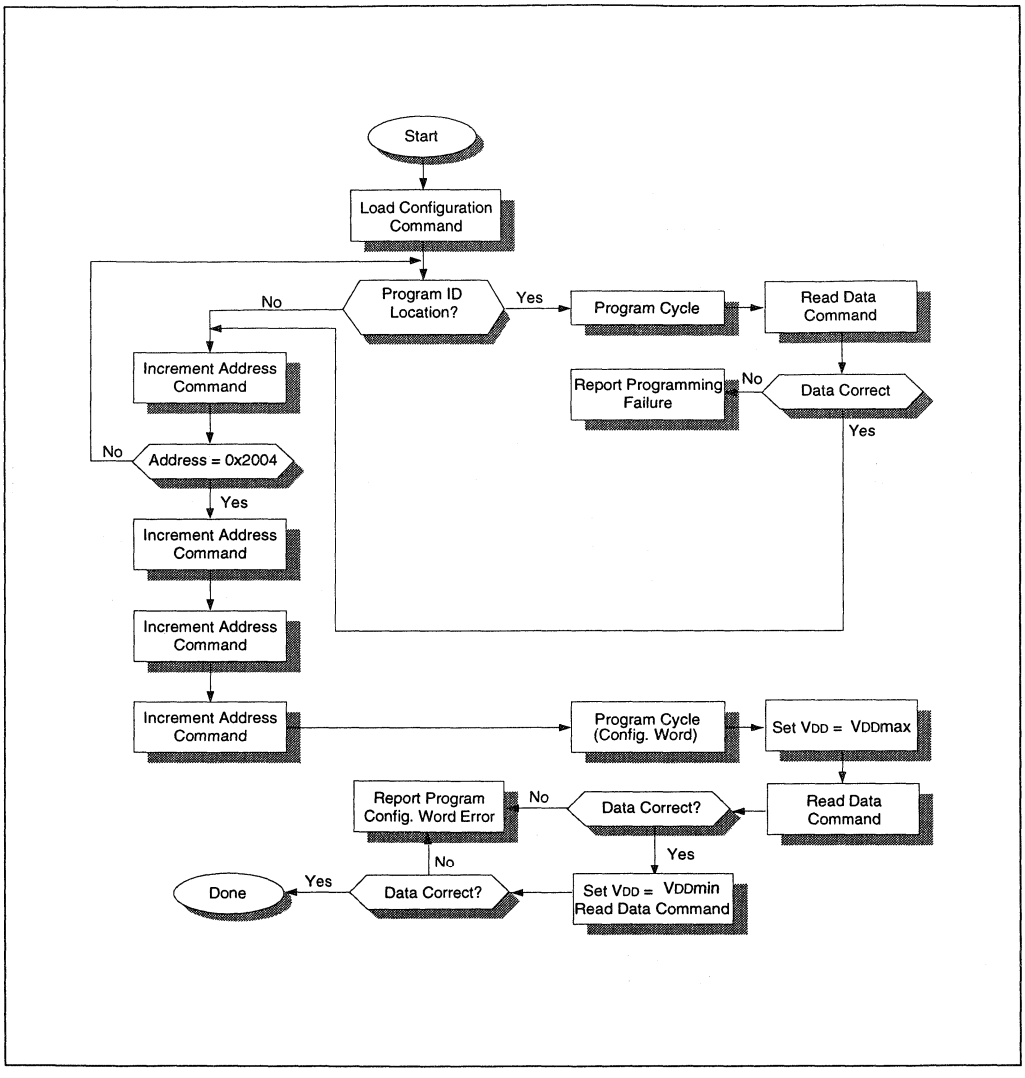


FIGURE 2-3: PROGRAM FLOW CHART - PIC16F8X CONFIGURATION MEMORY



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2.3.1.3 LOAD DATA FOR DATA MEMORY

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied. However, the data memory is only 8-bits wide, and thus only the first 8-bits of data after the start bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly. The data memory contains 64 words. Only the lower 8-bits of the PC are decoded by the data memory, and therefore if the PC is greater than 0x3F, it will wrap around and address a location within the physically implemented memory.

2.3.1.4 READ DATA FROM PROGRAM MEMORY

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.3.1.5 READ DATA FROM DATA MEMORY

After receiving this command, the chip will transmit data bits out of the data memory starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. As previously stated, the data memory is 8-bits wide, and therefore, only the first 8-bits that are output are actual data.

2.3.1.6 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.3.1.7 BEGIN PROGRAMMING

A load command must be given before every begin programming command. Programming of the appropriate memory (test program memory, user program memory or data memory) will begin after this command is received and decoded. An internal timing mechanism executes an erase before write. The user must allow 10ms for programming to complete. No "end programming" command is required.

2.3.1.8 BULK ERASE PROGRAM MEMORY

To perform a bulk erase of the program memory, the following sequence must be performed.

1. Do a "Load Data All 1's" command.
2. Do a "Bulk Erase User Memory" command.
3. Do a "Begin Programming" command.
4. Wait 10 ms to complete bulk erase.

If the address is pointing to the test program memory (0x2000 - 0x200F), then both the user memory and the test memory will be erased. The configuration word will not be erased, even if the address is pointing to location 0x2007.

2.3.1.9 BULK ERASE DATA MEMORY

To perform a bulk erase of the data memory, the following sequence must be performed.

1. Do a "Load Data All 1's" command.
2. Do a "Bulk Erase Data Memory" command.
3. Do a "Begin Programming" command.
4. Wait 10 ms to complete bulk erase.

2.4 Programming Algorithm Requires Variable VDD

The PIC16F8X uses an intelligent algorithm. The algorithm calls for program verification at VDDmin. as well as VDDmax. Verification at VDDmin. guarantees good "erase margin". Verification at VDDmax guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (See Table 5-1).

VDDP = VCC range required during programming.

VDDmin. = minimum operating VDD spec for the part.

VDDmax.= maximum operating VDD spec for the part.

Programmers must verify the PIC16F8X at its specified VDD max. and VDDmin levels. Since Microchip may introduce future versions of the PIC16F8X with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

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3.0 CONFIGURATION WORD

The PIC16F8X has five configuration bits. These bits can be set (reads '0') or left unchanged (reads '1') to select various device configurations.

FIGURE 3-1: CONFIGURATION WORD BIT MAP

Bit Number:	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIC16F83/ F84	CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
PIC16CR83/ CR84	CP	CP	CP	CP	CP	CP	DP	CP	CP	CP	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0

bit 4-13: **CP**, Code Protection Configuration Bit
1 = code protection off
0 = code protection on

bit 7: **PIC16CR83/CR84 only**
DP, Data Memory Code Protection Bit
1 = code protection off
0 = data memory is code protected

bit 3: **$\overline{\text{PWRTE}}$**, Power Up Timer Enable Configuration Bit
1 = Power up timer disabled
0 = Power up timer enabled

bit 3-2: **$\overline{\text{WDTE}}$**, WDT Enable Configuration Bits
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>**, Oscillator Selection Configuration Bits
11: RC oscillator
10: HS oscillator
01: XT oscillator
00: LP oscillator

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4.0 CODE PROTECTION

For PIC16F8X devices, once code protection is enabled, all program memory locations read all 0's. The ID locations and the configuration word read out in an unscrambled fashion. Further programming is disabled for the entire program memory as well as data memory. It is possible to program the ID locations and the configuration word.

4.1 Disabling Code-Protection

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off (code protect bit = 1) using this procedure; however, ***all data within the program memory and the data memory will be erased when this procedure is executed, and thus, the security of the data or code is not compromised.***

Procedure to disable code protect:

a) Execute load configuration (with a '1' in bit 4, code protect).
b) Increment to configuration word location (0x2007)
c) Execute command (000001)
d) Execute command (000111)
e) Execute 'Begin Programming' (001000)
f) Wait 10ms
g) Execute command (000001)
h) Execute command (000111)

4.2 Embedding Configuration Word and ID Information in the Hex File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, configuration word and ID information must be included. An option to not include this information may be provided.

Specifically for the PIC16F8X, the EEPROM data memory should also be embedded in the hex file (see Section 5.1).

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

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TABLE 4-1: CONFIGURATION WORD

PIC16F83

To code protect: 000000000XXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations [0x2000 : 0x2003]	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16CR83

To code protect: 000000000XXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled	Read Unscrambled
All memory	Read All 0's for Program Memory, Read All 1's for Data Memory - Write Disabled	Read Unscrambled, Data Memory - Write Enabled
ID Locations [0x2000 : 0x2003]	Read Unscrambled	Read Unscrambled

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PIC16CR84

To code protect: 000000000XXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled	Read Unscrambled
All memory	Read All 0's for Program Memory, Read All 1's for Data Memory - Write Disabled	Read Unscrambled, Data Memory - Write Enabled
ID Locations [0x2000 : 0x2003]	Read Unscrambled	Read Unscrambled

PIC16F84

To code protect: 000000000XXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations [0x2000 : 0x2003]	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

Legend: X = Don't care

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4.3 CHECKSUM COMPUTATION

4.3.1 CHECKSUM

Checksum is calculated by reading the contents of the PIC16F8X memory locations and adding up the opcodes up to the maximum user addressable location, e.g., 0x1FF for the PIC16F8X. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16F8X devices is shown in Table 4-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
PIC16F83	OFF ON	SUM[0x000:0x1FF] + CFGW & 0x3FFF CFGW & 0x3FFF + SUM_ID	0x3DFF 0x3E0E	0x09CD 0x09DC
PIC16CR83	OFF ON	SUM[0x000:0x1FF] + CFGW & 0x3FFF CFGW & 0x3FFF + SUM_ID	0x3DFF 0x3E0E	0x09CD 0x09DC
PIC16F84	OFF ON	SUM[0x000:0x3FF] + CFGW & 0x3FFF CFGW & 0x3FFF + SUM_ID	0x3BFF 0x3C0E	0x07CD 0x07DC
PIC16CR84	OFF ON	SUM[0x000:0x3FF] + CFGW & 0x3FFF CFGW & 0x3FFF + SUM_ID	0x3BFF 0x3C0E	0x07CD 0x07DC

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

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5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

5.1 Embedding Data EEPROM Contents in Hex File

The programmer should be able to read data EEPROM information from a hex file and conversely (as an option) write data EEPROM contents to a hex file along with program memory information and fuse information.

The 64 data memory locations are logically mapped starting at address 0x2100. The format for data memory storage is one data byte per address location, lsb aligned.

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions

Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (25°C is recommended)
Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.

Parameter No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions/Comments
	VDDP	Supply voltage during programming	4.5	5.0	5.5	V	
	VDDV	Supply voltage during verify	VDDmin		VDDmax	V	Note 1
	VIHH	High voltage on $\overline{MCLR}$ for test mode entry	12		14.0	V	Note 2
	IDDP	Supply current (from VDD) during program/verify			50	mA	
	IHH	Supply current from VIHH (on $\overline{MCLR}$)			200	µA	
	VIH1	(RB6, RB7) input high level	0.8 VDD			V	Schmitt Trigger input
	VIL1	(RB6, RB7) input low level $\overline{MCLR}$ (test mode selection)	0.2 VDD			V	Schmitt Trigger input
P1	TVHHR	$\overline{MCLR}$ rise time (VSS to VHH) for test mode entry			8.0	µs	
P2	Tset0	RB6, RB7 setup time (before pattern setup time)	100			ns	
P3	Tset1	Data in setup time before clock ↓	100			ns	
P4	Thld1	Data in hold time after clock ↓	100			ns	
P5	Tdly1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0			µs	
P6	Tdly2	Delay between clock ↓ to clock ↑ of next command or data	1.0			µs	
P7	Tdly3	Clock to data out valid (during read data)	80			ns	
P8	Thld0	RB <7:6> hold time after $\overline{MCLR}$ ↑	100			ns	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be greater than VDD + 4.5V to stay in programming/verify mode.

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FIGURE 5-1: LOAD DATA COMMAND (PROGRAM/VERIFY)

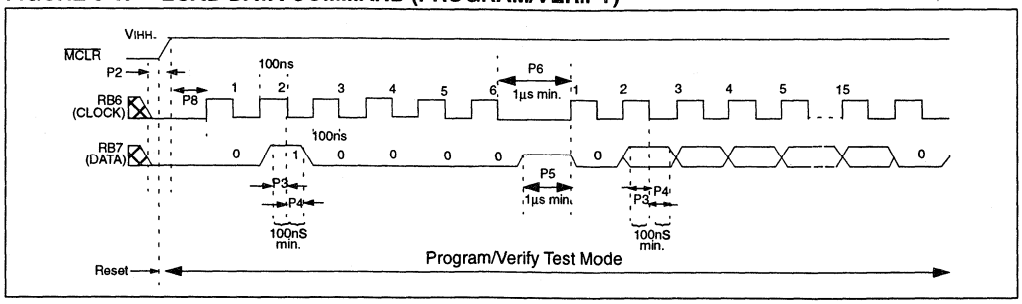


FIGURE 5-2: READ DATA COMMAND (PROGRAM/VERIFY)

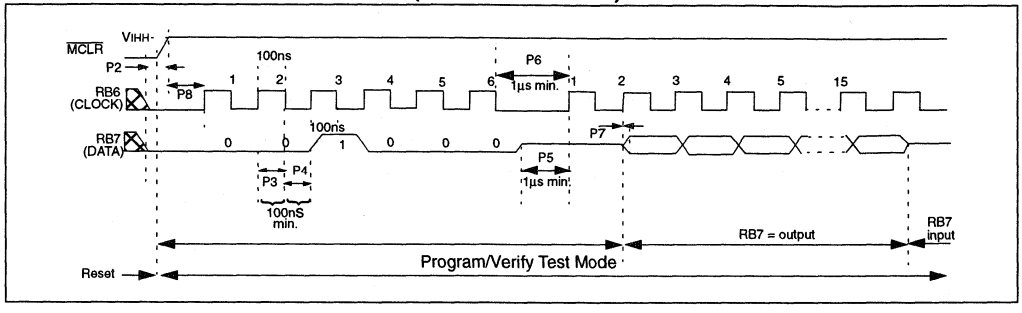
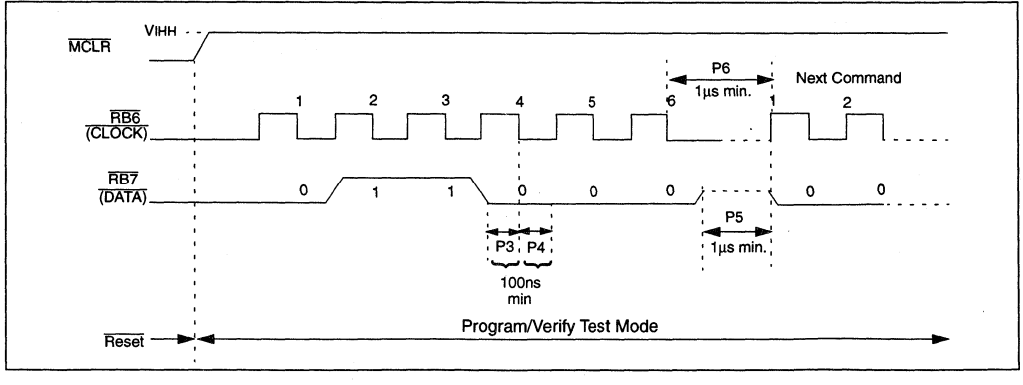


FIGURE 5-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)



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NOTES:

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EPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC17C42
- PIC17C42A
- PIC17CR42
- PIC17C43
- PIC17CR43
- PIC17C44

1.0 PROGRAMMING THE PIC17CXX

The PIC17CXX is programmed using the TABLWT instruction. The table pointer points to the internal EPROM location start. Therefore, a user can program an EPROM location while executing code (even from internal EPROM). This programming specification applies to PIC17CXX devices in all packages.

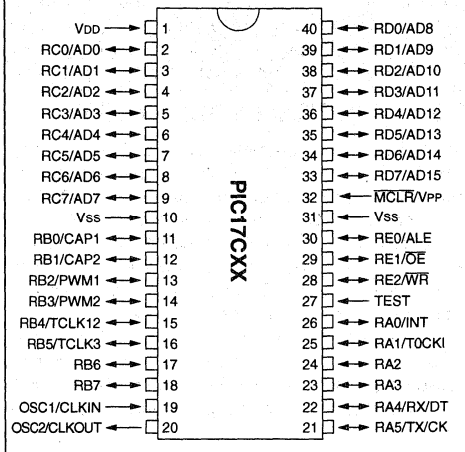
For the convenience of a programmer developer, a "program & verify" routine is provided in the on-chip test program memory space, the program resides in ROM and not EPROM. Therefore, it is not erasable. The "program/verify" routine allows the user to load any address, program a location, verify a location or increment to the next location. It allows variable programming pulse width.

1.1 Hardware Requirements

Since the PIC17CXX under programming is actually executing code from "boot ROM," a clock must be provided to the part. Furthermore, the PIC17CXX under programming may have any oscillator configuration (EC, XT, LF or RC). Therefore, the external clock driver must be able to overdrive pulldown in RC mode. CMOS drivers are required since the OSC1 input has a Schmitt trigger input with levels (typically) of 0.2VDD and 0.8VDD. See the PIC17C4X data sheet (DS30412A) for exact specifications.

Pin Diagram

40L PDIP, Windowed CERDIP



The PIC17CXX requires two programmable power supplies, one for VDD (2.5V to 6.0V recommended) and one for VPP (13 ± 0.25V). Both supplies should have a minimum resolution of 0.25V.

The PIC17CXX uses an intelligent algorithm. The algorithm calls for program verification at VDDmin as well as VDDmax. Verification at VDDmin guarantees good "erase margin". Verification at VDDmax guarantees good "program margin". Three times (3X) additional pulses will increase program margin then beyond VDD (max.) and insure safe operation in user system.

PIN DESCRIPTIONS (DURING PROGRAMMING): PIC17C42/42A/43/44

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RA <0:4>	RA <0:4>	I	Necessary in programming mode
TEST	TEST	I	Must be set to "high" to enter programming mode
RB <7:0>	PAD <15:8>	I/O	Address & data: high byte
RC <7:0>	PAD <7:0>	I/O	Address & data: low byte
MCLR/VPP	VPP	P	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

The actual programming must be done with VDD in the VDDP range (4.75 - 5.25V).

VDDP=VDD range required during programming.

VDD min.=minimum operating VDD spec for the part.

VDD max.=maximum operating VCC spec for the part.

Programmers must verify the PIC17CXX at its specified VDDmax and VDDmin levels. Since Microchip may introduce future versions of the PIC17CXX with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

2.0 PROGRAM MODE ENTRY

To execute the programming routine, the user must hold TEST pin high, RA2, RA3 must be low and RA4 must be high (after power-up) while keeping $\overline{MCLR}$ low and then raise $\overline{MCLR}$ pin from VIL to VDD or VPP. This will force FFE0h in the program counter and execution will begin at that location (the beginning of the boot code) following reset. Execution is forced to Internal mode by overriding the fuse configuration. The code protect bit is not overwritten. The program immediately polls PORT RB<7:0> to determine a branch address. Presenting E1h on PORT RB will cause the program to jump to and execute the "program/verify" routine.

Note:	The OSC must not have 72 osc clocks while the device $\overline{MCLR}$ is between VIL and VIHH.

All unused pins during programming are in high impedance state.

PORTB (RB) has internal weak pull-ups which are active during the programming mode. When TEST pin is high, Power-up timer (PWRT) and Oscillator Start-up Timers (OST) are disabled.

2.1 Program/Verify Mode

The program/verify mode is intended for full-feature programmers. This mode offers the following capabilities:

a) Load any arbitrary 16-bit address to start program and/or verify at that location.

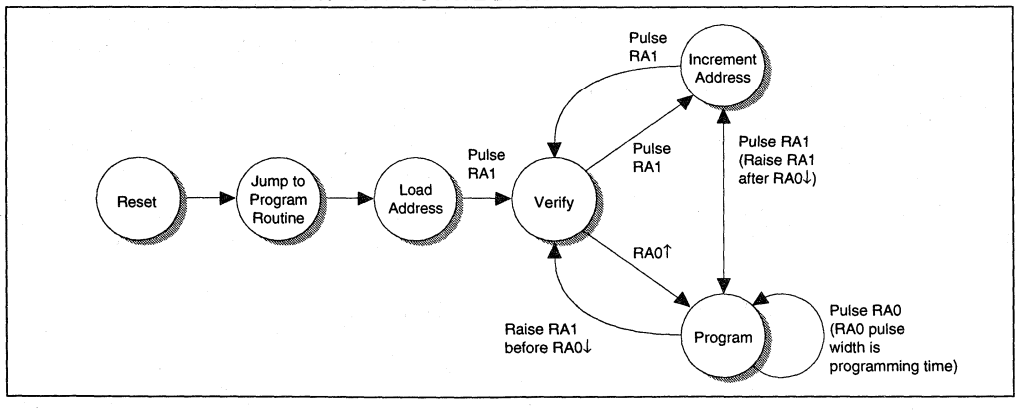
b) Increment address to program/verify the next location.

c) Allows arbitrary length programming pulse width.

d) Following a "verify" allows option to program the same location or increment and verify the next location.

e) Following a "program" allows options to program the same location again, verify the same location or to increment and verify the next location.

FIGURE 2-1: PROGRAMMING/VERIFY STATE DIAGRAM



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2.1.1 LOADING NEW ADDRESS

The program allows new address to be loaded right out of reset. A 16-bit address is presented on ports RB (high byte) and RC (low byte) and the RA1 is pulsed ($0 \rightarrow 1$, then $1 \rightarrow 0$). The address is latched on the rising edge of RA1. See timing diagrams for details. After loading an address, the program automatically goes into a "verify cycle". To load a new address at any time, the PIC17C4X must be reset and the programming mode re-entered.

2.1.2 VERIFY (OR READ) MODE

"Verify mode" can be entered from "Load address" mode, "program mode" or "verify mode". In verify mode pulsing RA1 will turn on PORTS RB and RC output drivers and output the 16-bit value from the current location. Pulsing RA1 again will increment location count and be ready for the next verify cycle. Pulsing RA0 will begin a program cycle.

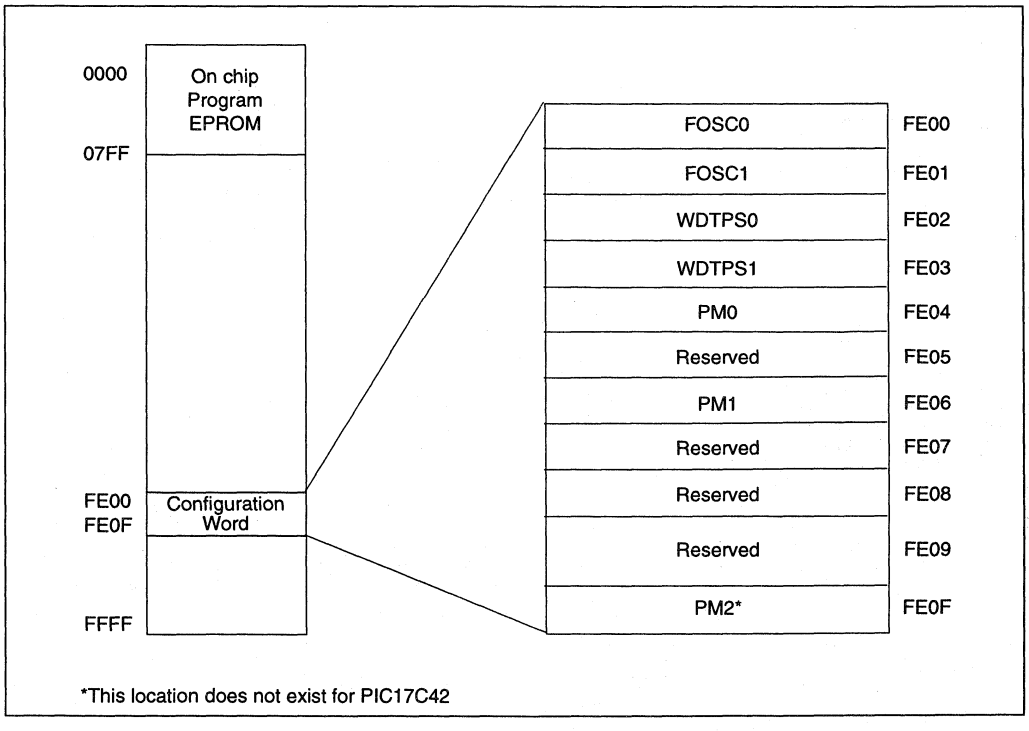
2.1.3 PROGRAM CYCLE

"Program cycle" is entered from "verify cycle" or program cycle" itself. After a verify, pulsing RA0 will begin a program cycle. 16-bit data must be presented on PORTS RB (high byte) and RC (low byte) before RA0 is raised.

The data is sampled 3 TCY cycles after the rising edge of RA0. Programming continues for the duration of RA0 pulse.

At the end of programming the user can choose one of three different routes. If RA1 is kept low and RA0 is pulsed again, the same location will be programmed again. This is useful for applying over programming pulses. If RA1 is raised before RA0 falling edge, then a verify cycle is started without address increment. Raising RA1 after RA0 goes low will increment address and begin verify cycle on the next address.

FIGURE 2-2: PIC17C4X PROGRAM MEMORY MAP



*This location does not exist for PIC17C42

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3.0 PROGRAMMING SPECIFICATIONS

FIGURE 3-1: PROGRAMMING ROUTINE FLOWCHART

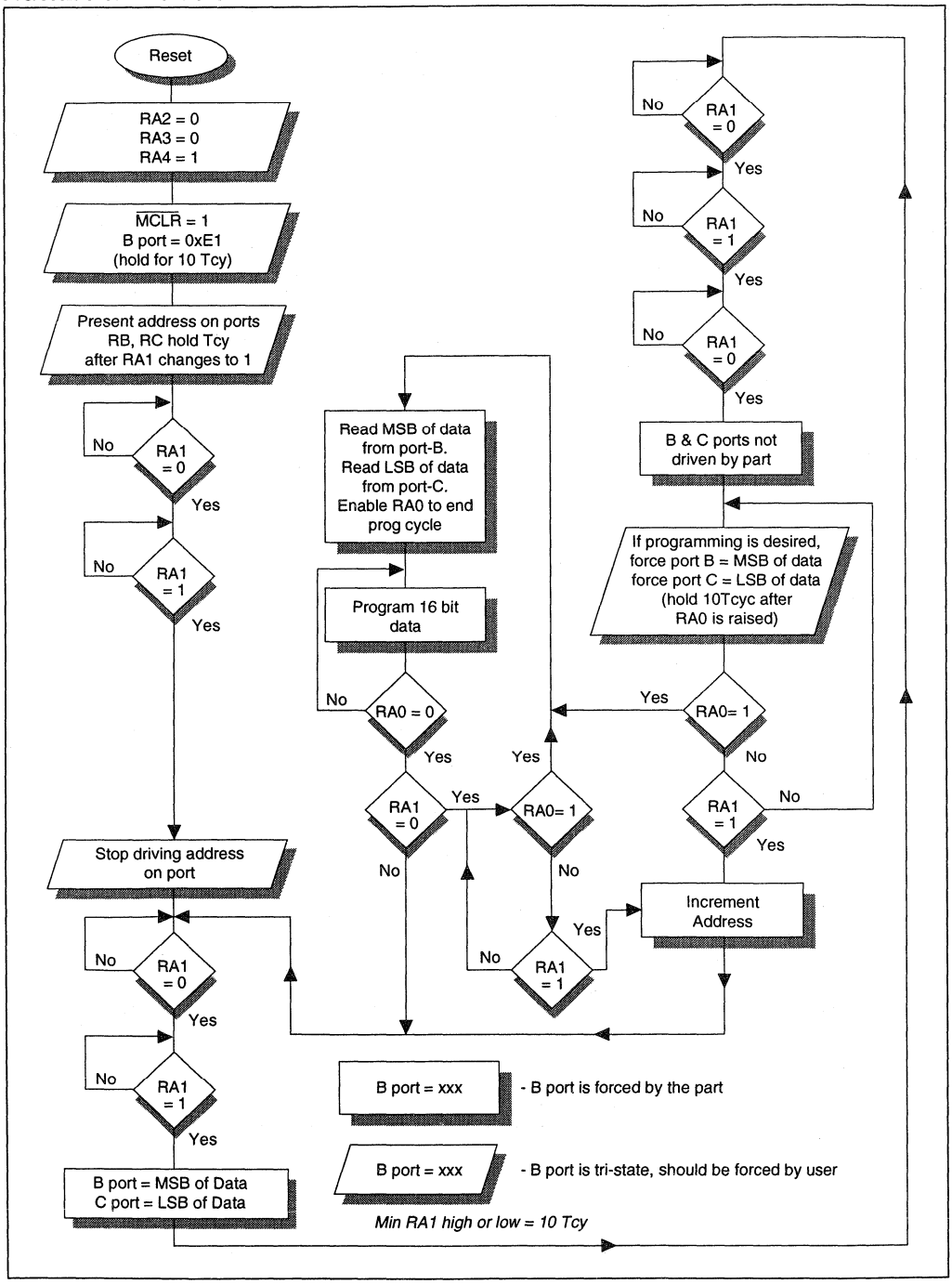

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FIGURE 3-2: RECOMMENDED PROGRAMMING ALGORITHM FOR USER EPROM

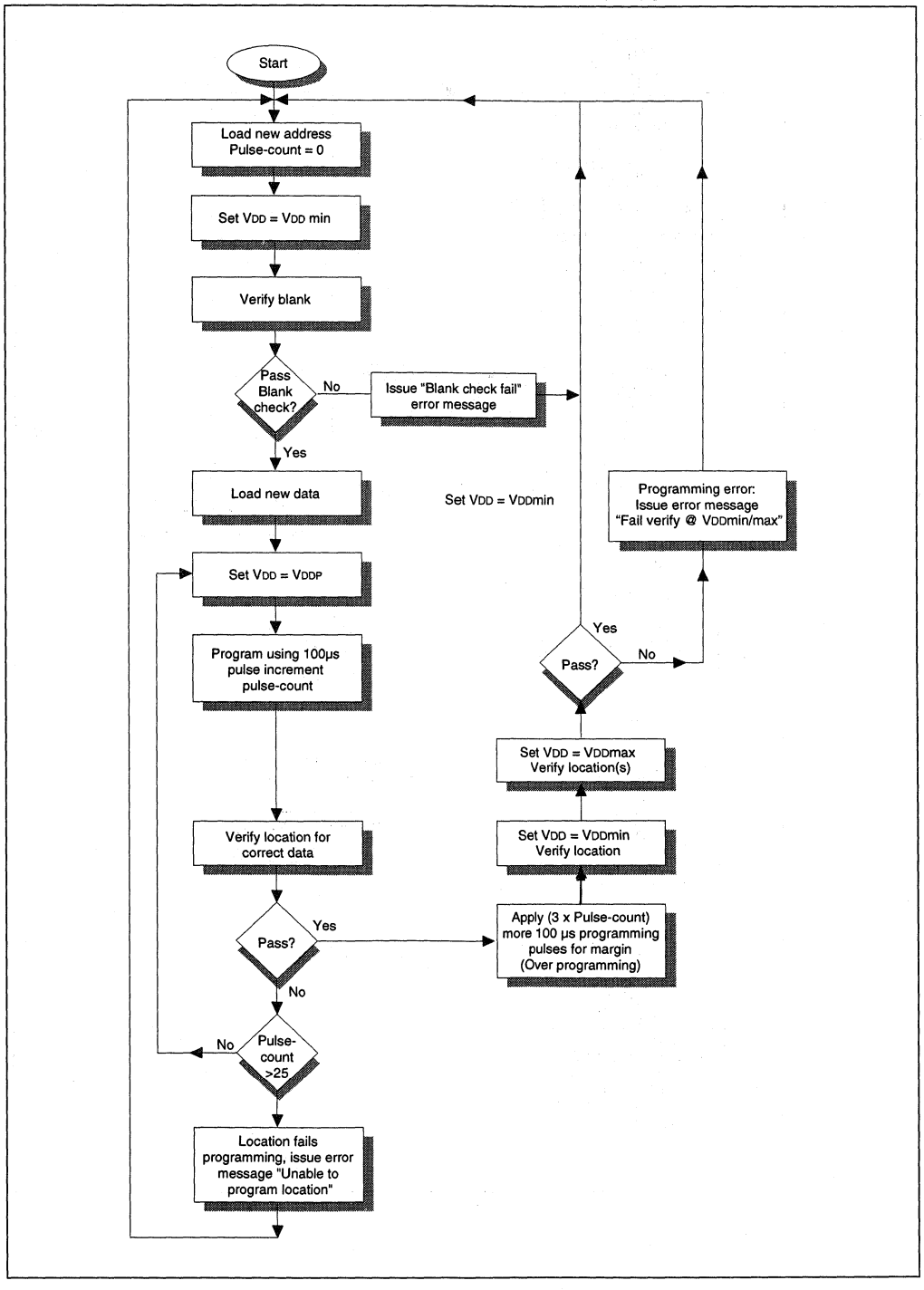

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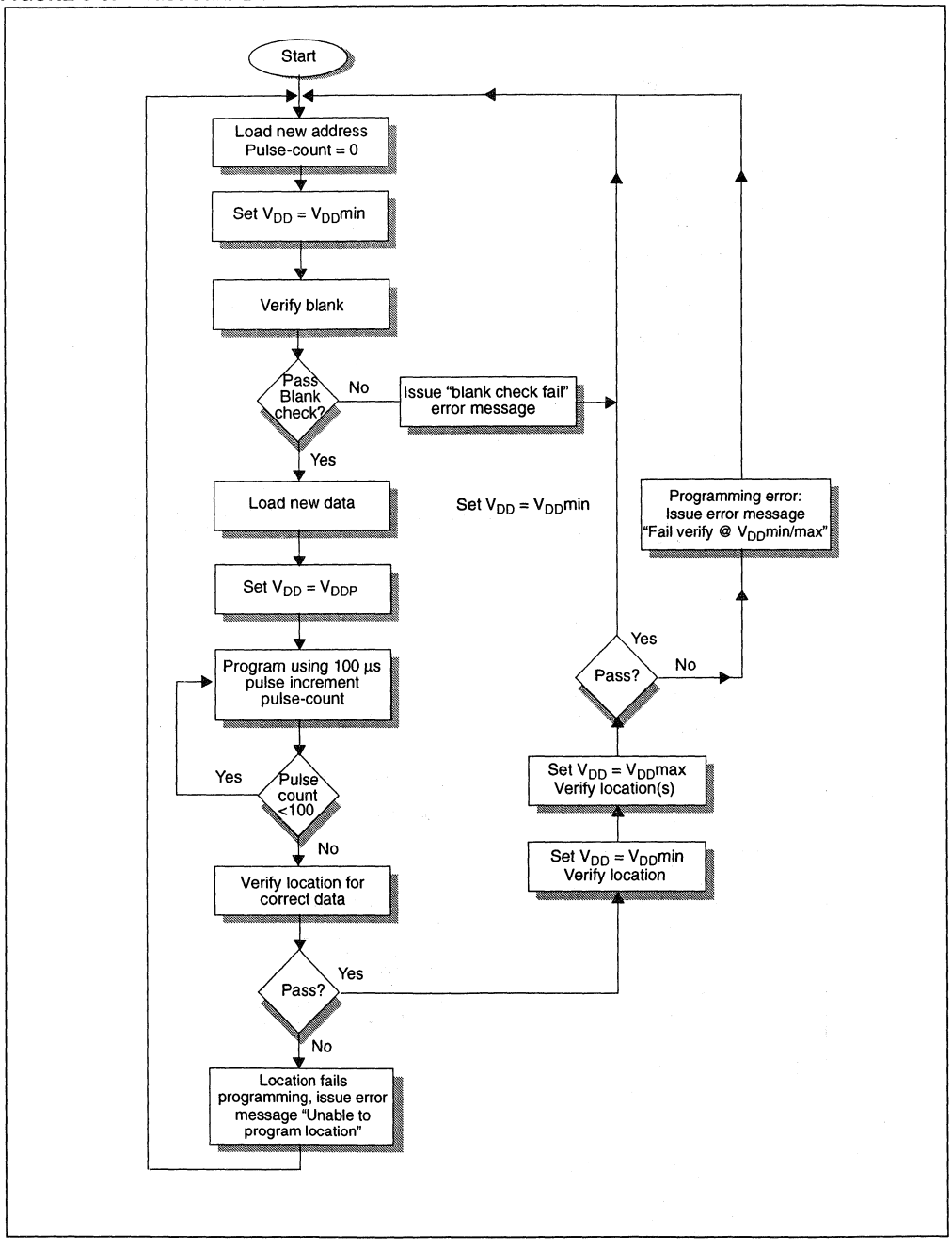
FIGURE 3-3: RECOMMENDED PROGRAMMING ALGORITHM FOR CONFIGURATION WORDS



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4.0 CONFIGURATION WORD

Configuration bits are mapped into program memory. Each bit is assigned one memory location. In erased condition a bit will read as '1'. To program a bit, the user needs to write to the memory address. The data is immaterial; the very act of writing will program the bit. The configuration word locations are shown in Table 4-3. **The programmer should not program the reserved locations to avoid unpredictable results and to be compatible with future variations of the PIC17C4X. It is also mandatory that configuration locations are programmed in the strict order starting from the first location (0xFE00) and ending with the last (0xFE0F). Unpredictable results may occur if the sequence is violated.**

4.1 Reading Configuration Word

The PIC17CXX has seven configuration locations (see Table 4-1). These locations can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. Any write to a configuration location, regardless of the data, will program that configuration bit. Reading any configuration location between 0xFE00 and 0xFE07 will place the low byte of the configuration word (see Table 4-2) into PAD<7:0> (PORTC). PAD<15:8> (PORTB) will be set to 0xFF. Reading a configuration location between 0xFE08 and 0xFE0F will place the high byte of the configuration word into PAD<7:0> (PORTC). PAD<15:8> (PORTB) will be set to 0xFF.

TABLE 4-1: CONFIGURATION BIT PROGRAMMING LOCATIONS

Bit	Address
FOSC0	0xFE00
FOSC1	0xFE01
WDTPS0	0xFE02
WDTPS1	0xFE03
PM0	0xFE04
PM1	0xFE06
PM2†	0xFE0F

†This location does not exist on the PIC17C42.

TABLE 4-2: READ MAPPING OF CONFIGURATION BITS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	—	PM1	—	PM0	WDTPS1	WDTPS0	FOSC1	FOSC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	PM2*	—	—	—	—	—	—	—

—=Unused

PM<2:0>, Processor Mode Select bits

111 = Microprocessor mode
110 = Microcontroller mode
101 = Extended Microcontroller mode
000 = Code protected microcontroller mode

WDTPS<1:0>, WDT Prescaler Select bits.

11 = WDT enabled, postscaler = 0
10 = WDT enabled, postscaler = 256
01 = WDT enabled, postscaler = 64
00 = WDT disabled, 16-bit overflow timer

FOSC<1:0>, Oscillator Select bits

11 = EC oscillator
10 = XT oscillator
01 = RC oscillator
00 = LF oscillator

* This bit does not exist on PIC17C42.

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4.2 Embedding Configuration Word Information in the Hex File

To allow portability of code, a PIC17C4X programmer is required to read the configuration word locations from the hex file when loading the hex file. If configuration word information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, all configuration word information must be included. An option to not include the configuration word information may be provided. When embedding configuration word information in the hex file, it should be to address FE00h.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 4-3: CONFIGURATION WORD

PIC17C42

To code protect:

- Protect all memory XXXXXXXXX0X0XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFE00)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read Scrambled, Write Disabled*	Read Unscrambled, Write Enabled

PIC17C42A

To code protect:

- Protect all memory 0XXXXXXXX0X0XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFE00)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read Scrambled, Write Disabled*	Read Unscrambled, Write Enabled

PIC17CR42

To code protect:

- Protect all memory 0XXXXXXX0X0XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFE00)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read Scrambled, Write Disabled*	Read Unscrambled, Write Enabled

PIC17C43

To code protect:

- Protect all memory 0XXXXXXX0X0XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFE00)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read Scrambled, Write Disabled*	Read Unscrambled, Write Enabled

PIC17CR43

To code protect:

- Protect all memory 0XXXXXXX0X0XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFE00)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read Scrambled, Write Disabled*	Read Unscrambled, Write Enabled

PIC17C44

To code protect:

- Protect all memory 0XXXXXXX0X0XXXX

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0xFE00)	Read Scrambled, Write Enabled	Read Unscrambled, Write Enabled
All memory	Read Scrambled, Write Disabled*	Read Unscrambled, Write Enabled

Legend: X = Don't care

*Write to on-chip EPROM memory is disabled. The only way these locations can be programmed is if a TABLWT instruction is issued from an "on-chip" program memory space to program an on-chip memory location.

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4.3 CHECKSUM COMPUTATION

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-4: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0xC0DE at 0 and max address
PIC17C42	MP mode	SUM[0x000:0x7FF] + CFGW & 0x005F + 0xFFA0	0xF7FF	0x79BD
	MC mode	SUM[0x000:0x7FF] + CFGW & 0x005F + 0xFFA0	0xF7EF	0x79AD
	EMC mode	SUM[0x000:0x7FF] + CFGW & 0x005F + 0xFFA0	0xF7BF	0x797D
	PMC mode	SUM_XNOR8[0x000:0x7FF] + CFGW & 0x005F + 0xFFA0	0xF7AF	0xBB73
PIC17C42A	MP mode	SUM[0x000:0x7FF] + CFGW & 0x015F	0xF95F	0x7B1D
	MC mode	SUM[0x000:0x7FF] + CFGW & 0x015F	0xF94F	0x7B0D
	EMC mode	SUM[0x000:0x7FF] + CFGW & 0x015F	0xF91F	0x7ADD
	PMC mode	SUM_XNOR8[0x000:0x7FF] + CFGW & 0x015F	0xF80F	0xBBD3
PIC17CR42	MP mode	SUM[0x000:0x7FF] + CFGW & 0x015F	0xF95F	0x7B1D
	MC mode	SUM[0x000:0x7FF] + CFGW & 0x015F	0xF94F	0x7B0D
	EMC mode	SUM[0x000:0x7FF] + CFGW & 0x015F	0xF91F	0x7ADD
	PMC mode	SUM_XNOR8[0x000:0x7FF] + CFGW & 0x015F	0xF80F	0xBBD3
PIC17C43	MP mode	SUM[0x000:0xFFF] + CFGW & 0x015F	0xF15F	0x731D
	MC mode	SUM[0x000:0xFFF] + CFGW & 0x015F	0xF14F	0x730D
	EMC mode	SUM[0x000:0xFFF] + CFGW & 0x015F	0xF11F	0x72DD
	PMC mode	SUM_XNOR8[0x000:0xFFF] + CFGW & 0x015F	0xF00F	0xB3D3
PIC17CR43	MP mode	SUM[0x000:0xFFF] + CFGW & 0x015F	0xF15F	0x731D
	MC mode	SUM[0x000:0xFFF] + CFGW & 0x015F	0xF14F	0x730D
	EMC mode	SUM[0x000:0xFFF] + CFGW & 0x015F	0xF11F	0x72DD
	PMC mode	SUM_XNOR8[0x000:0xFFF] + CFGW & 0x015F	0xF00F	0xB3D3
PIC17C44	MP mode	SUM[0x000:0x1FFF] + CFGW & 0x015F	0xE15F	0x631D
	MC mode	SUM[0x000:0x1FFF] + CFGW & 0x015F	0xE14F	0x630D
	EMC mode	SUM[0x000:0x1FFF] + CFGW & 0x015F	0xE11F	0x62DD
	PMC mode	SUM_XNOR8[0x000:0x1FFF] + CFGW & 0x015F	0xE00F	0xA3D3

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_XNOR8(a:b) = [Sum of 8-bit wide XNOR copied into upper and lower byte, of locations a to b inclusive]
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

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5.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions

Operating Temperature: +10°C ≤ TA ≤ +70°C, unless otherwise stated, (25°C is recommended)
Operating Voltage: 4.5V ≤ VDD ≤ 5.25V, unless otherwise stated.

Parameter No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions/Comments
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	IDDP	Supply current during programming			50	mA	Freq = 10MHz, VDD = 5.5V Note 3
PD3	VDDV	Supply voltage during verify	VDD min.		VDD max.	V	Note 2
PD4	VPP	Voltage on VPP/$\overline{MCLR}$ pin during programming	12.75		13.25	V	Note 1
PD6	IPP	Programming current on VPP/$\overline{MCLR}$ pin		25	50	mA	Note 3
P1	FOSCP	Osc/clockin frequency during programming	4		10	MHz	
P2	TCY	Instruction cycle	1		0.4	µs	TCY = 4/FOSCP
P3	TirV2tsH	RA0, RA1, RA2, RA3, RA4 setup before TEST↑	1			µs	
P4	TtsH2mcH	TEST↑ to $\overline{MCLR}$↑	1			µs	
P5	TbcV2irH	RC<7:0>, RB<7:0> valid to RA1 or RA0↑ :Address/Data input setup time	0			µs	
P6	TirH2bcI	RA1 or RA0↑ to RB<7:0>, RC<7:0> invalid ; Address data hold time;	10 TCY			µs	
P7	T0ckiL2rbcZ	RT↓ to RB<7:0>, RC<7:0> high impedance			8 TCY		
P8	T0ckiH2bcV	RA1↑ to data out valid			10 TCY		
P9	Tprog	Programming pulse width	10	100	1000	µs	
P10	TirH2irL	RA0, RA1 high pulse width	10 TCY			µs	
P11	TirL2irH	RA0, RA1 low pulse width	10 TCY			µs	
P12	T0ckiV2inL	RA1↑ before INT↓ (to go from prog cycle to verify w/o increment)	0			µs	
P13	TinL2rtI	RA1 valid after RA0 (to select increment or no increment going from program to verify cycle	10 TCY			µs	
P14	Tvpps	VPP setup time before RA0↑	100			µs	Note 1
P15	Tvpph	VPP hold time after INT↓	0			µs	Note 1
P16	TvdV2tsH	VDD stable to TEST↑	10			ms	
P17	TrbV2mcH	RB input (E1h) valid to VPP/$\overline{MCLR}$↑	0			µs	
P18	TmcH2rbI	RB input (E1h) hold after VPP/$\overline{MCLR}$↑	10 TCY			ns	
P19	TvpL2vdL	VDD power down after VPP power down	10			ms	

Note 1: VPP/$\overline{MCLR}$ pin must only be equal to or greater than VDD at times other than programming.
Note 2: Program must be verified at the minimum and maximum VDD limits for the part.
Note 3: These parameters are for design guidance only and are not tested nor characterized.

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FIGURE 5-1: PROGRAMMING AND VERIFY TIMINGS I

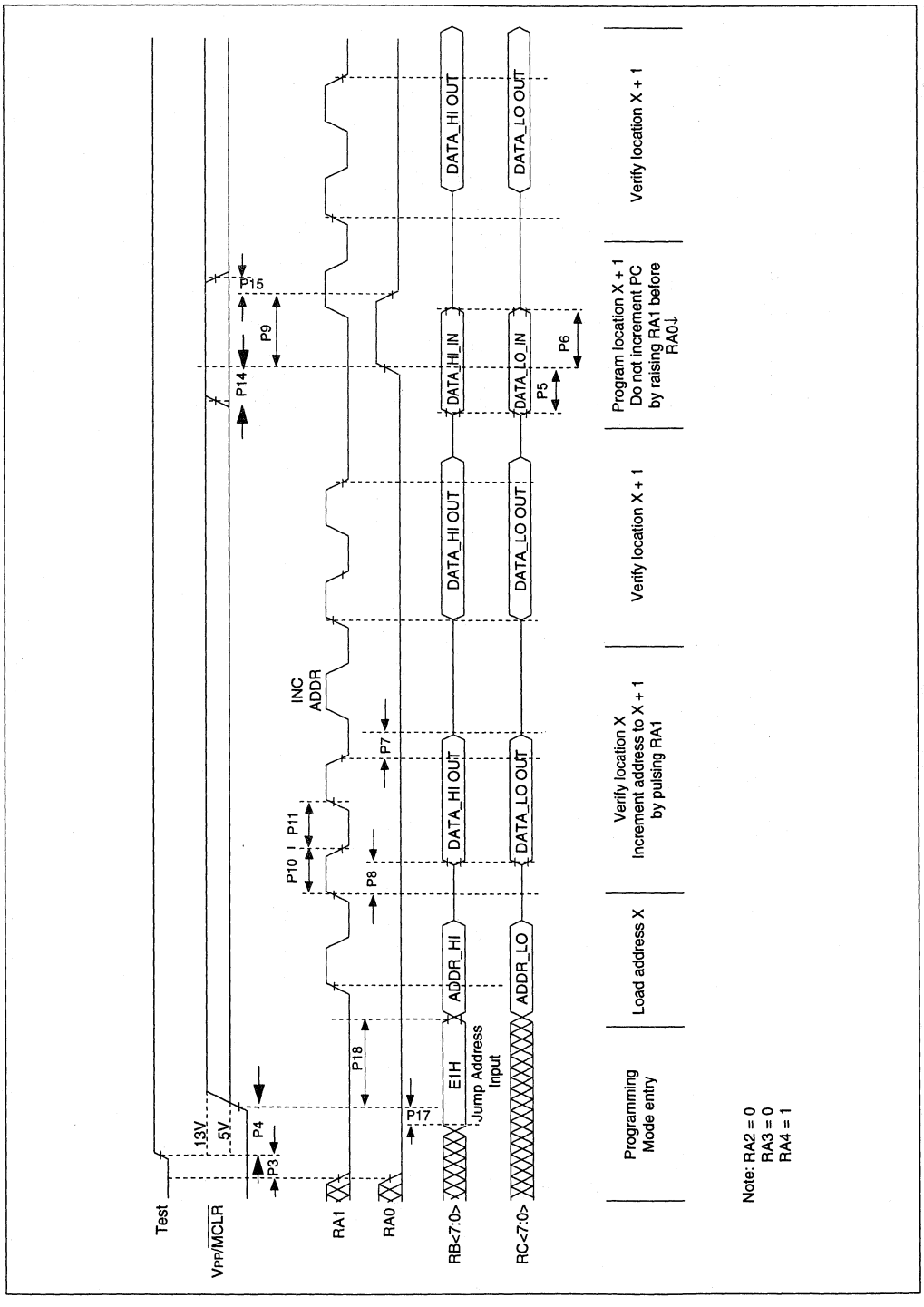

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FIGURE 5-2: PROGRAMMING AND VERIFY TIMINGS II

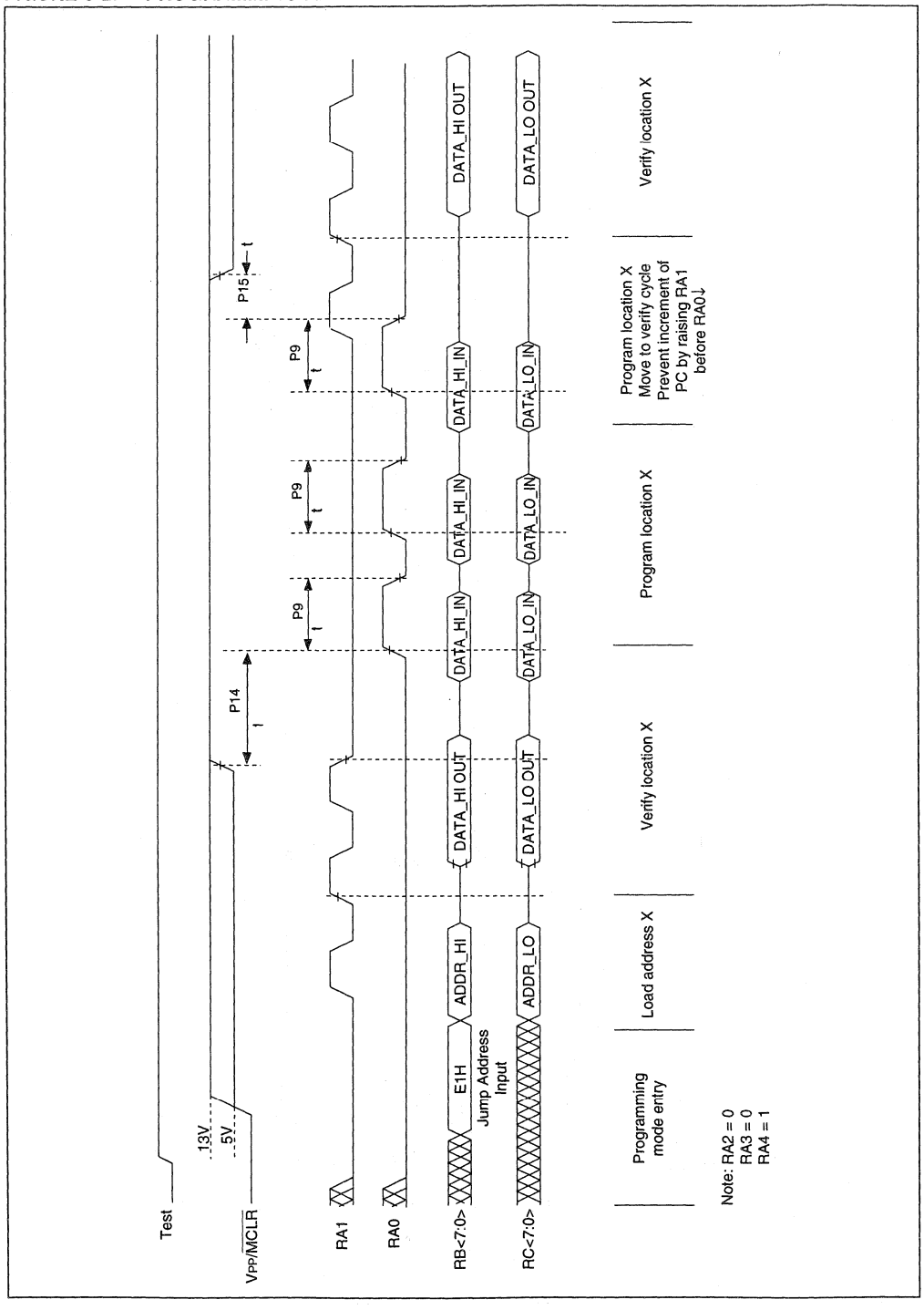

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FIGURE 5-3: PROGRAMMING AND VERIFY TIMINGS III

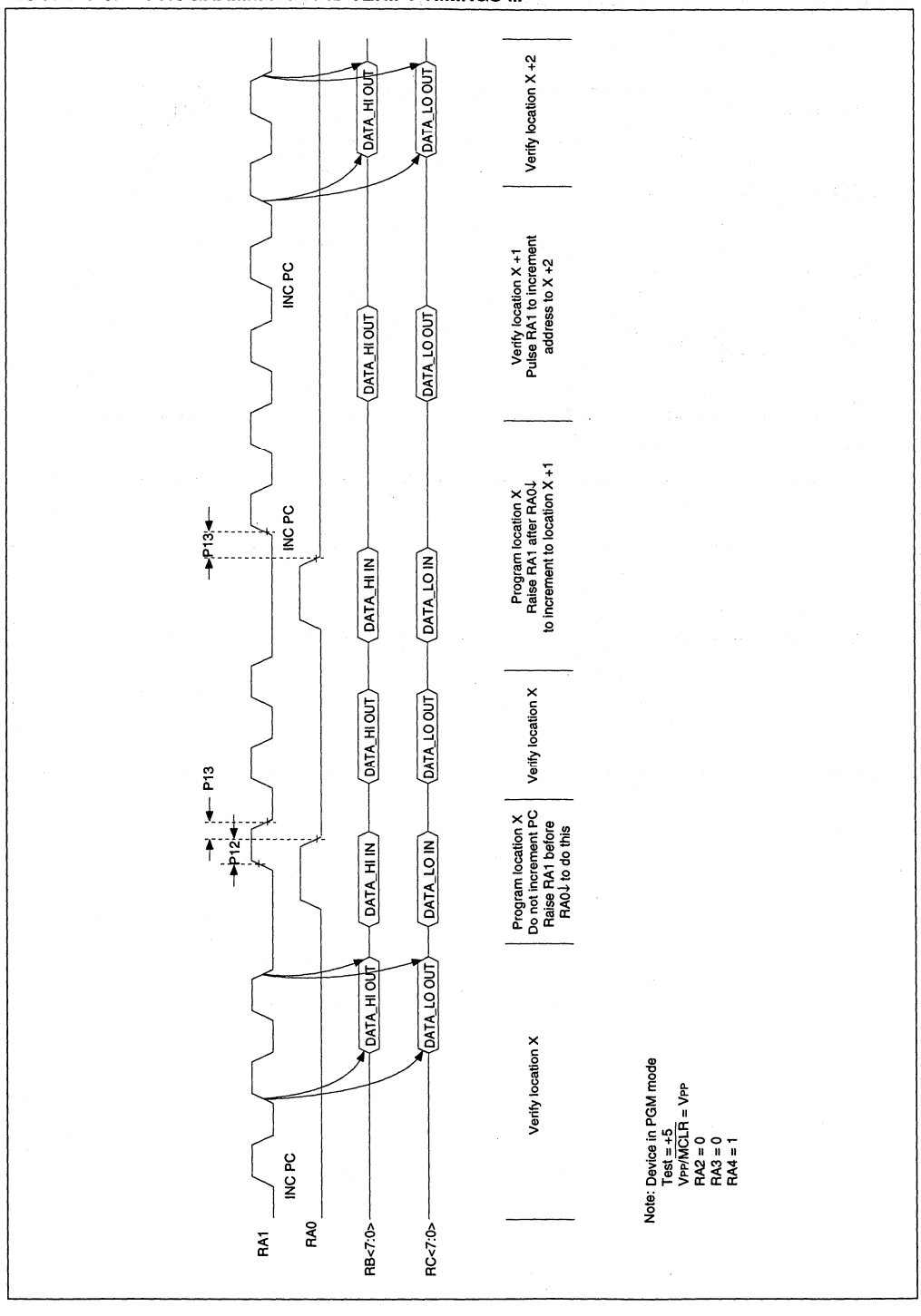

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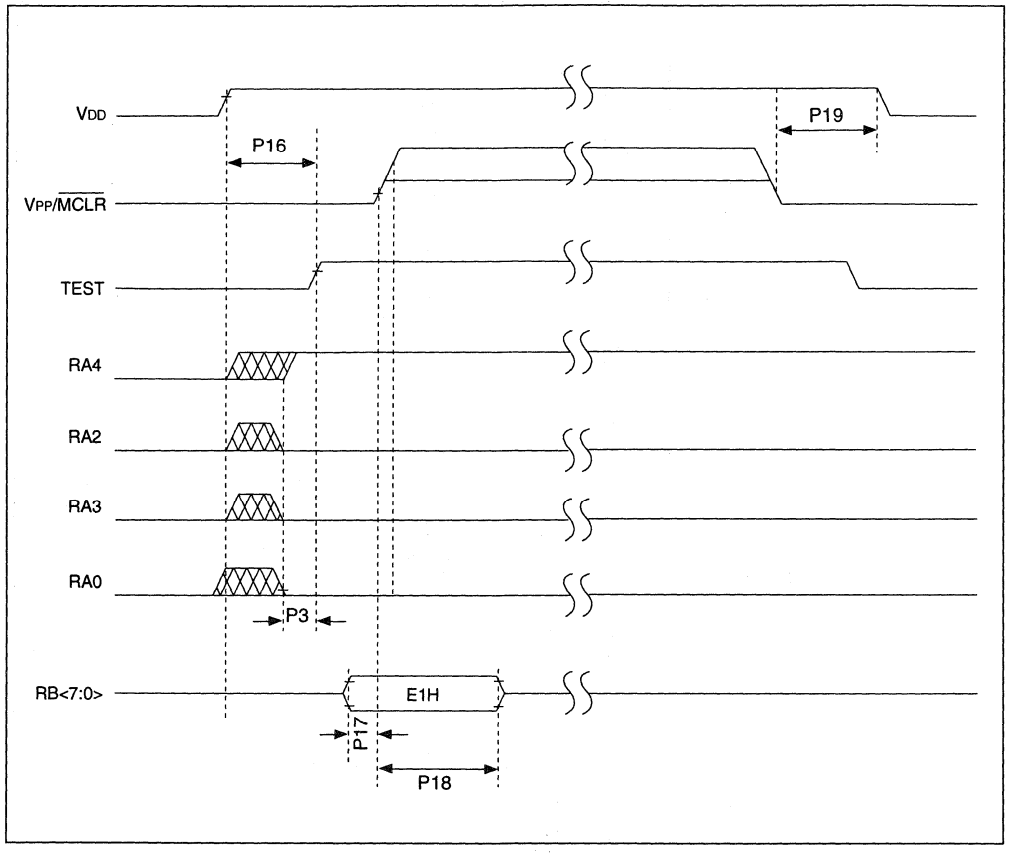
FIGURE 5-4: POWER-UP/DOWN SEQUENCE FOR PROGRAMMING



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SQTP℠ Specification for PIC16/17

Serialized Quick Turn Programming Specification for PIC16/17

OVERVIEW

Serialization is a method of programming PIC16/17 microcontrollers whereby each chip is programmed with a slightly different code. Typically, all locations are programmed with the same basic code except for a few contiguous bytes which are programmed with a different number (referred to as 'key' or 'ID number' or 'serial number') in each member. Typical applications of such programming are remote transmitters for car alarms or garage door openers where each unit must have a different access code.

Microchip offers a flexible SQTP program, whereby a customer can simply specify the nature of serialization. The 'serial number' generation and programming will be taken care of by the factory.

1.0 SERIALIZATION SCHEME SUPPORTED

1.1 Locations:

The serial number must reside in contiguous locations with up to sixteen locations used. Furthermore these locations must be coded as RETLW NN, where NN= 8-bit random code, in the finished product. For details on how the `RETLW` instruction is typically used for serialization purposes, please see Appendix A. The customer code must be supplied without the serial code in these locations. These locations must be blank or the assembled value of a `RETLW H'FF'` instruction. in the customer code provided to Microchip. Microchip will insert the serial code at these locations during programming. Hex files must be in Intel hex 8-bit merged format. See Appendix B for details.

1.2 Numbering Schemes:

Random: Truly random numbers are generated. However, there is no guarantee that the numbers will be non-repeating although the probability of such an occurrence will be infinitesimally small for a reasonably large field.

Pseudo-Random: Pseudo-random sequences of requested length (e.g. 32-bit long if four locations are used) starting with a 'seed value' selected by the factory. The customer may optionally specify the starting value. Pseudo-random sequences, by definition are non-repeating until all possible values are used.

Sequential: Sequential numbers are generated. User specifies the "starting number" and an increment value. In sequential numbering, the least significant digit is in the lowest memory location. The increment value must be between 1 and 255.

Numbers are always in hex and not in BCD or any other format.

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2.0 PROGRAMMING SEQUENCE

The factory will program the "basic code" first, then program the serial number and finally program the code-protection fuse. Program memory will be verified at each stage except after code protection. Optionally, the factory may choose to program the "basic code" and the "serial number" at the same time. The customer may specify an ID number (four hex digits) to be programmed in the ID locations or elect to leave them unprogrammed.

3.0 SAMPLES

Three (3) verification samples will be provided. These will be programmed with factory selected random or sequential codes in the serialization locations. The three parts will be programmed with three different serial codes. If order entry has been completed, then the samples will reflect the first three codes. If code protection is requested, then one of the three samples will be code protected.

4.0 THE FOLLOWING LIMITATIONS APPLY TO THE SQTP PROGRAM

1. During shipment of serialized parts, no particular sequence can be guaranteed.
2. In sequential or pseudo-random numbering scheme, there may be missing serial numbers (e.g. due to QC sampling).
3. A list of serial numbers programmed can not be provided, nor will such a list be generated or maintained by Microchip.
4. For sequential and pseudo-random numbering schemes, Microchip will maintain last number used in last shipment and use the next number as the starting number for the next shipment. The customer should be prepared to provide a "new starting number" in the event the flow is disrupted due to unforeseen events.

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APPENDIX A:

Implementing a table in the program memory of PIC16C5X and PIC16C5XA:

The PIC16C5X and the PIC16C5XA family uses Harvard architecture, in which the program memory is separate from data memory. All instructions operate on data that is fetched from the register file or data memory. Since there are no instructions to read from or write to the program memory, simply storing data words in program memory is of no use. There is, however, a simple and elegant way to implement constant tables in the program memory by using the RETLW instruction. This instruction returns from a subroutine as well as loads an 8-bit constant into the W register. The following example shows how to get a byte of "serial information" from the table stored at location 000h in PIC16C54:

```
            ORG    0        ;store serial numbers
            RETLW  0FFh
            RETLW  0FFh
            RETLW  0FFh
            RETLW  0FFh
            RETLW  0FFh
            RETLW  0FFh
            RETLW  0FFh
            RETLW  0FFh     ;end of serial
                            ;numbers
     •
     •
main_prog   ORG    XYZ      ;This is main program
     •
     •
     MOVLW  byte_num        ;byte_num = 0 for 1st
                            ;byte
     CALL   get_1byte;
     •
     •
get_1byte   MOVWF  PC       ;write W to program
                            ;counter
                            ;W = offset = 0 for
                            ;1st byte
                            ;end of get_1byte sub
                            ;routine
     •
     •
     •
     END
```

The next example shows how a serial number may reside at location other than 000h.

```
main_prog ORG   XYZ      ;This is main program
     •
     •
     MOVLW byte_num      ;byte_num = 0 for 1st
                         ;byte
     CALL  get_1byte;
     •
     •
get_1byte ADDWFPC       ;W = offset
          RETLW  0ffh   ;
          RETLW  0ffh   ;
          RETLW  0ffh   ;
          RETLW  0ffh   ;
          RETLW  0ffh   ;
          RETLW  0ffh   ;
          RETLW  0ffh   ;
          RETLW  0ffh   ;end of serial
                        ;numbers
     •
     •
     END
```

APPENDIX B:

Standard hex file format for serial programming:

The hex file containing the 'serial numbers' will be in Intel hex 8-bit format. Since the PIC16C5X and the PIC16C5XA have 12-bit data words, all addresses are doubled in this hex format. Each line of the hex file will be for a new part. Each line can contain only up to 16 bytes (i.e. eight PIC16C5X, PIC16C5XA instruction words). The format is as follows:

:NNAAAATTHHHHHH.....HHCC

where:

NN = byte count on current line (max 10h allowed)

AAAA = address in four hex digits

TT = record type, always 00 except 01 for EOF

HH = Two digit hex data byte

CC = Two digit hex checksum

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NOTES:

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MICROCHIP

SECTION 18
FlexROM™ MICROCONTROLLER PRODUCT SPECIFICATIONS

FlexROM™ Product Introduction 18-1
PIC16FR5X *FlexROM*™-Based 8-Bit CMOS Microcontroller Series 18-3
Enhanced PIC16FR5X *FlexROM*™-Based 8-Bit CMOS Microcontroller Series 18-5
PIC16FR6X 8-Bit CMOS *FlexROM*™ Microcontrollers 18-7
PIC16FR62X *FlexROM*™-Based 8-Bit CMOS Microcontroller 18-9
PIC16FR7X 8-Bit CMOS *FlexROM*™ Microcontrollers with A/D Converter 18-11
PIC17FR4X High Performance 8-Bit *FlexROM*™ Microcontroller 18-13

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FlexROM™ Product Introduction

Microchip's *FlexROM*™ devices are a migration path for customers whose application volume is considered to be at the same level as a mid- to high-volume ROM application. *FlexROM* bridges the customer requirement from OTP devices to those of ROM devices. *FlexROM* devices are either programmed at Microchip's factory or by a certified distributor. This allows faster turn times than with standard ROM devices.

The *FlexROM* program requires an NRE charge as well as a minimum lead time, but the terms and conditions are more favorable than standard ROM devices. For more information concerning FlexROM requirements, please contact your local Microchip Sales Office.

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MICROCHIP

PIC16FR5X

FlexROM™-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16FR54
- PIC16FR55
- PIC16FR56
- PIC16FR57

High-Performance RISC CPU Features:

- Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

Device	Pins	I/O	*FlexROM*	RAM
PIC16FR54	18	12	512	25
PIC16FR55	28	20	512	24
PIC16FR56	18	12	1K	25
PIC16FR57	28	20	2K	72

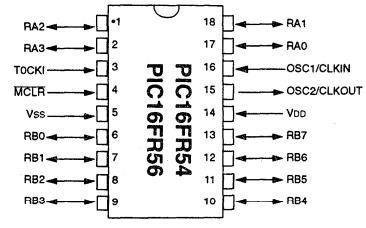
- 12-bit wide instructions
- 8-bit wide data path
- Seven or eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

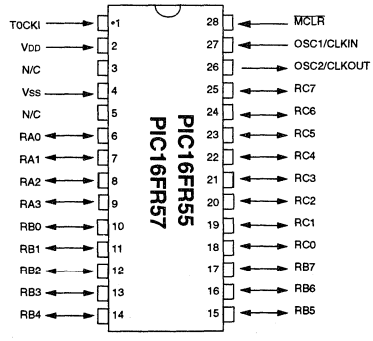
- 8-bit real time clock/counter (Timer0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power saving, low frequency crystal

Pin Diagrams

PDIP, SOC



PDIP, SOIC



CMOS Technology:

- Low-power, high-speed CMOS *FlexROM* technology
- Fully static design
- Wide-operating voltage range:
  - *FlexROM* Commercial/Industrial 2.5V to 6.25V
- Low-power consumption
  - < 2 mA typical @ 5.0V, 4 MHz
  - 15 µA typical @ 3.0V, 32 kHz
  - < 3 µA typical standby current (with WDT disabled) @ 3.0V, 0°C to 70°C

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NOTES:

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ENHANCED PIC16FR5X

FlexROM™-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16FR54A
- PIC16FR58A

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

Device	Pins	I/O	*FlexROM*	RAM
PIC16FR54A	18	12	512	25
PIC16FR58A	18	12	2K	73

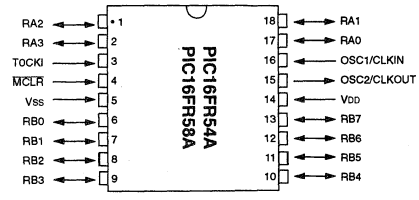
- 12-bit wide instructions
- 8-bit wide data path
- Seven special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

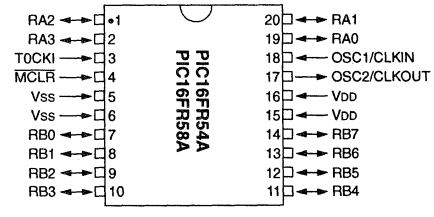
- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Selectable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power saving, low frequency crystal

Pin Diagrams

PDIP, SOIC



SSOP



CMOS Technology:

- Low-power, high-speed CMOS *FlexROM* technology
- Fully static design
- Wide-operating voltage range:
  - *FlexROM* Commercial/Industrial 2.5V to 6.25V
- Low-power consumption
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 kHz
  - < 0.6 µA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

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NOTES:

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MICROCHIP

PIC16FR6X

8-Bit CMOS *FlexROM*™ Microcontrollers

Devices included in this data sheet:

- PIC16FR62A
- PIC16FR63
- PIC16FR64A
- PIC16FR65
- PIC16FR65A

PIC16FR6X Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS *FlexROM* technology
- Fully static design
- Wide operating voltage range: 2.5V to 6.0V
- Commercial and Industrial Temperature Range
- Low-power consumption:
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

PIC16FR6X Peripheral Features:

- Timer0: 8-bit timer/counter with prescaler
- Timer1: 16-bit timer/counter with prescaler. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with period register, prescaler and postscaler
- Capture/Compare/PWM module(s)
- Capture is 16-bit, max resolution 12.5 ns, compare is 16-bit, max resolution 200 ns, max. PWM resolution is 10-bit.
- Synchronous Serial Port (SSP) with SPI and I^2C™
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bits wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls
- Brown-out dectection circuitry for Brown-out Reset (BOR)

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PIC16FR6X Features	62A	63	64A	65	65A
Program Memory (*FlexROM*)	2K	4K	2K	4K	4K
Data Memory (Bytes)	128	192	128	192	192
I/O Pins	22	22	33	33	33
Parallel Slave Port	—	—	Yes	Yes	Yes
Capture/Compare/PWM Module	1	2	1	2	2
Timer Modules	3	3	3	3	3
Serial Communication	SPI/I^2C	SPI/I^2C, USART	SPI/I^2C	SPI/I^2C, USART	SPI/I^2C, USART
Brown-out Reset	Yes	Yes	Yes	—	Yes
Interrupt Sources	7	10	8	11	11
Sink/Source Current (mA)	25/25	25/25	25/25	25/25	25/25

I^2C is a trademark of Philips Corporation. SPI is a trademark of Motorola Corporation.

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NOTES:

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PIC16FR62X

FlexROM™-Based 8-Bit CMOS Microcontroller

Devices included in this Data Sheet:

- PIC16FR620
- PIC16FR621
- PIC16FR622

High Performance RISC CPU Features:

- Only 35 instructions to learn
- All single cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle

Device	Program Memory	Data Memory
PIC16FR620	512	80
PIC16FR621	1K	80
PIC16FR622	2K	128

- Interrupt capability
- 16 special function hardware registers
- 8 level deep hardware stack
- Direct, indirect and relative addressing modes

Peripheral Features:

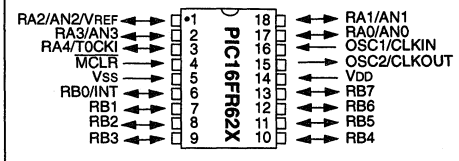
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
  - 2 analog comparators
  - Programmable on-chip voltage reference (VREF) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs can be output signals
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

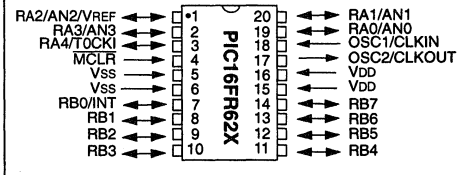
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Selectable code protection
- Power saving SLEEP mode
- Selectable oscillator options

Pin Diagrams

PDIP, SOIC



SSOP



CMOS Technology:

- Low-power, high-speed CMOS *FlexROM* technology
- Fully static design
- Wide operating voltage range
  - 2.5V to 6.0V
- Commercial and industrial temperature range
- Low power consumption
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz
  - < 1 µA typical standby current @ 3V

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NOTES:

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MICROCHIP

PIC16FR7X

8-Bit CMOS *FlexROM*™ Microcontrollers with A/D Converter

Devices included in this Data Sheet:

- PIC16FR71
- PIC16FR710
- PIC16FR711
- PIC16FR72
- PIC16FR73/73A
- PIC16FR74/74A

PIC16FR7X Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Selectable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- 8-bit multichannel Analog to Digital (A/D) converter
- Low-power, high-speed CMOS *FlexROM* technology
- Fully static design
- Wide operating voltage range: 3.0V to 6.0V
- High Sink/Source Current 25/25 mA
- Commercial and Industrial Temperature Range
- Low-power consumption:
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 kHz
  - < 1 µA typical standby current

PIC16FR7X Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module(s)
- Capture is 16-bit, max. resolution 12.5 ns, compare is 16-bit, max. resolution 200 ns, max. PWM resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™ and I^2C™
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP) 8-bit wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls
- Brown-out detection circuitry for Brown-out Reset (BOR)

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PIC16FR7X Features	PIC16FR71	PIC16FR710	PIC16FR711	PIC16FR72	PIC16FR73	PIC16FR73A	PIC16FR74	PIC16FR74A
Program Memory (*FlexROM*)	1K	512	1K	2K	4K	4K	4K	4K
Data Memory (Bytes)	36	36	68	128	192	192	192	192
I/O Pins	13	13	13	22	22	22	33	33
Parallel Slave Port	—	—	—	—	—	—	Yes	Yes
Capture/Compare/ PWM Modules	—	—	—	1	2	2	2	2
Timer Modules	1	1	1	3	3	3	3	3
A/D Channels	4	4	4	5	5	5	8	8
Serial Communication	—	—	—	SPI/I^2C	SPI/I^2C, USART	SPI/I^2C, USART	SPI/I^2C, USART	SPI/I^2C, USART
Brown-out Reset	—	Yes	Yes	Yes	—	Yes	—	Yes
Interrupt Sources	4	4	4	8	11	11	12	12

I^2C is a trademark of Philips Corporation.
SPI is a trademark of Motorola Corporation.

NOTES:

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MICROCHIP

PIC17FR4X

High-Performance 8-Bit CMOS *FlexROM*™ Microcontroller

Devices included in this data sheet:

- PIC17FR42A
- PIC17FR43
- PIC17FR44

High-Performance RISC CPU Features:

- Only 58 single word instructions to learn
- All single cycle instructions (160 ns) except for program branches which are two-cycle and table reads/writes
- Operating speed:
  - DC - 33 MHz clock input
  - DC - 121 ns instruction cycle
- Interrupt capability
- 16 levels deep hardware stack
- Direct, indirect and relative addressing modes
- Internal/External program memory execution
- 64K x 16 addressable program memory space

High-Performance DSP-like Features:

- Hardware Multiplier (single cycle)
- 8.25 MIPs throughput

Peripheral Features:

- 33 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - RA2 and RA3 are open collector, high voltage (12V), high current (60 mA), I/O
- Two capture inputs and two PWM outputs
  - Captures are 16-bit, max resolution 160 ns
  - PWM resolution is 1- to 10-bit
- TMR0: 16-bit timer/counter with 8-bit programmable prescaler
- TMR1: 8-bit timer/counter
- TMR2: 8-bit timer/counter
- TMR3: 16-bit timer/counter
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)

Special Microcontroller Features:

- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Selectable code-protection
- Power saving SLEEP mode
- Selectable oscillator options

CMOS Technology

- Low-power, high-speed CMOS *FlexROM* technology
- Fully static design
- Wide operating voltage range (2.5V to 6.0V)
- Commercial and Industrial Temperature Range
- Low-power consumption
  - < 5 mA @ 5V, 4 MHz
  - 100 μA typical @ 4.5V, 32 kHz
  - < 1 μA typical standby current @ 5V

PIC17FR4X Features	PIC17FR42A	PIC17FR43	PIC17FR44
Program Memory (*FlexROM*)	2K	4K	8K
Data Memory (Bytes)	232	454	454
I/O Pins	33	33	33
Capture inputs	2	2	2
PWM outputs	2	2	2
Timer Modules	4	4	4
Serial Communication	SPI, I^2C, USART	SPI, I^2C, USART	SPI, I^2C, USART
Interrupt Sources	11	11	11
Sink/Source Current (mA)	25/25	25/25	25/25

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SECTION 19
LOGIC PRODUCTS

AY0438 32-Segment CMOS LCD Driver 19-1

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AY0438

32-Segment CMOS LCD Driver

FEATURES

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS process for: wide supply voltage range, low- power operation, high-noise immunity, wide temperature range
- CMOS and TTL-compatible inputs
- Electrostatic discharge protection on all pins
- Cascadable
- On-chip oscillator
- Requires only three control lines

APPLICATIONS

- Industrial displays
- Consumer product displays
- Telecom product displays
- Automotive dashboard displays

DESCRIPTION

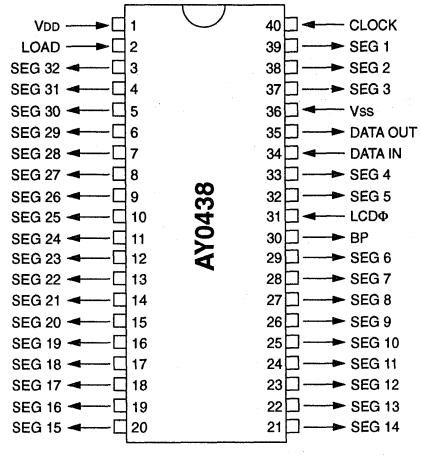
The AY0438 is a CMOS integrated device that drives a liquid crystal display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The AY0438 can drive any standard or custom parallel drive LCD display, whether it be field effect or dynamic scattering; 7-, 9-, 14- or 16-segment characters; decimals; leading + or -; or special symbols. Several AY0438 devices can be cascaded. The AC frequency of the LCD waveforms can either be supplied by the user or generated by attaching a capacitor to the LCD input, which controls the frequency of an internal oscillator.

The AY0438 is available in 40-lead dual in-line plastic and 44-lead PLCC packages. Unpackaged dice are also available.

PIN DIAGRAMS

40-Lead Dual In-line



44 PLCC

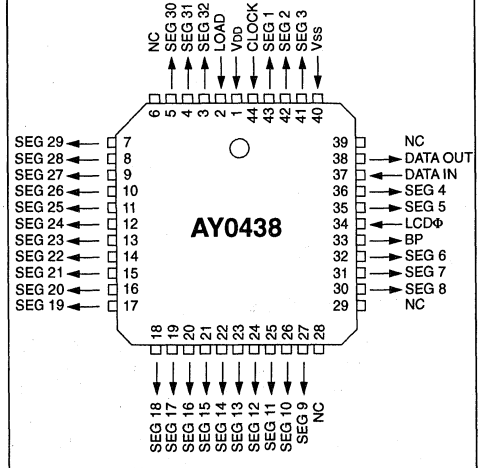


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FIGURE 1: PIN DESCRIPTIONS

Pin # (PDIP Only)	Name	Direction	Description
1	VDD	-	Supply voltage
2	Load	Input	Latch data from registers
3-29, 32, 33, 37-39	Seg 1-32	Output	Direct drive outputs
30	BP	Output	Backplane drive output
31	LCDΦ	Input	Backplane drive input
34	Data In	Input	Data input to shift register
35	Data Out	Output	Data output from shift register
36	VSS	Ground	Ground
40	Clock	Input	System clock input

FIGURE 2: BLOCK DIAGRAM

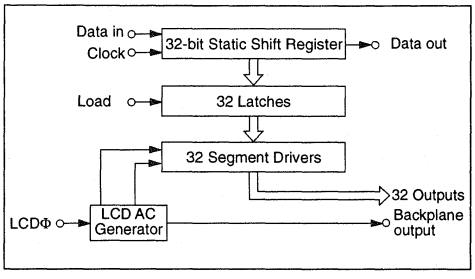


FIGURE 3: BACKPLANE AND SEGMENT OUTPUT

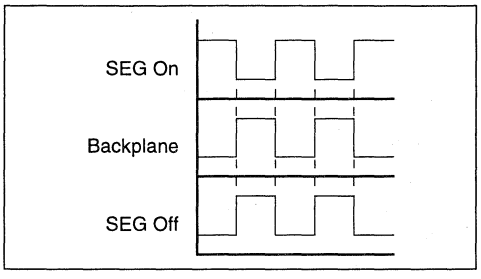
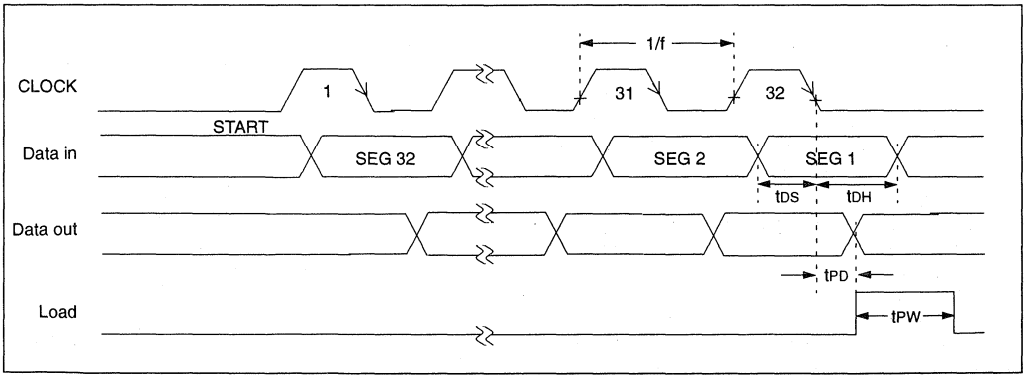


FIGURE 4: TIMING DIAGRAM



1.0 OPERATION:

1.1 Data In and Clock

The shift register shifts and outputs on the falling edge of the clock. Every clock falling edge does a logical left shift. As an example, if 32 clock pulses are supplied as in Figure 4, then the data input at the first clock will output at SEG 32, and the last data input (# 32) will output at SEG 1 when a LOAD signal is enabled (Figure 2). It is recommended that a complete 32 bit transfer be done every time the outputs are updated. A logic 1 at the Data In causes the corresponding segment to be enabled or visible, i.e. the output at Segment Output is 180° out-of-phase with the Backplane output (Figure 3).

1.2 Load

A logic 1 at the Load input (Figure 2) causes the parallel load of the data in the shift register into the latches that control the segment drivers. If the Load signal is tied high, then the latches become transparent and the segment drivers are always connected to the shift registers.

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1.3 LCDϕ

LCDϕ can be driven by an external signal or by connecting a capacitor between LCDϕ and ground (GND), which will enable the on-chip oscillator required to generate the backplane output voltage. Figure 5 shows the relationship between capacitance value and output frequency. Leaving the LCDϕ input unconnected is not recommended. When driven by an external clock, the backplane output is in phase with the input clock. When cascading two AY0438 devices (Figure 6 and Figure 7), the backplane output can be generated using a capacitor to GND on the first AY0438. This backplane output can then be connected to the LCDϕ input of the second AY0438. The backplane output of the second device is then used to drive the backplane of the LCD module.

FIGURE 5: OSCILLATOR FREQUENCY GRAPH (TYPICAL @ 25°C)

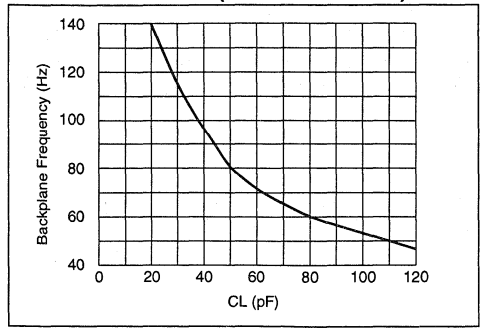


FIGURE 6: CASCADING TWO AY0438 DEVICES

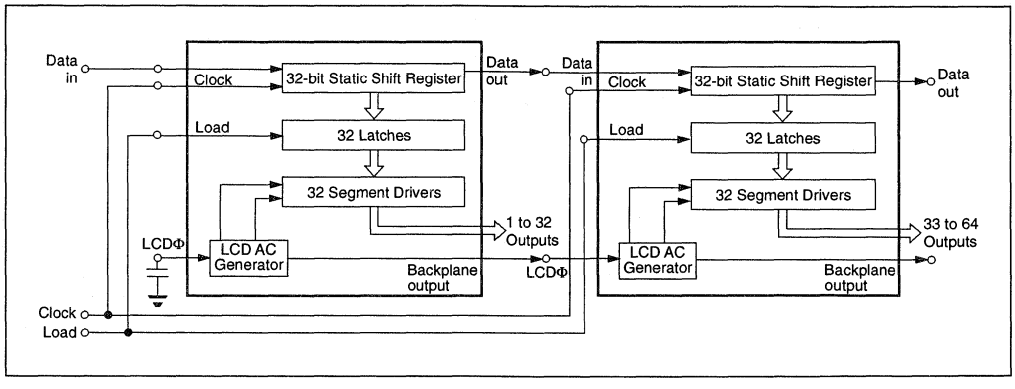
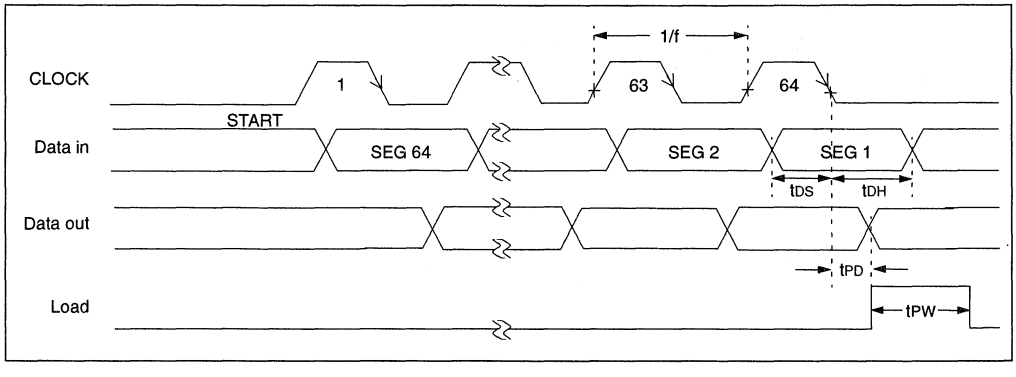


FIGURE 7: CASCADE TIMING DIAGRAM



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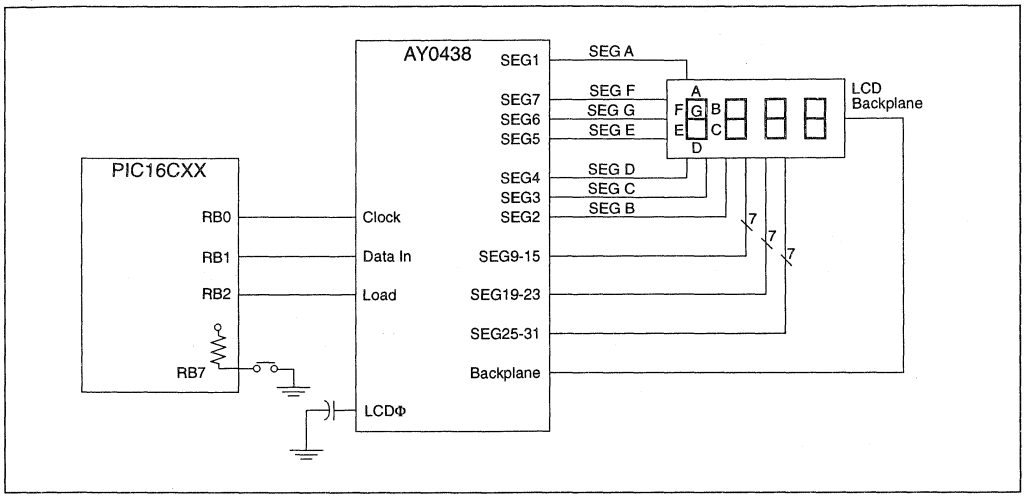
1.4 General

In order to avoid any race conditions, the Data In and Load signals should not be changed during a falling edge of the Clock. Figure 4 and Figure 7 show a typical timing diagram for a 32 segment and 64 segment LCD module.

1.5 Interfacing to a LCD Module and PIC16CXX Device

Figure 8 shows a typical layout of an AY0438 connected to a LCD module and interfaced to a PIC16CXX family device. Example 1 lists code used to program the PIC16CXX device. This code was complied using MPASM.

FIGURE 8: INTERFACING TO A LCD MODULE AND PIC16CXX DEVICE



EXAMPLE 1: EXAMPLE CODE

```
;*************************************************************************
;This program shows an interface between a PIC16CXX device
;and the AY0438 LCD controller to control a 7 Segment
;4 digit LCD module.
;The PIC16CXX interface to the AY0438 Hardware:
;
;       PORTB bit 0 --> CLK
;       PORTB bit 1 --> DATA IN
;       PORTB bit 2 --> LOAD
;
;The LCD module is connected to the AY0438 as follows:
;       Most Significant digit  --> seg1 to seg7
;       3rd Significant digit   --> seg9 to seg15
;       2nd Significant digit   --> seg17 to seg 23
;       Least Significant digit --> seg25 to seg 31
;
```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```
;The DP are not connected, but can be connected to seg8, 16, 24 & 32.
;For each digit, the segments are connected as:
;       Seg A --> seg(8*n + 1)
;       Seg B --> seg(8*n + 2)
;       Seg C --> seg(8*n + 3)
;       Seg D --> seg(8*n + 4)
;       Seg E --> seg(8*n + 5)
;       Seg F --> seg(8*n + 6)
;       Seg G --> seg(8*n + 7)
;where n = 0, 1, 2 and 3 for MSD, 3rdSD, 2ndSD and LSD respectively.
;The firmware uses the values in registers:
;       MSD, THRDSD, SCNDSD and LSD   to determine the values to be
;pulsed to the AY0438.
;In this example, a pushbutton connected to PORTB bit 7
;is checked periodically to see if it has been pressed. If so,
;the LCD values in locations MSD to LSD are updated.
;*****************************************************************************
        list p=16c71,f=inhx8m
;
;
MSD     equ     0x20
THRDSD  equ     0x21
SCNDSD  equ     0x22
LSD     equ     0x23
count   equ     0x24
temp    equ     0x25
PORTB   equ     0x06
#define CLK     PORTB,0
#define DATAIN  PORTB,1
#define LOAD    PORTB,2
#define UPDATELCD PORTB,7
w       equ     0
STATUS  equ     0x03
C       equ     0
RP0     equ     5
OPTION  equ     0x81
RBPU    equ     7
PCL     equ     0x02
PCLATH  equ     0x0A
;
;
        org     0
        goto    start
        org     0x10
;
;This DecodeValue table must reside in page 0 for this program to work
;
DecodeValue
        addwf   PCL
        retlw   B'00111111'     ;decode for 0
        retlw   B'00000110'     ;decode for 1
        retlw   B'01011011'     ;decode for 2
        retlw   B'01001111'     ;decode for 3
        retlw   B'01100110'     ;decode for 4
        retlw   B'01101101'     ;decode for 5
```


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```
        retlw   B'01111101'     ;decode for 6
        retlw   B'00000111'     ;decode for 7
        retlw   B'01111111'     ;decode for 8
        retlw   B'01101111'     ;decode for 9
;
;
start
        clrf    PORTB
        bsf     STATUS,RP0      ;set portb 0,1&2 as outputs
        movlw   B'11111000'     ;       /
        movwf   PORTB           ;       /
        bcf     OPTION,RBPU     ;enable pull-up for switch
        bcf     STATUS,RP0
wait
        btfsc   UPDATELCD       ;see if update switch is low
        goto    wait            ;no then wait
        bcf     LOAD            ;make sure load is disabled
        movf    LSD,w           ;get least significant value
        clrf    PCLATH          ;PCH = 0
        call    DecodeValue     ;decode the value
        call    Send8           ;serially output the seg values
        movf    SCNDSD,w        ;get 2nd significant digit
        call    DecodeValue     ;decode it
        call    Send8           ;serially output it
        movf    THRDSD,w        ;get 3rd significant digit
        call    DecodeValue     ;decode it
        call    Send8
        movf    MSD,w           ;get Most significant value
        call    DecodeValue     ;decode it
        call    Send8           ;serially send it
        bsf     LOAD            ;toggle the LOAD line
        bcf     LOAD            ;to enable the latches
KeyReleased
        btfss   UPDATELCD       ;wait for key to be released
        goto    KeyReleased
        goto    wait            ;repeat loop.
;
;Send8, sends the 8 bits in the W register
Send8
        movwf   temp            ;save in temp
        movlw   .8              ;init count
        movwf   count           ;to 8
sendloop
        bcf     DATAIN          ;make sure DATAIN is low
        rrf     temp            ;rotate value through carry
        btfsc   STATUS,C        ;if bit clear then skip
        bsf     DATAIN          ;else set data bit
        bsf     CLK             ;toggle clock
        bcf     CLK             ;       /
        decfsz  count           ;see if 8 done
        goto    sendloop        ;no then do all
        return                  ;else return

        end
```


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2.0 ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VDD ..... -0.3V to +12V
Inputs (CLK, Data In, Load) ..... VCC to VDD +0.3V
LCDΦ Input ..... -0.3V to VDD +0.3V
Power Dissipation ..... 250 mW
Storage Temperature ..... -65°C to +125°C
Operating Temperature Industrial ..... -40°C to +85°C

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

TABLE 2: DC CHARACTERISTICS

VDD = +5V unless otherwise noted, TA = 40°C to +85°C

Characteristics		Sym	Min	Typ	Max	Units	Conditions
Supply Voltage		VDD	+3.0	—	+8.5	V	
Supply Current		IDD	—	25	60	µA	LCDΦ OSC < 15 kHz
			—	13	30	µA	LCDΦ OSC < 100 Hz
Input High Level		VIH	0.5 VDD	—	VDD	V	
Input Low Level	Clock	VIL1	0	—	0.1 VDD	V	3.0V ≤ VDD ≤ 8.5V
	Data,	VIL2	0	—	0.1 VDD	V	3.0V ≤ VDD ≤ 8.5V
Input Leakage Current	Load	IL	—	0.01	±10	µA	VIN = 0V and +5.0V
Input Capacitance		CI	—	—	5.0	pF	VDD = +5.0V
Segment Output Voltage		VOH	0.8 VDD	—	VDD	V	IOH = -100 µA
		VOL	0	—	0.1 VDD	V	IOL = 100 µA
LCDΦ Input High Level		VIN	0.9 VDD	—	VDD	V	
LCDΦ Input Low Level		VIL	0	—	0.1 VDD	V	
LCDΦ Input Leakage		IL	—	—	10	µA	VIN = 0V and +5.0V
							VDD = +5.0V

TABLE 3: AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Clock Rate	f	DC	—	1.5	MHz	50% duty cycle
Data Set-up Time	tDS	150	—	—	nsec	Data change to Clk falling edge
Data Hold Time	tDH	50	—	—	nsec	
Load Pulse Width	tPW	175	—	—	nsec	
Data Out Prop. Delay	tPD	—	—	500	nsec	CL = 55 pF

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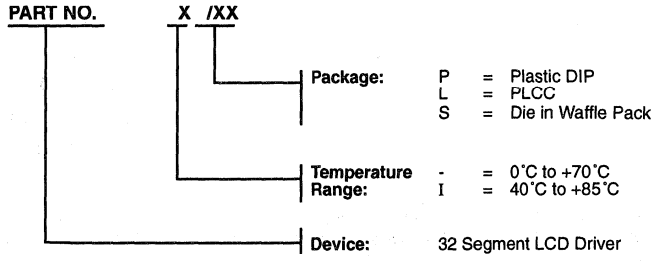
AY0438 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office.
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

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SECTION 20
PIC16/17 DIE PRODUCT INFORMATION

Overview of Microchip Die Specifications 20-1

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DIE SUPPORT

Overview of Microchip Die Specifications

INTRODUCTION

This overview is intended to give our customers a better understanding of Microchip's process of die usage and manufacture. This information is not intended as what is needed to manufacture die. It is highly recommended that a manufacturing site that is familiar in die manufacture be used.

A separate document containing device specific information is available from your regional Microchip Sales Office. This information includes the die size, bond pad coordinates, and die diagram for orientation.

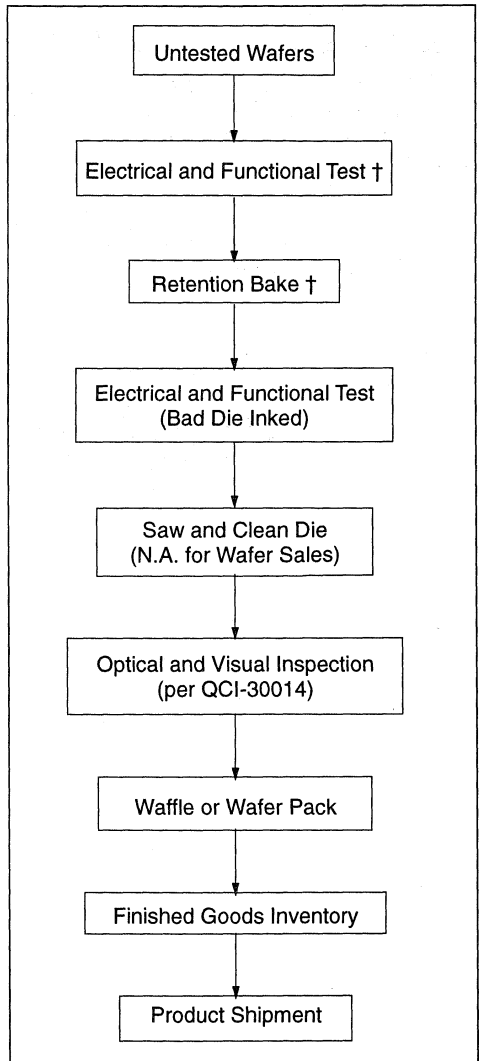
GENERAL DESCRIPTION

In some applications, the size of the product is of critical importance. In these applications it may be required to have the smallest possible size of all components. To support this customer requirement, Microchip offers several small package options including die. If none of the other device package options meet the application device footprint requirement, die offers the smallest size option. This option has some trade-offs.

Board manufacturing with die is more specialized and requires special equipment. This limits the options for manufacturing sites.

The production flow for die product is shown in Figure 1.

FIGURE 1: EEPROM, EEPROM, AND ROM PRODUCTION FLOW



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Die Support

TESTING

Die are tested at wafer probe. This testing is not as thorough as packaged devices (due to automatic handling issues). All devices are tested through a reduced temperature range.

For the microcontroller devices:
EPROM and EEPROM devices have all oscillator modes tested.
ROM devices have only the selected oscillator mode tested.

ELECTRICAL SPECIFICATIONS

The functional and electrical specifications of Microchip devices in die form are identical to those of a packaged version. Please refer to individual data sheets for complete details.

QTP

Quick Turnaround Production (QTP) applies only to EPROM and EEPROM microcontrollers.

With QTP devices, the program memory array is only tested against the code provided. This method ensures that the device will operate correctly as programmed, but does not ensure that every program memory bit can be programmed to every state.

Note:	Do not erase QTP devices and program them with a different code.

VISUAL INSPECTIONS

Dice supplied are inspected visually as per Microchip specification (document QCI-30014). Visual inspection criteria includes looking for ink-stains, cracks around the edges of a die or inside a die, metallization defects, passivation defects, particles and bond pad defects. For Microchip's standard die sales specifications please ask for documents QCI-30014 and QCI-30397.

DIE FORM SHIPPING

EPROM devices are supplied as fully erased programmable parts that are UV erasable and re-programmable by the user (except for QTP and SQTP devices).

EEPROM devices may not be supplied in a fully erased state, but are re-programmable by the user (except for QTP and SQTP devices).

ROM devices are supplied as fully programmed parts (program memory only). These are not re-programmable by the user.

Microchip product in die form can be shipped in waffle-pack. The waffle pack has sufficient cavity area to restrain the die, while maintaining their orientation. Lint free paper inserts are placed over the waffle packs, and each pack is secured with a plastic locking clip. Groups of waffle packs are assembled into sets for shipment. A label with lot number, quantity, and part number is attached.

These waffle packs are sealed in hermetic bags with a dry pack.

WAFER SHIPPING

Some products may also be shipped in wafer form (see ordering information). Wafers are shipped in a wafer tub. The tub is padded with non-conductive foam. Lint free paper inserts are placed around each wafer. A label with lot number, quantity, and part number is attached.

STORAGE PROCEDURES

Temperature and humidity greatly affect the storage life of die. It is recommended that the die be used as soon as possible after receipt. While stored by Microchip, these die are kept in a controlled environment.

Upon receipt, the sealed bags should be stored in a cool and dry environment (25°C and 25% relative humidity). In these conditions, sealed bags have a shelf life of 12 months. Temperatures or humidities greater than these will reduce the storage life.

Once a bag containing waffle packs has been opened, the devices should be assembled and encapsulated within 48 hrs (assuming, 25°C and 25% humidity).

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DIE HANDLING PROCEDURES

The sealed bags should only be opened when you intend to use the devices.

Once you receive the die, care should be taken in the handling and assembly of the die onto the application board.

Special Pic-n-Place handlers are required to handle the die.

Devices have a passivation covering to protect them during handling and to provide a hermetic seal at the die boundaries.

CAUTION

Some EEPROM devices use EEPROM cells for device configuration. Exposure to ultra-violet light or x-rays must be avoided. Exposure to ultra-violet light or x-rays may cause the device to operate improperly.

Extreme care is urged in the handling and assembly of these products since they are susceptible to damage from electro-static discharge.

SUBSTRATE BONDING

The die is attached to the system board by applying an adhesive to the device substrate. Some devices require that this adhesive be conductive and connect to system ground. For the other devices, this is recommended, but not required. Table 1 shows which devices are required to have the substrate grounded, and for which devices it is recommended. The back sides are backlapped and are without any gold coating.

TABLE 1: SUBSTRATE BONDING REQUIREMENTS

Device Family	Substrate Bonding to Ground
PIC16C5X †	Required
PIC16C5XA †	Recommended
PIC16CXX †	Recommended
PIC17CXX †	Recommended
PIC14XXX	Recommended
AY0438	Recommended
24XXXX	Recommended
85XXX	Recommended
93XXXX	Recommended
59XXX	Recommended
28XXXX	Recommended
27XXXXX	Recommended

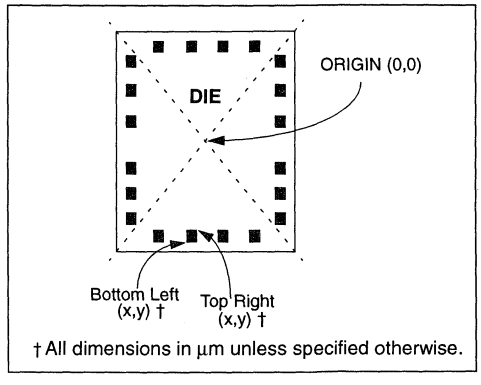
† Device family also includes the wide voltage (LC) and ROM (CR) versions.

BOND PAD COORDINATES

The die figures have associated bond pad coordinates. These coordinates assist in the attaching of the bond wire to the die. All the dimensions of these coordinates are in micrometers (µm) unless otherwise specified. The origin for the coordinates is the center of the die, as shown in Figure 2. These coordinates would be programmed into an auto-wire bonder for automated assembly.

The bond pad size is that of the passivation opening. The passivation overlaps the bond pad metal by at least 0.1 mil. There is a minimum bond pad to bond pad spacing. This spacing is measured from the edges of passivation openings. The device die specification sheet will specify the minimum spacing. Some of the VSS and VDD pad openings are larger then the standard bond pad for double bonding option.

FIGURE 2: DIE COORDINATE ORIGIN



† All dimensions in µm unless specified otherwise.

The die is capable of thermosonic gold or ultrasonic wire bonding. Die meet the minimum conditions of MIL-STD 883, Method 2011 on "Bond Strength (Destructive Bond Pull Test)". The Bond Pad metallization is silicon doped aluminum.

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Die Support

ENCAPSULATION

After the device has been attached and connected to the application board, the die needs to be protected from damage. Encapsulation is the process of protecting the device (and lead wires) from damage. There are two common methods for this encapsulation. These are:

1. Nonconductive potting material
2. Plastic transfer molding

The die should not be exposed to a temperature greater than 180°C.

MECHANICAL SPECIFICATION

The mechanical specifications for the die, excluding die size and bond pad coordinates, are show in Table 2 and Table 3.

ORDERING INFORMATION

Die sales must be conducted by contacting your Microchip Sales Office.

To order or obtain information (on pricing or delivery) for a specific device, use one of the following part numbers:

Devices in Waffle Pack
DEVICE_NUMBER/S

Devices in Wafer form
DEVICE_NUMBER/W

where DEVICE_NUMBER is the device that you require. The S specifies die in a waffle pack while a W specifies wafer sales. Example 1 shows some example part numbers.

Note: Microcontroller devices (PIC16/17) are NOT offered in wafer shipments

EXAMPLE 1: PART NUMBERS

Device	Product Identification System Number	
	Waffle Pack	Wafer
PIC16CR57A	PIC16CR57A/S	N.A.
PIC16C65	PIC16C65/S	N.A.
PIC17C44	PIC17C44/S	N.A.
PIC14000	PIC14000/S	N.A
24AA04	24AA04/S	24AA04/W
85C72	85C72/S	85C72/W
93AA46	93AA46/S	93AA46/W
59C11	59C11/S	59C11/W
28C04A	28C04A/S	28C04A/W
27C64	27C64/S	27C64/W

PRODUCT INFORMATION

For additional information concerning individual die specifications, please contact you local Microchip Technology Incorporated sales office.

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TABLE 2: DIE MECHANICAL DIMENSIONS

Specification	Min.	Typ.	Max.	Unit	Comments
Bond pad opening	§	§	—	mil µm	See Individual Die Data Sheet Note 1
Bond pad spacing	§	—	—	mil µm	See Individual Die Data Sheet Note 2
Die thickness					
PIC16/17 (EPROM/EEPROM/ROM)	14 356	15 381	16 406	mil µm	Note 3
Memory Products	14 356	15 381	16 406	mil µm	Note 3
Custom die thickness	N.A. N.A.	—	22 559	mil µm	Contact Microchip Factory Marketing Note 3, Note 4
Die thickness tolerance (Standard and Custom)	— —	—	± 1 ± 25.4	mil µm	Note 3

§ Refer to the Individual Device Die Data Sheet for this specification

Note 1: The bond pad size is that of the passivation opening. The passivation overlaps the bond pad metal by at least 0.1 mil. Some of the VSS and VDD pad openings are larger for double bonding option.
2: Bond pads are measured from the edges of passivation openings.
3: This specification is not tested. For design guidance only.
4: Custom die thickness is available (contact the Microchip Sales Office or Microchip Factory Marketing). As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow (up to the standard thickness).
5: The conversion rate is 25.4 µm / mil (a mil is 1/1000 of an inch).

TABLE 3: DIE MECHANICAL SPECIFICATIONS

Die backside preparation	Die backside are backlapped and without any backside gold.
Pad metallization	Pad metallization is silicon doped aluminum.
Bonding techniques	The die shall be capable of making a bond in one of the following ways: a) gold thermosonic b) aluminum ultrasonic
Die attach techniques	The dice are capable of bonding either by using a gold eutectic bond to a gold plated pedestal (containing 60 microinches of gold) or by using an electrically conductive adhesive (e.g. conductive epoxy) to any substrate. The substrate must be tied to VSS.

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NOTES:

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SECTION 21
QUALITY, RELIABILITY AND ENDURANCE

Product Quality 21-1
Product Reliability 21-9
EEPROM Endurance 21-17

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MICROCHIP

Product Quality

A CORPORATE COMMITMENT

Microchip Technology Inc. has evolved a culture where a commitment to quality is an integral part. By empowering every employee to be responsible for the quality of their work, the entire corporation is involved in the quality process. This interaction creates an environment for continuous improvement throughout the organization. The benefits of the system are then not only enhanced product quality and reliability but also product services.

THE CHALLENGE OF COMPLEXITY

Integrating an Ideal

Microchip's quality programs and business plan are vertically integrated and touch all levels of the company. From the top down, the President and CEO actively lead programs to ensure continuous improvement is a perpetual process. Improvement and cross functional teams work to enhance performance at every department level. Incorporating the improvement objectives into the business plan creates a unity of purpose and mandates that the two merge as one measurement.

Determination to be the Best

A fundamental concept at Microchip is the commitment to continuous improvement. All areas are constantly looking for ways to improve every aspect of the company. This has allowed products and processes to become world class in quality and reliability. These programs are the foundation for success.

PROCESS TECHNOLOGY

All the products manufactured at Microchip make use of a common N-Well CMOS baseline process to which modules are added in order to create the specific functions required by the product (EEPROM, Microcontroller, Logic and EPROM).

The baseline process, which has been in Manufacturing since 1988, uses minimum dimensions of 1.5µm, 360Å gate oxide thickness, N+ doped polysilicon gates and arsenic implanted source-drain diffusions for the N-channel devices.

A more advanced process uses minimum dimensions of 1µm, 250Å gate oxide thickness, polycide gate and LDD junction for the N-channel devices. A double level metal module can be added to both processes.

All of these devices utilize a proprietary passivation suitable for a wide variety of package types. Microchip's processes have been developed with reliability and manufacturability as their primary goals.

EEPROM

Microchip's CMOS floating gate EEPROM technology produces a non-volatile memory cell by storing or removing charge from the floating gate. Charge is transferred bidirectionally to the floating gate by Fowler-Nordheim tunneling through a sub-10 nm oxide over the drain of the transistor. This technology produces a memory cell with a typical endurance of $> 10^7$ cycles and greater than 40 years of data retention. (See EEPROM application note for details).

EPROM

This technology uses a non-volatile memory cell which stores charge on a self aligned floating gate. Electrons are provided to the floating gate via hot electron injection from the drain depletion region. Each byte can typically be programmed in 100 microseconds, and can retain that data for more than 10 years with unlimited reads. Block erasing is accomplished with a high intensity UV source through the package window. Windowed parts can be erased and reprogrammed more than 100 times.

Microcontroller and Logic

Logic products are built on a variety of Microchip's processes and their derivatives. These products have process modules for production of controllers that feature ROM, Analog, EPROM, and EEPROM. By utilizing the standard processing modules, the designs meld these technologies and their flexibility while maintaining the high quality and reliability standards expected.

QUALITY

Design for Quality and Reliability

Product reliability is designed into all Microchip processes and products. Design margins are established to guarantee every product can be produced economically, error-free and within the tolerances of the manufacturing process. Product Introduction Teams representing manufacturing, engineering, quality and product divisions ensure that exacting standards are met for each specific product.

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Documentation and Procurement Specifications

Microchip's documentation control program assures the correct and current document always is available at the point of use. Active documents are revision coded and serialized. Procurement specifications bear the same requirements. These document control procedures, which are common in the industry for military and high reliability products, are employed by Microchip, system wide.

In Line Controls and Process Assessment

Product integrity is assured by sampling and inspection plans performed in-line. This enables Microchip to control and improve product quality levels as product moves through the manufacturing operation. Microchip's acceptance sampling plans in assembly emphasize the attempt to eliminate defective product as it is discovered. Acceptance and sampling plans are based on proprietary low fraction defective (<1000ppm) quality statistics.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at selected process steps. In-process controls are performed by operators in the wafer fabrication and assembly operations. Operators take immediate corrective action if a process step is out of its control limit. Through these in-line controls the true capability of a process is generated. (See Appendix A:In Line Controls)

Control of Customer Quality is attained through a statistical program based on minimum defect capability levels. These levels are defined as the error levels associated with the circuit design and science limitations of the chemistry and physics of processing.

Material controls prevent defective piece parts from getting into the line. Microchip's assembly material control sample plan is typical of the emphasis placed on safeguards. (See Appendix B:Material Controls Package).

Testing for Margin

Microchip conducts a product's initial test under stringent requirements. All quality assurance tests are run to tighter limits than customer specifications. As part of an outgoing quality assurance program, products are tested at least two machine tolerances tighter than those limits specified by the customer on every parameter. Margin testing accounts for normal tolerances of any particular test system and provides the assurance that Microchip's products meet a customer's specifications.

Variation from Expectation

Microchip works to make variation from target as small as possible. The better process is the one that holds the narrowest dispersion. Processes are targeted to maintain Cpk's of >1.5 and currently have typical values of >2.0. Higher process capability values are continually strived for indicating that better process control is being obtained.

Outgoing Quality

Quality Control samples all outgoing product from final testing. These samples measure in-line defect levels after screens have been applied. Root cause analysis follows, initiating technical change to effect continuous improvement.

Programmability Yield

Using programmable devices adds a complexity to the Quality Level interpretation. It is not unlikely that some programmable devices will not program. The programmability yield is dependent on (but not limited to): programmers, technology, array size, and handling.

Any device that does not program properly will not be used in the end system. Therefore, programmability yields should not be used to calculate AQLs.

For convenience, Microchip offers programming services for certain devices. This service is an advantage to the customer since it not only eliminates programmability rejects, but also reduces the handling of the parts. See the individual data sheets for details on our Quick-Turnaround-Production (QTP) service.

RELIABILITY

Process Qualification

No priority is more important than the one where processes under which Microchip products are built operate without fail. All products are stressed beyond normal use limits when undergoing high temperature operating life and retention bake tests. This is done to ensure that the devices meet the strictest reliability guidelines and will maintain industry low failure rates.

Package Qualification

Package qualification measures a component's ability to withstand extreme thermal and mechanical stresses. All products are stressed to high level industrial specifications to ensure reliability.

Ongoing Sampling of Key Reliability Variables

Microchip conducts accelerated mechanical tests, operating life tests and memory retention tests to explore the many ways failures might occur. Data obtained from continuous testing is used to identify potential reliability problems and for defining action courses to improve product. Microchip's reliability knowledge is shared with customers. This data is available for use in customer's own quality and reliability improvement programs and is published in regular quarterly and yearly reports.

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RELIABILITY CONCEPTS

Definition

Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The reliability (or probability of survival) range runs from 0 (no chance of survival) to 1 (no chance of failure). Current microelectronic circuits are manufactured and controlled to such tight specifications that reliability figures for the total operation time approaching 1 (i.e., 0.9999) are common. As a result, the complement of reliability, or the failure probability, is more often quoted in current literature.

The failure rate is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per unit circuit-hour would generally be very small. To avoid reporting such small numbers, failure rates have been defined for greater circuit-hours. One thousand circuit-hours is defined as one circuit operating for one thousand hours, or 1,000 circuits operating for 1 hour, etc. The numbers of circuit-hours is the number of circuits multiplied by the number of operation hours for each circuit.

Two methods to define failure rate are commonly used:

- Percent failures per thousand circuit-hours
- Absolute failures per billion circuit-hours, or FITs.

Note that a failure rate of 0.0001%/1000 hours and 1 FIT are equivalent numbers.

Bathtub Curve: Failure Rate Over Time

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. (See Figure 1).

The early failure rate (infant mortality) period starts from initial operation (time T0) and decreases as time goes on.

Time T1 signifies the end of the infant mortality period. The next phase of the curve occurs between time T1 and T2. This long period of time is distinguished by a nearly constant and very low failure rate. After T2 is passed, the failure rate starts to increase slowly. This last phase of failure rate vs. time is known as the wear-out period.

Temperature Dependency

In order to establish failure rates in a reasonable time, it is necessary to accelerate the incidence of the failure modes. Higher environmental stress levels than those encountered under normal conditions are needed. The accelerating parameter most employed is junction temperature, although voltage and humidity, for example, are also used. Higher temperatures are capable of accelerating many common failure modes dramatically.

Arrhenius Equation

A number of mathematical models were developed to quantify the relationship between accelerated failure rates and increased junction temperatures. The one model most commonly used employs the Arrhenius Equation. It is as follows:

$$AF = e^{x}, \text{ where } x = \frac{E_A}{K}\left[\frac{1}{T_N} - \frac{1}{T_A}\right]$$

AF = Acceleration Factor (non-dimensional)

e = 2.718281828... (non-dimensional constant)

E_A = Activation energy level (electron volts)

k = Boltzmann's constant = 8.6172 x 10-5 (electron-volts/degree Kelvin)

T_N = Normal junction temperature (degrees Kelvin)

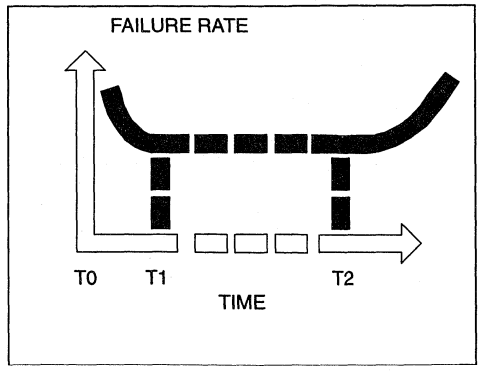
T_A = Accelerated junction temperature (degrees Kelvin)

Thus, the time to achieve a certain probability of failure at time T1 under temperature TN can be compressed to T1 divided by AF at the accelerated temperature, TA.

Note that for true acceleration, the acceleration factor AF is independent of the probability of the fail point specified.

AF, the dependent variable of the Arrhenius Equation is a function of several variables. TN and TA are specified for the situation under consideration. EA is a function of the particular mode of failure, and is determined by experimental evaluation.

FIGURE 1: BATHTUB CURVE



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Activation Energy Level

Activation energy levels in semiconductors generally are in the 0.3 - 1.1 electron-volt range. Each failure mode has its own activation energy. Some typical examples are:

FAILURE MECHANISM	E_A (eV)
Oxide/Dielectric Breakdown	0.3
Electromigration	0.5 to 0.7
Surface Related Contamination	1.0
Intermetallics	1.0
Floating Gate Charge Loss	0.6 to 1.2
Hot Electron Trapping	-.1
Charge Trapping	0.12

A compromise value of 0.6 electron-volts is often used when there is no specific information relating to the failure modes being accelerated.

RELIABILITY TESTS

Operating Life Test

The Operating Life Test is run under dynamic bias conditions where inputs are clocked. The test is conducted at high temperature to accelerate the failure mechanisms. The normal temperature for the test is +125°C for 1,000 hours. Readouts occur at 168 and 1,000 hours. Early hour failures are usually associated with manufacturing defects or otherwise marginal material.

Retention Bake

The Retention Bake Test is performed to accelerate data loss on floating gate devices. The test consists of unbiased baking at elevated temperature. Usually the test lasts for 1,000 hours at +150°C. The failure mechanism that is accelerated is charge leakage from a stored element.

Endurance Cycling

Endurance Cycling establishes the number of times a device can be programmed and erased. Normally the test is conducted at rated temperature conditions and is followed by retention bake. The standard cycling at Microchip is done at 85°C using a page cycle mode and is followed by a bake of both a checkerboard and an inverse checkerboard of 48 hours at 150°C.

Temperature Cycle

The Temperature Cycle test simulates stresses which occur to systems during power up/power down sequences. The test is intended to reveal any deficiencies resulting from thermal expansion mismatch of the die/package structure. Normally the test is conducted by cycling between -65°C and +150°C in an air ambient. Duration for the test is typically 500 cycles for both plastic and ceramic packages. Endpoint criteria are both electrical and visual/mechanical.

Thermal Shock

The Thermal Shock test is similar to the Temperature Cycle test except that the ambient during cycling is liquid-to-liquid. This stimulates rapid thermal environmental changes. The mechanisms accelerated are identical to those in the Temperature Cycle test except that the Thermal Shock test is a more accelerated test with temperatures normally +125°C to -55°C. The number of cycles are 500 for qualification testing.

Autoclave

The autoclave test determines the survivability of devices in molded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121°C and 15 pounds per square inch (one atmosphere) gauge pressure. The 168 or more hours of testing allows moisture to penetrate into the die. Chemical corrosion of the die metallization may occur if ionic contaminants are present and the die surface protection is deficient or damaged. Charge leaks from floating devices usually happen before a corrosion mechanism develops.

HAST

The Highly Accelerated Stress Test is similar to the Temperature Humidity Test but with more stringent temperature exposure. Devices are subjected to 130°C with 85% relative humidity and an alternating bias of 5 volts and ground on device pins. The duration of the test is 168 hours. This tests for ionic contamination and corrosion, but floating gate devices may also fail for charge loss, due to the high temperature.

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QUALIFICATION CATEGORIES

In general, qualification is required for new design, major changes in old design, process or material when either wafer fabrication or package assembly operations are affected. Cross functional teams which include reliability develop new products for introduction. In other areas, Microchip utilizes the concept of a Change Control Board which meets regularly to establish which criteria is to be used for all specific proposed changes. This board is made up of representative leaders of various groups and departments throughout Microchip to insure all concerns are heard early during the process.

QUALIFICATION PROGRAMS

Qualifications guarantee changes to or new processes and technologies are properly evaluated for reliability performance.

Reliability Monitoring

Microchip's reliability monitoring program is a comprehensive effort to measure the reliability of all process families with strict regularity. The program strives to improve performance through failure analysis and corrective action. Numerous screening procedures are used and estimates of product life and expected failure rates are provided.

Typical tests and frequencies include:

- Die Monitor on selected product for -
  - Dynamic Life
  - Retention Bake
  - Endurance
- Periodic (weekly, monthly and quarterly) package monitors to evaluate:
  - Mechanical stresses
  - Alignment
  - Temperature and moisture stresses
  - Corrosion resistance
  - Marking permanency

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APPENDIX A: IN LINE CONTROLS

TABLE 1: CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% sample LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	4X/Lot/Machine LTPD 15	X	—	N/A
Wire Bond	Machine Shut Down	1% AQL each 1/2 shift	X	—	MIL-STD-883C Method 2010
Post Wire Bond	Reject defectives 100% rescreen per LTPD	LTPD 15	X	—	MIL-STD-883C Method 2010
Mold Press	Machine Shut Down	One sample /4 hrs	X	—	N/A
Die Plating	Reject defectives 100% rescreen per LTPD	Every 4 hrs LTPD 10	X	—	N/A
Trim and Form	Reject defectives 100% rescreen per LTPD	Once/ 2 hrs LTPD 10	X	—	N/A
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

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TABLE 2: CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	Non-destruct each 2 hrs destruct each shift	X	—	MIL-STD-883C Method 2010
Wire Bond	Machine Shut Down	4X/shift/machine	X	—	MIL-STD-883C Method 2010
Preseal Visual	Reject defectives 100% rescreen per LTPD	100% LTPD 15	— X	X —	MIL-STD-883C Method 2010
Package Seal	Machine Shut Down	LTPD 15	X	—	N/A
Environmental Stress Centrifuge Temp Cycle	Machine Shut Down	LTPD 5 84(0) 84(0)	X	—	MIL-STD-883C Method 2001 Method 1010
Fine Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Gross Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Lead Trim	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2009
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

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APPENDIX B: MATERIAL CONTROLS PACKAGE

TABLE 3: MATERIALS CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Lead Frame	Reject defectives 100% rescreen per LTPD	Visual, LTPD 2 Functional, LTPD 10 and material spec	X	—	N/A
Die Attach Epoxy	Reject	Functional, LTPD 15 and material spec	X	—	N/A
Gold Wire	Reject	Per material spec	X	—	N/A
Molding Compound	Reject	Spiral flow, 3X/lot Functional, 1X/lot and material spec	X	—	N/A

TABLE 4: MATERIALS CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Base/Lead Frame	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Package	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Preform	Reject	Visual, LTPD 10 Functional, LTPD 15	X	—	MIL-M-38510
Bond Wire	Reject	Per material spec 2 spools/lot	X	—	MIL-M-38510
Lid	Reject	Visual, LTPD 7 Functional, LTPD 10 and material spec	X	—	MIL-M-38510

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MICROCHIP

Product Reliability

OVERVIEW

Microchip Technology Inc.'s products provide competitive leadership in quality and reliability, with demonstrated performance of less than 100 FITs (Failures in Time) operating life for most products. The designed-in reliability of Microchip's products are supported by ongoing reliability data monitors. This document presents current data for your use - to provide you with results you can count on.

The test descriptions included in this document explain Microchip's quality and reliability system. The product data demonstrates its results.

The customer's quality requirements are Microchip's top priority. Ongoing customer feedback and device performance monitoring drive Microchip, leading to continuing improvements in the long-term quality and reliability.

FAILURE RATE CALCULATION

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip Technology agree closely with those published in the literature. For complex CMOS devices in production at Microchip Technology, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. This activation energy also applies to some of our retention bake failures, though most are 1.2eV. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink, or air flow by convection is used.

Environment	Typical Failure Mechanism
Operating Life	Process parameter drift/shift Metal electromigration Internal leakage path Lifted bond/ball bond chip-out
Temperature Cycle	Lifted bond/ball chip-out Cracked die or surface cracks Bond pad corrosion
Autoclave	Inter-pin leakage Charge loss
High Temp. Bake	Charge loss
High Temp. Reverse Bias	Charge gain, Parameter drift/shift

DEFINITIONS

FIT (Failure In Time): Expresses the estimated field failure rate in number of failures per billion power-on device-hours. 100 FITS equals 0.01% fail per 1,000 device-hours.

Operating Life Test: The device is dynamically exercised at a high ambient temperature (usually 125°C) to quickly simulate field life. Derating from high temperature, an ambient use condition failure rate can be calculated.

Temperature Cycle: The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 15 minutes, 150°C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

Autoclave (pressure cooker): Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

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Thermal Shock: Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media.

Retention Bake: A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

HAST: Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 Volts and ground on alternating pins.

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system ensures that released products are designed, processed, packaged and tested to meet both design functionality and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability.

RELIABILITY DATA SUMMARY

Introduction

This section provides a reliability summary of Microchip Technology's product. Included is reliability data and packaging information obtained over the recent past.

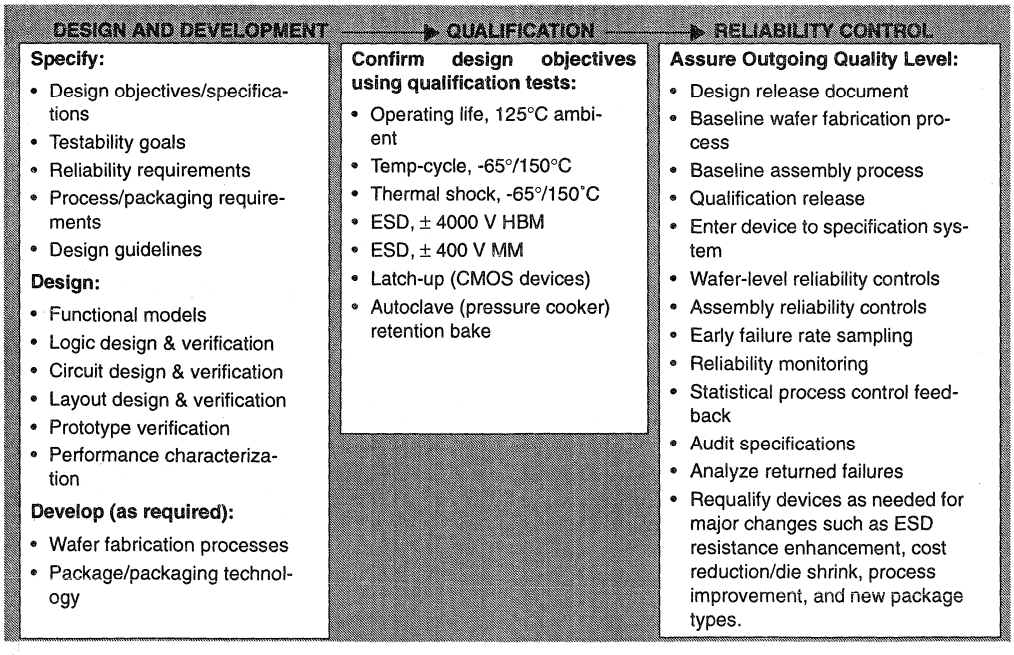
Plastic Package Characteristics and Codes

As part of an on going product program, Microchip Technology will apply its Quality and Reliability process in evaluating the latest developments in plastic packaging technology, and implement the highest reliability materials and assembly techniques. The plastic packages that are currently available from Microchip are listed in the table below.

Package Description Identification Code

Package Description	Identification Code
Plastic Leadless Chip Carrier	L
Plastic Dual In Line (600)	P
Plastic Dual In Line (300)	SP
Plastic SOIC (.150)	SL/SN
Plastic SOIC (.207)	SM
Plastic SOIC (.300)	SO
Plastic TSOP (8 x 20mm)	TS
Plastic SSOP (.207)	SS

FIGURE 1: RELIABILITY CONTROL SYSTEM DIAGRAM



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HIGH TEMPERATURE (125°C) DYNAMIC LIFE TEST

Graph set for EEPROM, PIC16/17 and EPROM for all conditions

High temperature dynamic life testing accelerates random failure modes which would occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems.

FIGURE 2: EEPROM DYNAMIC LIFE

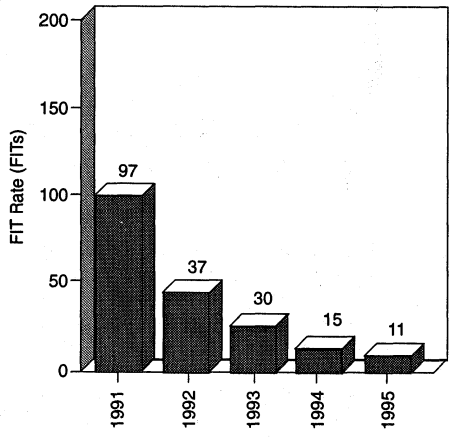


FIGURE 3: EPROM DYNAMIC LIFE

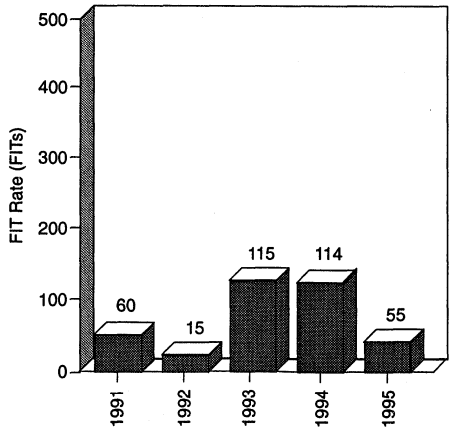
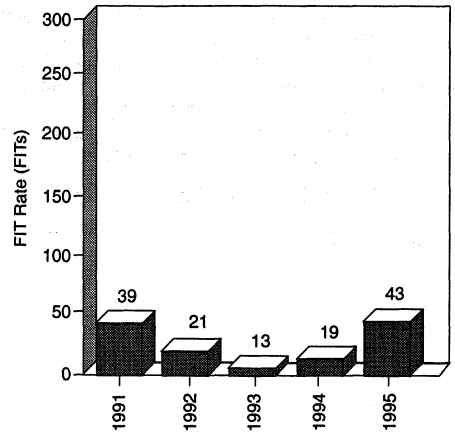


FIGURE 4: PIC16/17 MICROCONTROLLER DYNAMIC LIFE



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DATA RETENTION BAKE

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of zeroes to ones. In order to evaluate the level of this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell and 168 hours at 150°C is equivalent to greater than 250 years in the field at 55°C.

FIGURE 5: EEPROM RETENTION BAKE

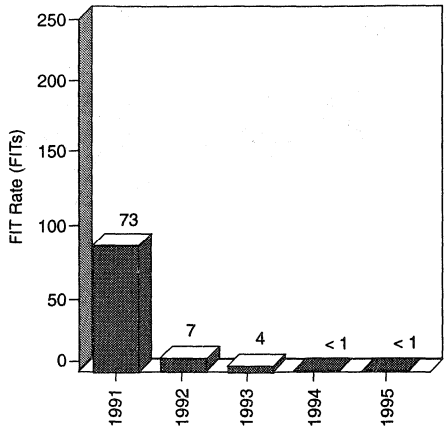


FIGURE 6: EPROM RETENTION BAKE

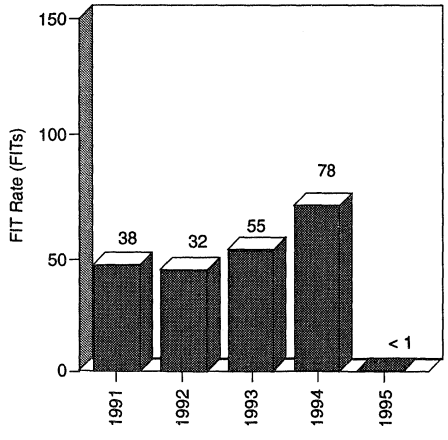
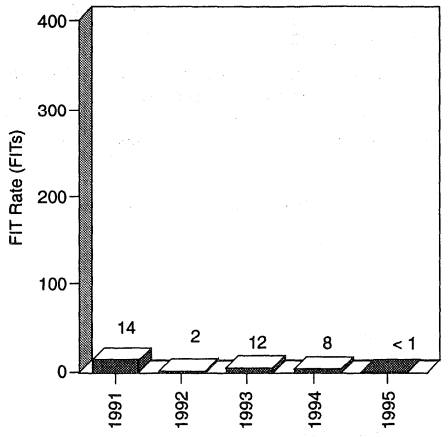


FIGURE 7: PIC16/17 MICROCONTROLLER RETENTION BAKE



NOTE: Representation of reliability data typically shows calendar year grouping along the x-axis, except for 1993 which includes only first, second and third quarters. This provides the equal time interval normally expected for graphical presentation. However, Chi-square statistics demand equivalent device-hours for fair interval comparison. Such data grouping assures that relatively small sample sizes do not indicate unrepresentative FIT rates.

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PCT (AUTOCLAVE)

Originally, this test was designed to evaluate corrosion of bond pads due to penetrating moisture combining with contaminant residue on the metal surface. The corrosion failure rate for this test has become nearly zero and a new failure mode has surfaced. This is memory cell charge loss due to moisture penetration along the floating gate allowing a conduction path for removal of stored charge. This moisture path is between the seal of the metal and the passivation which can then be traced to the substrate near the edge of the floating gate. This failure type is the primary mode in the data provided.

Operating Hours		
Package	**24**	**168**
PDIP	0/1334	0/1334
PLCC	0/1014	7/1014
SOIC	0/2439	0/2439
TSOP	0/192	0/192

PCT Failure Modes:
1 unit of 32L PLCC (27C256) failed due to lifted ball bonds.
5 units of 32L PLCC (27C256) failed due to lifted ball bonds.
1 unit of 32L PLCC (27C256) failed due to a leaky oxide causing single bit charge loss.

TEMPERATURE CYCLING

This thermal tests evaluates air to air rapid temperature change evaluating built in material stresses. This is a worst case simulation of system power up/power down and is based on stringent military packaging requirements.

Operating Results	
Package	**100 Cycles**
PDIP	0/364
PLCC	0/188
SOIC	0/964
TSOP	0/30
SSOP	0/60
VSOP	2/20

TC Failure Modes:
2 units of 28L VSOP (28C64A) failed due to lifted ball bonds.

THERMAL SHOCK

Thermal shock is the most extreme case of temperature cycling by using liquid immersion for the technique to change the device environment. This accelerates any stress related failures with the rapidly changing gradient. After the temperature stressing a constant force centrifuge test is also preformed prior to final electrical testing to further uncover any defects that may have occurred under stress.

Operating Results	
Package	**100 Cycles**
PDIP	0/354
PLCC	0/132
SOIC	0/872
TSOP	0/30
SSOP	0/60
VSOP	2/66

TS Failure Modes:
2 units of 28L VSOP (28C64A) failed due to oxide defects.

HAST (130°/85% R.H.)

Highly Accelerated Stress Testing evaluates plastic encapsulated devices' ability to withstand extreme high temperature, high humidity environments while under electrical bias. This is done by a new method known as HAST. This stress is designed to create corrosion of the metal or internal device leakage if ionic contaminants are present but also may cause charge loss in memory cells.

Operating Results		
Package	**48 Hours**	**168 Hours**
PDIP	0/969	1/969
PLCC	0/477	0/477
SOIC	8/2572	0/2482
TSOP	0/150	0/149

HAST Failure Modes:
8 units of 18L SOIC (PIC16CR54) failed due to high static Idd.
1 unit of 8L PDIP (24LC65) failed due to single bit charge loss.

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PRODUCT RELIABILITY DATA

CMOS PIC16/17						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hours	FITS 60% CL@55°C
PIC16C54	DLT	1/2281	1/1028	2	1,246,728	60
PIC16C54A	DLT	1/1520	3/760	4	893,760	75
PIC16C55	DLT	5/1474	0/710	5	844,032	179
PIC16C56	DLT	0/2286	0/1028	0	1,247,568	18
PIC16C57	DLT	0/1865	0/868	0	1,042,440	21
PIC16C58A	DLT	1/2670	0/720	1	1,053,360	25
PIC16C64	DLT	3/774	1/324	4	402,192	168
PIC16C71	DLT	0/1521	0/756	0	890,568	25
PIC16C74	DLT	0/405	2/162	2	204,120	196
PIC16C84	DLT	0/1523	1/723	1	863,184	56
PIC17C42	DLT	1/767	0/370	1	439,656	59
PIC17C44	DLT	0/342	0/162	0	193,536	61
PIC16C54	BAKE	1/2915	0/585	1	981,120	18
PIC16C54A	BAKE	0/1874	0/390	0	642,432	< 1
PIC16C55	BAKE	0/1869	0/382	0	634,872	12
PIC16C56	BAKE	3/2901	0/580	3	974,568	37
PIC16C57	BAKE	1/2312	1/464	2	778,176	34
PIC16C58A	BAKE	0/1887	0/385	0	640,416	< 1
PIC16C64	BAKE	0/950	0/190	0	319,200	< 1
PIC16C71	BAKE	0/1852	0/385	0	634,536	12
PIC16C74	BAKE	0/481	0/95	0	160,608	< 1
PIC16C84	BAKE	0/1392	0/295	0	481,656	< 1
PIC17C42	BAKE	0/928	0/190	0	315,504	< 1
PIC17C44	BAKE	0/438	0/99	0	156,744	< 1

Failure Modes - Dynamic Life:

1 unit of PIC16C58A failed static Idd.
5 units of PIC16C55 failed due to mishandling exacerbated by thermal stress.
1 unit of PIC16C54A failed dynamic Idd due to oxide defects.
2 units of PIC16C65/74 failed due to poor programming margin.
3 units of PIC16C64 failed for fuse charge gain.
1 unit of PIC16C64 had a column fail.
1 unit of PIC17C42 failed due to single bit charge loss.
1 unit of PIC16C84 failed continuity at high temperature.
1 unit of PIC16C54 failed due to high Idd standby.
1 unit of PIC16C54 failed leakage due to wire sweep.
3 units of PIC16C54A failed dynamic Idd.

Failure Modes - Retention Bake:

2 units of PIC16C56 failed single/double bits due to metal shorting the floating gates to ground.
2 units of PIC16C57 failed due to single bit charge loss.
1 units of PIC16C54 failed due to single bit charge loss.
1 units of PIC16C56 failed due to single bit charge loss.

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EEPROM						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hours	FITS 60% CL@55°C
24C01A/02A	DLT	0/2297	0/880	0	1,125,096	29
24C04	DLT	0/1530	0/842	0	964,320	20
93C06/46	DLT	0/1147	0/459	0	578,256	23
93LC46	DLT	0/2681	0/1078	0	1,355,928	38
93LC56/66	DLT	0/3447	0/1609	0	1,930,656	16
93LCS56/66	DLT	0/383	0/160	0	198,744	11
24LC01B	DLT	1/1915	0/779	1	976,080	29
24LC02B	DLT	0/2297	3/925	3	1,162,896	50
24LC04B	DLT	0/1519	0/612	0	769,272	86
24LC08B	DLT	0/1915	0/767	0	966,000	29
24LC16B	DLT	0/1915	0/767	0	966,000	23
24LC65	DLT	0/1149	0/688	0	770,952	23
24C01A/02A	BAKE	0/2320	0/480	0	792,960	< 1
24C04	BAKE	0/1392	0/285	0	473,256	< 1
93C06/46	BAKE	0/0	0/0	0	0	NA
93LC46	BAKE	1/2316	0/474	1	787,248	< 1
93LC56/66	BAKE	0/3712	0/765	0	1,266,216	< 1
93LCS56/66	BAKE	0/0	0/0	0	0	NA
24LC01B	BAKE	0/2320	0/480	0	792,960	< 1
24LC02B	BAKE	0/2320	0/494	0	804,720	< 1
24LC04B	BAKE	0/1856	0/380	0	631,008	< 1
24LC08B	BAKE	0/2336	0/500	0	812,448	< 1
24LC16B	BAKE	0/2320	0/475	0	788,760	< 1
24LC65	BAKE	2/928	0/195	2	319,704	< 1

Failure Modes - Dynamic Life:

1 unit of 24LC01B failed leakage on the SDA pin.
3 units of 24LC02B failed due to high standby current.

Failure Modes - Retention Bake:

1 unit of 93LC46 failed to program.
2 units of 24LC65 failed for single bit charge loss.

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EPROM						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hours	FITS 60% CL@55°C
27C256	DLT	4/5360	0/2291	4	2,824,920	44
27C512A	DLT	1/2310	5/929	6	1,163,440	81
27C256	BAKE	1/6496	0/1235	1	2,128,728	< 1
27C512A	BAKE	0/2771	0/570	0	944,328	< 1

Failure Modes - Dynamic Life:

2 units of 27C512A failed for single bit charge loss due to a hole in the oxide.
4 units of 27C512A failed for leadage due to a hole in the oxide.
4 units of 27C256 failed due to marginal Vih.

Failure Modes - Retention Bake:

1 unit of 27C256 failed due to an oxide defect in the 1st gate oxide.

Operation Legend: DLT - Dynamic Life Test (125°C) Bake -Retention Bake (150°C)

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MICROCHIP

EEPROM Endurance

INTRODUCTION

A unique feature of non-volatile memory devices is the dual requirement both to change and to maintain data states. It is this combination of requirements that provides the contrasting nature that defines the complexities involved in change and maintaining such change. Anything that enhances the physics to allow a data state change in contrast degrades the retention of that change. It also holds that any retention enhancements inhibit the data changing capabilities. A balance must be struck between the combinations to achieve the field requirements of customer applications.

Erase/Write cycling has many variables which greatly effect the lifetime of the device. To accurately make comparisons between specifications and the actual requirements, or any other comparisons, these factors must be well understood and taken into account.

TECHNOLOGY OVERVIEW

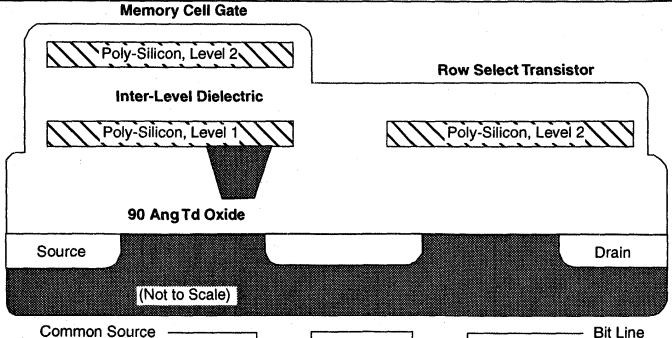
Silicon Technology

The basic technology employed by Microchip Technology for EEPROM's is a FLOTOX structure as drawn below. This is a an industry standard architecture base which has been enhanced by Microchip to provide improvements to the quality and reliability of the devices produced.

Circuit Technology

These cells are then structured in either an 8 or 16 bit word organization for data storage with between 32 words (256 byte device) and 8K words (64K device) using standard binary decoding schemes found industry wide on memory devices. Data can then be transmitted either into the device for storage or read from the device when needed along a single DATA pin, (I^2C bus) or a dual Data in/Data out configuration (3-wire bus). The device has no restriction on the number of read cycles that can be processed per byte without damage but the storage process does have finite limitations.

Currently two different schemes of error correction are being utilized on Microchip EEPROM's. The 24CXX, 93CXX, 85CXX, 59CXX and 28CXX device types utilize a modified Hamming code redundancy scheme with four parity bits per eight bit byte. This has been the industry standard correction scheme for enhancement of cycling lifetimes by eliminating single bit per word errors. An alternative approach has been developed utilizing an AND cell concept of redundant memory cells. This further enhances the write/erase lifetime over the Hamming code and has been implemented on the 24LCXX and 93LCXX circuits.



	Read	Write	Erase	Standby
Bit Line	1.6 volts	18.0 volts	0.0 volts	0.0 volts
Row Select Gate	5.0 volts	20.0 volts	20.0 volts	0.0 volts
Memory Cell Gate	5.0 volts	0.0 volts	20.0 volts	0.0 volts
Common Source	0.0 volts	Float	0.0 volts	0.0 volts

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Reliability Endurance

The endurance failure rate curve for the Microchip devices is presented in the standard form for this curve from EEPROM FLOTOX manufacturers. Microchip does write/erase cycle all EEPROM devices prior to shipment to remove the infant mortality endurance failures from the population. This characteristic curve, with two failure increase sections, is shown below for reference. Both sections have single bits failing as the dominant mechanism.

The first of the failure increase sections is usually related to breakdown of oxides from latent oxide defects that are inherent to any process. These oxides have reached a time dependent dielectric breakdown condition and permanently rupture. This generally characterizes the first 200K write/erase cycles under any conditions. The second curve is the standard trap up of electrons within the tunnel dielectric which closes the write/erase threshold window until the device no longer adequately programs or erases.

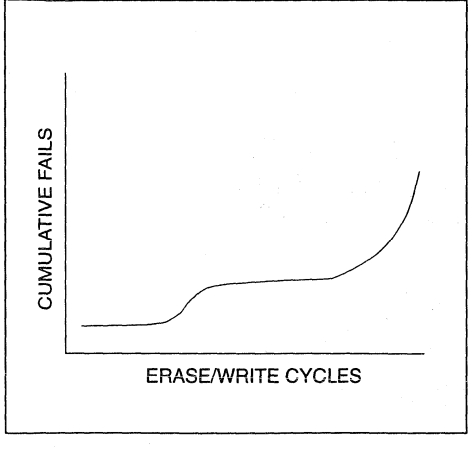
This curve depends on multiple parameters, but the trap up failure increase portion often does not occur until ten million write/erase cycles or greater.

The first failures from endurance cycling and the long term end of life failures are due to different mechanisms.

The failures from 200K to 500K cycles have historically been attributed to "fast trap up" around the industry. Analysis at Microchip has shown that these failures are not actually trap up but oxide breakdown in nature. They most often manifest themselves as single bit charge loss or charge pump failure, both due to the formation of a conductive path within the gate oxide layer.

These oxide breakdown failures can be related to defects of three types of categories.

Type 1 is a residual chemical stain left behind on the wafer after processing due to an inadequate rinse. These are very difficult to physically detect and are best inferred from a pattern of bits (a bit cluster) that fail.



Type 2 is a physical defect which can be found upon microscopic or SEM analysis resulting in the failure. This is most often a particle, polysilicon nodule or metal short.

Type 3 is a physical defect with low activation energy that cannot be detected until end of life evaluation because of it's change in state (subsequent consumption) during latter processing steps.

The end of life mechanism is called "oxide trap up". This is where the tunnel dielectric oxide layer loses it's ability to pass charge and begins to retain some portion of the charge that it passes to the floating gate. These excess electrons within the oxide act as a charge shield, resulting in insufficient charge movement while significantly raising the voltage required to continue transmitting a constant charge level. Since the programming voltage is not adjustable this results in less charge movement for either the write or erase state. These states, whether charged negatively or charged positively, approach a central point and become indistinguishable to the detection circuitry of the device. This results in a failure to read the correct pattern, (impossible to distinguish between a programmed one and a programmed zero) beginning with the extreme voltage values of the operating specification.

Microchip strives to offer the lowest failure rate for both early life and wearout fails. Early fails in Microchip products are in the PPM range, and wearout does not set in most applications until after ten million cycles.

MEASUREMENT OF CYCLING

Microchip Technology defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. All units shipped from Microchip have Error Correction circuitry engaged for customer use. Error Correction amends any one error per byte for Hamming and one error per bit for AND cell which allows the device to read correct data. An endurance failure is determined when any one bit is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices, (Microchip currently uses a cumulative 2.5 percent), have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from every wafer lot of material manufactured for shipment. Samples are subjected to byte cycling of a checkerboard pattern at 85°C in rapid succession to the specified number of guaranteed cycles. These units then are baked in both checkerboard and inverse checkerboard forms and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a monthly basis and reviewed to measure both results of continuous improvement programs and conformance against the device standards.

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ENDURANCE VARIABLES

a) **Temperature:** Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b) **Delay between cycles:** This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies this does have a positive effect, however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c) **Write timing:** The decrease in write time to the device correlates directly with write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.
Please note that the rise time of the signal, which the customer does not have control over is also a dominant effect.

d) **Vcc voltage:** The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.

Lower voltages this has the opposite effects on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at Vcc=5.5 Volts.

e) **Pattern effect:** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a nonvolatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric. (Please note that to write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to it's original state!) Conversely writing a one from a one then passes no charge through the cell and therefore does no damage to the cell but does stress the charge pump.

From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles that an all zero patterned device would last. In general this appears to be approximately correct but does neglect the charge pump and other peripheral wearout mechanisms.

f) **Cycling mode:** Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field. A second technique exists called block mode which exercises all the cells of the array simultaneously. The lifetime expectations are approximately ten times as long for these block cycled devices as equivalently cycled byte cycled circuits based on experimental findings. This effect has been traced back to the rise time of the programming signal at the memory cell. The faster this voltage rise occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate. Page mode offers the best balance of endurance and write cycle times.

g) **Array Size:** This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are therefore not directly related to array size.

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FIELD RESULTS

Microchip Technology, after significant experimentation, has developed a model of the Endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called Total Endurance™. This allows the customer to bypass confusing information and conditions other than their application and directly predict the failures seen in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system. Results for a typical application (obtained from the Total Endurance model are listed at right for reference).

Device	Application Life	Cumulative Percent
24C02A	10 years	154 PPM
24C04A	10 years	172 PPM
93C46	10 years	136 PPM
24LC02B	10 years	108 PPM
24LC04B	10 years	131 PPM
24LC16B	10 years	668 PPM
93LC46B	10 years	374 PPM
93LC56B	10 years	108 PPM
24LC65HE	10 years	131 PPM
24LC65SE	10 years	4061 PPM

Typical conditions used are 25°C, Byte mode operation with 24 cycles per day, V_{CC} = 4.5 Volts with a random pattern writing one quarter of the array at each occasion. The failure rates quoted are the expected failure rate at the end of the application life using an unlimited number of read cycles. For more information on Endurance, it is recommended that the user obtain a copy of Total Endurance.

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SECTION 22
PACKAGING INFORMATION

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Packaging Diagrams and Parameters 22-4
Product Tape and Reel Specifications 22-55
Devices in Die/Wafer Form - Non-Volatile Memory 22-57

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MICROCHIP

PACKAGING

Commercial/Industrial Outlines and Parameters

PART NUMBER SUFFIX DESIGNATIONS:

XXXXXXXXXX -XX X /XX XXX

Device Type	Options	Speed or Frequency	Temperature	Package	Pattern

Examples:

24LC65-I/SN
PIC16C54-RCI/SO

Memory Products

Device Type
C = CMOS
LC = Low Power CMOS
AA = 1.8V
LV = Low Voltage EPROM
HC = High Speed EPROM
LCS = Low Power Security

Options
Blank = twc = 1 ms
F = twc = 200 us (28CXX devices)
X = Rotated pinout (93LCXX devices)
T = Tape and Reel

Speed
55 = 55 ns
70 = 70 ns
90 = 90 ns
10 = 100 ns
12 = 120 ns
15 = 150 ns
17 = 170 ns
20 = 200 ns
25 = 250 ns
30 = 300 ns

Temperature
Blank = 0°C to +70°C
I = -40°C to +85°C
E = -40°C to +125°C

Package
L = Plastic Leaded Chip Carrier
P = Plastic Dual In-Line Package
S = Die in Waffle Pack
W = Die in Wafer Form
SL = 14-Lead Small Outline - 150 mil
SM = 8-Lead Small Outline - 208 mil
SN = 8-Lead Small Outline - 150 mil
SO = Small Outline - 300 mil
SS = Shrink Small Outline Package - 209 mil
ST = Thin Shrink Small Outline Package - 4.4 mm
TS = Thin Small Outline - 8mm x 20mm
VS = Very Small Outline - 8mm x 13.4mm
WF = Sawed Wafer in Form

Pattern
QTP, SQTP, ROM Code or Special Requirements

Mircocontroller Products

Device Type
C = CMOS
LC = Low Power CMOS
CR = CMOS ROM
LCR = Low Power CMOS ROM
LV = Low Voltage
F = Flash Program Memory
FR = Flex ROM

Options
T = Tape and Reel

Crystal Frequency Designator
LP = Low Power Crystal
RC = Resistor Capacitor
XT = Standard Crystal/Resonator
HS = High Speed Crystal
02 = 2 MHz
04 = 200 kHz (LP mode)
04 = 4 MHz (XT & RC mode)
10 = 10 MHz
20 = 20 MHz
25 = 25 MHz
33 = 33 MHz

Temperature
Blank = 0°C to +70°C
I = -40°C to +85°C
E = -40°C to +125°C

Package
L = Plastic Leaded Chip Carrier (PLCC)
P = Plastic Dual In-Line Package (PDIP)
S = Die in Waffle Pack
W = Die in Wafer Form
CB = Chip On Board (COB)
CL = 68-Lead Ceramic Quad (CERQUAD) with Window
JW = Ceramic Dual In-Line Package (CERDIP) with Window
PQ = Plastic Metric Quad Flat Pack (MQFP)
PT = Thin Quad Flatpack (TQFP)
SM = 8-Lead Small Outline - 208 mil
SO = Small Outline (SOIC) - 300 mil
SP = Skinny PDIP
SS = Shrink Small Outline Package (SSOP) - 209 mil
TS = Thin Small Outline (TSOP) - 8mm x 20mm
TQ = Thin Quad Flatpack (TQFP)

Pattern
QTP, SQTP, ROM Code or Special Requirements

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Packaging Diagrams and Parameters

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Packaging Diagrams and Parameters

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Packaging Diagrams and Parameters

Ceramic Side Brazed Dual In-Line Family

Symbol List for Ceramic Side Brazed Dual In-Line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body (lid)
A1	Distance between seating plane and base plane
A2	Distance from base plane to highest point of body (lid)
A3	Base body thickness
B	Width of terminal leads
B1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E1	Body width parameters not including leads
eA	Linear spacing of true minimum lead position center line to center line
eB	Linear spacing between true lead position outside of lead to outside of lead
e1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
S	Distance from true position center line of Number 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B1" is nominal.

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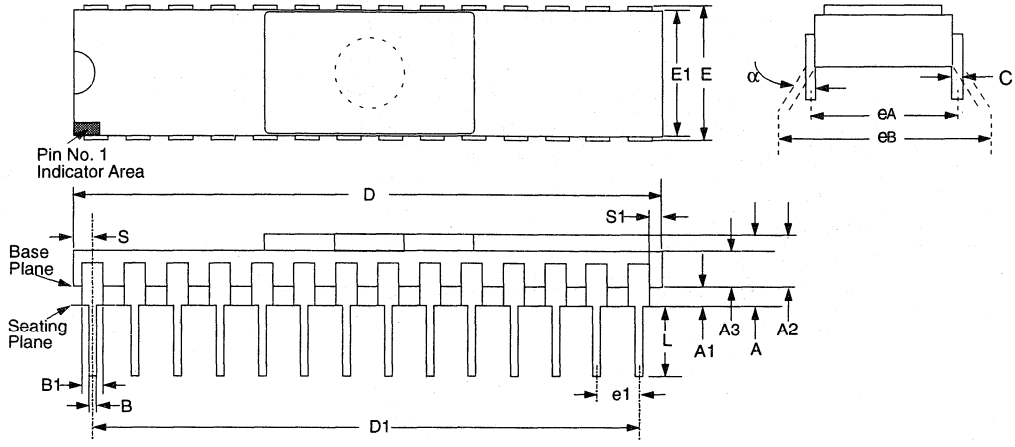
Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Side Brazed Dual In-Line with Window (JW) (300 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.937	5.030		0.155	0.198	
A1	1.016	1.524		0.040	0.060	
A2	2.921	3.506		0.115	0.138	
A3	1.930	2.388		0.076	0.094	
B	0.406	0.508		0.016	0.020	
B1	1.219	1.321	**Typical**	0.048	0.052	
C	0.228	0.305	**Typical**	0.009	0.012	
D	35.204	35.916		1.386	1.414	
D1	32.893	33.147	**BSC**	1.295	1.305	
E	7.620	8.128		0.300	0.320	
E1	7.366	7.620		0.290	0.300	
e1	2.413	2.667	**Typical**	0.095	0.105	
eA	7.366	7.874	**BSC**	0.290	0.310	
eB	7.594	8.179		0.299	0.322	
L	3.302	4.064		0.130	0.160	
S	1.143	1.397		0.045	0.055	
S1	0.533	0.737		0.021	0.029	

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Packaging Diagrams and Parameters

Ceramic Dual In-Line (CERDIP) Family

Symbol List for Ceramic CERDIP Dual In-Line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body (lid)
A1	Distance between seating plane and base plane
A2	Distance from base plane to highest point of body (lid)
A3	Base body thickness
B	Width of terminal leads
B1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E1	Body width parameters not including leads
eA	Linear spacing of true minimum lead position center line to center line
eB	Linear spacing between true lead position outside of lead to outside of lead
e1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
S	Distance from true position center line of Number 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B1" is nominal.

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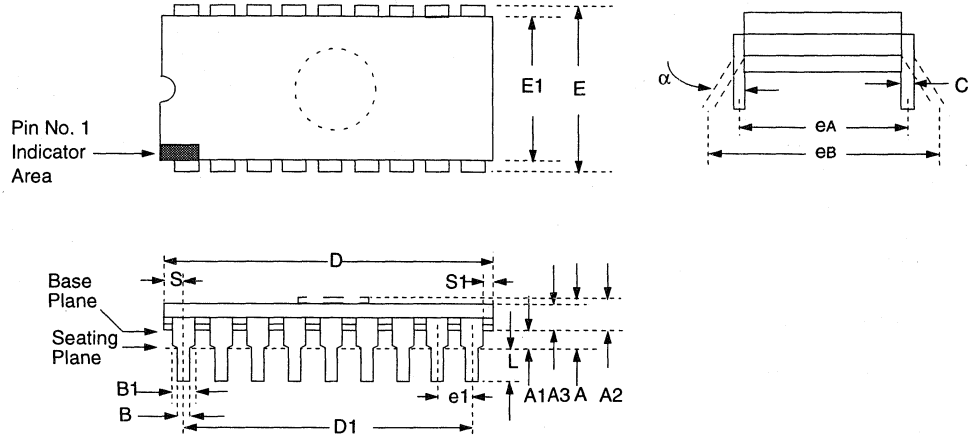
Packaging Diagrams and Parameters

Package Type: 18-Lead Ceramic Dual In-Line with Window (JW) - (300 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.7780		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	**BSC**	0.800	0.800	**BSC**
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	**BSC**	0.100	0.100	**BSC**
eA	7.366	8.128	**Typical**	0.290	0.320	**Typical**
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

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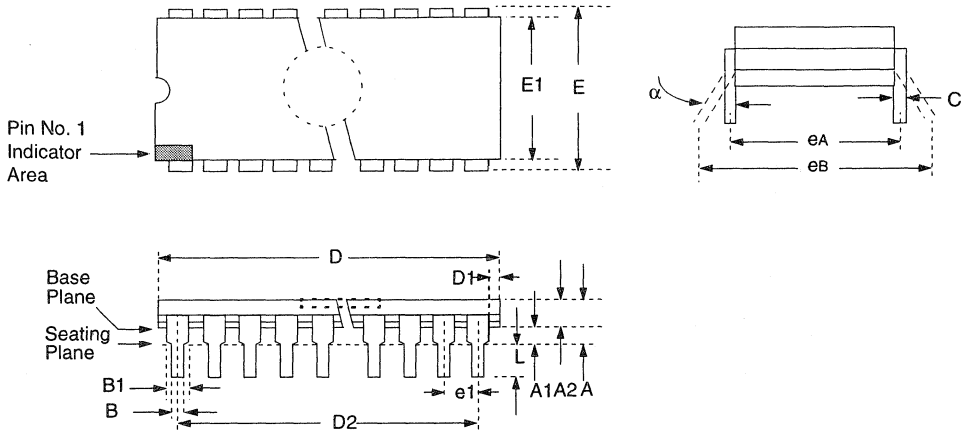
Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Dual In-Line with Window (JW) - (300 mil))



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.30	5.84		.130	0.230	
A1	0.38	—		0.015	—	
A2	2.92	4.95		0.115	0.195	
B	0.35	0.58		0.014	0.023	
B1	1.14	1.78	**Typical**	0.045	0.070	**Typical**
C	0.20	0.38	**Typical**	0.008	0.015	**Typical**
D	34.54	37.72		1.360	1.485	
D2	32.97	33.07	**BSC**	1.298	1.302	**BSC**
E	7.62	8.25		0.300	0.325	
E1	6.10	7.87		0.240	0.310	
e	2.54	2.54	**Typical**	0.100	0.100	**Typical**
eA	7.366	8.128	**BSC**	0.290	0.320	**BSC**
eB	7.620	11.430		0.300	0.450	
L	2.92	5.08		0.115	0.200	
D1	0.13	—		0.005	—	

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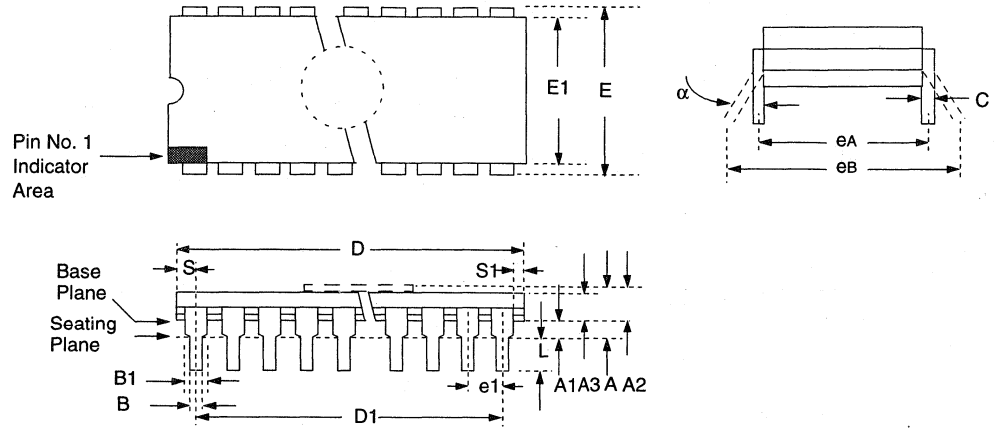
Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Dual In-Line with Window (JW) - (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	36.195	37.465		1.425	1.475	
D1	33.020	33.020	**BSC**	1.300	1.300	**BSC**
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	14.986	15.748	**BSC**	0.590	0.620	**BSC**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

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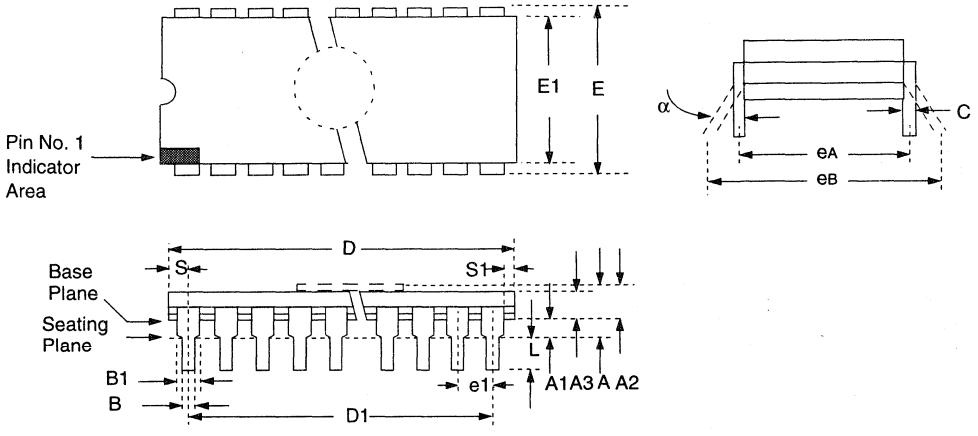
Packaging Diagrams and Parameters

Package Type: 40-Lead Ceramic Dual In-Line with Window (JW) - (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	**BSC**	1.900	1.900	**BSC**
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**BSC**	0.100	0.100	**BSC**
eA	14.986	16.002	**Typical**	0.590	0.630	**Typical**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

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Packaging Diagrams and Parameters

Ceramic Chip Carrier Family

Symbol List for Ceramic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body
A1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D1/E1	Body dimension
D2/E2	Footprint
D3/E3	Footprint
LT	Lead thickness

Notes:

5. All dimensions and tolerances conform to ANSI Y14.5M-1982.
6. Datum plane -H- located at top of parting line and coincident with top of lead. Where lead exits body.
7. Datums D-E and F-G to be determined where center leads exit body at datum plane -H-.
8. To be determined at seating plane -C-.
9. Transition is optional.
10. Square: Details of pin1 identifier are optional but must be located within one of the two zones indicated. If the number of terminals on a side is odd terminal 1 is the center terminal.
    Rectangle: Details of pin1 are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.
11. Location to datums -A- and -B- to be determined at plane -H-.
12. All dimensions and tolerances include lead trim offset and lead finish.
13. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
14. Controlling dimension: inches.

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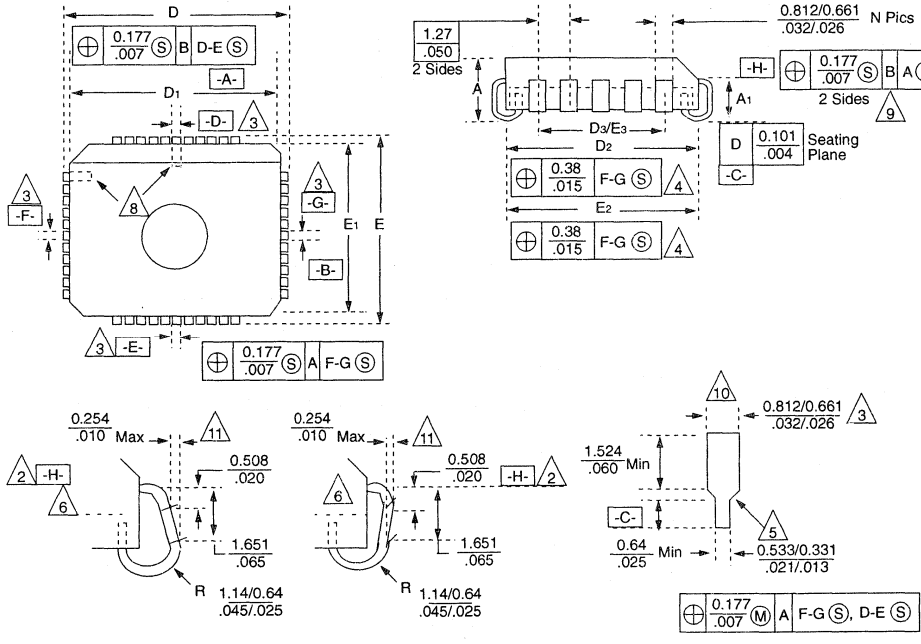
Packaging Diagrams and Parameters

Package Type: 68-Lead Ceramic Leaded (CL) Chip Carrier with Window



Package Group: Ceramic Leaded Chip Carrier (CLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		0.165	0.185	
A1	2.286	3.048		0.090	0.120	
D	24.968	25.222		0.983	0.993	
D1	23.977	24.333		0.944	0.958	
D2	22.860	23.876		0.900	0.940	
D3	20.320	—	BSC	0.800	—	BSC
E	24.968	25.222		0.983	0.993	
E1	23.977	24.333		0.944	0.958	
E2	22.860	23.876		0.900	0.940	
E3	20.320	—	BSC	0.800	—	BSC
CP	—	0.102		—	0.004	
LT	0.152	0.204		0.006	0.008	

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Packaging Diagrams and Parameters

Plastic Dual In-Line (PDIP) Family

Symbol List for Plastic In-Line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
A2	Base body thickness
B	Width of terminal leads
B1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E1	Body width parameters not including leads
eA	Linear spacing of true minimum lead position center line to center line
eB	Linear spacing between true lead position outside of lead to outside of lead
e1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
S	Distance from true position center line of Number 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B1" is nominal.
5. Details of pin Number 1 identifier are optional.
6. Parameters "D + E1" do not include mold flash/protrusions. Mold flash or protrusions shall not exceed .010 inches.

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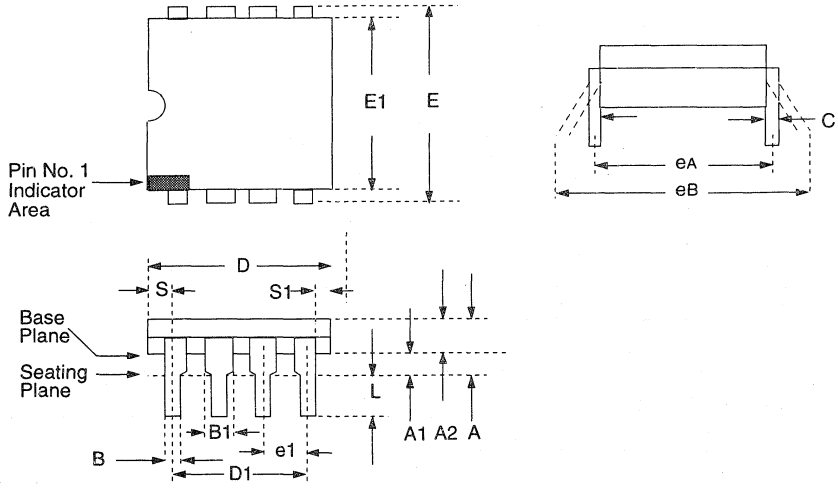
Packaging Diagrams and Parameters

Package Type: 8-Lead Plastic Dual In-Line (P) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	4.064		—	0.160	
A1	0.381	—		0.015	—	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.397	1.651		0.055	0.065	
C	0.203	0.381	Typical	0.008	0.015	Typical
D	9.017	10.922		0.355	0.430	
D1	7.620	7.620	BSC	0.300	0.300	BSC
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	BSC	0.300	0.300	BSC
eB	8.128	9.906		0.320	0.390	
L	3.048	3.556		0.120	0.140	
S	0.889	—		0.035	—	
S1	0.254	—		0.010	—	

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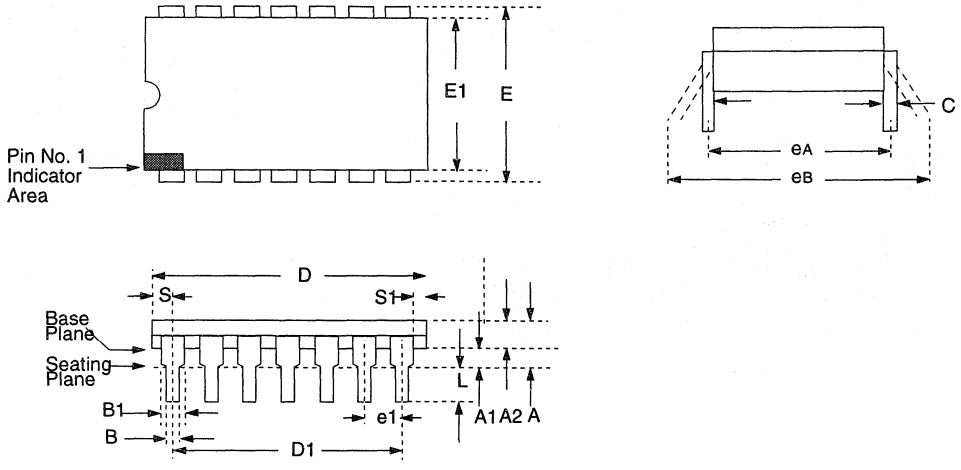
Packaging Diagrams and Parameters

Package Type: 14-Lead Plastic Dual In-Line (P) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	4.064		—	0.160	
A1	0.381	—		0.015	—	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	**BSC**	0.060	0.060	**BSC**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	18.415	19.431		0.725	0.765	
D1	15.240	15.240	**BSC**	0.600	0.600	**BSC**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**BSC**	0.300	0.300	**BSC**
eB	8.128	9.906		0.320	0.390	
L	3.048	3.556		0.120	0.140	
S	0.889	—		0.035	—	
S1	0.127	—		0.005	—	

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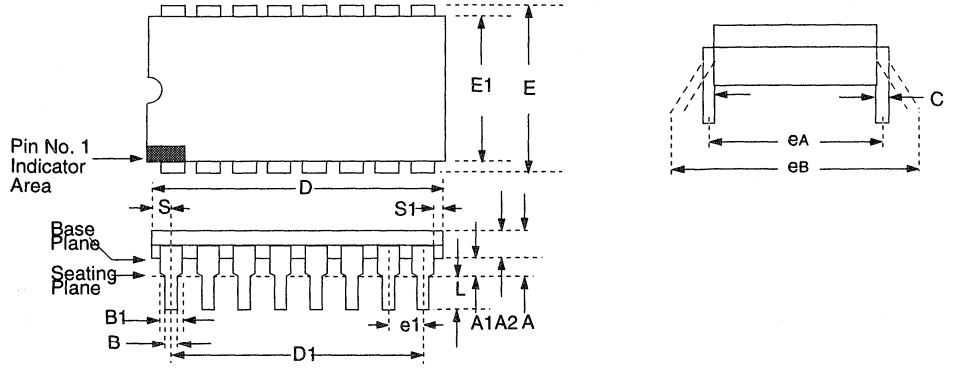
Packaging Diagrams and Parameters

Package Type: 16-Lead Plastic Dual In-Line (P) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	4.064		—	0.160	
A1	0.381	—		0.015	—	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	**BSC**	0.060	0.060	**BSC**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	18.923	19.939		0.745	0.785	
D1	17.780	17.780	**BSC**	0.700	0.700	**BSC**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**BSC**	0.300	0.300	**BSC**
eB	8.128	9.906		0.320	0.390	
L	3.048	3.556		0.120	0.140	
S	0.889	—		0.035	—	
S1	0.127	—		0.005	—	

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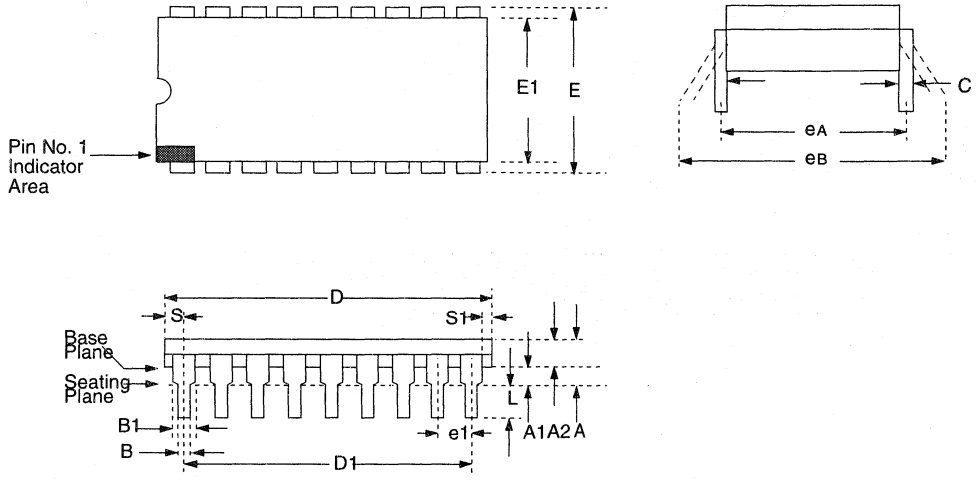
Packaging Diagrams and Parameters

Package Type: 18-Lead Plastic Dual In-Line (P) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	4.064		—	0.160	
A1	0.381	—		0.015	—	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	**BSC**	0.060	0.060	**BSC**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.479	23.495		0.885	0.925	
D1	20.320	20.320	**BSC**	0.800	0.800	**BSC**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**BSC**	0.300	0.300	**BSC**
eB	8.128	9.906		0.320	0.390	
L	3.048	3.556		0.120	0.140	
S	0.889	—		0.035	—	
S1	0.127	—		0.005	—	

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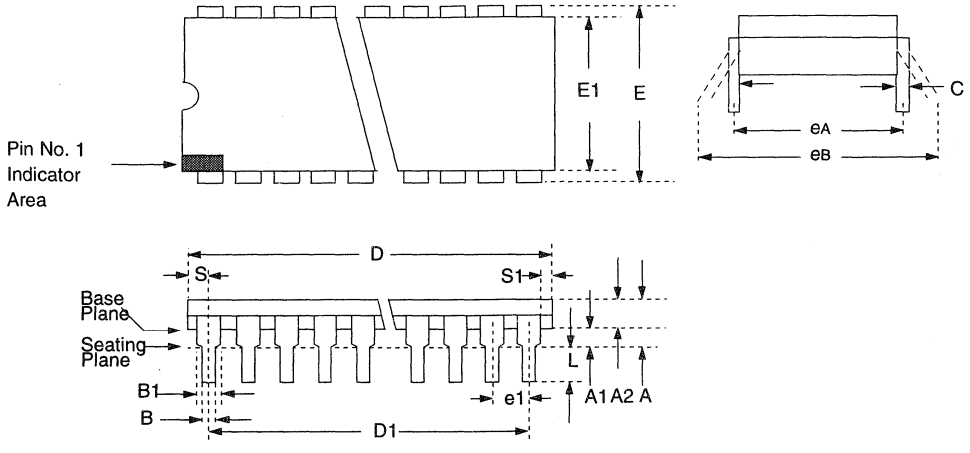
Packaging Diagrams and Parameters

Package Type: 22-Lead Plastic Dual In-Line (P) - 400 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	4.572		—	0.180	
A1	0.381	—		0.015	—	
A2	3.175	3.810		0.125	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	**BSC**	0.060	0.060	**BSC**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	26.670	28.448		1.050	1.120	
D1	25.400	25.400	**BSC**	1.000	1.000	**BSC**
E	9.906	10.795		0.390	0.425	
E1	8.382	9.398		0.330	0.370	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	10.160	10.160	**BSC**	0.400	0.400	**BSC**
eB	10.668	12.192		0.420	0.480	
L	3.048	3.556		0.120	0.140	
S	0.889	—		0.035	—	
S1	0.127	—		0.005	—	

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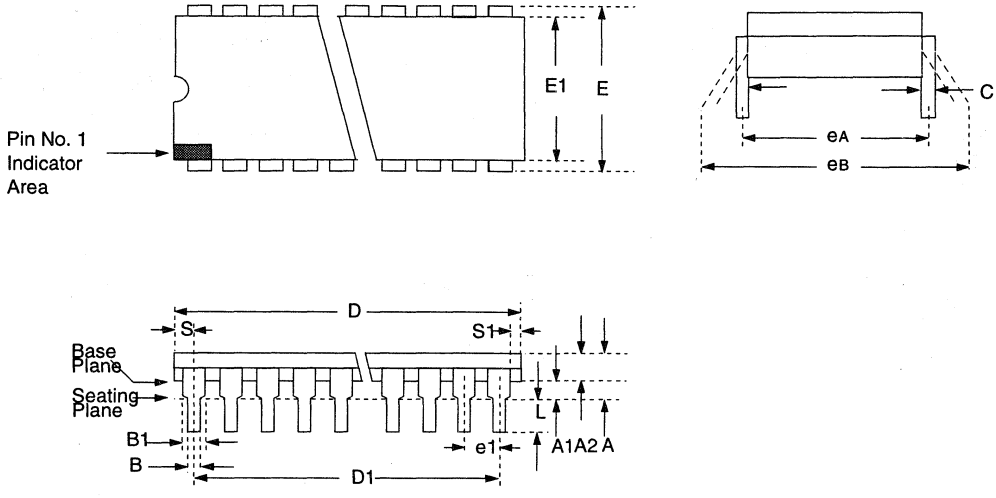
Packaging Diagrams and Parameters

Package Type: 24-Lead Plastic Dual In-Line (P) - 600 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	5.080		—	0.200	
A1	0.508	—		0.020	—	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	30.353	32.385		1.195	1.275	
D1	27.940	27.940	**BSC**	1.100	1.100	**BSC**
E	15.240	15.875		0.600	0.625	
E1	12.827	14.224		0.505	0.560	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**BSC**	0.600	0.600	**BSC**
eB	15.748	17.272		0.620	0.680	
L	3.048	3.556		0.120	0.140	
S	0.889	—		0.035	—	
S1	0.127	—		0.005	—	

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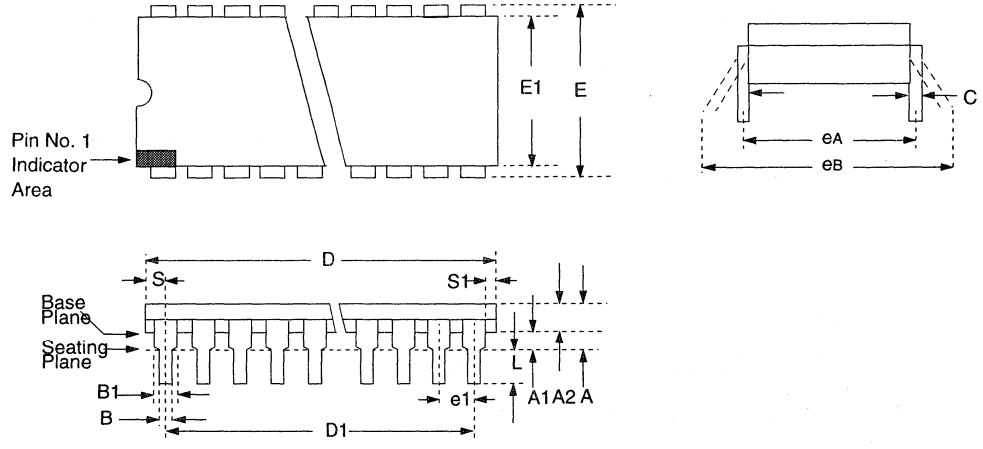
Packaging Diagrams and Parameters

Package Type: 24-Lead Skinny Plastic Dual In-Line (SP) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	4.064		—	0.160	
A1	0.381	—		0.015	—	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	31.242	32.258		1.230	1.270	
D1	27.940	27.940	**BSC**	1.100	1.100	**BSC**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**BSC**	0.300	0.300	**BSC**
eB	8.128	9.906		0.320	0.390	
L	3.048	3.556		0.120	0.140	
S	0.889	—		0.035	—	
S1	0.381	—		0.015	—	

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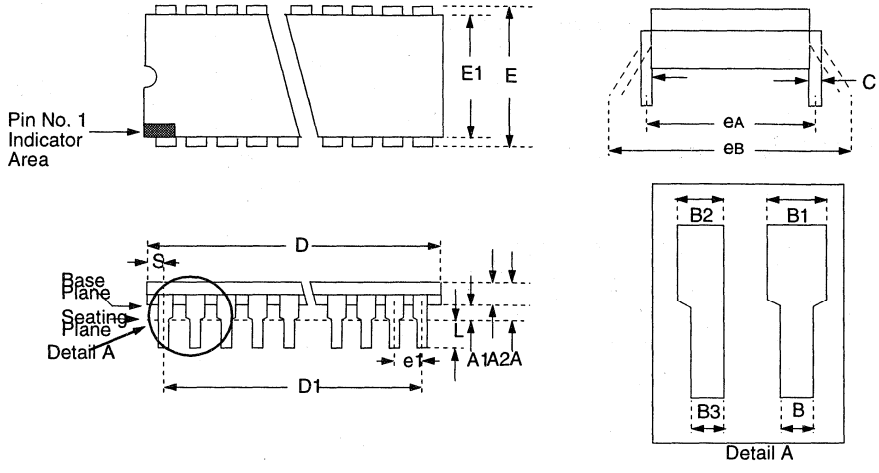
Packaging Diagrams and Parameters

Package Type: 28-Lead Skinny Plastic Dual In-Line (SP) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.632	4.572		0.143	0.180	
A1	0.381	—		0.015	—	
A2	3.175	3.556		0.125	0.140	
B	0.406	0.559		0.016	0.022	
B1	1.016	1.651	**Typical**	0.040	0.065	**Typical**
B2	0.762	1.016	**4 places**	0.030	0.040	**4 places**
B3	0.203	0.508	**4 places**	0.008	0.020	**4 places**
C	0.203	0.331	**Typical**	0.008	0.013	**Typical**
D	34.163	35.179		1.385	1.395	
D1	33.020	33.020	**BSC**	1.300	1.300	**BSC**
E	7.874	8.382		0.310	0.330	
E1	7.112	7.493		0.280	0.295	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	7.874	7.874	**BSC**	0.310	0.310	**BSC**
eB	8.128	9.906		0.320	0.390	
L	3.175	3.683		0.125	0.145	
S	0.584	1.220		0.023	0.048	

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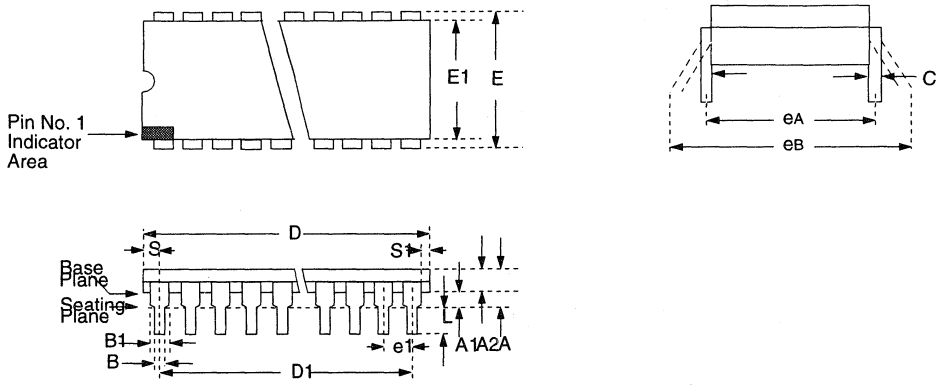
Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Dual In-Line (P) - 600 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	5.080		—	0.200	
A1	0.508	—		0.020	—	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.778	**Typical**	0.050	0.070	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	35.052	37.084		1.380	1.460	
D1	33.020	33.020	**BSC**	1.300	1.300	**BSC**
E	15.240	15.875		0.600	0.625	
E1	12.827	13.970		0.505	0.550	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**BSC**	0.600	0.600	**BSC**
eB	15.748	17.272		0.620	0.680	
L	2.921	3.683		0.115	0.145	
S	0.889	—		0.035	—	
S1	0.508	—		0.020	—	

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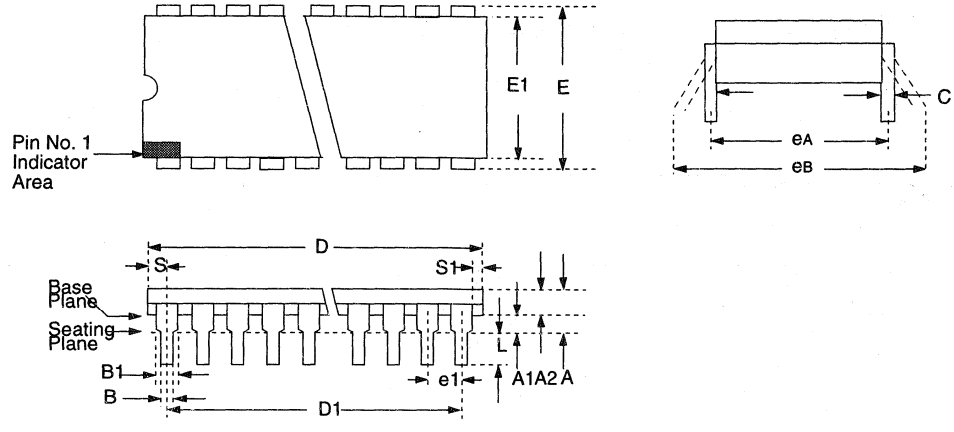
Packaging Diagrams and Parameters

Package Type: 40-Lead Plastic Dual In-Line (P) - 600 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	5.080		—	0.200	
A1	0.381	—		0.015	—	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.181	52.197		2.015	2.055	
D1	48.260	48.260	BSC	1.900	1.900	BSC
E	15.240	15.875		0.600	0.625	
E1	13.462	13.970		0.530	0.550	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	BSC	0.600	0.600	BSC
eB	15.748	17.272		0.620	0.680	
L	2.921	3.683		0.115	0.145	
S	1.270	—		0.050	—	
S1	0.508	—		0.020	—	

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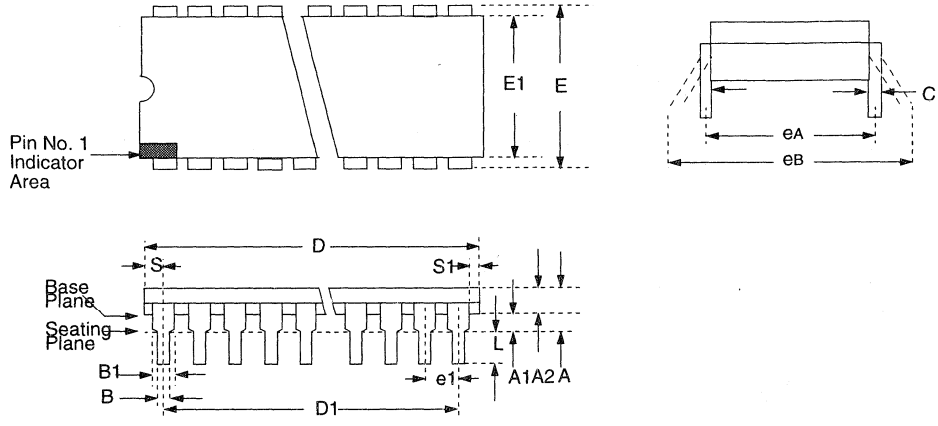
Packaging Diagrams and Parameters

Package Type: 48-Lead Plastic Dual In-Line (P) - 600 mil



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	—	5.080		—	0.200	
A1	0.381	—		0.015	—	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	61.468	62.230		2.420	2.450	
D1	58.420	58.420	**BSC**	2.300	2.300	**BSC**
E	15.240	15.875		0.600	0.625	
E1	13.716	14.224		0.540	0.560	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**BSC**	0.600	0.600	**BSC**
eB	15.748	17.272		0.620	0.680	
L	2.921	3.683		0.115	0.145	
S	1.270	—		0.050	—	
S1	0.508	—		0.020	—	

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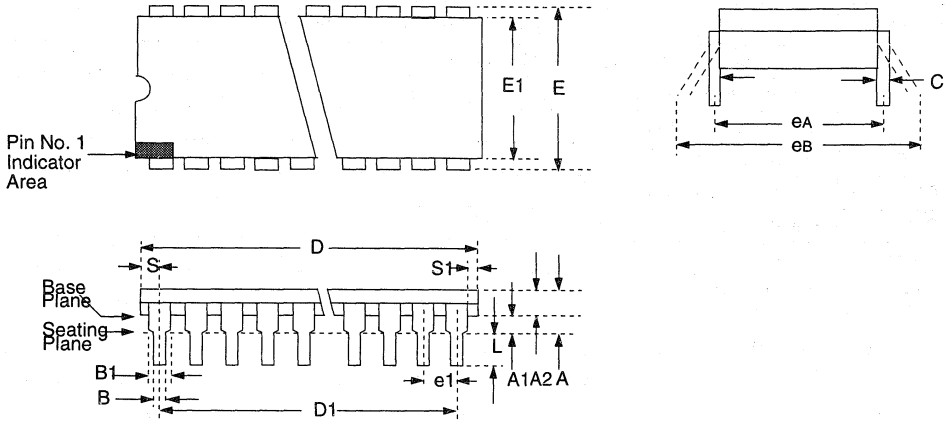
Packaging Diagrams and Parameters

Package Type: 64-Lead Shrink Plastic Dual In-Line (SP) - 750 mil



Package Group: Plastic Dual In-Line (PLA)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	—	5.08		—	0.200	
A1	0.51	—		0.020	—	
A2	3.38	4.27		0.133	0.168	
B	0.38	0.56		0.015	0.022	
B1	.076	1.27	Typical	0.030	0.050	Typical
C	0.20	0.30	Typical	0.008	0.012	Typical
D	57.40	57.91		2.260	2.280	
D1	55.12	55.12	BSC	2.170	2.170	BSC
E	19.05	19.69		0.750	0.775	
E1	16.76	17.27		0.660	0.680	
e1	1.73	1.83	Typical	0.068	0.072	Typical
eA	19.05	19.05	BSC	0.750	0.750	BSC
eB	19.05	21.08		0.750	0.830	
L	3.05	3.43		0.120	0.135	
S	1.19	—		0.047	—	
S1	0.686	—		0.027	—	

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Packaging Diagrams and Parameters

Plastic Leaded Chip Carrier (PLCC) Family

Symbol List for Plastic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body
A1	Distance between lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D1/E1	Plastic body dimension
D2/E2	Footprint
D3/E3	Footprint
LT	Lead thickness

Notes:

7. All dimensions and tolerances conform to ANSI Y14.5M-1982.
8. Datum plane -H- located at top of mold parting line and coincident with top of lead where lead exits plastic body.
9. Datums D-E and F-G to be determined where center leads exit plastic body at datum plane -H-.
10. To be determined at seating plane -C-.
11. Transition is optional.
12. Plastic body details between leads are optional.
13. Dimension D1 and E1 do not include mold protrusion. Allowable mold protrusion is .254mm/.010in. per side. Dimensions D and E include mold mismatch and are determined at parting line.
14. Square: Details of pin 1 identifier are optional but must be located within one of the two zones indicated. Rectangle: Details of pin 1 identifier are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.
15. Location of datums -A- and -B- to be determined at plane -H-.
16. All dimensions and tolerances include lead trim offset and lead finish.
17. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
18. Controlling dimension: inches.

X. Sum of dambar protrusions to be 0.17 (.007) max. per lead.

Y. Feature is not required, but is optional at manufacturer's discretion.

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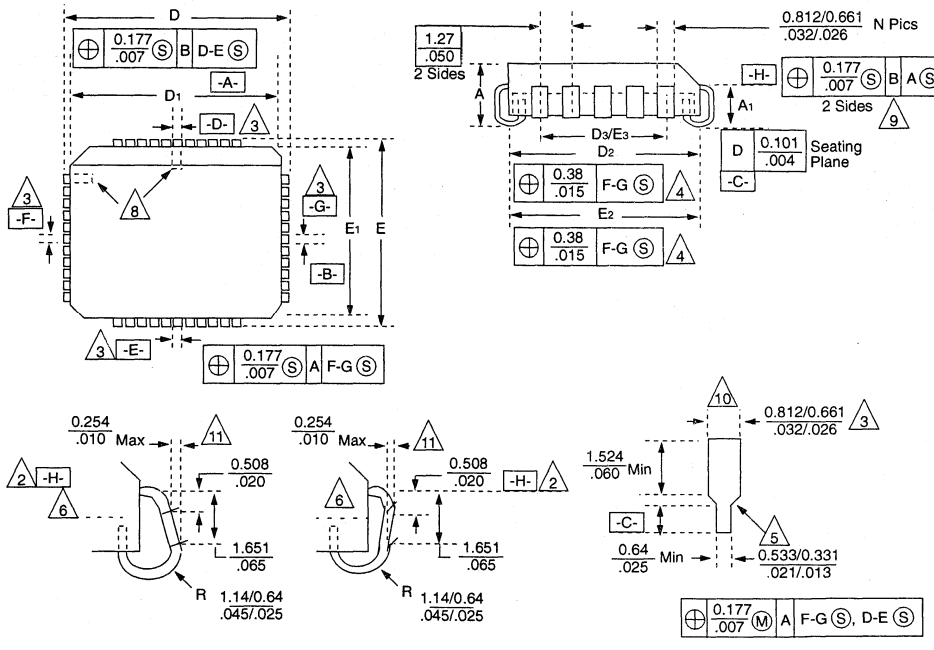
Packaging Diagrams and Parameters

Package Type: 20-Lead Plastic Leaded Chip Carrier (L) -Square



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.286	3.048		0.090	0.120	
D	9.779	10.033		0.385	0.395	
D1	8.89	9.042		0.350	0.356	
D2	7.366	8.382		0.290	0.330	
D3	5.080	5.080	BSC	0.200	0.200	BSC
E	9.779	10.033		0.385	0.395	
E1	8.89	9.042		0.350	0.356	
E2	7.366	8.382		0.290	0.330	
E3	5.080	5.080	BSC	0.200	0.200	BSC
CP	—	0.102		—	0.004	
LT	0.203	0.381		0.008	0.015	

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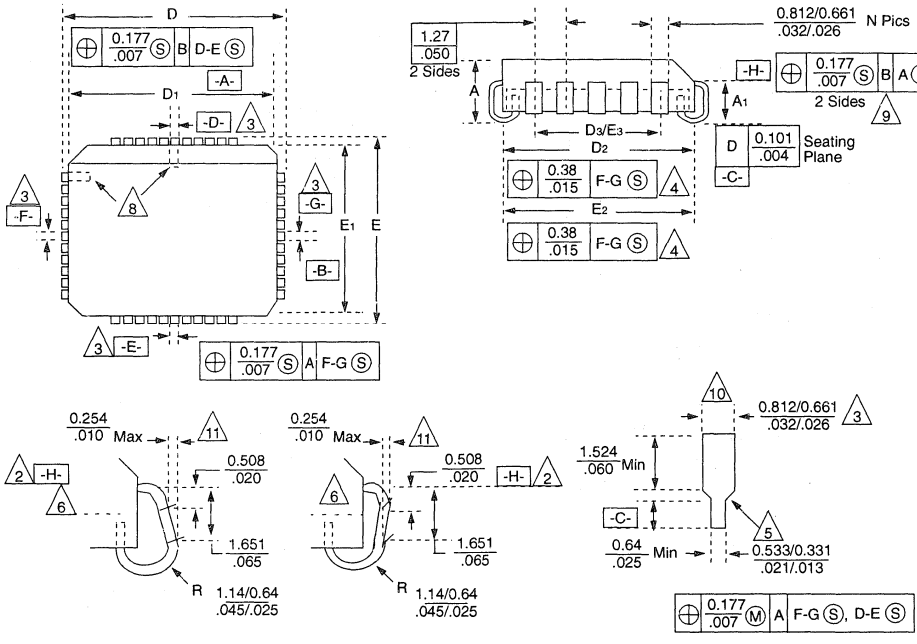
Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Leaded Chip Carrier (L) -Square



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.286	3.048		0.090	0.120	
D	12.319	12.573		0.485	0.495	
D1	11.430	11.583		0.450	0.456	
D2	10.414	10.922		0.410	0.430	
D3	7.620	7.620	BSC	0.300	0.300	BSC
E	12.319	12.573		0.485	0.495	
E1	11.430	11.583		0.450	0.456	
E2	10.414	10.922		0.410	0.430	
E3	7.620	7.620	BSC	0.300	0.300	BSC
CP	—	0.102		—	0.004	
LT	0.203	0.381		0.008	0.015	

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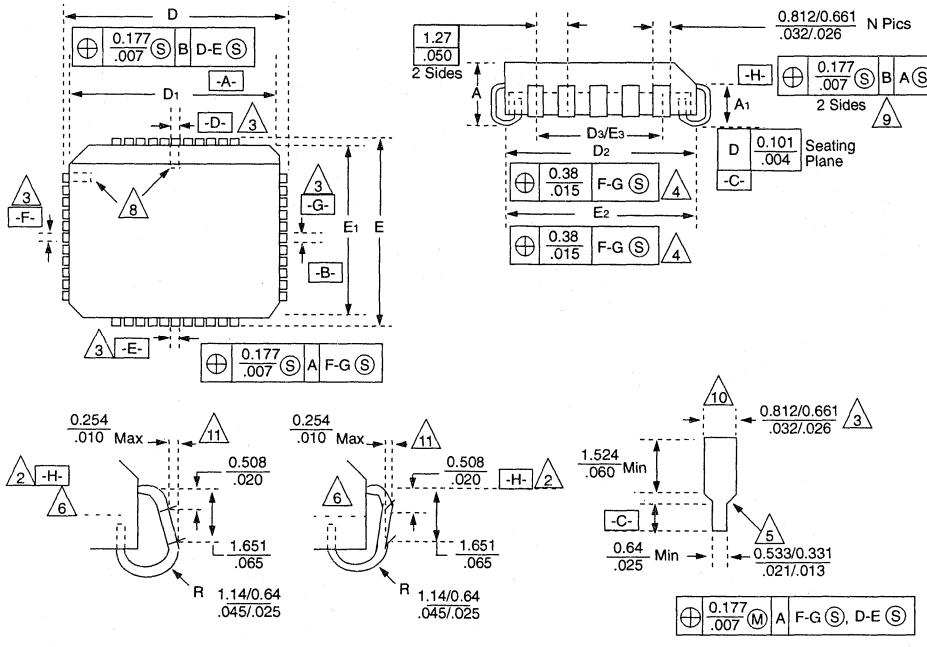
Packaging Diagrams and Parameters

Package Type: 32-Lead Plastic Leaded Chip Carrier (L) - Rectangle



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.048	3.556		0.120	0.140	
A1	1.905	2.413		0.075	0.095	
D	12.319	12.573		0.485	0.495	
D1	11.353	11.507		0.447	0.453	
D2	9.310	10.780		0.380	0.440	
D3	7.620	7.620	BSC	0.300	0.300	BSC
E	14.859	15.113		0.585	0.595	
E1	13.893	14.047		0.547	0.553	
E2	11.760	13.230		0.480	0.540	
E3	10.160	10.160	BSC	0.400	0.400	BSC
CP	—	0.102		—	0.004	
LT	0.203	0.381		0.008	0.015	

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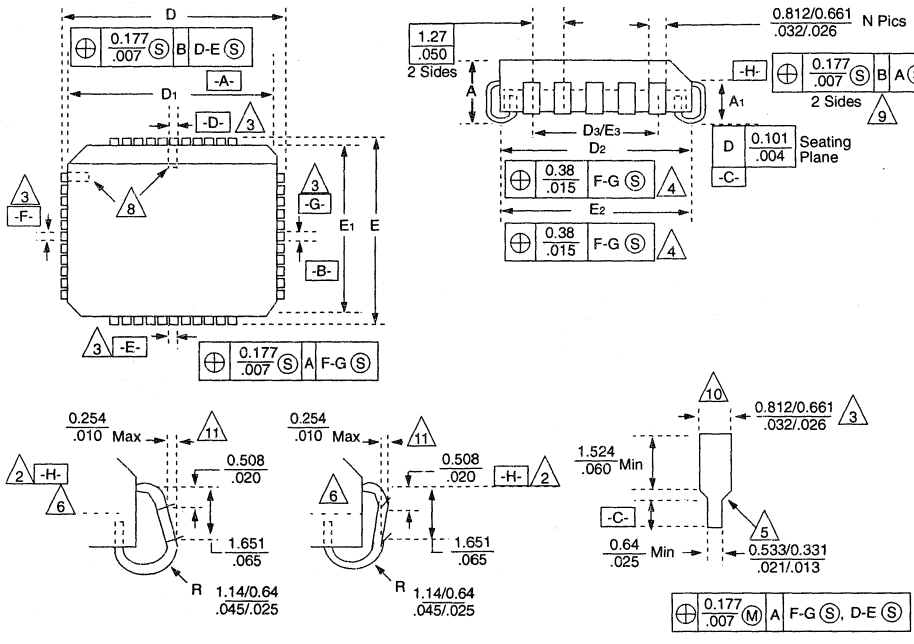
Packaging Diagrams and Parameters

Package Type: 44-Lead Plastic Leaded Chip Carrier (L) - Square



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	17.399	17.653		0.685	0.695	
D1	16.510	16.663		0.650	0.656	
D2	15.494	16.002		0.610	0.630	
D3	12.700	12.700	BSC	0.500	0.500	BSC
E	17.399	17.653		0.685	0.695	
E1	16.510	16.663		0.650	0.656	
E2	15.494	16.002		0.610	0.630	
E3	12.700	12.700	BSC	0.500	0.500	BSC
CP	—	0.102		—	0.004	
LT	0.203	0.381		0.008	0.015	

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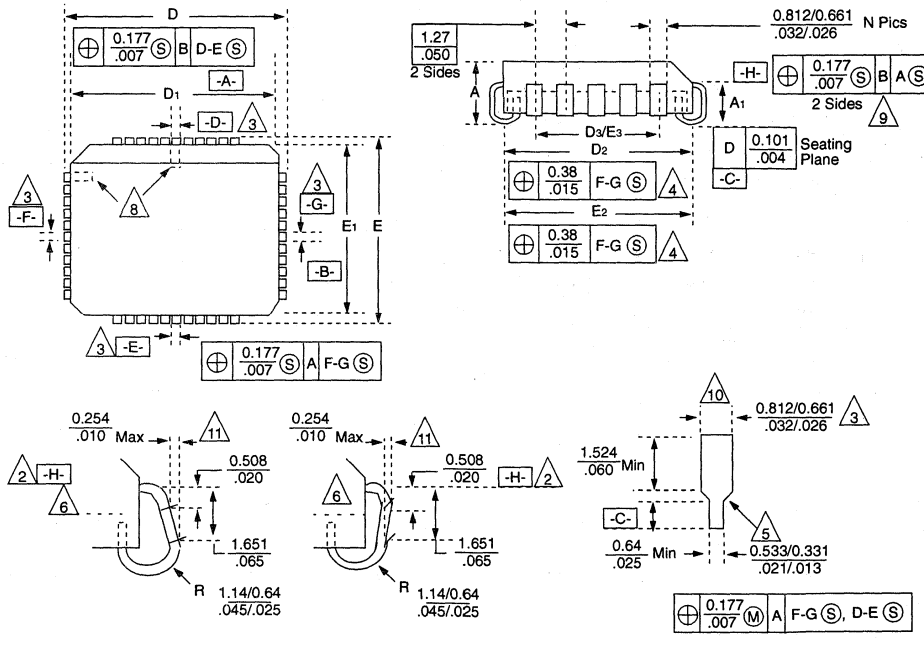
Packaging Diagrams and Parameters

Package Type: 68-Lead Plastic Leaded Chip Carrier (L) - Square



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		0.165	0.185	
A1	2.286	2.794		0.090	0.110	
D	25.019	25.273		0.985	0.995	
D1	24.130	24.334		0.950	0.958	
D2	22.860	23.622		0.900	0.930	
D3	20.320	20.320	**BSC**	0.800	0.800	**BSC**
E	25.019	25.273		0.985	0.995	
E1	24.130	24.334		0.950	0.958	
E2	22.860	23.622		0.900	0.930	
E3	20.320	20.320	**BSC**	0.800	0.800	**BSC**
CP	—	0.102		—	0.004	
LT	0.203	0.254		0.008	0.010	

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Packaging Diagrams and Parameters

Plastic Small Outline (SOIC) Family

Symbol List for Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: inches.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .006 package ends and .010 on sides.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area to indicate pin1 position.
5. Terminal numbers are shown for reference.

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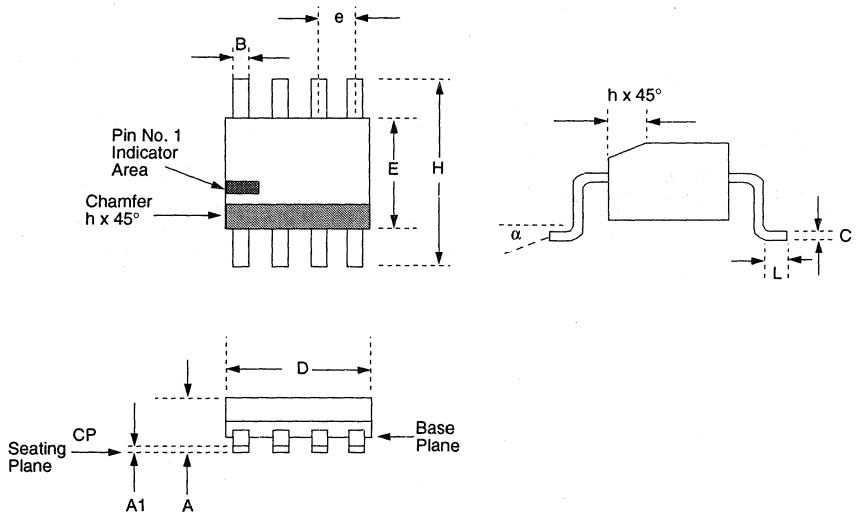
Packaging Diagrams and Parameters

Package Type: 8-Lead Plastic Small Outline (SN) - Narrow, 150 mil Body



Package Group: Plastic SOIC (SN)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.371	1.728		0.054	0.068	
A1	0.101	0.249		0.004	0.010	
B	0.355	0.483		0.014	0.019	
C	0.190	0.249		0.007	0.010	
D	4.800	4.979		0.189	0.196	
E	3.810	3.988		0.150	0.157	
e	1.270	1.270	BSC	0.050	0.050	BSC
H	5.816	6.198		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
CP	—	0.102		—	0.004	

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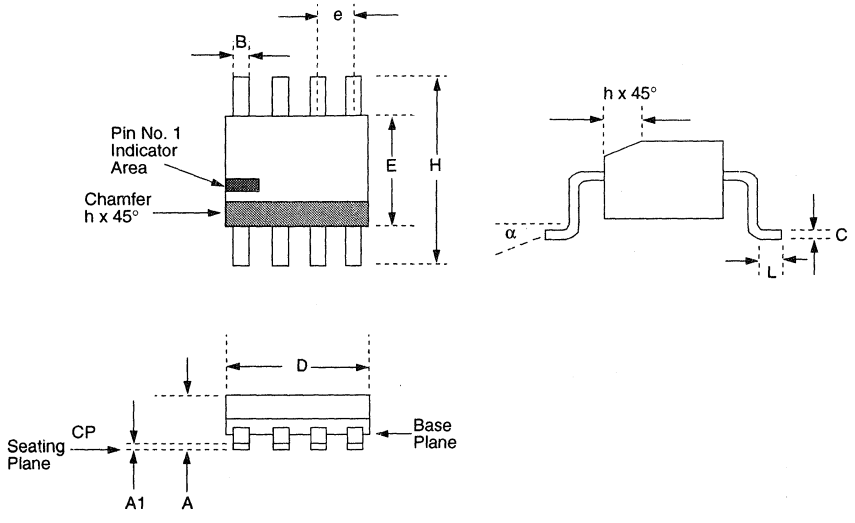
Packaging Diagrams and Parameters

Package Type: 8-Lead Plastic Small Outline (SM) - Medium, 208 mil Body



Package Group: Plastic SOIC (SM)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.778	2.00		0.070	0.029	
A1	0.101	0.249		0.004	0.010	
B	0.355	0.483		0.014	0.019	
C	0.190	0.249		0.007	0.010	
D	5.080	5.334		0.200	0.210	
E	5.156	5.411		0.203	0.213	
e	1.270	1.270	**BSC**	0.050	0.050	**BSC**
H*	7.670	8.103		0.302	0.319	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
CP	—	0.102		—	0.004	

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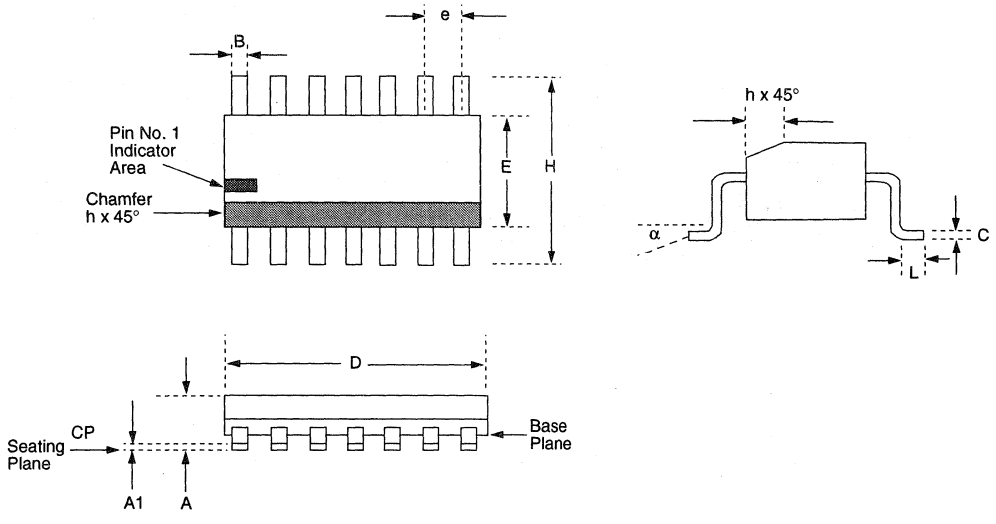
Packaging Diagrams and Parameters

Package Type: 14-Lead Plastic Small Outline (SL) - Narrow, 150 mil Body



Package Group: Plastic SOIC (SL)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.371	1.728		0.054	0.068	
A1	0.101	0.249		0.004	0.010	
B	0.355	0.483		0.014	0.019	
C	0.190	0.249		0.008	0.010	
D	8.559	9.983		0.337	0.393	
E	3.810	3.988		0.150	0.157	
e	1.270	1.270	BSC	0.050	0.050	BSC
H	5.816	6.198		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
CP	—	0.102		—	0.004	

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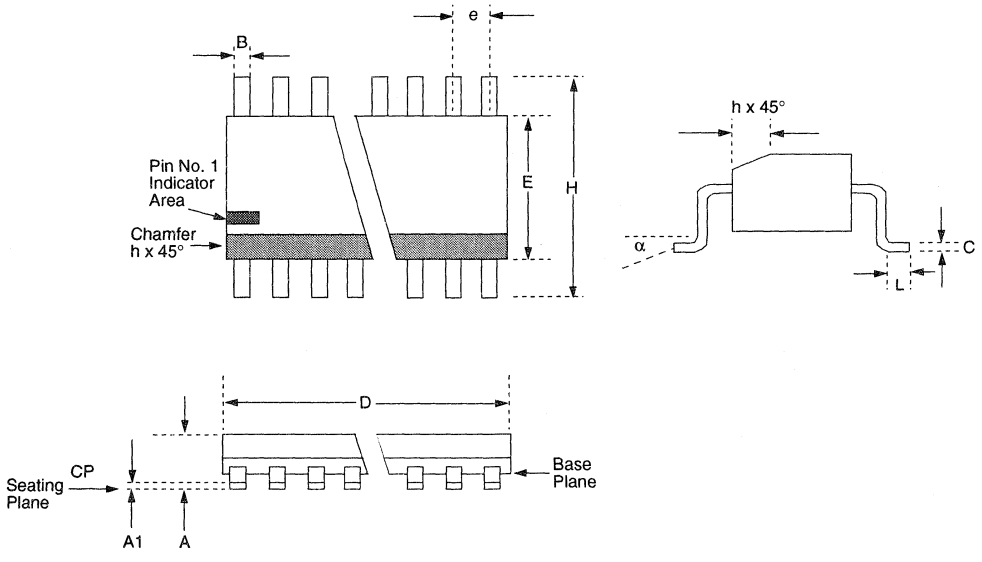
Packaging Diagrams and Parameters

Package Type: 18-Lead Plastic Small Outline (SO) - Wide, 300 mil Body



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	11.353	11.735		0.447	0.462	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	**BSC**	0.050	0.050	**BSC**
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
CP	—	0.102		—	0.004	

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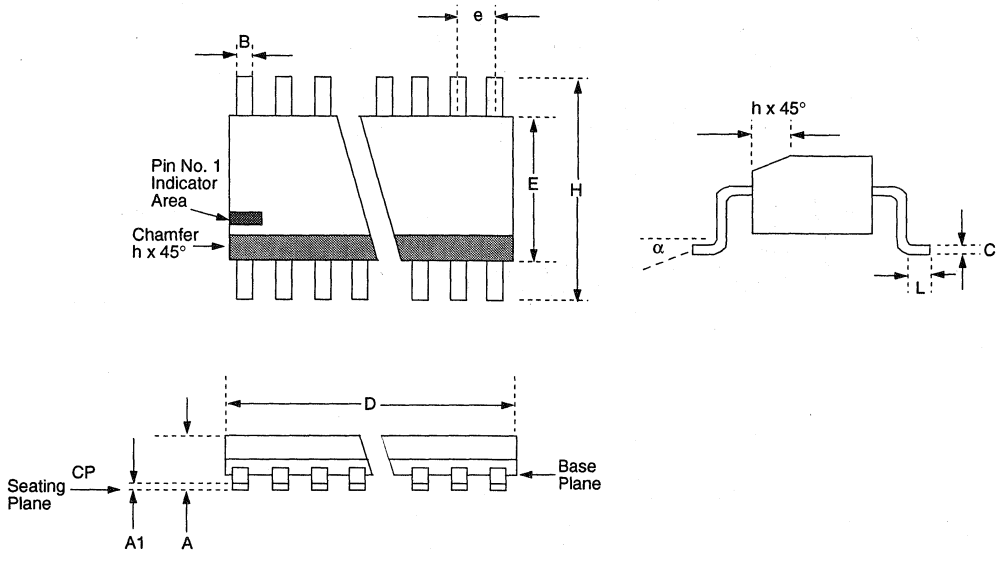
Packaging Diagrams and Parameters

Package Type: 24-Lead Plastic Small Outline (SO) - Wide, 300 mil Body



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	15.214	15.596		0.599	0.614	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	**BSC**	0.050	0.050	**BSC**
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
CP	—	0.102		—	0.004	

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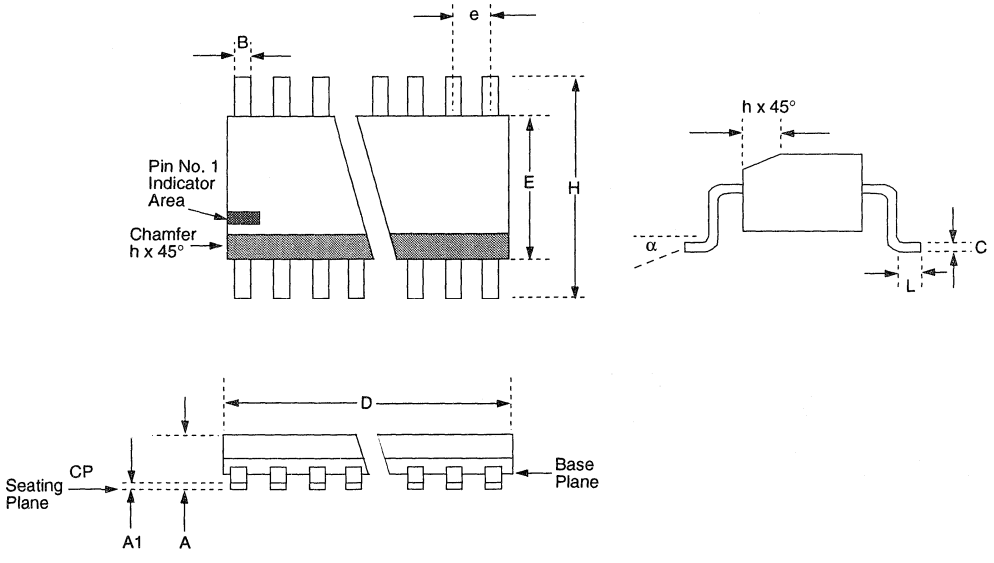
Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Small Outline (SO) - Wide, 300 mil Body



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	17.703	18.085		0.697	0.712	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	**BSC**	0.050	0.050	**BSC**
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
CP	—	0.102		—	0.004	

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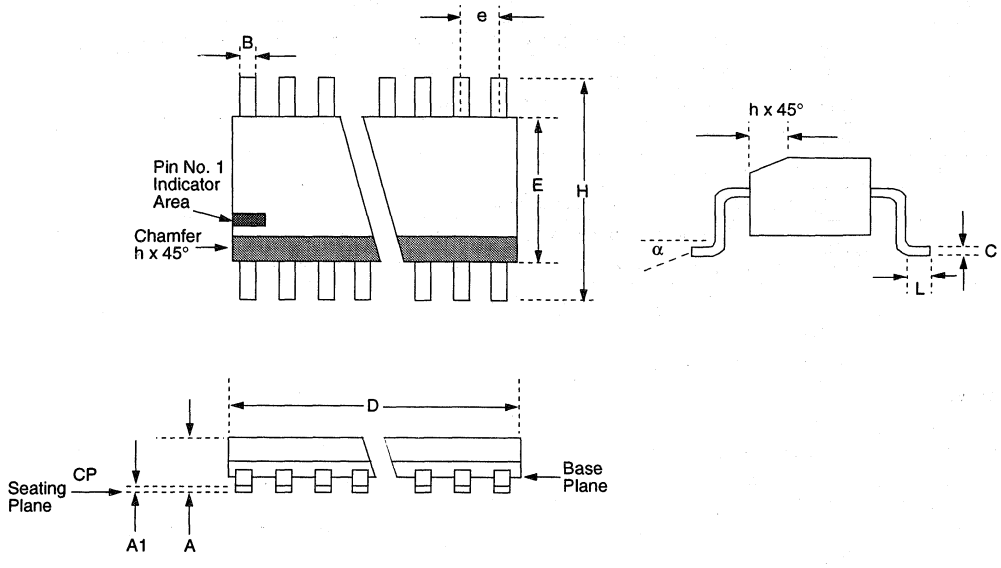
Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Small Outline (SO) - Wide, 330 mil Body



Package Group: Plastic SOIC (SW)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	2.286	2.642		0.090	0.104	
A1	0.101	0.280		0.004	0.011	
B	0.355	0.508		0.014	0.020	
C	0.228	0.305		0.009	0.012	
D	17.780	18.085		0.700	0.712	
E	8.636	8.890		0.340	0.350	
e	1.270	1.270	BSC	0.050	0.050	BSC
H	11.760	12.116		0.463	0.477	
h	0.254	0.737		0.010	0.029	
L	0.508	1.067		0.020	0.042	
CP	—	0.102		—	0.004	

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Packaging Diagrams and Parameters

Plastic Shrink Small Outline (SSOP) Family

Symbol List for Shrink Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: mm.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .015mm .006 package ends and .010" on sides.
4. A .25mm visual index feature must be located within the shaded area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

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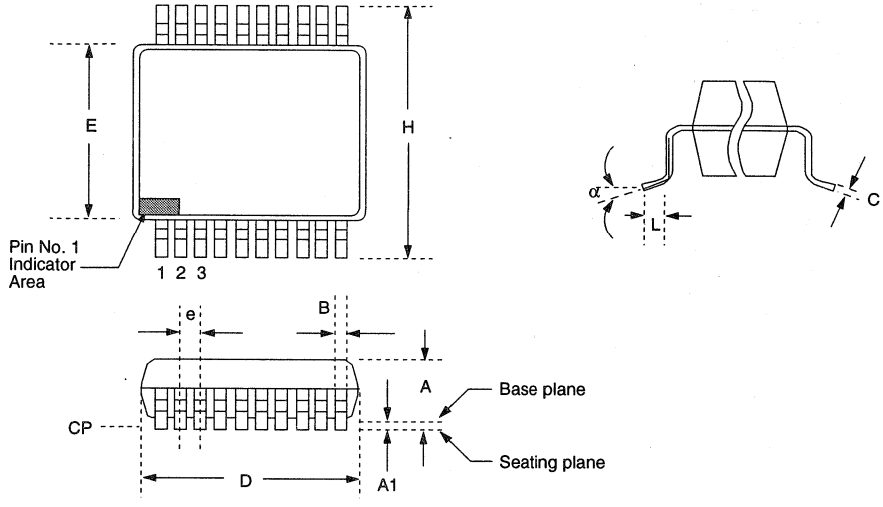
Packaging Diagrams and Parameters

Package Type: 20-Lead Plastic Shrink Small Outline (SS) - 209 mil Body 5.30 mm



Package Group: Plastic SSOP (SS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	7.070	7.330		0.278	0.289	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	**BSC**	0.026	0.026	**BSC**
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
CP	—	0.102		—	0.004	

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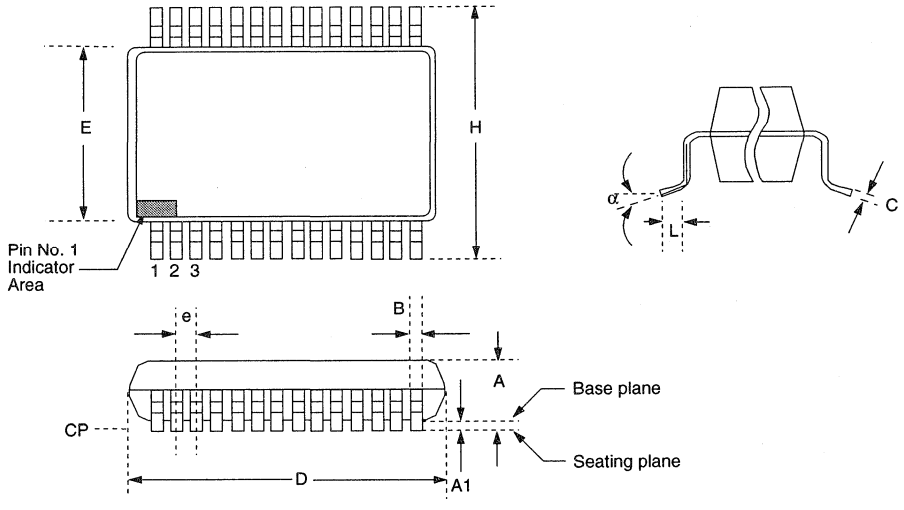
Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Shrink Small Outline (SS) - 209 mil Body 5.30 mm



Package Group: Plastic SSOP (SS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	10.070	10.330		0.396	0.407	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	**BSC**	0.026	0.026	**BSC**
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
CP	—	0.102		—	0.004	

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Packaging Diagrams and Parameters

Plastic Thin Shrink Small Outline (TSSOP) Family

Symbol List for Thin Shrink Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: mm.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .015mm per side.
4. The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusions and an adjacent lead to be 0.14mm.
5. A .25mm visual index feature must be located within the shaded area to indicate pin 1 position.
6. Terminal numbers are shown for reference.

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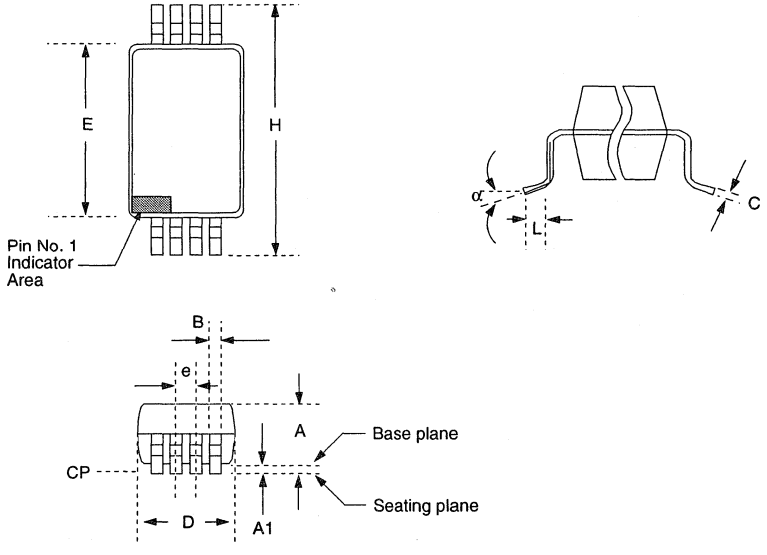
Packaging Diagrams and Parameters

Package Type: 8-Lead Thin Shrink Small Outline (ST) - 4.4 mm



Package Group: Plastic TSSOP (ST)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	—	1.1000		—	0.0433	
A1	0.0500	0.1500		0.0020	0.0060	
B	0.1900	0.3000		0.0075	0.0118	
C	0.0900	0.2000		0.0035	0.0079	
D	2.9000	3.1000		0.1140	0.1220	
E	4.3000	4.5000		0.1690	0.1770	
e	0.6500	0.6500	**BSC**	0.0256	0.0256	**BSC**
H	6.2500	6.5000		0.2460	0.2560	
L	0.5000	0.7000		0.0200	0.0280	
CP	—	0.1020		—	0.0040	

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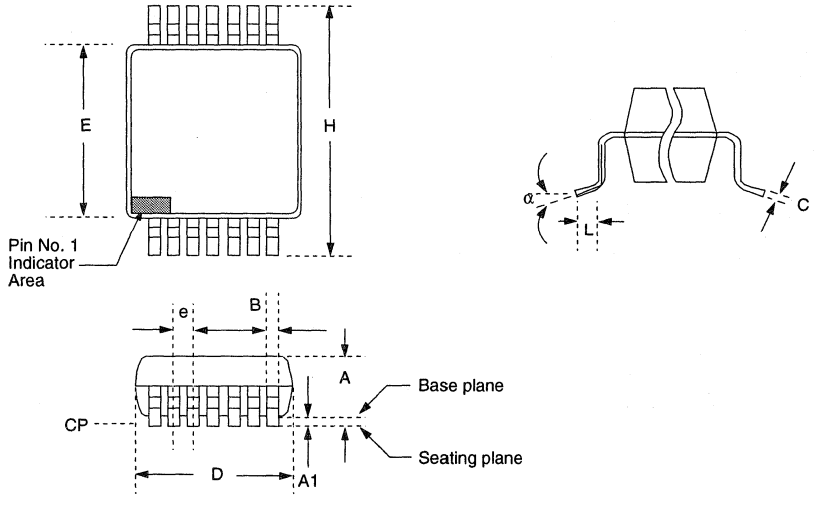
Packaging Diagrams and Parameters

Package Type: 14-Lead Thin Shrink Small Outline (ST) - 4.4 mm



Package Group: Plastic TSSOP (ST)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	—	1.1000		—	0.0433	
A1	0.0500	0.1500		0.0020	0.0060	
B	0.1900	0.3000		0.0075	0.0118	
C	0.0900	0.2000		0.0035	0.0079	
D	4.9000	5.1000		0.1930	0.2010	
E	4.3000	4.5000		0.1690	0.1770	
e	0.6500	0.6500	BSC	0.0256	0.0256	BSC
H	6.2500	6.5000		0.2460	0.2560	
L	0.5000	0.7000		0.0200	0.0280	
CP	—	0.1020		—	0.0040	

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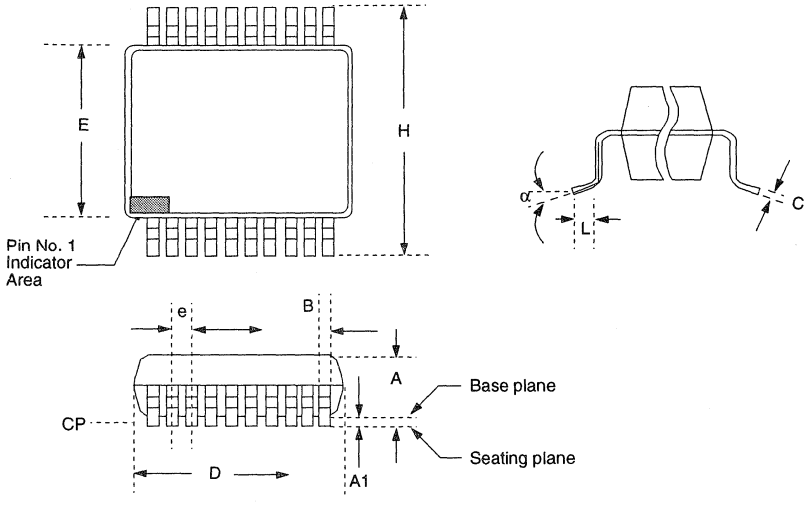
Packaging Diagrams and Parameters

Package Type: 20-Lead Thin Shrink Small Outline (ST) - 4.4 mm



Package Group: Plastic TSSOP (ST)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	—	1.1000		—	0.0433	
A1	0.0500	0.1500		0.0020	0.0060	
B	0.1900	0.3000		0.0075	0.0118	
C	0.0900	0.2000		0.0035	0.0079	
D	6.4000	6.6000		0.2520	0.2600	
E	4.3000	4.5000		0.1690	0.1770	
e	0.6500	0.6500	BSC	0.0256	0.0256	BSC
H	6.2500	6.5000		0.2460	0.2560	
L	0.5000	0.7000		0.0200	0.0280	
CP	—	0.1020		—	0.0040	

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Packaging Diagrams and Parameters

Plastic Thin Small Outline (TSOP) and Very Small Outline (VSOP) Families

Symbol List for Thin Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: inches.
2. All packages are gull wing lead form.
3. "D" and "E" are BSC datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005 per side.
4. A visual index feature must be located within the crosshatched area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

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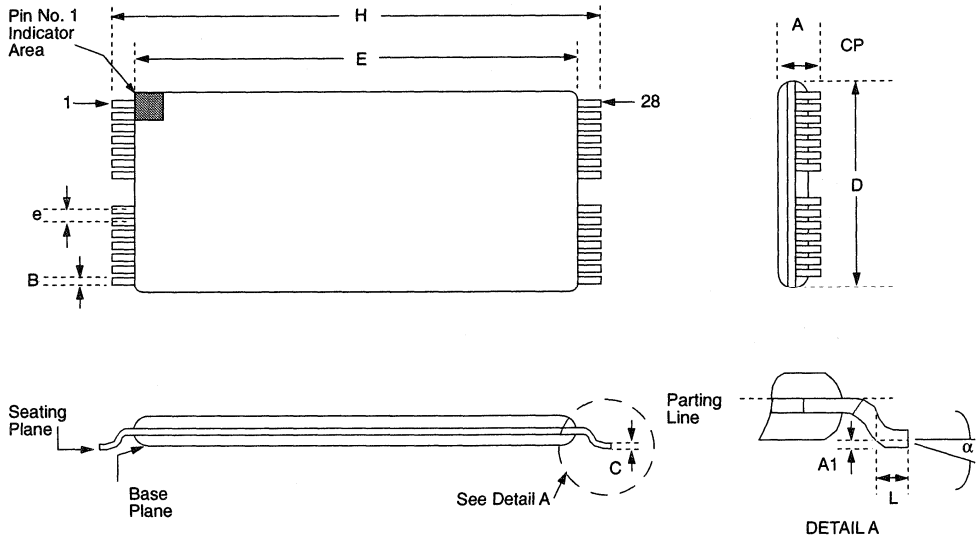
Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Thin Small Outline (TS) - 8 x 20 mm



Package Group: Plastic TSOP (TS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	—	1.190		—	0.047	
A1	0.050	0.150		0.002	0.006	
B	0.150	0.250		0.006	0.010	
C	0.100	0.200		0.004	0.008	
D	7.800	8.200		0.307	0.323	
E	18.290	18.490		0.720	0.728	
e	0.510	—	BSC	0.020	—	BSC
H	19.810	20.190		0.780	0.795	
L	0.410	0.610		0.016	0.024	
CP	—	0.102		—	0.004	

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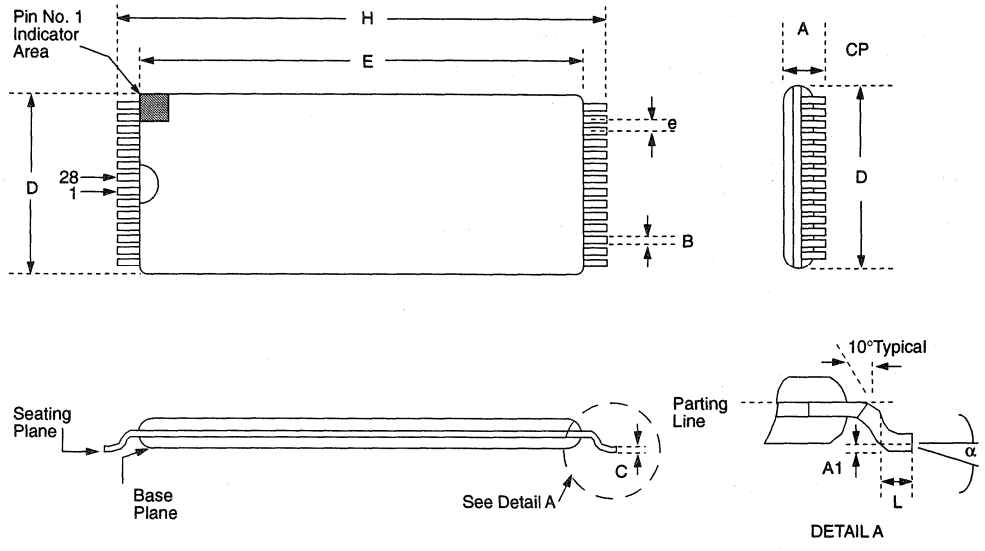
Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Very Small Outline (VS) - 8 x 13.4 mm



Package Group: Plastic VSOP (VS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	1.000	1.250		0.039	0.049	
A1	0.000	0.200		0.000	0.008	
B	0.150	0.300		0.006	0.012	
C	0.130	0.220		0.005	0.009	
D	7.900	8.100		0.311	0.319	
E	11.700	11.900		0.460	0.468	
e	0.550	—	BSC	0.022	—	BSC
H	13.100	13.700		0.516	0.539	
L	0.300	0.700		0.012	0.027	
CP	—	0.102		—	0.004	

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Packaging Diagrams and Parameters

Plastic Quad Flatpack (QFP) Family

Symbol List for Metric Plastic Quad Flatpack Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
A2	Distance from base plane to highest point of body
b	Width of terminals
C	Thickness of terminals
D1/E1	Largest overall package parameter including leads
D/E	Largest overall package parameter including leads
D3/E3	Center of end lead to center of end lead
e	Linear spacing of true minimum lead position center line to center line
L	Length of terminal for soldering to a substrate
CP	Seating plane coplanarity

Notes:

6. All dimensions and tolerances conform to ANSI Y14.5M-1982.
7. Datum plane -H- is located at bottom of mold parting line and coincident with bottom of lead, where lead exits body.
8. Datums A-B and -D- to be determined at datum plane -H-.
9. To be determined at seating plane -C-.
10. Dimension D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25mm per side. Dimensions D1 and E1 do not include mold mismatch and are determined at datum plane -H-.
11. Details of pin 1 identifier are optional but must be located within the zone indicated.
12. These dimensions to be determined at datum plane -H-.
13. All dimensions are in millimeters.
14. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.
15. Exact shape of this feature is optional.
16. Controlling parameter: millimeters.
17. All packages are gull wing lead form.

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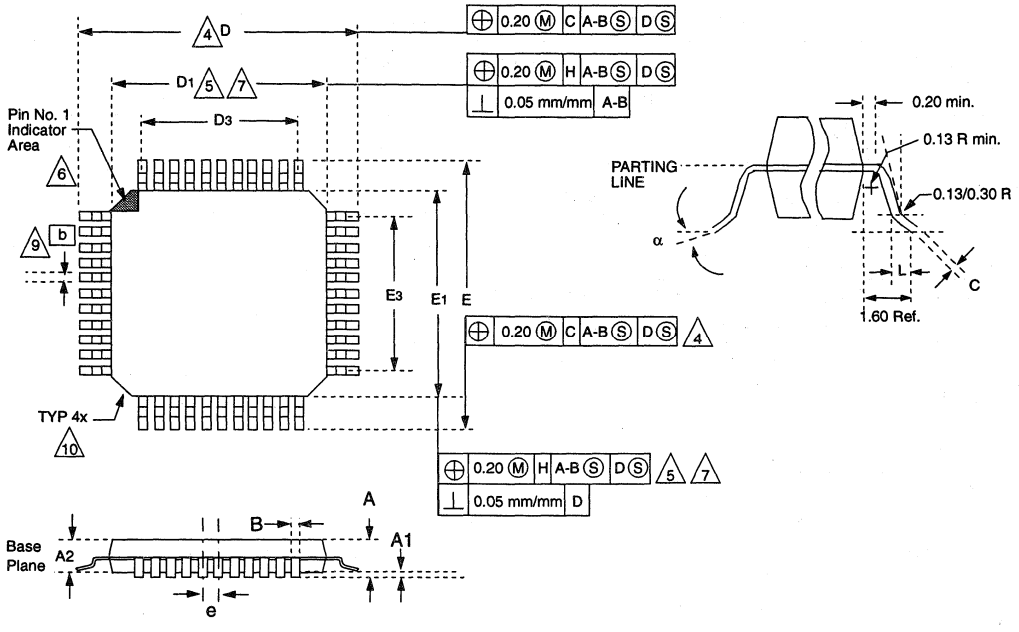
Packaging Diagrams and Parameters

Package Type: 44-Lead Plastic Quad Flatpack (PQ) - 10x10x2 mm Body 1.6/0.15 mm Lead Form



Package Group: Plastic MQFP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	2.000	2.350		0.078	0.093	
A1	0.050	0.250		0.002	0.010	
A2	1.950	2.100		0.768	0.083	
b	0.300	0.450	Typical	0.011	0.018	Typical
C	0.150	0.180		0.006	0.007	
D	12.950	13.450		0.510	0.530	
D1	9.900	10.100		0.390	0.398	
D3	8.000	8.000	BSC	0.315	0.315	BSC
E	12.950	13.450		0.510	0.530	
E1	9.900	10.100		0.390	0.398	
E3	8.000	8.000	BSC	0.315	0.315	BSC
e	0.800	0.800		0.031	0.032	
L	0.730	1.030		0.028	0.041	
CP	0.102	—		0.004	—	

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Packaging Diagrams and Parameters

Thin Plastic Quad Flatpack (TQFP) Family

Symbol List for Metric Plastic Quad Flatpack Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
A2	Distance from base plane to highest point of body
b	Width of terminals
C	Thickness of terminals
D1/E1	Largest overall package parameter including leads
D/E	Largest overall package parameter including leads
D3/E3	Center of end lead to center of end lead
e	Linear spacing of true minimum lead position center line to center line
L	Length of terminal for soldering to a substrate
CP	Seating plane coplanarity

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- is located at bottom of mold parting line and coincident with bottom of lead, where lead exits body.
3. Datums A-B and -D- to be determined at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimension D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25mm per side. Dimensions D1 and E1 do not include mold mismatch and are determined at datum plane -H-.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. These dimensions to be determined at datum plane -H-.
8. All dimensions are in millimeters.
9. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.
10. Exact shape of this feature is optional.
11. Controlling parameter: millimeters.
12. All packages are gull wing lead form.

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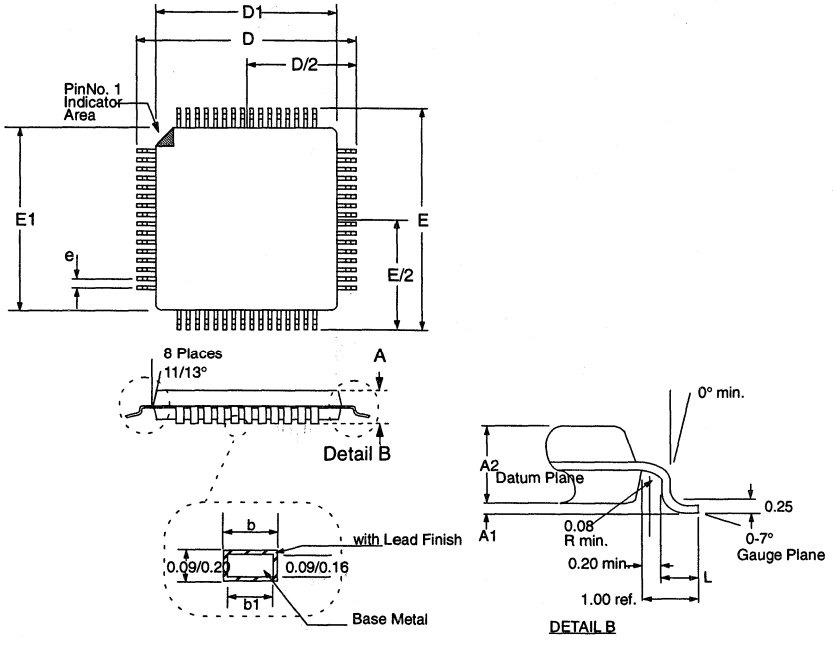
Packaging Diagrams and Parameters

Package Type: 44-Lead Thin Plastic Quad Flatpack (PT/TQ) - 10x10x1 mm Body 1.0/0.10 mm Lead Form



Package Group: Plastic TQFP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	—	1.200		—	0.047	
A1	0.050	0.150		0.002	0.006	
A2	0.950	1.050		0.037	0.041	
b	0.300	0.450		0.012	0.018	
b1	0.300	0.400		0.012	0.016	
D	12.0	12.0	BSC	0.472	0.0472	BSC
D1	10.0	10.0	BSC	0.394	0.394	BSC
E	12.0	12.0	BSC	0.472	0.472	BSC
E1	10.0	10.0	BSC	0.394	0.394	BSC
e	0.8	0.8	BSC	0.031	0.031	BSC
L	0.450	0.750		0.018	0.030	

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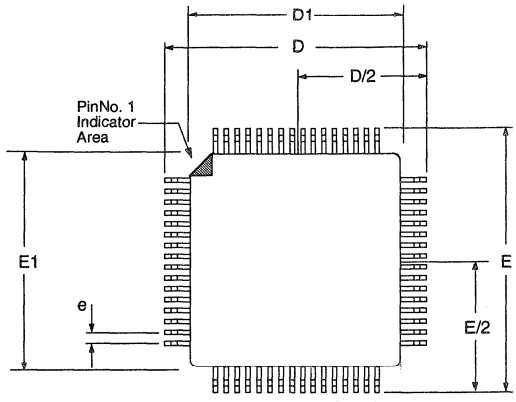
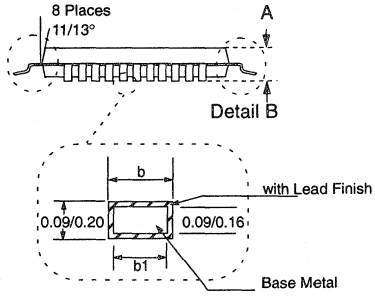
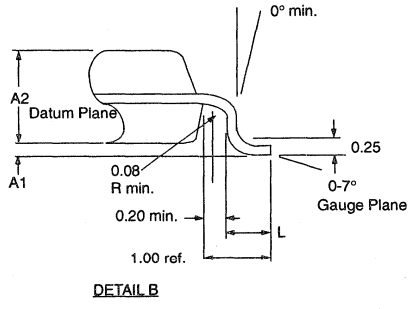
Packaging Diagrams and Parameters

Package Type: 64-Lead Thin Plastic Quad Flatpack (PT/TQ) - 10x10x1 mm Body 1.0/0.10 mm Lead Form







Package Group: Plastic TQFP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	—	1.200		—	0.047	
A1	0.050	0.150		0.002	0.006	
A2	0.950	1.050		0.037	0.041	
b	0.170	0.270		0.007	0.011	
b1	0.170	0.230		0.007	0.009	
D	12.0	12.0	BSC	0.472	0.472	BSC
D1	10.0	10.0	BSC	0.394	0.394	BSC
E	12.0	12.0	BSC	0.472	0.472	BSC
E1	10.0	10.0	BSC	0.394	0.394	BSC
e	0.5	0.5	BSC	0.020	0.020	BSC
L	0.450	0.750		0.018	0.030	

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Product Tape and Reel Specifications

FIGURE 1: EMBOSSED CARRIER DIMENSIONS (8, 12,16, AND 24MM TAPE ONLY)

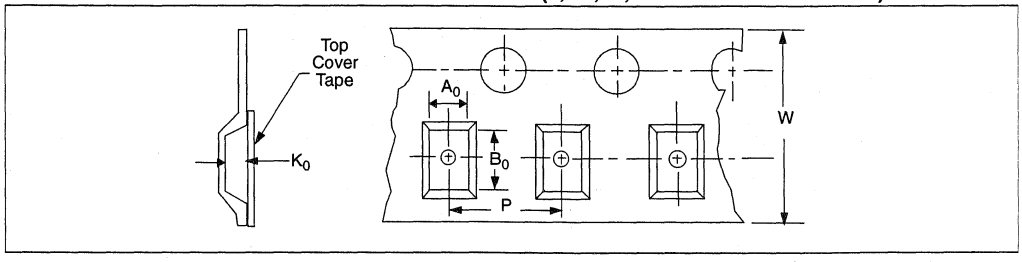

TABLE 1: CARRIER TAPE/CAVITY DIMENSIONS

Case Outline	Package Type		Carrier Dimensions		Cavity Dimensions			Output Quantity Units	Reel Diameter in mm
			W mm	P mm	A0 mm	B0 mm	K0 mm		
SN	SOIC .150"	8L	12	8	6.4	5.2	2.1	3300	330
SO	SOIC .300"	18L	24	12	10.9	13.3	3.0	1600	330
SO	SOIC .300"	20L	24	12	10.9	13.3	3.0	1600	330
SO	SOIC .300"	28L	24 24	12 12	10.9 11.1	18.3 18.5	3.0 3.0	1600 1600	330 330
L	PLCC	28L	24	16	13.0	13.0	4.9	750	330
L	PLCC	32L	24	16	13.1	15.5	3.9	900	330
L	PLCC	44L	32 32	24 24	18.0 18.0	18.0 18.0	4.9 5.0	500 500	330
SM	SOIC .208"	8L	16	12	8.3	5.7	2.2	2100	330
SL	SOIC .150"	14L	16	8	6.5	9.5	2.1	2600	330
TS	TSOP	28L/ 32L	32	16	8.6	20.6	2.1	1500	330
SS	SSOP	20L	16	12	8.2	7.6	3.0	1600	330
SS	SSOP	28L	24	12	8.4	10.9	2.4	2100	330
PQ	MQFP	44L	24	24	16.6	16.6	2.8	900	330
PT	TQFP	44L	24	24	16.6	16.6	2.1	1200	330
VS	VSOP	28L	24	12	8.7	13.9	2.1	2500	330

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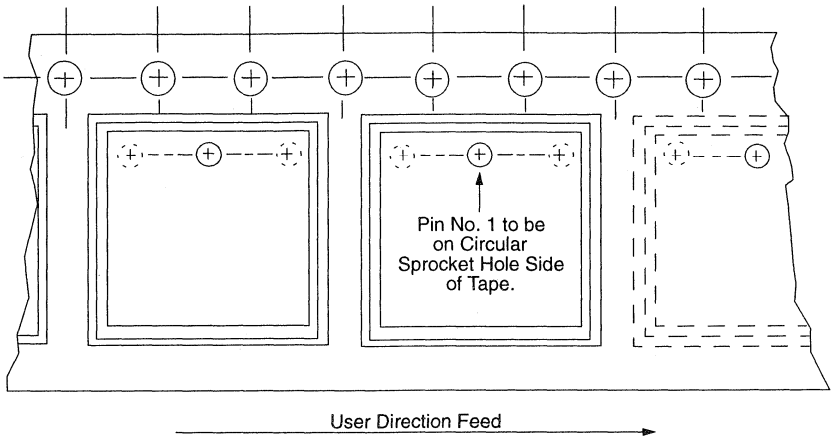
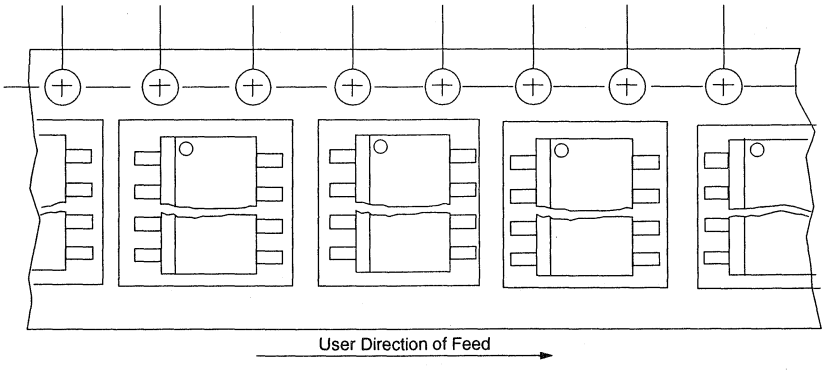
FIGURE 2: MECHANICAL POLARIZATION (PCC AND LCC DEVICES)



Note 1: Top view shown with cover tape removed.

2: Only single sprocket tape shown - polarization for double sprocket tape (32 mm and wider) is the same as shown.

FIGURE 3: MECHANICAL POLARIZATION (SOIC DEVICES)



Note 1: Top view shown with cover tape removed.

2: Only single sprocket tape shown – polarized for double sprocket tape (32 mm and wider) is the same as shown.

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MICROCHIP

Devices in Die/Wafer Form - Non-Volatile Memory

INTRODUCTION

Microchip Technology Inc.'s non-volatile memory devices are available in wafer form and in die form. All products sold as die or wafers have been characterized and qualified according to the requirements of Microchip Technology Inc. Specifications SPI-41014, "Characterization and Qualification of Integrated Circuits", and QCI-39000, "Worldwide Quality Conformance Requirements".

PRODUCT INTEGRITY

Product supplied in die or wafer form will be sample inspected to the criteria defined in Microchip Technology Inc. Specification, QCI-30014, "Standard Visual Inspection Procedure of Dice Prior to Assembly for Commercial Products"

CAUTION

Some EEPROM products use EEPROM cells for device configuration. Exposure to ultra-violet light or x-rays must be avoided. Exposure to ultra-violet light or x-rays may cause the device to operate improperly.

These products are susceptible to damage from electro-static discharge. Extreme care is urged in the handling and assembly of these products.

BONDABILITY OF DIE TO SUBSTRATE

Die/Wafer thickness is 15 mils depending.

Wafers at reduced thicknesses are also available.

Dice are capable of bonding either by using a gold eutectic bond to a gold plated pedestal containing 60 micro-inches of gold, or by using an electrically conductive adhesive (e.g. epoxy) to any substrate.

BONDABILITY OF WIRES TO DIE

Dice shall be capable of thermosonic gold or ultrasonic wire bonding such that the minimum conditions of MIL-STD 883, Method 2011 on "Bond Strength (Destructive Bond pull Test)" are met.

PAD METALLIZATION

Pad metallization is silicon doped aluminum.

BACK SIDE PREPARATION

Die and wafer back sides are backlapped and are without any gold coating.

ELECTRICAL

Dice are guaranteed to fully meet data sheet specifications at the commercial temperature range of 0°C to 70°C.

The die back side is grounded through contacts internal to the part. Thus, it is permitted to float the die mounting surface. It is recommended that the die mounting surface be grounded in multi-chip assemblies.

PACKAGING

Die shipped by Microchip Technology Inc. are placed in a "waffle pack" with sufficient cavity area to restrain the die while maintaining their orientation. Lint free paper inserts are placed over the waffle packs and each pack is secured with a plastic locking clip. Groups of waffle packs are assembled into sets for shipment. A label with lot number, quantity, part number and packing date is placed on each waffle pack.

Wafers shipped by Microchip Technology Inc. are separated by lint free paper and dry packed in a shipping container of appropriate size which is labeled with lot number, quantity, part number and packing date.

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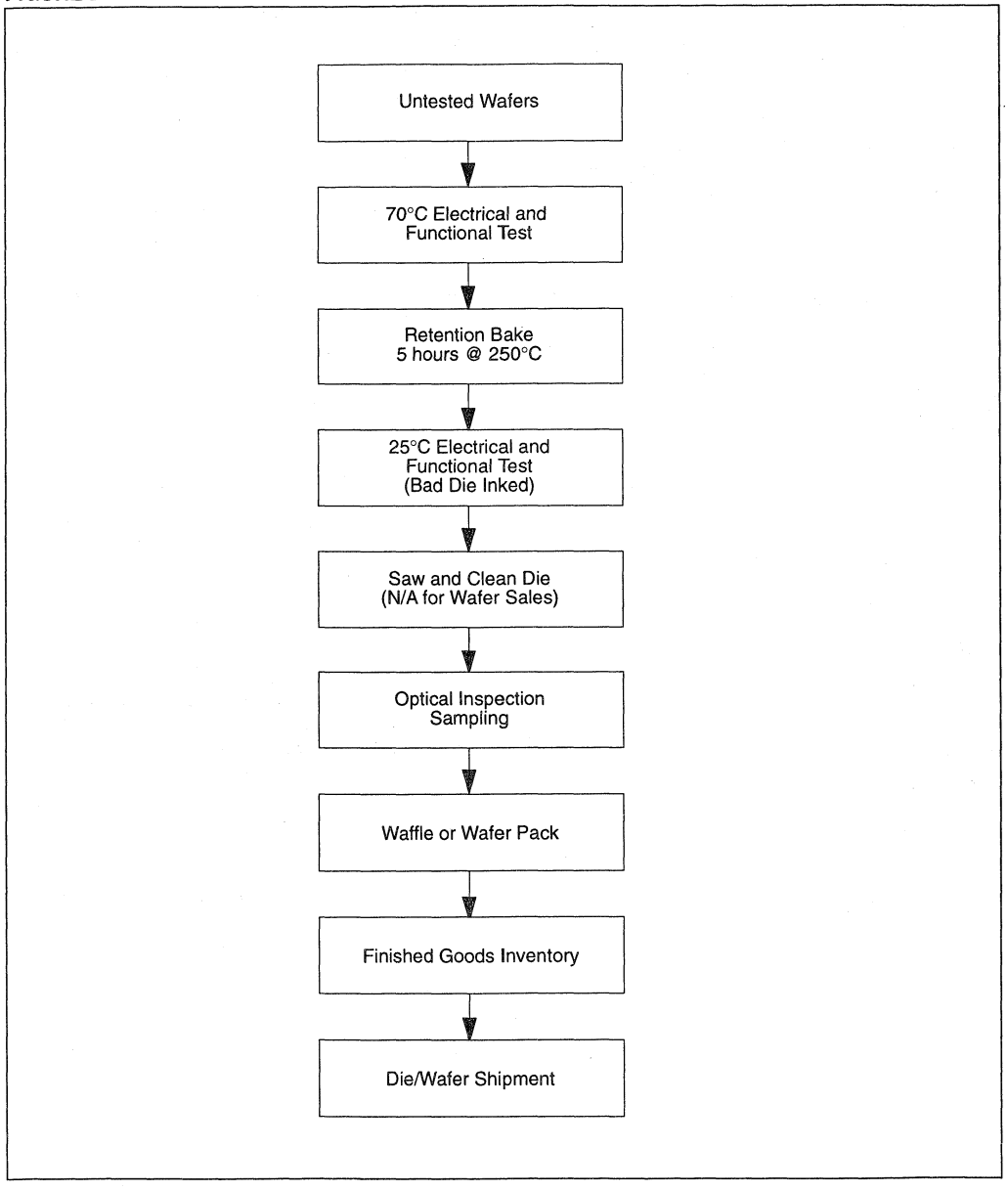
DIE/WAFER PRODUCT OFFERING

All Microchip Technology Inc.'s serial EEPROMs, parallel EEPROMs and EPROMS are available in die or wafer form in the commercial temperature range of 0°C to 70°C. Part number suffixes of /s and /w are used to designate devices in die and wafer form, respectively.

TEST FLOW

All Microchip Technology Inc.'s die products are subjected to functional and parametric testing at the wafer level. The typical EEPROM test flow is shown in Figure 2.

FIGURE 2: EEPROM TEST FLOW



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SECTION 23
OFFICE LOCATIONS

Factory Representatives 23-1
Distributors 23-7
Factory Sales 23-21

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MICROCHIP

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